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(54) **ORGANIC LIGHT-EMITTING DISPLAY DEVICE**

(57) Disclosed is an organic light-emitting display device, which reduces the area of a pixel drive circuit and increases the aperture ratio of a pixel by forming lines inside the pixel using a semiconductor pattern that forms a channel of each thin-film transistor array. The light-emitting display device includes a plurality of pixels arranged in a matrix form and a plurality of lines config-

ured to supply a signal for driving each pixel, each pixel includes a thin-film transistor including an active layer having a first area and a second area, which are configured as conductors, and a gate electrode, and at least one of the first area and the second area is directly connected to a corresponding line among the lines.

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Description

BACKGROUND

Field

[0001] The present disclosure relates to an organic light-emitting display device, and more particularly, to an organic light-emitting display device, which may increase the aperture ratio of each pixel by using a semiconductor pattern of a thin-film transistor array as a line.

Discussion of the Related Art

[0002] An image display device, which realizes various pieces of information on a screen, is a core technology of the information and communication age, and is being developed in the direction of becoming thinner, lighter, more portable, and having higher performance. In response, as a flat panel display device that is thinner and lighter than a cathode ray tube (CRT), for example, an organic light-emitting display device, which controls the amount of light emitted from an organic light-emitting layer to display an image, is in the spotlight.

[0003] In an organic light-emitting display device, a plurality of pixels is arranged in a matrix form to display an image. Here, each pixel includes a light-emitting element, and a pixel drive circuit including, for example, a plurality of transistors and storage capacitors to independently drive the light-emitting element.

[0004] Recently, since the area of individual pixels is reduced with an improvement in the resolution of the organic light-emitting display device, in order to minimize a reduction in the aperture ratio of each pixel due to the reduced area of the pixel, the area of each pixel drive circuit also needs to be reduced. However, when the area of the pixel drive circuit is reduced, distances between respective lines, transistors, and storage capacitors are reduced, causing parasitic capacitance between components of the pixel drive circuit, which may cause coupling of multiple signals, or a short-circuit phenomenon in which the lines become interconnected. Thereby, there is a limitation to the extent to which the area of the pixel drive circuit can be reduced.

[0005] In particular, in an organic light-emitting display device of the related art, respective electrodes of storage capacitors and thin-film transistors of each pixel drive circuit are connected to a shield layer, which is a lower layer on a substrate, and metal lines, which are formed in the same layer as source and drain electrodes of the thin-film transistor, which is an upper layer on the substrate, through contact holes. Accordingly, since the organic light-emitting display device of the related art requires a predetermined number or more of contact holes according to the structure of the pixel drive circuit, and has a limitation on the extent to which the area of each contact hole can be reduced in order to prevent the parasitic capacitance and short-circuit mentioned above, the

extent to which the area of the pixel drive circuit can be reduced is consequently limited due to the presence of the contact holes.

[0006] Due to the problems described above, in a high-resolution organic light-emitting display device, when the area of the pixel drive circuit is not sufficiently reduced in proportion to the reduction in the area of the pixel, the aperture ratio of each pixel may be reduced, causing a reduction in the brightness and luminous efficacy of the organic light-emitting display device.

SUMMARY

[0007] Accordingly, the present disclosure is directed to an organic light-emitting display device that substantially addresses one or more problems due to limitations and disadvantages of the related art.

[0008] An object of the present disclosure is to provide an organic light-emitting display device, which may reduce the area of a pixel drive circuit and increase the aperture ratio of a pixel by forming lines inside the pixel using a semiconductor pattern that forms a channel of each thin-film transistor array.

[0009] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following. The objectives and other advantages may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0010] To achieve these objects and other advantages, as embodied and described herein, an organic light-emitting display device includes a plurality of pixels and a plurality of lines configured to drive the pixels, wherein each pixel includes a thin-film transistor including an active layer having a first area and a second area, which are configured as conductors, and a gate electrode. Here, at least one of the first area and the second area of the thin-film transistor is directly connected to a corresponding line among the lines.

[0011] An area connected to the line includes an electrode portion integrally formed with a channel area of the thin-film transistor and an extension portion configured to extend from the electrode portion to a top of the line so as to be directly connected to the line.

[0012] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The accompanying drawings, which are included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this application, illustrate embodiment(s) and together with the description serve to explain the principle of the disclosure.

FIG. 1 is a plan view for explaining a pixel structure of an organic light-emitting display device according to one embodiment.

FIG. 2 is a cross-sectional view for explaining the cross section of portion I-I' of FIG. 1.

FIG. 3 is a cross-sectional view for explaining portion II-II' of FIG. 1; and

FIG. 4 is a view illustrating variation in the structure of portions designated by dotted squares of FIG. 1, compared to the related art.

DETAILED DESCRIPTION

[0014] Hereinafter, exemplary embodiments will be described with reference to the accompanying drawings. In the entire specification, the same or similar elements are denoted by the same reference numerals even though they are depicted in different drawings. In the following description, a detailed description of known functions and configurations incorporated herein will be omitted when it may make the subject matter unclear. Also, the terms used in the following description are terms defined taking into consideration the functions obtained in accordance with the present disclosure, and may differ from the names of parts of actual products.

[0015] In the case of a description with respect to positional relations, when an element is referred to as being, for example, "on", "above", "under", and "aside" another element, it may be directly on the other element or intervening elements may also be present.

[0016] Although terms such as, for example, "first" and "second" are used to describe various components, these components are not limited by these terms. These terms are merely used to distinguish any one component from another component. Thus, "a first component" mentioned below may be "a second component" within the technical spirit of the present invention.

[0017] In the drawings, the thickness and size of each component are illustrated for convenience of description, and the present disclosure is not necessary to be limited to the size and thickness of the illustrated component.

[0018] Hereinafter, various embodiments will be described in detail with reference to the accompanying drawings.

[0019] FIG. 1 is a plan view for explaining a pixel structure of an organic light-emitting display device according to one embodiment, and FIG. 2 is a cross-sectional view for explaining the cross section of portion I-I' of FIG. 1. In addition, FIG. 3 is a cross-sectional view for explaining portion II-II' of FIG. 1.

[0020] The organic light-emitting display device includes a plurality of pixels SP1 to SP4 arranged in a matrix form. Each of the pixels SP1 to SP4 includes a light-emitting area A/A having a light-emitting layer. In addition, the pixels SP1 to SP4 include respective pixel drive circuits, and include a plurality of lines, which transmit signals to the pixel drive circuits. For example, the organic light-emitting display device according to an embodiment

of the present invention may include a gate line GL for supplying a gate signal to the respective pixels SP1 to SP4, a data line DL for supplying a data signal to the respective pixels SP1 to SP4, a power line VDD for applying a power voltage VDD to the pixel drive circuit, and a reference line RL for supplying a reference voltage to the respective pixels SP1 to SP4 and sensing a voltage charged in the respective pixels SP1 to SP4, without being necessarily limited thereto.

[0021] The pixel drive circuit includes a plurality of thin-film transistors. Here, each thin-film transistor includes an active layer 200 having a channel area and first and second areas, which are configured as conductors, and a gate electrode. In the present embodiment, for convenience, a source area is described as the first area and a drain area is described as the second area. However, the first area and the second area are not necessarily limited thereto, and the first area may be the drain area and the second area may be the source area according to the structure of the thin-film transistor.

[0022] In at least one of the thin-film transistors, at least one area among the first area and the second area may be directly connected to any one of the lines. In other words, instead of forming source and drain electrodes on the first area and the second area, the active layer 200 of the thin-film transistor is configured as a conductor and is utilized as an electrode and a line so that the active layer 200 is directly connected to the other lines.

[0023] The feature described above will be described below in detail with reference to the embodiment of FIGs. 1 to 3. The pixel drive circuit of the organic light-emitting display device according to the embodiment of FIGs. 1 to 3 has a 3T1C structure that includes a switching transistor 220, a driving transistor 210, a sensing transistor 230, and a storage capacitor Cst, which are disposed on a substrate 100. However, the pixel drive circuit according to the present disclosure is not necessarily limited to the above-described structure, and various other structures may be applied according to the design of the pixel drive circuit.

[0024] A gate electrode of the switching transistor 220 may constitute a portion of the gate line GL and may be disposed along with the gate line GL. An input electrode 222 of the switching transistor 220 may be connected to the data line DL, and an output electrode 223 may be connected to an intermediate electrode 252 of the storage capacitor Cst. Here, the input electrode may be formed by extending from the data line DL, and the output electrode may be formed by extending from the intermediate electrode of the storage capacitor Cst. However, the switching transistor 220 of the present disclosure is not necessarily limited to the above-described structure.

[0025] The switching transistor 220 includes an active layer 221 configured to overlap the gate electrode. The active layer is configured such that a channel area is formed in the area thereof that overlaps the gate electrode and such that first and second areas are formed at opposite sides of the channel area so as to come into

contact with the input electrode 222 and the output electrode 223 respectively.

[0026] In an N-type transistor, the first area 222 may be a source area and the second area 223 may be a drain area. In a P-type transistor, the first area 222 may be a drain area and the second area 223 may be a source area.

[0027] Referring to FIGs. 2 and 3, the driving transistor 210 includes a gate electrode 211 and an active layer 200. Explaining the active layer 200 in more detail, a channel area 216 is formed below the gate electrode 211 and a gate insulation layer 110 is located between the gate electrode 211 and the channel area 216. In addition, a first area 213 and a second area 218, which are configured as conductors, are located at opposite sides of the channel area 216. Here, the second area 218 may be an input area that receives a drive voltage from a power line VDD, and the first area 213 may be an output area that outputs the drive voltage.

[0028] Referring to FIG. 2, the second area 218 extends to the top of the power line VDD. Here, the second area 218 includes a first electrode portion 212, which is integrally formed with the channel area 216 and is configured as a conductor, and a first extension portion 214, which extends from the first electrode portion 212 and comes into contact with the power line VDD. Here, the first extension portion 214 may come into contact with first electrode portions 212 of two neighboring pixels SP at the same time. Thereby, the first extension portion 214 supplies the drive voltage, input from the power line VDD, to the first electrode portions 212 of the two neighboring pixels SP at the same time.

[0029] A buffer layer 261 is located between the power line and the first extension portion 214. The buffer layer 261 has the feature of preventing the permeation of moisture or impurities through the substrate 100.

[0030] A portion of the power line VDD is exposed through a fourth contact hole 704. The first extension portion 214 comes into contact with the power line VDD through the fourth contact hole 704.

[0031] The first area 213 may extend from the channel area 216 so as to be integrally formed with the channel area 216, and the active layer in the first area 213 may serve as a lower electrode of the storage capacitor Cst.

[0032] The configuration of the storage capacitor Cst will be described below. The gate insulation layer 110 described above is located on the active layer 200, which constitutes a lower electrode 237, and an interlayer insulation layer 120 is located so as to cover the gate electrode 211. An intermediate electrode 252 is formed on the interlayer insulation layer 120 in the area in which the intermediate electrode 252 overlaps the lower electrode 237, and a planarization layer 130 is located so as to cover the intermediate electrode 252. An upper electrode 253 is located on the planarization layer 130. In this way, the storage capacitor Cst, which includes double capacitors between the lower electrode 237 and the intermediate electrode 252 and between the intermediate elec-

trode 252 and the upper electrode 253, is provided. Here, a shield layer 251 is located on the substrate 110 below the lower electrode 237 in the same layer as the power line VDD using the same material as the power line VDD, for example, a metal material. As mentioned above, the buffer layer 261 is located on the power line VDD and the shield layer 251. The buffer layer 261 further includes a first contact hole 701, which exposes a portion of the shield layer 251. The lower electrode 237 is connected to the shield layer 251 through the first contact hole 710 so that the lower electrode 237 and the shield layer 251 have an equivalent potential therebetween.

[0033] The shield layer 251 may prevent light from being introduced into a semiconductor layer 200 and may reduce parasitic capacitance generated between the lower electrode 237 and the data lines DL, thereby reducing a phenomenon of coupling between the data line DL and the gate electrode 211 of the driving transistor 210. Although the shield layer 251 of the related art has been connected to the intermediate electrode 252 through a contact hole, in the embodiment, the shield layer 251 is connected to the active layer 200, which enables a reduction in the area of the first contact hole 701, resulting in an additional increase in the aperture ratio of the pixel.

[0034] A portion of the interlayer insulation layer 120 and the gate insulation layer 110 is removed in the area that corresponds to the lower electrode 237, i.e. the edge of the first area 213 of the active layer 200 so as to form a second contact hole 702, which exposes a portion of the first area 213. A connection electrode 217 is formed so as to come into contact with the first area 213 through the second contact hole 702. Here, the connection electrode 217 may be an output electrode of the driving transistor 210, for example, a source electrode, without being necessarily limited thereto. The connection electrode 217 is formed in the same layer as the intermediate electrode 252 of the storage capacitor Cst using the same material as the intermediate electrode 252. The planarization layer 130 is formed on the connection electrode 217 and the intermediate electrode 252. A portion of the planarization layer 130 is removed to form a third contact hole 703, which exposes the connection electrode 217. The upper electrode 253 is connected to the connection electrode 217 through the third contact hole 703. Thereby, the upper electrode 253 and the lower electrode 237, which are interconnected via the connection electrode 217, form an equivalent potential therebetween.

[0035] Meanwhile, referring to FIG. 3, the intermediate electrode 252 is connected to the gate electrode 211 of the driving transistor 210 through a sixth contact hole 706. Thereby, the intermediate electrode 252 is connected to both the gate electrode 211 of the driving transistor 210 and the output electrode of the switching transistor 220, thereby functioning as a node that interconnects the gate electrode 211 of the driving transistor 210, the output electrode of the switching transistor 220, and the intermediate electrode of the storage capacitor Cst.

[0036] Here, the active layer 200 or 221 may be formed of silicon, amorphous silicon, poly-silicon, or low-temperature poly-silicon (LTPS). In addition, the gate electrode 211 on the active layer 200 or the area in which no gate line GL is formed may be doped with, for example, an N-type dopant or a P-type dopant, thereby being configured as a conductor.

[0037] In addition, the active layer 200 or 211 may be formed of a semiconductor oxide. The semiconductor oxide may be selected from among, for example, indium gallium zinc oxide (InGaZnO), indium tin zinc oxide (In-SnZnO), indium zinc oxide (InZnO), and tin zinc oxide (SnZnO). In addition, the active layer 200 or 211 may be configured as a conductor via, for example, plasma processing using the gate electrode 211 and the gate line GL as a mask.

[0038] Referring to FIGs. 1 and 3, the upper electrode 253 extends to the display area A/A so as to form a pixel electrode 301. Here, the drive voltage, input from the power line PL, is supplied to the pixel electrode 301 by way of the connection electrode 217 of the driving transistor 210 and the upper electrode 253. In other words, the upper electrode 253 functions as a node that interconnects the storage capacitor Cst, the pixel electrode 301 and the first area 213 of the driving transistor 210.

[0039] Here, a bank layer 140 is provided in the remaining area excluding the display area A/A, and the display area A/A is defined by the bank layer 140.

[0040] The bank layer 140 may be formed of an organic insulation material such as, for example, poly acryl or polyimide, without being necessarily limited thereto.

[0041] An organic layer 302 is formed on the bank layer 140 and the pixel electrode 301. The organic layer 302 may include a light-emitting layer in the area that corresponds to the display area A/A, and may be located on the entire surface of the bank layer 140 and the display area A/A.

[0042] Here, the organic layer 302 is divided into an electron injection layer (EIL), an electron transport layer (ETL), an emission layer, a hole transport layer (HTL), and a hole injection layer (HIL). In the light-emitting layer, excitons generated via recombination of electrons from a negative electrode and holes from a positive electrode return to a ground state, thereby emitting light within a specific wavelength range.

[0043] A second electrode 303 is formed on the organic layer 302. The second electrode 303 may be formed on the entire surface of the substrate 100.

[0044] Here, when the first electrode 301 is a positive electrode, the second electrode 303 may be a negative electrode. Alternatively, when the second electrode 303 is a positive electrode, the first electrode 301 may be a negative electrode.

[0045] The shield layer 251 and the intermediate electrode 252 may be formed of a single metal or an alloy thereof selected from among silver (Ag), nickel (Ni), gold (Au), platinum (Pt), aluminum (Al), copper (Cu), molybdenum (Mo), titanium (Ti), and neodymium (Nd), without

being necessarily limited thereto.

[0046] In addition, the first electrode 301 and the second electrode 303 may be formed of a transparent conductive material such as, for example, indium tin oxide (ITO), indium zinc oxide (IZO), or indium gallium zinc oxide (IGZO), or a single metal or an alloy thereof among the metals that form the shield layer 251 and the intermediate electrode 252, without being necessarily limited thereto.

[0047] The sensing transistor 230 includes a channel area 235, a first area 238 and a second area 232. A gate electrode of the sensing transistor 230 may be formed as a portion of the gate line GL, the first area may be a source area, and the second area may be a drain area, without being necessarily limited thereto.

[0048] The first area 238 includes a second electrode portion 233, which is in contact with the channel area 235 of the sensing transistor 203 so as to be integrally formed with the channel area 235, and a second extension portion 234, which extends from the second electrode portion 233 and comes into contact with the reference line RL. The reference line RL may be formed in the same layer as the shield layer 251 and the power line VDD using the same material as the shield layer 251 and the power line VDD, without being necessarily limited thereto. The second extension portion 234 is directly connected to the reference line RL through a fifth contact hole 705 formed in the buffer layer 261.

[0049] The second area 232 extends from the first area 213 of the driving transistor, i.e. the lower electrode 237 of the storage capacitor Cst so as to be integrally formed with the lower electrode 237. Here, the first area 232 of the sensing transistor 230 serves as an input electrode, and the sensing transistor 230 does not include a separate input electrode.

[0050] The shield layer 251, the power line VDD, and the reference line RL are formed of the same metal material. Here, when edge portions of these components are vertically formed, there is a possibility of disconnection of the active layer 200 located thereon. Therefore, in order to prevent disconnection of the active layer 200, the respective edge portions of the shield layer 251, the power line VDD, and the reference line RL may have a tapered shape, and in other words, may be formed to have slopes.

[0051] As described above, the driving transistor 220 and the sensing transistor 230 of the present invention has the feature that at least one of input and output electrodes, i.e. source and drain electrodes is omitted and the active layer 200, which is configured as a conductor, is in contact with the respective lines. To this end, the active layer 200, which is configured as a conductor, extends in a line form in order to come into contact with the respective lines, and is connected to the respective lines through contact holes.

[0052] Accordingly, the organic light-emitting display device according to the present invention may achieve a simplified pixel structure and may reduce the genera-

tion of parasitic capacitance, which may be generated between several metals located in different layers, because lines, which have conventionally been formed using a metal of the shield layer or the source/drain electrodes, are formed using the active layer. In addition, when the lines in the pixel are formed using the active layer as described above, the number of contact holes, which are required to interconnect several lines located in different layers and the active layer, may be greatly reduced. Therefore, although a reduction in the area of the pixel drive circuit has conventionally been limited due to a large number of contact holes even if the area of each pixel is reduced, according to the present disclosure, the pixel drive circuit may be further densely formed owing to a great reduction in the number of contact holes. In this way, according to the present disclosure, the area of the pixel drive circuit may be reduced in proportion to the reduction in the area of the pixel, which may secure a high aperture ratio of the pixel.

[0053] FIG. 4 is a view illustrating variation in the structure of portions designated by dotted squares of FIG. 1, compared to the related art.

[0054] In the related art, a drain electrode 219 is formed in the same layer as the upper electrode 253 on the drain area of the driving transistor 210 using the same metal as the upper electrode 253, and a line 2191 extending from the drain electrode 219 is connected to the top of the power line VDD through a contact hole.

[0055] In addition, the intermediate electrode 252 extends to the area in which the connection electrode 217 is formed and is connected to the shield layer 251 thereunder through a contact hole 2192. The upper electrode 253 extends to form a drain electrode 2321 of the sensing transistor 230. Meanwhile, a source electrode 2311 is located on the first area of the sensing transistor 231, i. e. the source area.

[0056] On the other hand, according to one embodiment, since no line extends from the upper electrode 252 and the active layer 200 forms a line, the drain electrode 219 of the driving transistor 210 is omitted, and the source and drain electrodes 2311 and 2321 of the sensing transistor 230 are also omitted. Thereby, contact holes, which are required to form the source and drain electrodes, are not formed, and a contact hole 701 may be formed only in the buffer layer 261 in order to interconnect the active layer 200 and the shield layer 251. In this case, the area of the contact hole is greatly reduced, compared to a conventional contact hole for interconnecting the metal of the source and drain electrodes and the shield layer 251.

[0057] As described above, the organic light-emitting display device according to one embodiment may achieve a reduction in the number of contact holes and a great reduction in the area of some contact holes, thereby securing additional available space to enable a reduction in the area of the pixel drive circuit. That is, when the area of the pixel drive circuit is reduced, a display area of the pixel is increased, which increases the aperture

ratio of the pixel.

[0058] As is apparent from the above description, in an organic light-emitting display device according to one embodiment, since some of lines, which have conventionally been formed using a metal material of a shield layer or source and drain electrodes, are formed using an active layer, a simplified pixel structure may be achieved and the possibility of generation of parasitic capacitance between several metals located in different layers may be reduced.

[0059] In addition, when the lines in a pixel are formed using the active layer, the number of contact holes, which are required to interconnect several lines located in different layers and the active layer, may be greatly reduced. Therefore, although a reduction in the area of the pixel drive circuit has conventionally been limited due to a large number of contact holes even if the area of each pixel is reduced, according to the present disclosure, the pixel drive circuit may be further densely formed owing to a great reduction in the number of contact holes. In this way, according to the present disclosure, the area of the pixel drive circuit may be reduced in proportion to the reduction in the area of the pixel, which may secure a high aperture ratio of the pixel.

[0060] Although the embodiments have been described above in detail with reference to the accompanying drawings, it will be apparent to those skilled in the art that the present disclosure is not limited to the embodiments described above, and various substitutions, modifications, and alterations may be devised within the scope of the disclosure. Accordingly, various embodiments are not intended to limit the present disclosure, and the scope of the disclosure is not limited by the embodiments. Accordingly, the disclosed embodiments are provided for the purpose of description and are not intended to limit the technical scope of the disclosure, and the technical scope of the disclosure is not limited by the embodiments. The range of the disclosure should be interpreted based on the following claims.

[0061] Further embodiments are defined in the following numbered clauses:

1. An organic light-emitting display device comprising a plurality of pixels arranged in a matrix form and a plurality of lines configured to supply a signal for driving each pixel, wherein each pixel includes a thin-film transistor including an active layer having a first area and a second area, which are configured as conductors, and a gate electrode, and wherein at least one of the first area and the second area is directly connected to a corresponding line among the lines.

2. The device according to clause 1, wherein the area directly connected to the line, among the first and second areas, includes an electrode portion integrally formed with a channel area of the thin-film transistor and an extension portion configured to extend from the electrode portion so as to be directly

connected to the line.

3. The device according to clause 1, wherein each pixel further includes a capacitor, and wherein the capacitor includes: a shield layer located on a substrate; a lower electrode configured to overlap the shield layer with a buffer layer interposed therebetween, the lower electrode being connected to the shield layer through a first contact hole and being formed of the active layer, which is configured as a conductor; an intermediate electrode configured to overlap the active layer with a gate insulation layer and an interlayer insulation layer interposed therebetween; and an upper electrode configured to overlap the intermediate electrode with a passivation layer interposed therebetween.

4. The device according to clause 1, wherein one of the thin-film transistors is a driving transistor, and wherein the driving transistor further includes a connection electrode configured to come into contact with the first area through a second contact hole, the connection electrode is connected to a pixel electrode through a third contact hole, and the second area is directly connected to a power line, which supplies a drive voltage to the pixel and is arranged in a vertical direction, among the lines through a fourth contact hole.

5. The device according to clause 4, wherein the second area of the driving transistor includes a first electrode portion integrally formed with a channel area of the driving transistor and a first extension portion configured to extend from the first electrode portion so as to be connected to the power line.

6. The device according to clause 5, wherein the first electrode portion extends from the channel area and is connected to the first electrode portion of the driving transistor of another neighboring pixel, and the first extension portion extends from a point at which the first electrode portions of two neighboring pixels are connected to each other and is connected to the power line.

7. The device according to clause 1, wherein one of the thin-film transistors is a sensing transistor, and wherein the first area of the sensing transistor is directly connected to a reference line, which supplies a reference voltage to the pixel and senses a voltage charged in the pixel, among the lines through a fifth contact hole, and wherein the second area of the sensing transistor extends from the first area of the driving transistor and is integrally formed with the first area.

8. The device according to clause 7, wherein the first area of the sensing transistor includes a second electrode portion configured to come into contact with a channel area of the sensing transistor so as to be integrally formed with the channel area and a second extension portion configured to extend from the second electrode portion so as to be connected to the reference line, which is arranged in a vertical direc-

tion, through the fifth contact hole.

9. The device according to clause 8, wherein the second electrode portion comes into contact with the second electrode portion of the sensing transistor provided in a neighboring pixel, and wherein the second extension portion extends from a point at which the second electrode portions of two neighboring sensing transistors are connected to each other and is directly connected to the reference line through the fifth contact hole.

10. The device according to clause 3, wherein the shield layer is formed in the same layer as a power line, which supplies a drive voltage to each pixel, and a reference line, which supplies a reference voltage to the pixel and senses a voltage charged in the pixel, among the lines, using the same material as the power line and the reference line.

11. The device according to clause 7, wherein the gate electrode of the sensing transistor is connected to a gate line, which supplies a gate signal to each pixel, among the lines.

12. The device according to clause 10, wherein the shield layer, the reference line and the power line include edge portions each having a tapered shape.

Claims

1. An organic light-emitting display device comprising a plurality of pixels arranged in a matrix form and a plurality of lines each configured to supply a signal for driving each pixel, wherein each pixel includes a thin-film transistor including an active layer having a first area (222) and a second area (223), which are configured as conductors, and a gate electrode, and wherein at least one of the first area and the second area is directly connected to a corresponding line among the plurality of lines.
2. The device according to claim 1, wherein the area directly connected to the corresponding line, among the first and second areas, includes an electrode portion (212, 233) integrally formed with a channel area (235) of the thin-film transistor and an extension portion (214, 234) configured to extend from the electrode portion so as to be directly connected to the corresponding line.
3. The device according to claim 1 or 2, wherein each pixel further includes a capacitor (Cst), and wherein the capacitor includes:

a shield layer (251) located on a substrate (100);
a lower electrode (237) configured to overlap the shield layer with a buffer layer (261) interposed therebetween, the lower electrode being connected to the shield layer through a first con-

- tact hole (701) and being formed of the active layer, which is configured as a conductor;
 an intermediate electrode (252) configured to overlap the active layer with a gate insulation layer (110) and an interlayer insulation layer (120) interposed therebetween; and
 an upper electrode (253) configured to overlap the intermediate electrode with a planarization layer 130 interposed therebetween.
4. The device according to any previous claim, wherein the thin-film transistor is a driving transistor (210), and
 wherein the driving transistor further includes a connection electrode (217) configured to come into contact with the first area through a second contact hole (702), the connection electrode is connected to a pixel electrode (301) through a third contact hole (703), and the second area is directly connected to a power line (VDD), which supplies a drive voltage to the pixel and is arranged in a vertical direction, among the plurality of lines through a fourth contact hole (704) .
 5. The device according to claim 4, wherein the second area of the driving transistor includes a first electrode portion (212) integrally formed with a channel area of the driving transistor and a first extension portion (214) configured to extend from the first electrode portion so as to be connected to the power line (VDD).
 6. The device according to claim 5, wherein the first electrode portion of a first pixel of the plurality of pixels extends from the channel area of the first pixel and is connected to the first electrode portion of the driving transistor of a second pixel of the plurality of pixels, the second pixel neighboring the first pixel, wherein the first extension portion of the first pixel extends from a point at which the first electrode portion of the first pixel connects to the first extension portion of the second pixel and is connected to the power line.
 7. The device according to any of claims 1 to 3, wherein the thin-film transistor is a sensing transistor (230), and
 wherein the first area of the sensing transistor is directly connected to a reference line (RL), which supplies a reference voltage to the pixel and senses a voltage charted in the pixel, among the plurality of lines through a fifth contact hole (705), and
 wherein the second area of the sensing transistor extends from the first area of the driving transistor and is integrally formed with the first area.
 8. The device according to claim 7, wherein the first area of the sensing transistor includes a second electrode portion (233) configured to come into contact with a channel area (235) of the sensing transistor so as to be integrally formed with the channel area and a second extension portion (234) configured to extend from the second electrode portion so as to be connected to the reference line, which is arranged in a vertical direction, through the fifth contact hole.
 9. The device according to claim 8, wherein the second electrode portion of a first pixel of the plurality of pixels comes into contact with the second electrode portion of the sensing transistor of a second pixel of the plurality of pixels, the first pixel neighboring the second pixel, and
 wherein the second extension portion of the first pixel extends from a point at which the second electrode portions of the first and second pixels are connected to each other and is directly connected to the reference line through the fifth contact hole.
 10. The device according to claim 3, wherein the shield layer is formed in the same layer as a power line, which supplies a drive voltage to each pixel, and a reference line, which supplies a reference voltage to the pixel and senses a voltage charged in the pixel, among the plurality of lines, using the same material as the power line and the reference line.
 11. The device according to any of claims 7 to 10, wherein the gate electrode of the sensing transistor is connected to a gate line, which supplies a gate signal to each pixel, among the plurality of lines.
 12. The device according to claim 10 or 11, wherein the shield layer, the reference line and the power line include edge portions each having a tapered shape.

FIG. 1

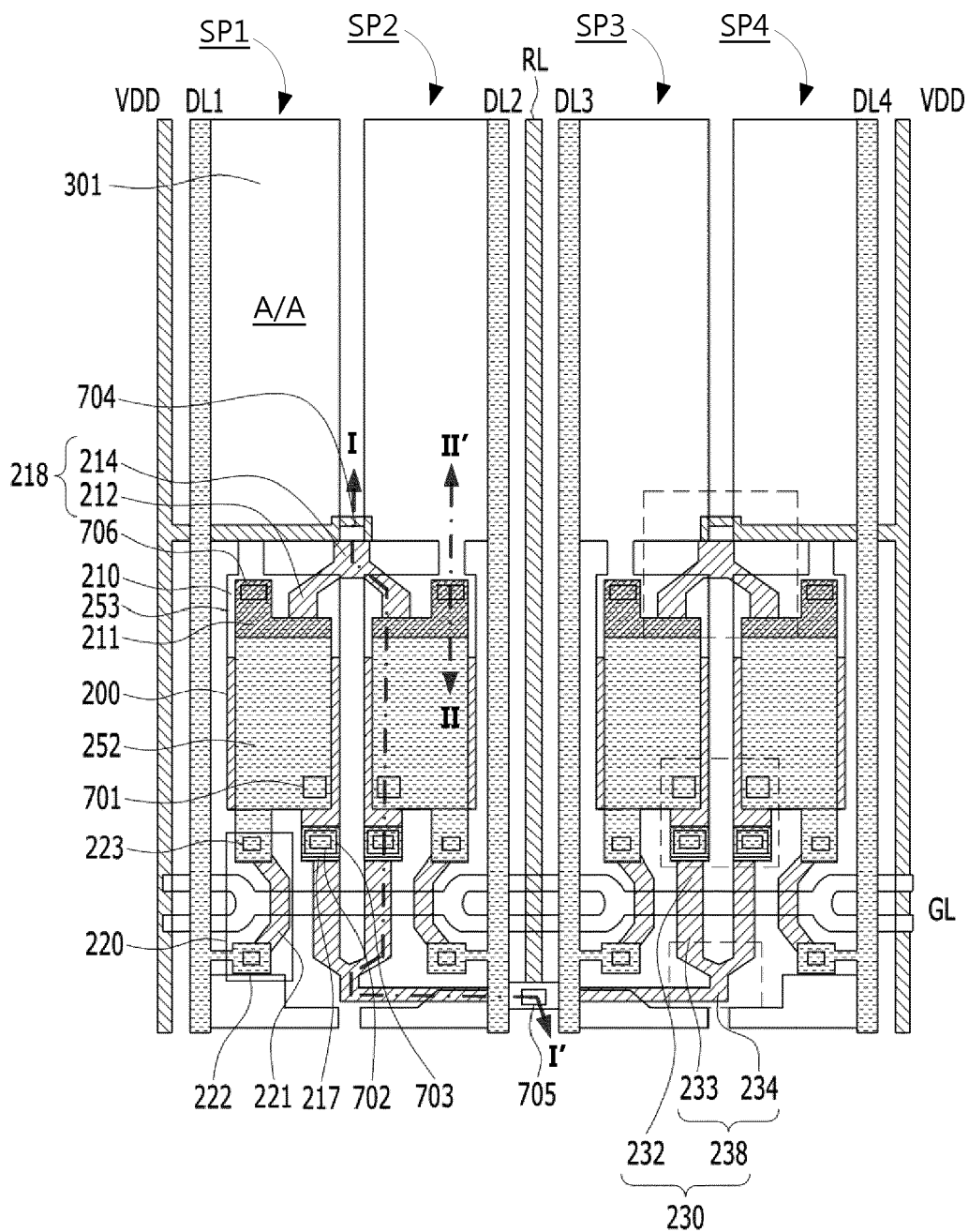


FIG. 2

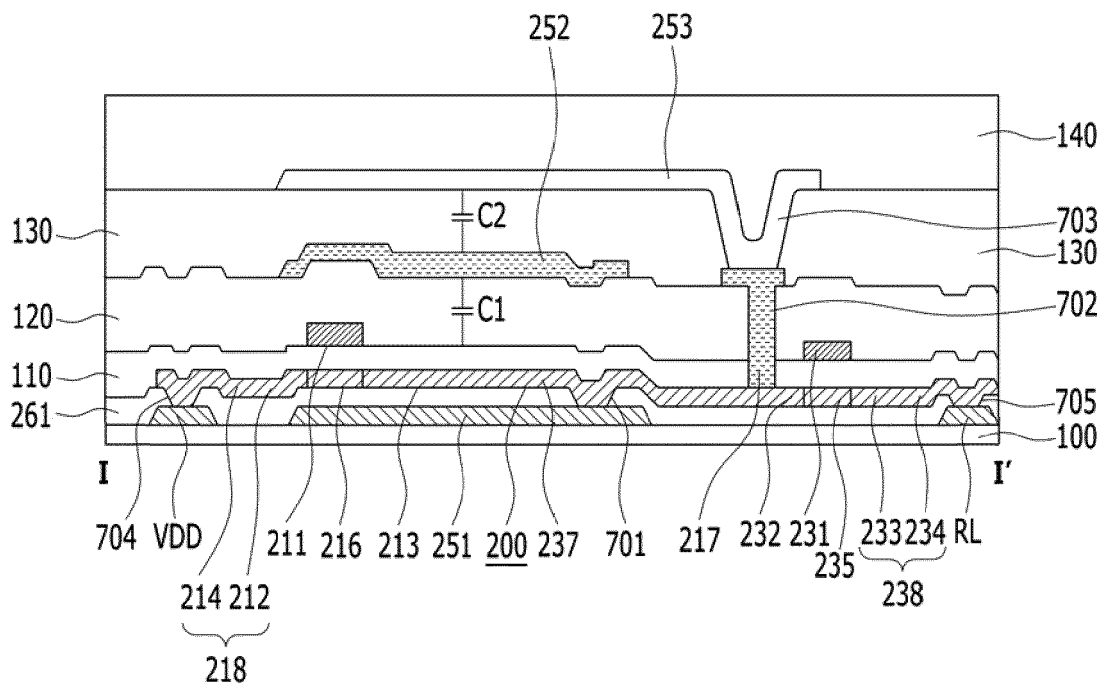


FIG. 3

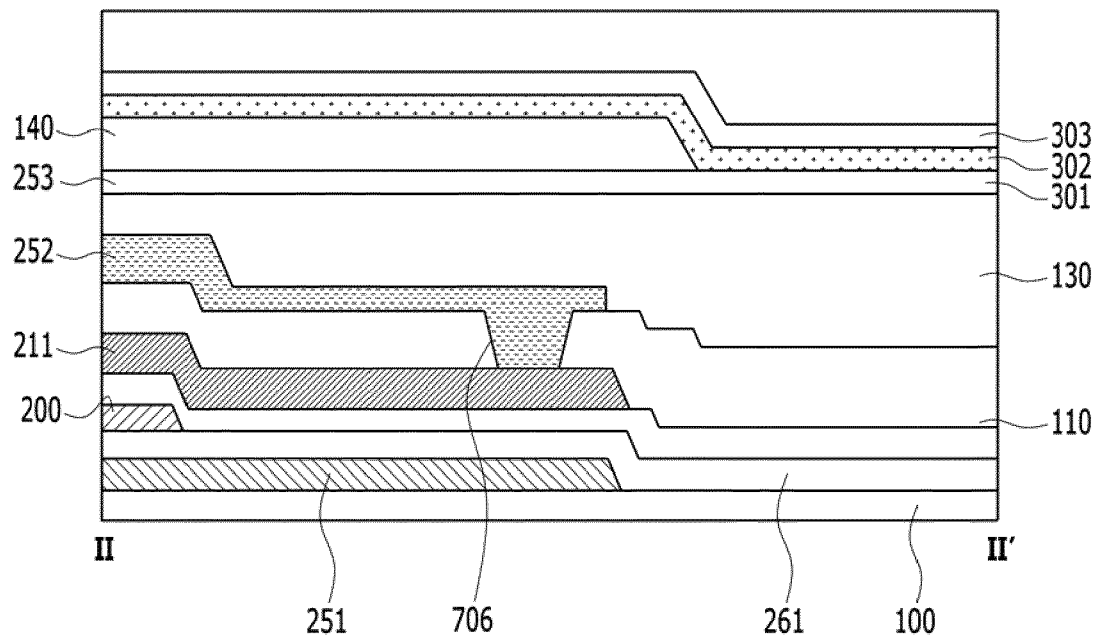
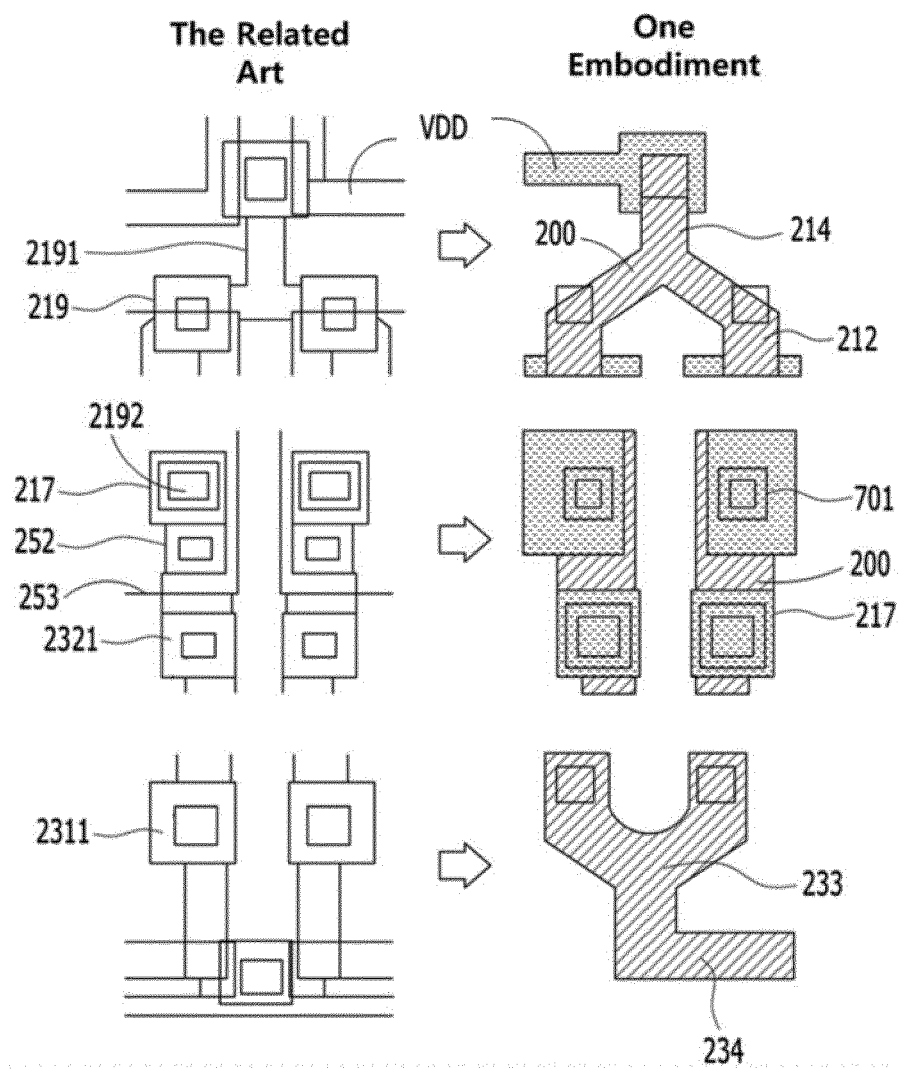


FIG. 4





EUROPEAN SEARCH REPORT

Application Number
EP 17 19 7796

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2016/005804 A1 (OH KUM-MI [KR] ET AL) 7 January 2016 (2016-01-07) * paragraphs [0032], [0035] - [0044], [0053] - [0073]; figures 4,6A-14B *	1,2,4,5, 7,8,11 3,9,10, 12	INV. H01L27/32
A	----- US 2009/295773 A1 (TANEDA TAKAYUKI [JP] ET AL) 3 December 2009 (2009-12-03) * paragraphs [0073] - [0078], [0097] - [0099]; figures 4b,15, 17, 19 *	1,2,4-6	
X	----- US 2007/069205 A1 (JINNO YUSHI [JP]) 29 March 2007 (2007-03-29) * paragraphs [0025], [0030]; figures 2B,4,5 *	1,2,4,5	
A	----- EP 3 029 733 A1 (LG DISPLAY CO LTD [KR]) 8 June 2016 (2016-06-08) * paragraphs [0076] - [0086]; figure 2D *	1-12	

			TECHNICAL FIELDS SEARCHED (IPC)
			H01L
The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 15 March 2018	Examiner Faou, Marylène
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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EPO FORM 1503 03.02 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 17 19 7796

5 This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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15-03-2018

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2016005804 A1	07-01-2016	CN 105280137 A	27-01-2016
		KR 20160004843 A	13-01-2016
		US 2016005804 A1	07-01-2016
US 2009295773 A1	03-12-2009	CN 101593768 A	02-12-2009
		JP 4582195 B2	17-11-2010
		JP 2009288467 A	10-12-2009
		TW 200951925 A	16-12-2009
		US 2009295773 A1	03-12-2009
		US 2014209917 A1	31-07-2014
US 2007069205 A1	29-03-2007	JP 2007114726 A	10-05-2007
		KR 20070034948 A	29-03-2007
		TW 200718278 A	01-05-2007
		US 2007069205 A1	29-03-2007
EP 3029733 A1	08-06-2016	EP 3029733 A1	08-06-2016
		US 2016163780 A1	09-06-2016

FIG. 1

