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(54) ORGANIC LIGHT-EMITTING DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME

(57) An organic light-emitting display device and a method of fabricating the same, which may simplify the configuration of the organic light-emitting display device and may reduce the number of mask processes. The organic light-emitting display device includes a thin film transistor (100) disposed on a substrate (101) having a plurality of trenches (101a), a light-emitting diode (130) connected to the thin film transistor, an upper auxiliary electrode (166) connected to any one of an anode and a cathode of the light-emitting diode, and a lower auxiliary electrode (162) connected to the upper auxiliary electrode. The lower auxiliary electrode is embedded in a trench of the substrate, thus ensuring structural stability.

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Description

[0001] This application claims the benefit of Korean Patent Application No.2015-0188439, filed on December 29, 2016.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to an organic light-emitting display device and a method of fabricating the same, and more particularly to an organic light-emitting display device and a method of fabricating the same, which may simplify the configuration of the organic light-emitting display device and may reduce the number of mask processes.

Discussion of the Related Art

[0003] An image display device, which realizes various information on a screen, is the core technology of the information communication age and is being developed to be thinner, lighter, and more portable, and to exhibit higher performance. As one example of a flat panel display device, which has a reduced weight and volume compared to a heavy and bulky cathode ray tube (CRT), an organic light-emitting display (OLED) device, which displays an image by controlling the emission of light from an organic light-emitting layer, is receiving attention. The OLED device is a self-illuminating device and has low power consumption, high response speed, high luminance efficacy, high brightness, and a wide viewing angle.

[0004] In order to fabricate such an OLED device, a mask process using a photomask is performed a plurality of times. Each mask process involves subsequent processes, such as washing, exposure, developing, and etching processes. To this end, whenever an additional mask process is added, the time and costs for the fabrication of the OLED device increase, and the rate of generation of defective products increases, which causes a lower production yield. Therefore, there is the demand for a simplified configuration and a reduction in the number of mask processes in order to reduce production costs and to enhance production yield and production efficiency.

SUMMARY OF THE INVENTION

[0005] Accordingly, the present invention is directed to an organic light-emitting display device and a method of fabricating the same that substantially obviate one or more problems due to limitations and disadvantages of the related art.

[0006] An object of the present invention is to provide an organic light-emitting display device and a method of fabricating the same, which may simplify the configuration of the organic light-emitting display device and may reduce the number of mask processes.

[0007] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0008] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, an organic light-emitting display device includes a thin film transistor disposed on a substrate, a light-emitting diode connected to the thin film transistor, an upper auxiliary electrode connected to any one of an anode and a cathode of the light-emitting diode, and a lower auxiliary electrode connected to the upper auxiliary electrode, wherein the lower auxiliary electrode is embedded in an auxiliary electrode trench of the substrate, thus ensuring structural stability.

[0009] The organic light-emitting display may also comprise a plurality of trenches. A first buffer layer may be formed on the substrate.

[0010] The organic light-emitting display device may further comprise a light shielding layer spanning and aligning with the thin-film transistor, the light shielding layer being embedded in a light shielding trench of the substrate.

[0011] Optionally, the organic light-emitting display may further comprise a heat-resistant buffer layer, and a second buffer layer; wherein the first buffer layer, the heat-resistant buffer layer, and the second buffer layer are sequentially stacked one above another between the light shielding layer and the thin film transistor.

[0012] Preferably, the heat-resistant buffer layer is composed of an organic film material having a lower dielectric constant than those of the first and second buffer layers. The organic light-emitting display device may further comprise a lower pad electrode embedded in a lower pad trench of the substrate and an upper pad electrode connected to the lower pad electrode through the first buffer layer.

[0013] The organic light-emitting display device may further comprises: a signal link located above the lower auxiliary electrode; and a signal pad connected to the signal link,
wherein the first buffer layer, the heat-resistant buffer layer, and the second buffer layer are sequentially stacked one above another between the lower auxiliary electrode and the signal link, and
wherein: the signal pad includes the lower pad electrode and the upper pad electrode; the upper pad electrode is connected to the lower pad electrode through a pad contact hole, and the pad contact hole being located in the first buffer layer and an interlayer insulator film.

[0014] The organic light-emitting display device may further comprise an alignment key embedded in an alignment key trench of the substrate.

[0015] The present invention also relates to a method of fabricating an organic light-emitting display device, the method comprising: providing a substrate having a plurality of trenches in which a lower auxiliary electrode is embedded; forming a thin film transistor on the substrate in which the lower auxiliary electrode has been formed; forming an anode connected to the thin film transistor and an upper auxiliary electrode connected to the lower auxiliary electrode; forming an organic light-emitting layer on the anode; and forming a cathode on the organic light-emitting layer.

[0016] Optionally providing may include: forming a photoresist pattern on the substrate; forming the trenches by etching the substrate using the photoresist pattern; depositing a seed metal throughout a surface of the substrate on which the photoresist pattern remains; removing the photoresist pattern and the seed metal on the photoresist pattern; and forming the lower auxiliary electrode and an alignment key, which are embedded in the trenches, by growing the seed metal.

[0017] Optionally, providing may include: forming, on the substrate, an opaque metal layer and a multi-stepped photoresist pattern on the opaque metal layer; forming the trenches by etching the substrate and the opaque metal layer using the multi-stepped photoresist pattern; ashing the multi-stepped photoresist pattern; forming an alignment key by etching the opaque metal layer using the ashed photoresist pattern; and forming the lower auxiliary electrode embedded in the trench, formed in the substrate in which the alignment key has been formed.

[0018] The fabrication method may further comprises: simultaneously forming a light shielding layer, in an area overlapping the thin film transistor, and the lower auxiliary electrode in respective trenches of the substrate; forming a first buffer layer on the substrate in which the light shielding layer, the lower auxiliary electrode, and the alignment key have been formed; forming, on the first buffer layer, a heat-resistant buffer layer, a second buffer layer, and a semiconductor layer of the thin film transistor, which overlap the light shielding layer, and simultaneously forming the heat-resistant buffer layer and the second buffer layer, which overlap the lower auxiliary electrode; forming a gate insulator pattern and a gate electrode of the thin film transistor on the semiconductor layer of the thin film transistor; forming an interlayer insulator film on the gate electrode of the thin film transistor; and forming source and drain electrodes of the thin film transistor and a signal link on the interlayer insulator film.

[0019] The fabrication method may further comprises: simultaneously forming a light shielding layer, in an area overlapping the thin film transistor, and the lower auxiliary electrode in respective trenches in the substrate; ; forming a first buffer layer on the substrate in which the light shielding layer, the lower auxiliary electrode, and the alignment key have been formed; forming, on the first buffer layer, a heat-resistant buffer layer, a second buffer layer, and a semiconductor layer of the thin film transistor, which overlap the light shielding layer, and simultaneously forming the heat-resistant buffer layer and the second buffer layer, which overlap the lower auxiliary electrode; forming a gate insulator pattern and a gate electrode of the thin film transistor on the semiconductor layer of the thin film transistor; forming an interlayer insulator film on the gate electrode of the thin film transistor; and forming source and drain electrodes of the thin film transistor and a signal link on the interlayer insulator film.

[0020] The fabrication method may further comprise forming a buffer layer on the provided substrate.

[0021] The provided substrate may also have a lower auxiliary electrode embedded and the method may further comprise connecting an upper pad electrode to the embedded lower pad electrode through the buffer layer.

[0022] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

FIG. 1 is a sectional view illustrating a first embodiment of an organic light-emitting display device in accordance with the present invention;

FIG. 2 is a sectional view illustrating a second embodiment of an organic light-emitting display device in accordance with the present invention;

FIGs. 3A to 3D are sectional views illustrating a method of fabricating a light shielding layer, a lower auxiliary electrode, a lower pad electrode, an alignment key, and trenches illustrated in FIG. 1;

FIGs. 4A to 4D are sectional views illustrating a method of fabricating a light shielding layer, a lower auxiliary electrode, a lower pad electrode, an alignment key, and trenches illustrated in FIG. 2;

FIG. 5 is a view comparing a comparative example in which no surface treatment is performed on a substrate and an example in which a surface treatment is performed on a substrate with each other; and

FIGs. 6A to 6H are sectional views illustrating a method of fabricating the organic light-emitting display device of FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

[0024] Hereinafter, embodiments in accordance with the present invention will be described in detail with reference to the accompanying drawings.

[0025] FIG. 1 is a sectional view illustrating an organic light-emitting display device in accordance with the present invention.

[0026] As illustrated in FIG. 1, the organic light-emitting display device in accordance with the present invention includes a switching thin-film transistor (not illustrated), a driving thin-film transistor 100, an organic light-emitting diode 130, a storage capacitor 140, an auxiliary electrode 160, a signal pad 150, and an alignment key 170.

[0027] The driving thin-film transistor 100 includes a gate electrode 106, a source electrode 108, a drain electrode 110, and an oxide semiconductor layer 104. Meanwhile, the switching thin-film transistor has the same configuration as that of the driving thin-film transistor 100, and thus includes the same components as those of the driving thin-film transistor 100.

[0028] The gate electrode 106 is formed on a gate insulator pattern 112, which is the same as the pattern of the gate electrode 106. The gate electrode 106 overlaps the oxide semiconductor layer 104 with the gate insulator pattern 112 interposed therebetween. The gate electrode 106 may be a single layer or multiple layers formed of any one selected from among molybdenum (Mo), aluminum (Al), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), and copper (Cu), or an alloy of them, without being limited thereto.

[0029] The source electrode 108 is connected to the oxide semiconductor layer 104 through a source contact hole 124S, which penetrates an interlayer insulator film 116. The drain electrode 110 is connected to the oxide semiconductor layer 104 through a drain contact hole 124D, which penetrates the interlayer insulator film 116. In addition, the drain electrode 110 is connected to an anode 132 through a pixel contact hole 120, which penetrates a protective film 118 and a planarization layer 148.

[0030] Each of the source electrode 108 and the drain electrode 110 includes a transparent conductive layer 172a and an opaque conductive layer 172b formed on the transparent conductive layer 172a. The transparent conductive layer 172a may be formed of a transparent conductive material, such as indium tin oxide (ITO), and the opaque conductive layer 172b may be a single layer or multiple layers formed of any one selected from among molybdenum (Mo), aluminum (Al), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), and copper (Cu) or an alloy of them, without being limited thereto.

[0031] The oxide semiconductor layer 104 is formed so as to be below the gate insulator pattern 112 and so as to overlap, or extend beyond at least one dimension of, the gate electrode 106, thereby forming a channel between the source electrode 108 and the drain electrode 110. The oxide semiconductor layer 104 is formed of an oxide including at least one metal selected from among Zn, Cd, Ga, In, Sn, Hf and Zr. A first buffer layer 126, a heat-resistant buffer layer 122, and a second buffer layer 128 may be sequentially stacked one above another between the oxide semiconductor layer 104 and a light shielding layer 102 and between a signal link 174 and a lower auxiliary electrode 162, so as to effectively ensure the stability of the device. Here, the heat-resistant buffer layer 122 and the second buffer layer 128 have the same pattern.

[0032] The heat-resistant buffer layer 122 is formed of an organic film material having a lower dielectric constant than those of the first and second buffer layers 126 and 128, for example, acryl resin. The heat-resistant buffer layer 122 is formed below the oxide semiconductor layer 104 of the switching/driving thin-film transistor 100. In addition, the heat-resistant buffer layer 122 is formed below signal links 174, each of which connects at least one signal line, selected from among a gate line, a data line, and a power line, with the signal pad 150. Moreover, the heat-resistant buffer layer 122 is also formed between the signal line and the lower auxiliary electrode 162, which intersects (overlaps) the signal line. In this way, the parasitic capacitance between the signal line, each signal link, and the lower auxiliary electrode 162 embedded in a trench 101a of a substrate 101 and the parasitic capacitance between each electrode of the switching/driving thin-film transistor 100 and the light shielding layer 102 are reduced in proportion to the dielectric constant of the heat-resistant buffer layer 122. In this way, signal interference between the signal line, each signal link, and the lower auxiliary electrode 162 embedded in the trench 101a of the substrate 101 and signal interference between each electrode of the switching/driving thin-film transistor 100 and the light shielding layer 102 may be minimized.

[0033] The second buffer layer 128 is formed on the heat-resistant buffer layer 122 in the same pattern as the heat-resistant buffer layer 122 and serves to prevent the generation of fumes in the heat-resistant buffer layer 122, which is formed of an organic film material. Therefore, the second buffer layer 128 may prevent, for example, deterioration of the thin-film transistor 100 due to such fumes. The second buffer layer 128 is formed of SiNx or SiOx, in the same manner as the first buffer layer 126.

[0034] The light shielding layer 102, which overlaps the oxide semiconductor layer 104, is embedded in the trench 101a of the substrate 101. The light shielding layer 102 may absorb or reflect light introduced from the outside, and therefore may minimize the introduction of light to the oxide semiconductor layer 104. The light shielding layer 102 is formed of an opaque metal, such as Mo, Ti, Al, Cu, Cr, Co, W, Ta, Ni, Au, Ag, Sn, and Zn.

[0035] The storage capacitor 140 includes a storage lower electrode 142 and a storage upper electrode 144, which overlap each other with the interlayer insulator film 116 therebetween. The storage lower electrode 142, which is the same layer as the gate electrode 106, is formed on the gate insulator pattern 112 using the same material as that of the gate electrode 106. The storage upper electrode 144, which is the same layer as the source electrode 108, is formed on the interlayer insulator film 116 using the same material as that of the source electrode 108.

[0036] The light-emitting diode 130 includes the anode

132 connected to the drain electrode 110 of the thin-film transistor 100, an organic light-emitting layer 134 formed on the anode 132, and a cathode 136 formed over the organic light-emitting layer 134.

[0037] The anode 132 is connected to the drain electrode 110, which is exposed through the pixel contact hole 120, which penetrates the protective film 118 and the planarization layer 148. Meanwhile, in the case of a top emission type organic light-emitting display device, the anode 132 takes the form of a stack in which a transparent conductive layer, which is formed of, for example, indium tin oxide (ITO) or indium zinc oxide (IZO), and a metal layer, which is formed of, for example, aluminum (Al), silver (Ag), or APC (Ag;Pb;Cu) are stacked one above another.

[0038] The organic light-emitting layer 134 is formed on the anode 132 in a light-emitting area defined by a bank 138. The organic light-emitting layer 134 is formed by stacking, on the anode 132, a hole-related layer, a light-emitting layer, and an electron-related layer, either in that order or in the reverse order.

[0039] The bank 138 has an inner side surface in contact with the organic light-emitting layer 134, and an outer side surface disposed along the side surface of the anode 132 so as to cover the side surface of the anode 132. As such, because the bank 138 is formed along the rim of the anode 132 except the light-emitting area so as to cover the side surface of the anode 132, the light-emitting area has an island shape. The bank 138 may be formed of an opaque material (e.g. a black material) in order to prevent optical interference between neighboring subpixels. In this case, the bank 138 includes a light shielding formed of at least one selected from among a color pigment, organic black materials and carbon materials.

[0040] The cathode 136 is formed on the upper surface and the side surface of the organic light-emitting layer 134 and the bank 138 so as to be opposite the anode 132 with the organic light-emitting layer 134 interposed therebetween. In the case of a top emission type organic light-emitting display device, the cathode 136 is formed of a transparent conductive oxide (TCO).

[0041] The auxiliary electrode 160 is formed in order to reduce the resistance of the cathode 136, which increases as the area of the organic light-emitting display device increases. The auxiliary electrode 160 includes the lower auxiliary electrode 162, an intermediate auxiliary electrode 164, and an upper auxiliary electrode 166.

[0042] The lower auxiliary electrode 162 is embedded in the trench 101a of the substrate 101 and is formed of the same material as that of the light shielding layer 102. Because the lower auxiliary electrode 162 is embedded in the trench 101a of the substrate 101 so as to be formed below the heat-resistant buffer layer (thick film), which prevents signal interference, unlike a conventional lower auxiliary electrode, which is formed on a thick organic film, process failure, such as erosion, may be prevented, which may ensure structural stability.

[0043] The intermediate auxiliary electrode 164 is electrically connected to the lower auxiliary electrode 162, which is exposed through a first auxiliary contact hole 168a, which penetrates the first buffer layer 126 and the interlayer insulator film 116. The intermediate auxiliary electrode 164 includes the transparent conductive layer 172a and the opaque conductive layer 172b formed on the transparent conductive layer 172a.

[0044] The upper auxiliary electrode 166 is electrically connected to the intermediate auxiliary electrode 164, which is exposed through a second auxiliary contact hole 168b, which penetrates the protective film 118 and the planarization layer 148. The upper auxiliary electrode 166 is formed in the same plane as the anode 132 using the same material as that of the anode 132.

[0045] A partition 146, which is formed on the upper auxiliary electrode 166, has an inversely tapered shape, the width of which gradually increases with decreasing distance to the upper surface of the partition 146. Through the provision of the partition 146, the organic light-emitting layer 134, which is straightly grown, is formed only on the upper surface of the partition 146 and the upper surface of the anode 132, which is located in the light-emitting area exposed by the bank 138. On the other hand, because the cathode 136, which has step coverage superior to that of the organic light-emitting layer 134, is also formed on the side surfaces of the partition 146 and the bank 138, the cathode 136 may be easily brought into contact with the upper auxiliary electrode 166. Meanwhile, although the case where the upper auxiliary electrode 162 is connected to the cathode 136 has been described by way of example, the upper auxiliary electrode 162 may be connected to the anode 132.

[0046] The signal pad 150 is connected to at least one signal line among the gate line, the data line, and the power line through the signal link 174. The signal pad 150 includes a lower pad electrode 152 and an upper pad electrode 154.

[0047] The lower pad electrode 152 is formed of the same material as that of the light shielding layer 102, and is embedded in the trench 101a of the substrate 101. The upper pad electrode 154 is electrically connected to the lower pad electrode 152, which is exposed through a pad contact hole 156, which penetrates the first buffer layer 126 and the interlayer insulator film 116. The upper pad electrode 154 includes the transparent conductive layer 172a. The upper pad electrode 154 is exposed outward through a pad hole 158, which penetrates the first protective film 118.

[0048] The alignment key 170 serves as a rule for positional alignment between the substrate 101 and a fabrication device (e.g. a photomask or a shadow mask) that is used to form a thin film on the substrate 101. The alignment key 170 may be embedded in the trench 101a of the substrate 101, in the same manner as the light shielding layer 102, the lower auxiliary electrode 162, and the lower pad electrode 152 as illustrated in FIG. 1, or may be formed on the substrate 101 in the state in which each of the light shielding layer 102, the lower auxiliary electrode 162, and the lower pad electrode 152 is embedded in the trench 101a.

[0049] The alignment key 170 illustrated in FIG. 1 is formed via electroplating or electroless plating as illustrated in FIGs. 3A to 3D. Specifically, after a photoresist pattern 182 is formed on the substrate 101 via a photolithography process as illustrated in FIG. 3A, the substrate 101 is patterned via an etching process in which the photoresist pattern 182 is used as a mask, whereby a plurality of trenches 101a is formed in the substrate 101. Subsequently, as illustrated in FIG. 3B, a seed metal 184 is deposited at room temperature on the substrate 101 on which the photoresist pattern 182 remains. Here, the seed metal 184 is a low-resistance metal, such as silver (Ag), gold (Au), copper (Cu), nickel (Ni), tin (Sn), or zinc (Zn). Subsequently, as illustrated in FIG. 3C, the photoresist pattern 182 and the seed metal 184 on the photoresist pattern 182 are removed via the stripping of the photoresist pattern 182. Subsequently, as the seed metal 184 remaining in the trenches 101a is grown, as illustrated in FIG. 3D, the light shielding layer 102, the lower auxiliary electrode 162, the lower pad electrode 152, and the alignment key 170 are simultaneously formed in the trenches 101a. Meanwhile, the light shielding layer 102, the lower auxiliary electrode 162, the lower pad electrode 152, and the alignment key 170, which are formed of the seed metal (e.g. Cu) using electroplating or electroless plating, have the same resistivity as a thin layer, which is formed of copper Cu via deposition.

[0050] The alignment key 170 illustrated in FIG. 2 is formed using a multi-stepped photoresist pattern 186 as illustrated in FIGs. 4A to 4D. Specifically, as illustrated in FIG. 4A, after an opaque metal layer 170a is deposited throughout the surface of the substrate 101, the multi-stepped photoresist pattern 186 is formed on the opaque metal layer 170a via a photolithography process using a halftone mask. The multi-stepped photoresist pattern 186 includes a first photoresist pattern 186a having a first thickness and a second photoresist pattern 186b having a second thickness, which is greater than the first thickness. By etching the opaque metal layer 170a and the substrate 101 via an etching process in which the multi-stepped photoresist pattern 186 is used as a mask, as illustrated in FIG. 4B, the opaque metal layer 170a remains between the multi-stepped photoresist pattern 186 and the substrate 101, and the trenches 101a are formed in the substrate 101.

[0051] Subsequently, by ashing the photoresist pattern 186, the second photoresist pattern 186b is reduced in thickness, and the first photoresist pattern 186a is removed. By etching the opaque metal layer 170a using the second photoresist pattern 186b, having a reduced thickness, as a mask, as illustrated in FIG. 4C, the remaining opaque metal layer 170a excluding the opaque metal layer 170a located below the second photoresist pattern 186b is removed. The remaining opaque metal layer 170a below the second photoresist pattern 186b becomes the alignment key 170. The photoresist pattern 186b remaining on the alignment key 170, as illustrated in FIG. 4D, is removed via a stripping process. After the alignment key 170 is formed, an opaque metal layer is deposited on the substrate 101 in which the trenches 101a have been formed, and thereafter is patterned via a photolithography process and an etching process. Thereby, the light shielding layer 102, the lower auxiliary electrode 162, and the lower pad electrode 152 are simultaneously formed in the trenches 101a.

[0052] Meanwhile, an etching process using the photoresist pattern 182 as a mask is required in order to from the trenches 101a in the substrate 101. However, in the case of a comparative example in which the adhesive force between the substrate 101 and the photoresist pattern 182 is not good, as illustrated in FIG. 5, an etching solution permeates between the substrate 101 and the photoresist pattern 182. Thereby, an undercut having a first width D1 is formed between the side surface of the substrate 101 and the photoresist pattern 182. The width of the substrate 101 located between the neighboring trenches 101a may be reduced, thus causing short circuits between electrodes embedded in the trenches 101a and extending the tails of the electrodes in the trenches 101a, which makes it difficult to achieve high resolution.

[0053] On the other hand, in an example of the present invention, prior to applying a photoresist onto the substrate 101, hexamethyldisilazane (HMDS) is applied onto the substrate 101 for the surface treatment of the substrate 101. Because HMDS serves to increase adhesive force between the substrate 101 and the photoresist, upon etching of the substrate 101, it is possible to prevent an etching solution from permeating between the substrate 101 and the photoresist pattern 182. Thereby, an undercut having a second width D2, which is smaller than that of the comparative example, is formed between the side surface of the substrate 101 and the photoresist pattern 182. In this way, the width of the substrate 101 located between the neighboring trenches 101a may be greater than that in the comparative example, thus preventing short circuits between electrodes embedded in the trenches 101a and shortening the tails of the electrodes in the trenches 101a, which makes it easy to achieve high resolution.

[0054] FIGs. 6A to 6H are sectional views illustrating a method of fabricating the organic light-emitting display device of FIG. 1. Meanwhile, because the method of fabricating the organic light-emitting display device of FIG. 2 is the same as the method of fabricating the organic light-emitting display device of FIG. 1 from the formation of the first buffer layer 126, a description related to the method of fabricating the organic light-emitting display device of FIG. 2 is omitted therein.

[0055] Referring to FIG. 6A, as described above with reference to FIGs. 3A to 3D, the trenches 101a are formed in the substrate 101, and the light shielding layer 102, the lower auxiliary electrode 162, the lower pad electrode 152, and the alignment key 170 are embedded in the trenches 101a.

[0056] Referring to FIG. 6B, the first buffer layer 126 is formed on the substrate 101 in which the light shielding layer 102, the lower auxiliary electrode 162, the lower pad electrode 152, and the alignment key 170 have been formed in the trenches 101a, and the heat-resistant buffer layer 122, the second buffer layer 128, and the oxide semiconductor layer 104 are formed on the first buffer layer 126.

[0057] Specifically, the first buffer layer 126, the heat-resistant buffer layer 122, the second buffer layer 128, and the oxide semiconductor layer 104 are formed via deposition on the substrate 101 in which the light shielding layer 102, the lower auxiliary electrode 162, the lower pad electrode 152, and the alignment key 170 have been formed in the trenches 101a. Subsequently, the heat-resistant buffer layer 122, the second buffer layer 128, and the oxide semiconductor layer 104 are selectively etched via a photolithography process using a halftone mask and an etching process. Thereby, the heat-resistant buffer layer 122, the second buffer layer 128, and the oxide semiconductor layer 104, which have the same pattern, are sequentially stacked one above another in the area at which they overlap the light shielding layer 102, and the heat-resistant buffer layer 122 and the second buffer layer 128 are sequentially stacked one above another in the area at which they overlap the lower auxiliary electrode 162.

[0058] In this way, the heat-resistant buffer layer 122 and the second buffer layer 128 are formed via the same mask process as the oxide semiconductor layer 104. In this case, because the heat-resistant buffer layer 122, which has different etching properties from those of the second buffer layer 128 and the oxide semiconductor layer 104, is disposed below the second buffer layer 128 and the oxide semiconductor layer 104, process failure, such as the occurrence of undercutting may be prevented after the etching process, and process stability may be acquired.

[0059] Referring to FIG. 6C, the gate insulator pattern 112, the lower storage electrode 142, and the gate electrode 106 are formed on the substrate 101 on which the heat-resistant buffer layer 122, the second buffer layer 128, and the oxide semiconductor layer 104 have been formed.

[0060] Specifically, a gate insulator film is formed on the substrate 101 on which the heat-resistant buffer layer 122, the second buffer layer 128, and the oxide semiconductor layer 104 have been formed, and a gate metal layer is formed on the gate insulator film via deposition, such as sputtering. The gate insulator film is formed of an inorganic insulation material, such as SiOx or SiNx. The gate metal layer may be a single layer formed of a metal, such as Mo, Ti, Cu, AlNd, Al, or Cr, or an alloy thereof, or may be multiple layers using the same. Subsequently, by simultaneously patterning the gate metal layer and the gate insulator film via a photolithography process and an etching process, each of the gate electrode 106 and the lower storage electrode 142 is formed in the same pattern as the gate insulator pattern 112.

[0061] Referring to FIG. 6D, the interlayer insulator film 116, which has the source and drain contact holes 124S and 124D, the first pad contact hole 156, and the first auxiliary contact hole 168a, is formed on the substrate 101 on which the gate electrode 106 and the lower storage electrode 142 are formed.

[0062] Specifically, the interlayer insulator film 116 is formed on the substrate 101, on which the gate electrode 106 and the lower storage electrode 142 are formed, via deposition, such as PECVD. Subsequently, by patterning the interlayer insulator film 116 and the first buffer layer 126 via a photolithography process and an etching process, the source and drain contact holes 124S and 124D, the first pad contact hole 156, and the first auxiliary contact hole 168a are formed.

[0063] Referring to FIG. 6E, the source electrode 108, the drain electrode 110, the upper storage electrode 144, and the upper pad electrode 154 are formed on the interlayer insulator film 116, which has the source and drain contact holes 124S and 124D, the first pad contact hole 156, and the first auxiliary contact hole 168a.

[0064] Specifically, the transparent conductive layer 172a and the opaque conductive layer 174 are sequentially deposited via, for example, sputtering on the interlayer insulator film 116, which has the source and drain contact holes 124S and 124D, the first pad contact hole 156, and the first auxiliary contact hole 168a. Subsequently, by patterning transparent conductive layer 172a and the opaque conductive layer 174 via a photolithography process using a halftone mask and an etching process, the source electrode 108, the drain electrode 110, the upper storage electrode 144, and the upper pad electrode 154 are formed. At this time, the source electrode 108, the drain electrode 110, and the upper storage electrode 144 take the form of a stack including the transparent conductive layer 172a and the opaque conductive layer 174, and the upper pad electrode 154 is formed of the transparent conductive layer 172a, which has high corrosion resistance and acid resistance.

[0065] Referring to FIG. 6F, the protective film 118 and the planarization layer 148, which have the pixel contact hole 120 and the second auxiliary contact hole 168b, are formed on the interlayer insulator film 116, on which the source electrode 108, the drain electrode 110, the upper storage electrode 144, and the upper pad electrode 154 have been formed.

[0066] Specifically, the protective film 118 and the planarization layer 148 are sequentially formed on the interlayer insulator film 116, on which the source electrode 108, the drain electrode 110, the upper storage electrode 144, and the upper pad electrode 154 have been formed. The protective film 118 is formed of an inorganic insulation material, such as SiOx or SiNx, and the planarization layer 148 is formed of an organic insulation material, such as photoacryl. Subsequently, by selectively etching the protective film 118 and the planarization layer 148 via a photolithography process using a halftone mask and an etching process, the pixel contact hole 120 and the second auxiliary contact hole 168b are formed. The pixel contact hole 120 penetrates the protective film 118 and the planarization layer 148 so as to expose the drain electrode 110, and the second auxiliary contact hole 168b penetrates the protective film 118 and the planarization layer 148 so as to expose the intermediate auxiliary electrode 164. Then, the planarization layer 148 is selectively removed from the top of the signal pad 150 so that the protective film 118 on the top of the signal pad 150 is exposed.

[0067] Referring to FIG. 6G, the anode 132, the bank 138, and the pad hole 158 are formed on the substrate 101 on which the protective film 118 and the planarization layer 148, which have the pixel contact hole 120 and the second auxiliary contact hole 168b, have been formed.

[0068] Specifically, an opaque conductive film and a bank photosensitive film are applied throughout the surface of the substrate 101 on which the protective film 118 has been formed. Subsequently, by patterning the bank photosensitive film, the opaque conductive film, and the protective film 118 via a photolithography process using a halftone mask and an etching process, the anode 132, the bank 138, and the pad hole 158 are formed.

[0069] Referring to FIG. 6H, the partition 146, the organic light-emitting layer 134, and the cathode 136 are sequentially formed on the substrate 101, which has the anode 132, the bank 138, and the pad hole 158.

[0070] Specifically, after a partition photosensitive film is applied onto the substrate having the anode 132, the bank 138, and the pad hole 158, the partition photosensitive film is patterned via a photolithography process so as to form the inversely tapered partition 146. Subsequently, the organic light-emitting layer 134 is formed in the light-emitting area exposed by the bank 138, and the cathode 136 is formed on the substrate 101 on which the organic light-emitting layer 134 has been formed.

[0071] As described above, in the organic light-emitting display device in accordance with the present invention, the light shielding layer 102 and the lower auxiliary electrode 162 are formed via the same single mask process, and the oxide semiconductor layer 104, the heat-resistant buffer layer 122, and the second buffer layer 128 are formed via the same single mask process. In this way, the organic light-emitting display device in accordance with the present invention may reduce the number of mask processes by a total of at least 2 processes compared to the prior art, thereby achieving enhanced productivity and reduced costs.

[0072] In addition, in the present invention, because the lower auxiliary electrode 162 is embedded in the trench 101a of the substrate 101 and the heat-resistant buffer layer 122 is disposed on the substrate 101, the heat-resistant buffer layer may prevent corrosion failure of a signal line including the lower auxiliary electrode 162, thereby ensuring structural stability.

[0073] Meanwhile, although the present invention has described the case where the semiconductor layer 104 of the driving thin-film transistor 100 is formed of an oxide by way of example, the semiconductor layer 104 of the driving thin-film transistor 100 may be formed of polysilicon.

[0074] It will be apparent to those skilled in the art that the present invention described above is not limited to the embodiments described above and the accompanying drawings, and various substitutions, modifications, and alterations may be devised within the scope of the present invention, which is defined by the appended claims.

[0075] The following is a list of aspects of the present invention.

Aspect 1. An organic light-emitting display device comprising:

- a substrate having a plurality of trenches;
- a thin film transistor disposed on the substrate;
- a light-emitting diode connected to the thin film transistor;
- an upper auxiliary electrode connected to any one of an anode and a cathode of the light-emitting diode; and
- a lower auxiliary electrode embedded in the trench and connected to the upper auxiliary electrode.

Aspect 2. The device according to aspect 1, further comprising:

- a light shielding layer located in an area overlapping the thin-film transistor and embedded in the trench; and
- a first buffer layer, a heat-resistant buffer layer, and a second buffer layer sequentially stacked one above another between the light shielding layer and the thin film transistor.

Aspect 3. The device according to aspect 2, wherein the heat-resistant buffer layer is composed of an organic film material having a lower dielectric constant than those of the first and second buffer layers.

Aspect 4. The device according to aspect 3, further comprising:

- a signal link located above the lower auxiliary electrode; and
- a signal pad connected to the signal link,

wherein the first buffer layer, the heat-resistant buffer layer, and the second buffer layer are sequentially stacked one above another between the lower auxiliary electrode and the signal link, and

wherein the signal pad includes:

- a lower pad electrode embedded in the trench; and an upper pad electrode connected to the lower pad electrode exposed through a pad contact hole, the pad contact hole penetrating the first buffer layer and an interlayer insulator film.

Aspect 5. The device according to aspect 4, further comprising an alignment key embedded in the trench, or disposed on the substrate.

Aspect 6. A method of fabricating an organic light-emitting display device, the method comprising:

providing a substrate having a plurality of trenches in which a lower auxiliary electrode is embedded;
forming a thin film transistor on the substrate in which the lower auxiliary electrode has been formed;
forming an anode connected to the thin film transistor and an upper auxiliary electrode connected to the lower auxiliary electrode;
forming an organic light-emitting layer on the anode; and
forming a cathode on the organic light-emitting layer.

Aspect 7. The method according to aspect 6, wherein the providing includes:

forming a photoresist pattern on the substrate;
forming the trenches by etching the substrate using the photoresist pattern;
depositing a seed metal throughout a surface of the substrate on which the photoresist pattern remains;
removing the photoresist pattern and the seed metal on the photoresist pattern; and
forming the lower auxiliary electrode and an alignment key embedded in the trenches by growing the seed metal.

Aspect 8. The method according to aspect 6, wherein the providing includes:

Forming, on the substrate, an opaque metal layer and a multi-stepped photoresist pattern on the opaque metal layer;
forming the trenches by etching the substrate and the opaque metal layer using the multi-stepped photoresist pattern;
ashing the multi-stepped photoresist pattern;
forming an alignment key by etching the opaque metal layer using the ashed photoresist pattern; and
forming the lower auxiliary electrode embedded in the trench, formed in the substrate in which the alignment key has been formed.

Aspect 9. The method according to aspect 7, further comprising:

forming a light shielding layer, which is disposed in an area overlapping the thin film transistor and is embedded in the trench, simultaneously with formation of the lower auxiliary electrode;
forming a first buffer layer on the substrate in which the light shielding layer, the lower auxiliary electrode, and the alignment key have been formed;
forming, on the first buffer layer, a heat-resistant buffer layer, a second buffer layer, and a semiconductor layer of the thin film transistor, which overlap the light shielding layer, and simultaneously forming the heat-resistant buffer layer and the second buffer layer, which overlap the lower auxiliary electrode;
forming a gate insulator pattern and a gate electrode of the thin film transistor on the semiconductor layer of the thin film transistor;
forming an interlayer insulator film on the gate electrode of the thin film transistor; and
forming source and drain electrodes of the thin film transistor and a signal link on the interlayer insulator film.

Aspect 10. The method according to aspect 8, further comprising:

forming a light shielding layer, which is disposed in an area overlapping the thin film transistor and is embedded in the trench, simultaneously with formation of the lower auxiliary electrode;
forming a first buffer layer on the substrate in which the light shielding layer, the lower auxiliary electrode, and the alignment key have been formed;
forming, on the first buffer layer, a heat-resistant buffer layer, a second buffer layer, and a semiconductor layer of the thin film transistor, which overlap the light shielding layer, and simultaneously forming the heat-resistant buffer layer and the second buffer layer, which overlap the lower auxiliary electrode;
forming a gate insulator pattern and a gate electrode of the thin film transistor on the semiconductor layer of the thin film transistor;
forming an interlayer insulator film on the gate electrode of the thin film transistor; and
forming source and drain electrodes of the thin film transistor and a signal link on the interlayer insulator film.

Claims

1. An organic light-emitting display device comprising:

a substrate (101) having a plurality of trenches (101a);
a thin film transistor (100) disposed on the substrate (101) ;
a light-emitting diode (130) connected to the thin film transistor (100);
an upper auxiliary electrode (166) connected to any one of an anode (132) and a cathode (136) of the light-emitting diode (130); and
a lower auxiliary electrode (162) embedded in an auxiliary electrode trench of the substrate and connected to the upper auxiliary electrode (166).

2. The organic light-emitting display device of claim 1, further comprising a first buffer layer (126) formed on the substrate (101).

3. The organic light-emitting display device of claim 2, further comprising a light shielding layer (102) overlapping with the thin-film transistor (100), wherein the light shielding layer (102) is embedded in a light shielding trench of the substrate (101).

4. The organic light-emitting display device of claim 3, further comprising:

a heat-resistant buffer layer (122), and
a second buffer layer (128);
wherein the first buffer layer (126), the heat-resistant buffer layer (122), and the second buffer layer (128) are sequentially stacked one above another between the light shielding layer (102) and the thin film transistor (100).

5. The organic light-emitting display device of claim 4, wherein the heat-resistant buffer layer (122) is composed of an organic film material having a lower dielectric constant than those of the first (126) and second buffer layers (128).

6. The organic light-emitting display device of any one of the preceding claims that is dependent on claim 2, further comprising a lower pad electrode (152) embedded in a lower pad trench of the substrate (101) and an upper pad electrode (154) connected to the lower pad electrode (152) through the first buffer layer (126).

7. The organic light-emitting display device of claim 6, further comprising:

a signal link (174) located above the lower auxiliary electrode (162); and
a signal pad (150) connected to the signal link, wherein the first buffer layer (126), the heat-resistant buffer layer (122), and the second buffer layer (128) are sequentially stacked one above another between the lower auxiliary electrode (162) and the signal link (174), and
wherein:

the signal pad (150) includes the lower pad electrode (152) and the upper pad electrode (154);
the upper pad electrode (154) is connected to the lower pad electrode (152) through a pad contact hole (156), and
the pad contact hole (156) being located the first buffer layer (126) and an interlayer insulator film (116).

8. The organic light-emitting display device of claims 1 to 7, further comprising an alignment key (170) embedded in an alignment key trench of the substrate (101), or disposed on the substrate (101).

9. A method of fabricating an organic light-emitting display device, the method comprising:

Providing a substrate (101) having a plurality of trenches (101a) in which a lower auxiliary electrode is embedded (162);
forming a thin film transistor (100) on the substrate (101) in which the lower auxiliary electrode (162) has been formed;
forming an anode (132) connected to the thin film transistor (100) and an upper auxiliary electrode (166) connected to the lower auxiliary electrode (162);
forming an organic light-emitting layer (134) on the anode; and
forming a cathode (136) on the organic light-emitting layer (134).

10. The method according to claim 9, wherein the providing includes:

forming a photoresist pattern (182) on the substrate (101) ;
forming the trenches by etching the substrate (101) using the photoresist pattern (182);
depositing a seed metal (184) throughout a surface of the substrate (101) on which the photoresist pattern (182) remains;
removing the photoresist pattern (182 and the seed metal on the photoresist pattern; and
forming the lower auxiliary electrode (162) and an alignment key (170), which are embedded in the trenches, by growing the seed metal.

11. The method according to claim 9, wherein the providing includes:

forming, on the substrate, an opaque metal layer and a multi-stepped photoresist pattern (186) on the opaque metal layer (170a);

forming the trenches (101a) by etching the substrate and the opaque metal layer (170a) using the multi-stepped photoresist pattern (186);
ashing the multi-stepped photoresist pattern (186);
forming an alignment key (170) by etching the opaque metal layer (170a) using the ashed photoresist pattern; and
forming the lower auxiliary electrode (162) in the trench formed in the substrate in which the alignment key (170) has been formed.

12. The method according to claim 10, further comprising:

simultaneously forming a light shielding layer (102), in an area overlapping the thin film transistor (100), and the lower auxiliary electrode (162) in respective trenches in the substrate (101);
forming a first buffer layer (126) on the substrate (101) in which the light shielding layer (102), the lower auxiliary electrode (162), and the alignment key (170) have been formed;
forming, on the first buffer layer (126), a heat-resistant buffer layer (122), a second buffer layer (128), and a semiconductor layer (104) of the thin film transistor (101) which overlap the light shielding layer (102), and simultaneously forming the heat-resistant buffer layer (122) and the second buffer layer (128), which overlap the lower auxiliary electrode (160);
forming a gate insulator pattern (112) and a gate electrode (106) of the thin film transistor (100) on the semiconductor layer (104) of the thin film transistor (100);
forming an interlayer insulator film (116) on the gate electrode (106) of the thin film transistor (100); and
forming source (108) and drain (110) electrodes of the thin film transistor (100) and a signal link (174) on the interlayer insulator film (116).

13. The method according to claim 11, further comprising:

simultaneously forming a light shielding layer (102), in an area overlapping the thin film transistor (100), and the lower auxiliary electrode (162) in respective trenches of the substrate;
forming a first buffer layer (126) on the substrate (101) in which the light shielding layer (102), the lower auxiliary electrode (162), and the alignment key (170) have been formed;
forming, on the first buffer layer (126), a heat-resistant buffer layer (122), a second buffer layer (128), and a semiconductor layer (104) of the thin film transistor (100), which overlap the light shielding layer (102), and simultaneously forming the heat-resistant buffer layer (122) and the second buffer layer (128), which overlap the lower auxiliary electrode (162);
forming a gate insulator pattern (112) and a gate electrode (106) of the thin film transistor (100) on the semiconductor layer (104) of the thin film transistor (100);
forming an interlayer insulator film (116) on the gate electrode (106) of the thin film transistor (100); and
forming source (108) and drain (110) electrodes of the thin film transistor (100) and a signal link (174) on the interlayer insulator film (116).

14. The method of fabricating an organic light-emitting display device of claim 9, further comprising forming a buffer layer on the provided substrate (101).

15. The method of fabricating an organic light-emitting display device of claim 9, wherein the provided substrate (101) has a lower pad electrode (152) embedded, and the method further includes connecting an upper pad electrode (154) to the lower pad electrode (152) through the buffer layer.

FIG. 1

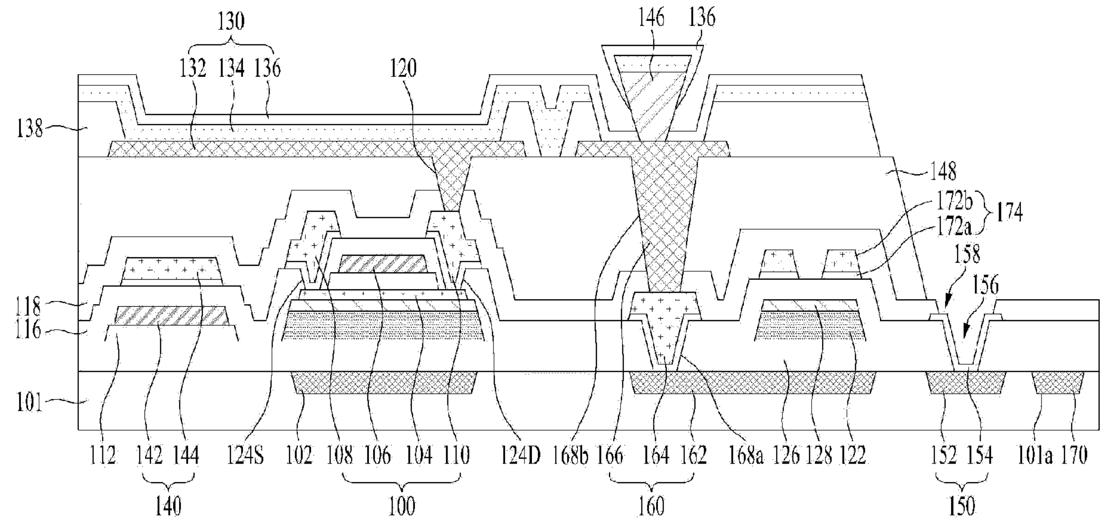
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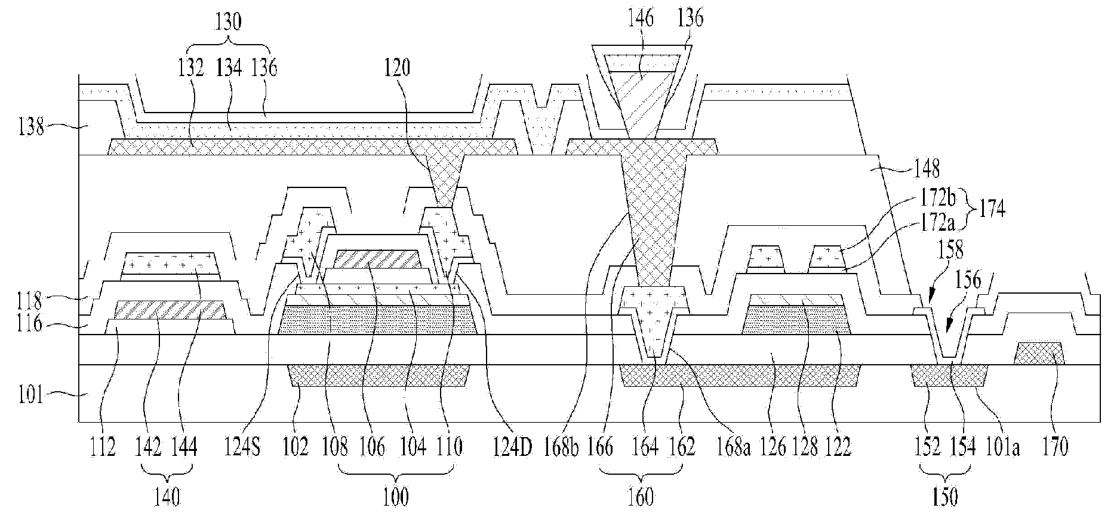
FIG. 2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124D 168b 166 164 162 168a 126 128 122
152 154 101a 170
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FIG. 3A

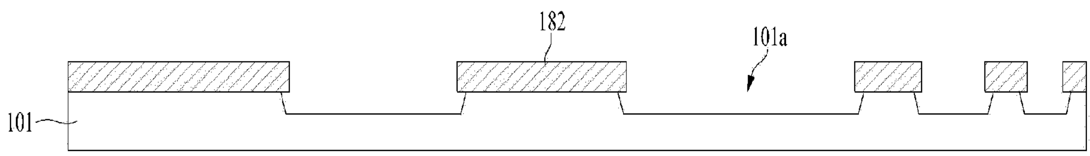

FIG. 3B

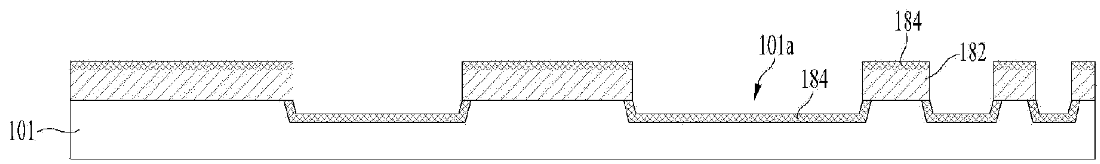

FIG. 3C

FIG. 3D

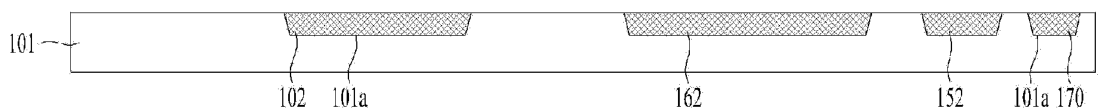

FIG. 4A

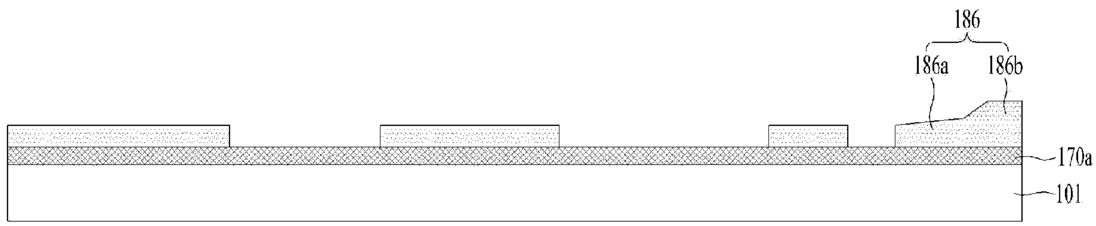

FIG. 4B

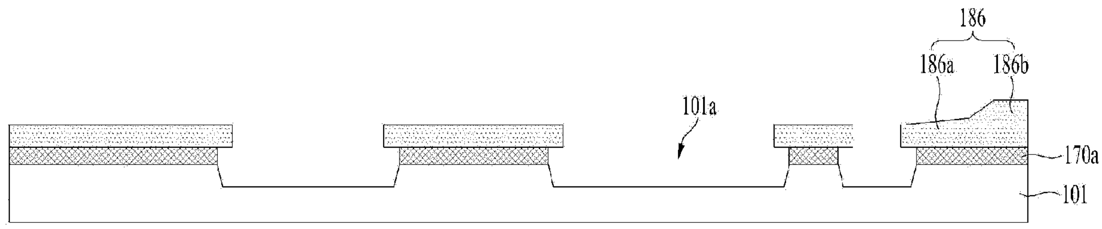

FIG. 4C

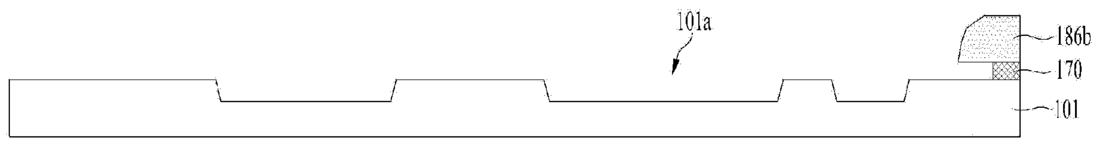

FIG. 4D

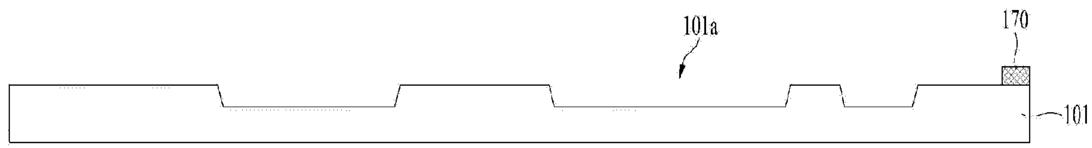

FIG. 5

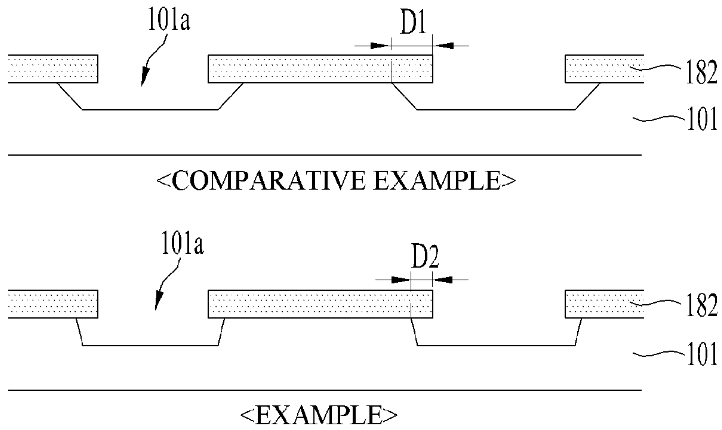

FIG. 6A

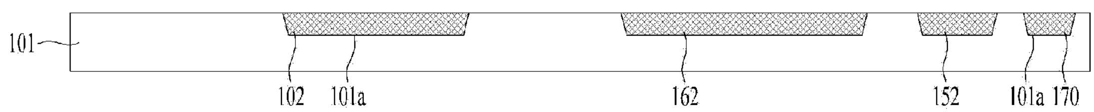

FIG. 6B

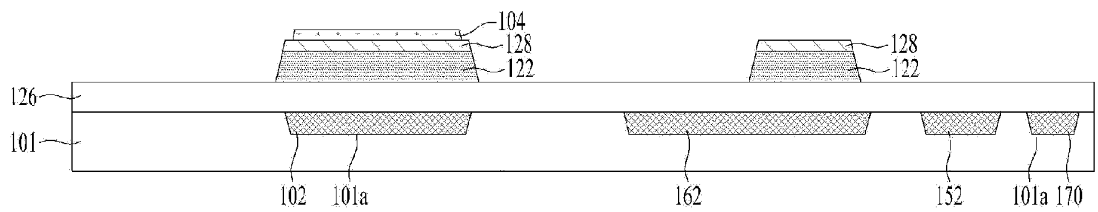

FIG. 6C

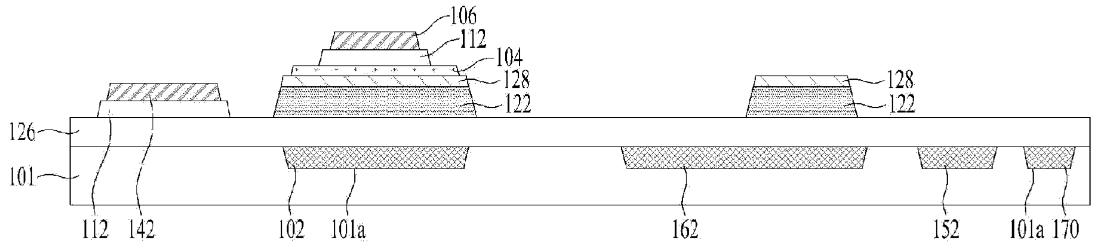

FIG. 6D

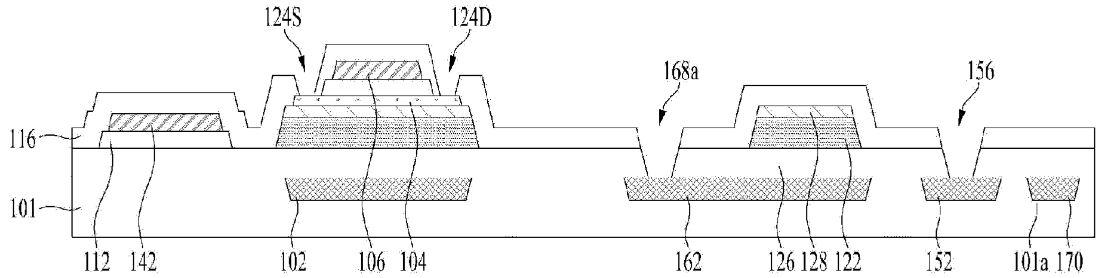

FIG. 6E

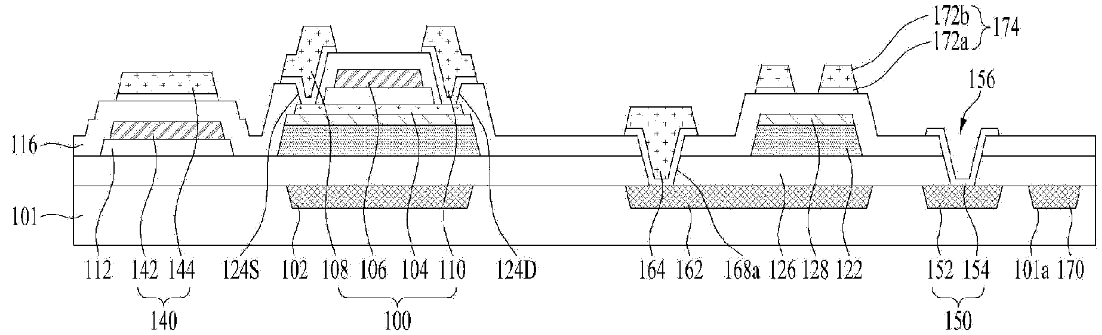

FIG. 6F

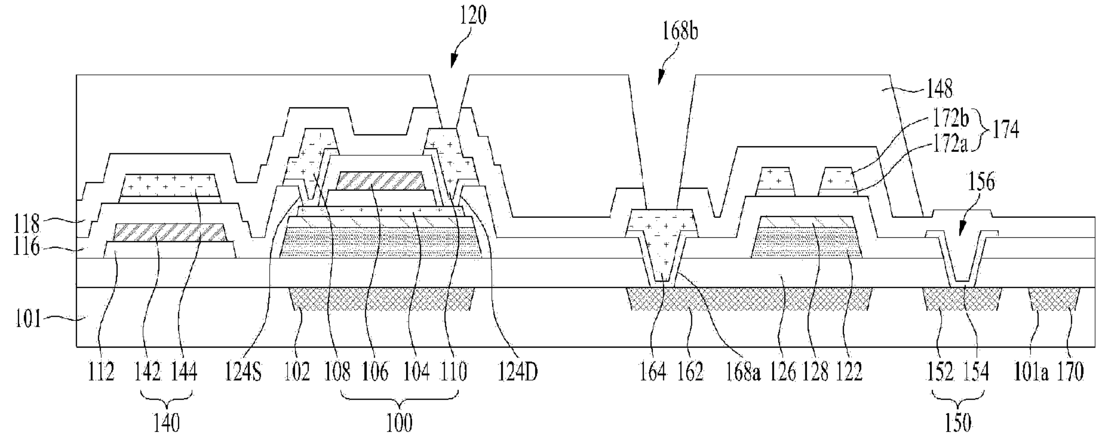
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FIG. 6G

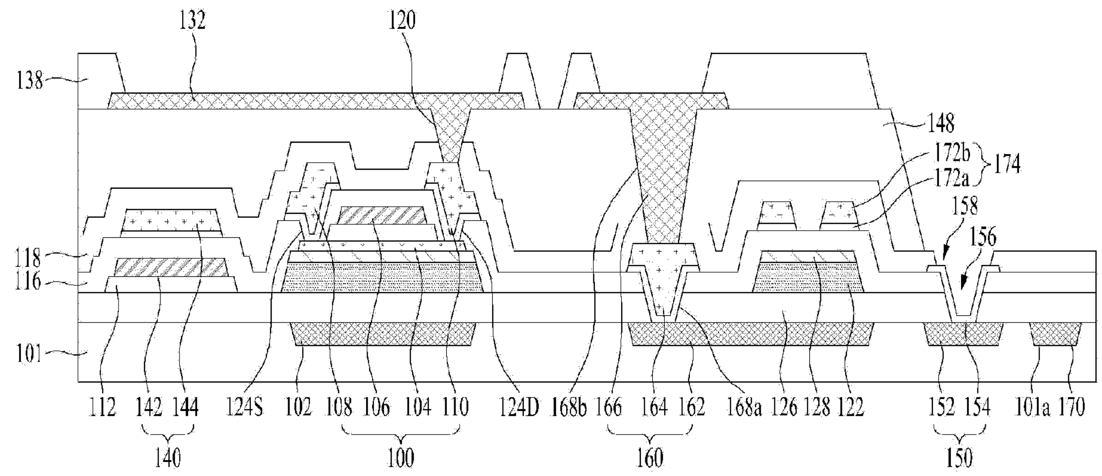
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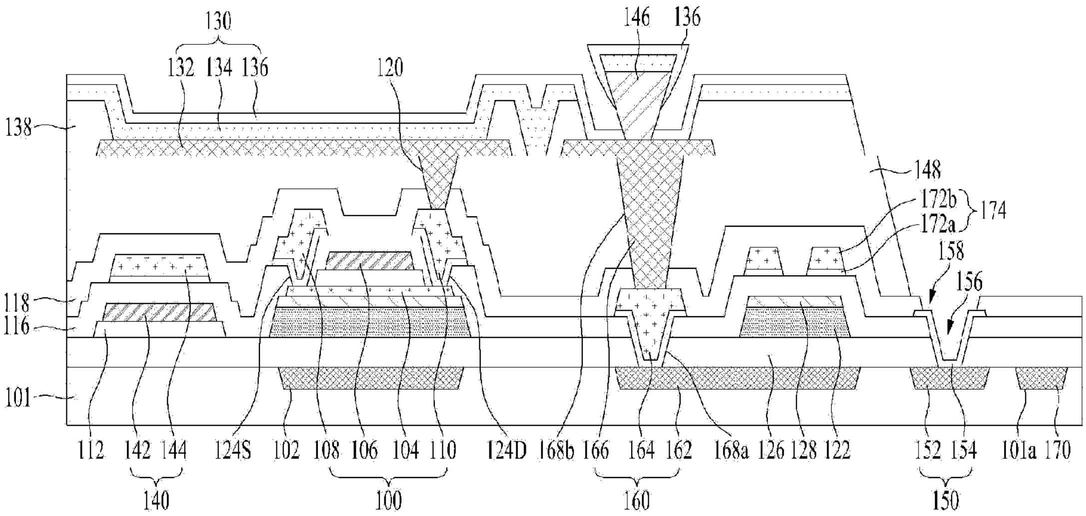
FIG. 6H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101a 170

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EUROPEAN SEARCH REPORT

Application Number
EP 16 18 7892

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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A	US 2010/156860 A1 (YAMAMOTO TETSURO [JP] ET AL) 24 June 2010 (2010-06-24) * paragraphs [0078] - [0082]; figure 3 *	1-15	
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H01L
H05B

The present search report has been drawn up for all claims

1

Place of search	Date of completion of the search	Examiner
The Hague	10 May 2017	Faou, Marylène

CATEGORY OF CITED DOCUMENTS

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EPO FORM 1503 03.82 (P04C01)

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10-05-2017

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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专利名称(译)	有机发光显示装置及其制造方法		
公开(公告)号	EP3188274A1	公开(公告)日	2017-07-05
申请号	EP2016187892	申请日	2016-09-08
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	NAM KYOUNG JIN KIM JEONG OH KIM YONG MIN PARK EUN YOUNG		
发明人	NAM, KYOUNG-JIN KIM, JEONG-OH KIM, YONG-MIN PARK, EUN-YOUNG		
IPC分类号	H01L51/52 H01L27/32		
CPC分类号	H01L27/3244 H01L27/3248 H01L51/52 H01L51/56 H01L2227/32 H01L2227/323 H01L2251/10 H01L2251/50 H01L27/3246 H01L27/3272 H01L27/3276 H01L51/5228 H01L23/544 H01L27/1218 H01L27/1225 H01L27/1288 H01L27/3262 H01L51/5212 H01L2223/54426		
优先权	1020150188439 2015-12-29 KR		
其他公开文献	EP3188274B1		
外部链接	Espacenet		

摘要(译)

一种有机发光显示装置及其制造方法，其可以简化有机发光显示装置的配置并且可以减少掩模处理的数量。有机发光显示装置包括设置在具有多个沟槽（101a）的基板（101）上的薄膜晶体管（100），与薄膜晶体管连接的发光二极管（130），上部辅助电极（166），连接到所述发光二极管的阳极和阴极中的任一个，以及连接到所述上辅助电极的下辅助电极（162）。下辅助电极嵌入衬底的沟槽中，从而确保结构稳定性。

FIG. 1

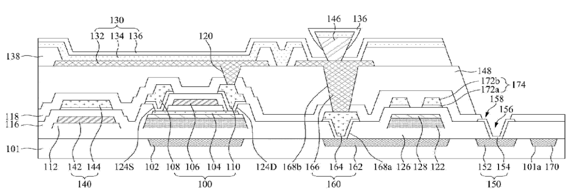

FIG. 2