(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 3 142 099 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
24.07.2019 Bulletin 2019/30

(21) Application number: **14861144.5**

(22) Date of filing: **30.09.2014**

(51) Int Cl.:
G09G 3/3233 *(2016.01)*

(86) International application number:
PCT/CN2014/087897

(87) International publication number:
WO 2015/169043 (12.11.2015 Gazette 2015/45)

(54) **COMPENSATION PIXEL CIRCUIT AND DISPLAY DEVICE**

KOMPENSATIONSPIXELSCHALTUNG UND ANZEIGEVORRICHTUNG

CIRCUIT DE PIXEL DE COMPENSATION ET DISPOSITIF D'AFFICHAGE

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **08.05.2014 CN 201410194265**

(43) Date of publication of application:
15.03.2017 Bulletin 2017/11

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Description

TECHNICAL FIELD

[0001] The present invention relates to a compensation pixel circuit and a display apparatus.

BACKGROUND

[0002] Active matrix organic light emitting diode (AMOLED) display is a display technique applied to a television and a mobile device, and has a broad application prospect in a power-sensitive portable electronic device due to its characteristics of lower power consumption, low cost and large size.

[0003] At present, in the AMOLED display field, in particular, in the large-size substrate design, a backplane thin film transistor (TFT) has problems of uniformity and stability in the technical process of production. On one hand, this would cause that a threshold voltage offset exists between different TFTs; on the other hand, stability of TFT is reduced after opening a bias voltage for a long time. These problems cause non-uniformity and instability of current for driving an OLED, thereby affecting the display effect.

[0004] In the prior art, there are many AMOLED compensation circuit designs performed by considering only the problem of the threshold voltage offset. However, these designs neglect the problem that the load of a gate signal line is raised gradually with the trend of the large size of AMOLED, which results in occurrence of voltage attenuation on the gate signal line, so as to affect current uniformity in the display area. These problems cause non-uniformity of light emitting of OLED, which reduces the display effect.

[0005] US 2009/243977 A1 discloses an OLED display device including: a plurality of pixels, each of the pixels including an OLED and a pixel circuit for driving the OLED, the pixel circuit including: a first transistor for transferring a data signal supplied from a data line to a current scan line; a second transistor for controlling an amount of current corresponding to the data signal that flows from a first pixel power supply to the OLED; a third transistor for diode-connecting the second diode according to the current scan signal; a storage capacitor for maintaining a gate voltage of the second transistor in accordance with the data signal; and a fourth transistor for initializing a first node according to a previous scan signal supplied before the current scan signal is supplied, the fourth transistor in a pixel region of a previous row pixel.

[0006] US 2010/194716 A1 discloses a display device and a driving method thereof. The display device includes a plurality of pixels arranged in a matrix. Each pixel includes a light-emitting element, a driving transistor including an input terminal connected to a first node, a control terminal connected to a second node, and an output terminal, a capacitor connected between the second node and a driving voltage terminal, a switching transistor to transmit a data voltage to the first node, an emission control transistor connected between the output terminal of the driving transistor and the light-emitting element, a first compensation transistor connected between the second node and the output terminal of the driving transistor, a second compensation transistor to transmit a mobility compensation voltage to the first node, a driving control transistor to transmit a driving voltage to the first node; and a reset transistor to transmit a reset voltage to the emission control transistor.

[0007] CN 102 881 253 A discloses a pixel circuit and a TFT rear panel. The pixel circuit comprises a drive transistor, a storage capacitor, a signal loading module and an illumination control module. The source of the drive transistor is connected with the fourth end of the illumination control module and the fourth end of the signal loading module respectively; the grid of the drive transistor is connected with the first end of the storage capacitor and the second end of the signal loading module respectively; the drain of the drive transistor is connected with the third end of the illumination control module and the third end of the signal loading module respectively; the second end of the storage capacitor is connected with the second end of the illumination control module and the first end of the signal loading module respectively; the fifth end of the signal loading module receives an image frame data signal; and the first end of the illumination control module receives a first voltage signal and the fifth end of the illumination control module outputs a luminous signal.

[0008] US 2014/078233 A1, considered to be the closest prior art, discloses a light emitting apparatus including a light emitting element, a driving circuit which has a driving transistor having a gate, a drain, and a source, and a capacitor having one end connected to the gate, a power line, and first and second voltage lines, and, in a period in which the gate and the drain are short-circuited and the drain and the light emitting element are blocked, the source is connected to the first voltage line and the other end of the capacitor is connected to the second voltage line to hold a voltage in the capacitor, and, in a period in which the gate and the drain are disconnected and the drain and the light emitting element are connected, the source is connected to the power line, and the other end of the capacitor is connected to the source to supply a current to the light emitting element.

SUMMARY

[0009] In view of deficiencies of the prior art, it is an object of the present invention to provide a compensation pixel

circuit and a display apparatus, which has not only the function of compensating for the threshold voltage offset but also the function of resetting a gate voltage of a driving transistor, thereby reducing greatly the influence of signals from frame to frame.

[0010] The object is achieved by the features of the respective independent claim. Further embodiments are defined in the respective dependent claims.

[0011] The embodiments of the present disclosure have at least following beneficial effects:

[0012] The configuration of the compensation pixel circuit provided in the embodiments of the present disclosure makes that the current finally driving the OLED to emit light is unrelated to a threshold voltage Vth and a bias voltage V_{DD}, so that it can not only compensate the OLED current difference caused by the threshold voltage offset but also have the function of compensating the influence of the signal voltage attenuation on the current.

[0013] At the same time, since the resetting module in the circuit can reset the gate voltage of the driving transistor, it makes that an upper frame signal has litter impact on a lower frame signal, thereby reducing influence of signals from frame to frame greatly.

[0014] Of course, any product or method that implements the embodiments of the present disclosure does not necessarily require achieving all of the above advantages simultaneously.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015]

Fig.1 is a schematic diagram of configuration of a compensation pixel circuit in an embodiment of the present disclosure;

Fig.2 is schematic diagram of a circuit structure of a 7T1C compensation pixel circuit in an embodiment of the present disclosure;

Fig.3 is an operation timing schematic diagram of a 7T1C compensation pixel circuit in an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0016] In order to make the purpose, the technical solutions and the advantages of embodiments of the present disclosure clearer, embodiments of the present disclosure will be described clearly and completely by combining with the accompanying figures.

First embodiment

[0017] Fig.1 shows schematically configuration of a compensation pixel circuit of a first embodiment of the present disclosure. As shown in Fig.1, the circuit comprises an organic light emitting diode D1 and a driving transistor M1. A first terminal of the driving transistor M1 is connected to an anode of the organic light emitting diode D1 via a switching module. The compensation pixel circuit further comprises:

a resetting module including a capacitor C1 whose first terminal is connected to a gate of the driving transistor M1 and configured to make the gate of the driving transistor M1 discharge so that a gate voltage is reduced to a magnitude of a threshold voltage of the organic light emitting diode D1;

a data voltage writing module configured to supply a data voltage VData to a second terminal of the driving transistor M1 after the gate of the driving transistor M1 discharges and the gate voltage is made reduced to the magnitude of the threshold voltage of the organic light emitting diode D1;

a light emitting control module configured to connect a source of the driving transistor M1 and a second terminal of the capacitor C1 to an operating voltage V_{DD} at a high level after data voltage writing is completed (a corresponding operating voltage at a low level is V_{SS} connected to a cathode of D1); and

a switching module configured to disconnect the driving transistor M1 from the organic light emitting diode D1 when the data voltage is supplied to the second terminal of the driving transistor M1.

[0018] It is well known that a transistor has a gate, a source and a drain, but "the first terminal of the driving transistor

M1" herein refers to a terminal connected to the anode of the organic light emitting diode D1. This terminal may be a source or a drain of the transistor depending on different types of selected transistors.

[0019] Since the resetting module is configured to make the gate of the driving transistor M1 discharge so that the gate voltage is reduced to magnitude of the threshold voltage of the organic light emitting diode D1, and it includes the capacitor C1 whose first terminal is connected to the gate of the driving transistor M1, this discharging process is completed apparently by the capacitor C1. Since it is evident that the anode of D1 has to be connected to one terminal of the capacitor C, the gate terminal of M1, the second terminal of C1 and the anode of D1 have to be connected to one point in order to realize such function, i.e., connecting the second terminal of the capacitor C1 to a constant voltage having a higher voltage value compared with an operating voltage at a low level, so that a potential at the gate of the driving transistor M1 is discharged via D1, thereby finally making the potential at this point become the threshold voltage of D1. Thus, it is implied herein a connecting relationship of the gate of M1 being also connected to D1. Likewise, the connecting relationship as shown in Fig.1 is also comprised in the description about the configuration or function.

[0020] It is thus clear that the compensation pixel circuit can be divided into three operating phases in time order, i.e., a resetting phase, a data voltage writing phase and a light emitting phase. The whole operating process is performed sequentially according to the order of the resetting module, the data writing module and the light emitting module. That is, the three modules realize their major functions in sequence in the three operating phases corresponding to the three modules, and the switching module and the data writing module realize their functions simultaneously.

[0021] In order to describe the technical solution of the present disclosure more clearly, the technical solution and technical effect of the embodiment of the present disclosure will be introduced below by a 7T1C compensating pixel circuit under an exemplary condition.

[0022] Fig.2 schematically shows a circuit structure of a 7T1C compensation pixel circuit in an embodiment of the present disclosure. Referring to Fig.2, the circuit comprises the organic light emitting diode D1, the driving transistor M1, second to seventh switching elements M2-M7 and the storage capacitor C1.

[0023] Except for the capacitor C1, the resetting module further comprises a sixth switching element M6 and a seventh switching element M7. A first terminal and a second terminal of the sixth switching element M6 are connected to the gate and the first terminal of the driving transistor M1 respectively. A second terminal of the seventh switching element M7 is connected to a predetermined voltage Vinitial, and a first terminal thereof is connected to the second terminal of the capacitor C1.

[0024] Gates of the sixth switching element M6 and the seventh switching element M7 are connected to a signal line G2. The signal line G2 is configured to control the two switching elements M6 and M7 to be in a turn-on state when the resetting module and the data voltage writing module are operating and to be in a turn-off state when the light emitting control module is operating.

[0025] The data voltage writing module comprises a third switching element M3, whose first terminal is connected to the second terminal of the driving transistor M1 and second terminal is connected to a data voltage line VData.

[0026] A gate of the third switching element M3 is connected to a signal line G1. The signal line G1 is configured to control the third switching element M3 to be in the turn-on state when the data voltage writing module is operating and to be in the turn-off state when the resetting module and the light emitting control module are operating.

[0027] The light emitting control module comprises a fourth switching element M4 and a fifth switching element M5 whose second terminals are connected to an operation voltage line V_{DD} at the high level. A first terminal of the fourth switching element M4 is connected to the second terminal of the driving transistor M1. A first terminal of the fifth switching element M5 is connected to the second terminal of the capacitor C1.

[0028] Gates of the fourth switching element M4 and the fifth switching element M5 are connected to a signal line EMI. The signal line EMI is configured to control the two switching elements M4 and M5 to be in the turn-off state when the resetting module and the data voltage writing module are operating and to be in the turn-on state when the light emitting control module is operating.

[0029] The switching module comprises a second switching element M2, whose first terminal is connected to the anode of the organic light emitting diode D1, and second terminal is connected to the first terminal of the driving transistor M1.

[0030] Since the switching module is configured to disconnect the driving transistor M1 from the organic light emitting diode D1 when the data voltage VData is supplied to the second terminal of the driving transistor M1, a signal EM2 connected to the control terminal of the second switching element M2 is actually an inverse signal of the signal G1.

[0031] Herein, the switching element refers to an element whose first terminal and second terminal are controlled by a signal of the control terminal to be connected or disconnected. Of course, it can be implemented by a variety of specific electrical elements.

[0032] It is thus clear that in the basis constitution and connecting relationship of the circuit, as described above, the driving transistor M1 and the organic light emitting diode D1 constitute the basic OLED driving relationship, while the second to seventh switching elements M2-M7 can be controlled to be in the turn-on/turn-off state by the signals of their respective control terminals connected thereto. Of course, zero points of potentials of all the bias voltages are connected

to a same common terminal, and zero points of potentials of all the signal voltages are connected to a same common terminal.

[0033] Alternatively, the driving transistor and the second to seventh switching elements are thin film transistors TFTs. Herein, the thin film transistors adopted in the present embodiment are P type channel thin film transistors. By corresponding to this situation, the first terminals of the driving transistor and the second to seventh switching elements represent drains, the second terminals thereof represent sources, and the control terminals of the second to seventh switching element represent gates. Of course, other types of transistors can also be used as equivalent substitutes.

[0034] Thus, because the compensation pixel circuit comprises seven TFTs and one capacitor, it can be called as a new type 7T1C compensation pixel circuit in a naming manner conventionally used in the art.

[0035] Fig.3 shows schematically an operation timing of the 7T1C compensation pixel circuit in the embodiment of the present disclosure. Based on the 7T1C compensating pixel circuit under the above exemplary condition, the operating principle of the circuit can be described below by referring to Fig.3.

[0036] As shown in Fig.3, referring to the operation timing diagram of the circuit, the operating process of the circuit can be divided into for example three phases in general, i.e., a resetting phase (a-b), a data writing phase (b-c), and light emitting phase (c-).

[0037] Specifically, in the resetting phase, the signal EM1 and the signal G1 are at the high level, so that the transistors M3, M4, M5 are in the turn-off state; whereas the signals EM2 and G2 are at the low level, and the low level of the signal EM2 makes the transistor M2 turned on, and at the same time makes nodes C and D of the source and drain of the transistor M2 turned on and connected. The low level of the signal G2 makes the transistors M6 and M7 turned on, so that the turn-on of the transistor M7 makes the potential at a node A of the storage capacitor C1 is reset as the signal Vinitial. In addition, the turn-on of the transistor M6 makes the gate and drain of driving transistor M 1 connected to each other. In this way, the nodes B, C, and D are then connected to each other, and the potential at the node B of the storage capacitor C1 is discharged to a low voltage via the organic light emitting diode D1. This low voltage is the threshold voltage of the organic light emitting diode D1. Of course, the organic light emitting diode D1 is now in the turn-off state and does not emit light.

[0038] In the data writing phase, the signal EM2 becomes the high level, so that the transistor M2 is turned off. The signal G2 is maintained at the low level, and at the same time the signal G1 also becomes the low level, so that the transistor M3 is turned on, and the data signal VData is written into the source of the driving transistor M1 via the transistor M3. Now, since the signal G2 is continuously maintained at the low level, the transistor M1 connected to OLED operates in a saturation region, and then the potential at the node B becomes VData+Vth. As the potential at the node A is Vinitial, the potentials at the two terminals of the storage capacitor C1 becomes Vinitial and VData+Vth respectively.

[0039] In the light emitting phase, the signals G1 and G2 become the high level, so that the transistors M3, M6 and M7 are turned off. The signals EM1 and EM2 become the low level, so that the transistors M4, M5 and M2 are turned on. After the transistor M5 is turned on, the potential at the node A of the storage capacitor C1 becomes V_{DD} from Vinitial. According to the principle of charge conservation, the potential at the node A becomes V_{DD}+VData+Vth-Vinitial. Now, the transistor M1 is in the saturation region. According to the current formula of the saturation region, it can be known that the current outflowing from the transistor M1 is:

$$\begin{aligned} I_{DS} &= \frac{1}{2}K(V_{GS} - Vth)^2 \\ &= \frac{1}{2}K(V_{DD} + Vdata + Vth - Vinitial - V_{DD} - Vth)^2 \\ &= \frac{1}{2}K(Vdata - Vinitial)^2 \end{aligned}$$

where K in the same structure is stable relatively and can be regarded as a constant herein.

[0040] Therefore, in the process of light emitting of OLED, the current flowing through the organic light emitting diode D1 connected to the drain of the driving transistor M1 is only related to Vinitial and VData, but is not unrelated to Vth and V_{DD}. As Vinitial does not form a current loop, the gate voltage of the driving transistor M1 can be reset to a fixed value each time under the effect of the resetting module, and would not be affected by the IR drop (voltage drop, i.e., the voltage attenuation of the gate signal line described in the background section) phenomenon. As a result, the problem of the current flowing through OLED being non-uniform in magnitude is not caused by the non-uniformity of the threshold voltage Vth due to the manufacturing process of the backplane, that is, the problem of non-uniformity of light emitting is not caused. At the same time, the potential at the node A of the storage capacitor C1 is always the signal V_{DD} in the process of light emitting, and no charge loss occurs, which ensures the stability of the potential at the node A, so that

the current flowing through the driving transistor M1 is stable, and thus the organic light emitting diode D1 emits light stably. Of course, the above embodiment is only used to describe the technical solution of the present disclosure, but not to limit the present disclosure. Although the present disclosure is described in detail by referring to the above embodiments, those ordinary skilled in the art shall understand that no matter what kind of structure the resetting module, the data writing module and the light emitting control module and the switching module adopt in a specific implementation process, the present disclosure can be implemented by referring to the operating principle described in the embodiment of the present disclosure only if the resetting module, the data writing module and the light emitting control module and the switching module have the function of the above compensation pixel circuit, which certainly does not depart from the scope of the technical solutions of the embodiment of the present disclosure.

Second embodiment.

[0041] Based on the same inventive concept, an embodiment of the present disclosure further provides a display apparatus comprising any one of the compensation pixel circuits described above. The display apparatus may be any product or component having the function of displaying, such as an OLED panel, a mobile phone, a tablet computer, a television, a display, a notebook computer, and a digital photo frame, and a navigator and the like.

[0042] When the circuit is designed to be a pixel unit in the array substrate, since the signal lines G1 and G2 are signals being configured to control the data voltage writing, according to the high level or the low level of the gate driving signal, one of the signals G1 and G2 can be connected to the gate line corresponding to the row while the other thereof is made to be its inverse signal. For the signal lines EM1 and G2, they are configured to reset the gate voltage, and thus the signal lines EM1 and G2 can be implemented by designing corresponding resetting switch signal lines or can be obtained through certain logic circuit operation according to the gate line signal.

[0043] The display apparatus provided in the embodiment of the present disclosure can solve the same technical problem and produce the same technical effect because it has the same technical features as any one of the compensation pixel circuits as described above.

[0044] To sum up, the configuration of the compensation pixel circuit provided in the embodiments of the present disclosure makes the current that finally drives OLED to emit light is unrelated to the threshold voltage Vth and the bias voltage V_{DD}, so that the compensation pixel circuit can not only compensate for the OLED current difference due to the threshold voltage offset but also have the function of compensating for the influence of the signal voltage attenuation on the current. At the same time, the resetting module in the circuit can reset the gate voltage of the driving transistor, i.e., making that the upper frame signal has little impact on the lower frame signal, thereby reducing influence of signals from frame to frame greatly. Therefore, the compensation pixel circuit and the display apparatus provided in the present disclosure have not only the function of compensating for the threshold voltage offset but also the function of resetting the gate voltage of the driving transistor, thereby reducing influence of signals from frame to frame greatly and at the same time ensuring the non-uniformity and stability of the light emitting of OLED.

[0045] It should be noted that the relationship terms such as "first" and "second" in the present disclosure are just used to distinct one entity or one operation from another entity or another operation, instead of requiring or suggesting that any actual relationship or order exist among these entities or operations.

Claims

1. A display apparatus comprising a plurality of compensation pixel circuits, wherein each of the plurality of compensation pixel circuits comprises:

   an organic light emitting diode, OLED, (D1);
   a driving transistor (M1);
   a resetting module including a capacitor (C1) whose first terminal is connected to a gate of the driving transistor (M1) and configured to discharge a potential at the gate of the driving transistor (M1) under control of a first signal line(G2);
   a data voltage writing module configured to supply a data voltage (VData) to a second terminal of the driving transistor (M1) under control of a second signal line (G1);
   a light emitting control module configured to connect the second terminal of the driving transistor (M1) to an operating voltage (VDD) at a high level under control of a third signal line (EM1); and
   a switching module connected between a first terminal of the driving transistor (M1) and an anode of the OLED and configured to disconnect the driving transistor (M1) from the OLED (D1) under control of a fourth signal line (EM2);
   wherein the light emitting control module is further configured to connect a second terminal of the capacitor

(C1) to the operating voltage (VDD) at a high level under the control of the third signal line (EM1);
wherein the data voltage writing module comprises a data voltage writing switching element (M3) having a control terminal connected to the second signal (G1), a first terminal connected to the second terminal of the driving transistor (M1), and a second terminal connected to the data voltage (Data); and
wherein the light emitting control module comprises:

a first light emitting control switching element (M4) having a control terminal connected to the third signal line (EM1), a first terminal connected to the second terminal of the driving transistor (M1), and a second terminal connected to the operating voltage (VDD); and
a second light emitting control switching element (M5) having a control terminal connected to the third signal line (EM1), a first terminal connected to the second terminal of the capacitor (C1), and a second terminal;
, wherein the resetting module further comprises a first resetting switching element (M6) and a second resetting switching element (M7), wherein:

a first terminal and a second terminal of the first resetting switching element (M6) are connected to the gate and the first terminal of the driving transistor (M1), respectively, and a control terminal of the first resetting switching element (M6) is connected to the first signal line (G2); and
a second terminal of the second resetting switching element (M7) is connected to a predetermined voltage (Vinitial), a first terminal thereof is connected to the second terminal of the capacitor (C1),
characterized in that
a control terminal of the second resetting switching element (M7) is connected to the first signal line (G2); the second terminal of the second light emitting control switching element (M5) is directly connected to the operating voltage.

2. The display apparatus according to claim 1, wherein the switching module comprises a switching element (M2), whose first terminal is connected to the anode of the OLED (D1), second terminal is connected to the first terminal of the driving transistor (M1), and control terminal is connected to the fourth signal line (EM2).

3. The display apparatus according to any one of claims 1 to 2, wherein the driving transistor (M1), the second to seventh switching elements (M2-M7) are thin film transistors.

Patentansprüche

1. Anzeigevorrichtung mit einer Vielzahl von Kompensationspixelschaltungen, wobei jede der Vielzahl von Kompensationspixelschaltungen aufweist:

eine organische lichtemittierende Diode, OLED, (DI);
einen Ansteuertransistor (M1);
ein Rücksetz-Modul mit einem Kondensator (C1), dessen erster Anschluss mit einem Gate-Anschluss des Ansteuertransistors (M1) verbunden ist und der konfiguriert ist, ein Potential an dem Gate-Anschluss des Ansteuertransistors (M1) unter Steuerung einer ersten Signalleitung (G2) zu entladen;
ein Datenspannung-Schreibmodul, das konfiguriert ist, eine Datenspannung (VD) an einen zweiten Anschluss des Ansteuertransistors (M1) unter Steuerung einer zweiten Signalleitung (G1) bereitzustellen;
ein Lichtemission-Steuerungsmodul, das konfiguriert ist, den zweiten Anschluss des Ansteuertransistors (M1) mit einer Betriebsspannung (VDD) bei einem Hoch-Pegel unter Steuerung einer dritten Signalleitung (EM1) zu verbinden; und
ein Schalt-Modul, das zwischen einem ersten Anschluss des Ansteuertransistors (M1) und einer Anode der OLED geschaltet ist und konfiguriert ist, den Ansteuertransistor (M1) von der OLED (D1) unter Steuerung einer vierten Signalleitung (EM2) zu trennen;
wobei das Lichtemission-Steuermodul weiter konfiguriert ist, einen zweiten Anschluss des Kondensators (C1) mit der Betriebsspannung (VDD) bei einem Hoch-Pegel unter der Steuerung der dritten Signalleitung (EM1) zu verbinden;
wobei das Datenspannung-Schreibmodul aufweist ein Datenspannung-Schreibschaltelement (M3) mit einem Steueranschluss, der mit der zweiten Signalleitung (G1) verbunden ist, einem ersten Anschluss, der mit dem zweiten Anschluss des Ansteuertransistors (M1) verbunden ist, und einem zweiten Anschluss, der mit der Datenspannung (Data) verbunden ist; und
wobei das Lichtemission-Steuermodul aufweist:

ein erstes Lichtemission-Steuerschaltelement (M1) mit einem Steueranschluss, der mit der dritten Signalleitung (EM1) verbunden ist, einem ersten Anschluss, der mit dem zweiten Anschluss des Ansteuertransistors (M1) verbunden ist, und einem zweiten Anschluss, der mit der Betriebsspannung (VDD) verbunden ist; und

ein zweites Lichtemission-Steuerschaltelement (M5) mit einem Steueranschluss, der mit der dritten Signalleitung (EM1) verbunden ist, einem ersten Anschluss, der mit dem zweiten Anschluss des Kondensators (C1) verbunden ist, und einem zweiten Anschluss;

wobei das Rücksetz-Modul weiter aufweist ein erstes Rücksetz-Schaltelement (M6) und ein zweites Rücksetz-Schaltelement (M7), wobei:

ein erster Anschluss und ein zweiter Anschluss des ersten Rücksetz-Schaltelements (M6) jeweils mit dem Gate-Anschluss und dem ersten Anschluss des Ansteuertransistors (M1) verbunden sind und ein Steueranschluss des ersten Rücksetz-Schaltelements (M6) mit der ersten Signalleitung (G2) verbunden ist; und

ein zweiter Anschluss des zweiten Rücksetz-Schaltelements (M7) mit einer vorbestimmten Spannung (Vinitial) verbunden ist, sein erster Anschluss mit dem Anschluss des Kondensators (C1) verbunden ist, **dadurch gekennzeichnet, dass**

ein Steueranschluss des zweiten Rücksetz-Schaltelements (M7) mit der ersten Signalleitung (G2) verbunden ist;

der zweite Anschluss des zweiten Lichtemission-Steuerschaltelements (M5) direkt mit der Betriebsspannung verbunden ist.

2. Anzeigevorrichtung gemäß Anspruch 1, wobei das Schalt-Modul aufweist ein Schaltelement (M2), dessen erster Anschluss mit der Anode der OLED (D1) verbunden ist, dessen zweiter Anschluss mit dem ersten Anschluss des Ansteuertransistors (M1) verbunden ist, und dessen Steueranschluss mit der vierten Signalleitung (EM2) verbunden ist.

3. Anzeigevorrichtung gemäß einem der Ansprüche 1 bis 2, wobei der Ansteuertransistor (M1), die zweiten bis siebten Schaltelemente (M2-M7) Dünnschichttransistoren sind.

Revendications

1. Appareil d'affichage comprenant une pluralité de circuits de pixel de compensation, dans lequel chacun de la pluralité de circuits de pixel de compensation comprend :

une diode émettrice de lumière organique, OLED, (D1) ;

un transistor de pilotage (M1) ;

un module de réinitialisation qui inclut un condensateur (C1) dont une première borne est connectée à une grille du transistor de pilotage (M1) et qui est configuré de manière à ce qu'il décharge un potentiel au niveau de la grille du transistor de pilotage (M1) sous la commande d'une première ligne de signal (G2) ;

un module d'écriture de tension de données qui est configuré de manière à ce qu'il alimente une tension de données (VData) sur une seconde borne du transistor de pilotage (M1) sous la commande d'une deuxième ligne de signal (G1) ;

un module de commande d'émission de lumière qui est configuré de manière à ce qu'il connecte la seconde borne du transistor de pilotage (M1) à une tension de fonctionnement (VDD) à un niveau haut sous la commande d'une troisième ligne de signal (EM1) ; et

un module de commutation qui est connecté entre une première borne du transistor de pilotage (M1) et une anode de l'OLED et qui est configuré de manière à ce qu'il déconnecte le transistor de pilotage (M1) vis-à-vis de l'OLED (D1) sous la commande d'une quatrième ligne de signal (EM2) ; dans lequel :

le module de commande d'émission de lumière est en outre configuré de manière à ce qu'il connecte une seconde borne du condensateur (C1) à la tension de fonctionnement (VDD) à un niveau haut sous la commande de la troisième ligne de signal (EM1) ; dans lequel :

le module d'écriture de tension de données comprend un élément de commutation d'écriture de tension de données (M3) qui comporte une borne de commande qui est connectée à la deuxième ligne de signal (G1), une première borne qui est connectée à la seconde borne du transistor de pilotage (M1) et une seconde borne qui est connectée à la tension de données (Data) ; et dans lequel :

le module de commande d'émission de lumière comprend :

un premier élément de commutation de commande d'émission de lumière (M4) qui comporte une borne de commande qui est connectée à la troisième ligne de signal (EM1), une première borne qui est connectée à la seconde borne du transistor de pilotage (M1) et une seconde borne qui est connectée à la tension de fonctionnement (VDD) ; et

un deuxième élément de commutation de commande d'émission de lumière (M5) qui comporte une borne de commande qui est connectée à la troisième ligne de signal (EM1), une première borne qui est connectée à la seconde borne du condensateur (C1) et une seconde borne ; dans lequel :

le module de réinitialisation comprend en outre un premier élément de commutation de réinitialisation (M6) et un deuxième élément de commutation de réinitialisation (M7) ; dans lequel :

une première borne et une seconde borne du premier élément de commutation de réinitialisation (M6) sont respectivement connectées à la grille et à la première borne du transistor de pilotage (M1), et une borne de commande du premier élément de commutation de réinitialisation (M6) est connectée à la première ligne de signal (G2) ; et

une seconde borne du deuxième élément de commutation de réinitialisation (M7) est connectée à une tension prédéterminée (Vinitial) et sa première borne est connectée à la seconde borne du condensateur (C1) ;

caractérisé en ce que :

une borne de commande du deuxième élément de commutation de réinitialisation (M7) est connectée à la première ligne de signal (G2) ;

la seconde borne du deuxième élément de commutation de commande d'émission de lumière (M5) est connectée directement à la tension de fonctionnement.

2. Appareil d'affichage selon la revendication 1, dans lequel le module de commutation comprend un élément de commutation (M2) dont une première borne est connectée à l'anode de l'OLED (D1), dont une seconde borne est connectée à la première borne du transistor de pilotage (M1) et dont une borne de commande est connectée à la quatrième ligne de signal (EM2).

3. Appareil d'affichage selon l'une quelconque des revendications 1 et 2, dans lequel le transistor de pilotage (M1) ainsi que les deuxième à septième éléments de commutation (M2-M7) sont des transistors à film mince.

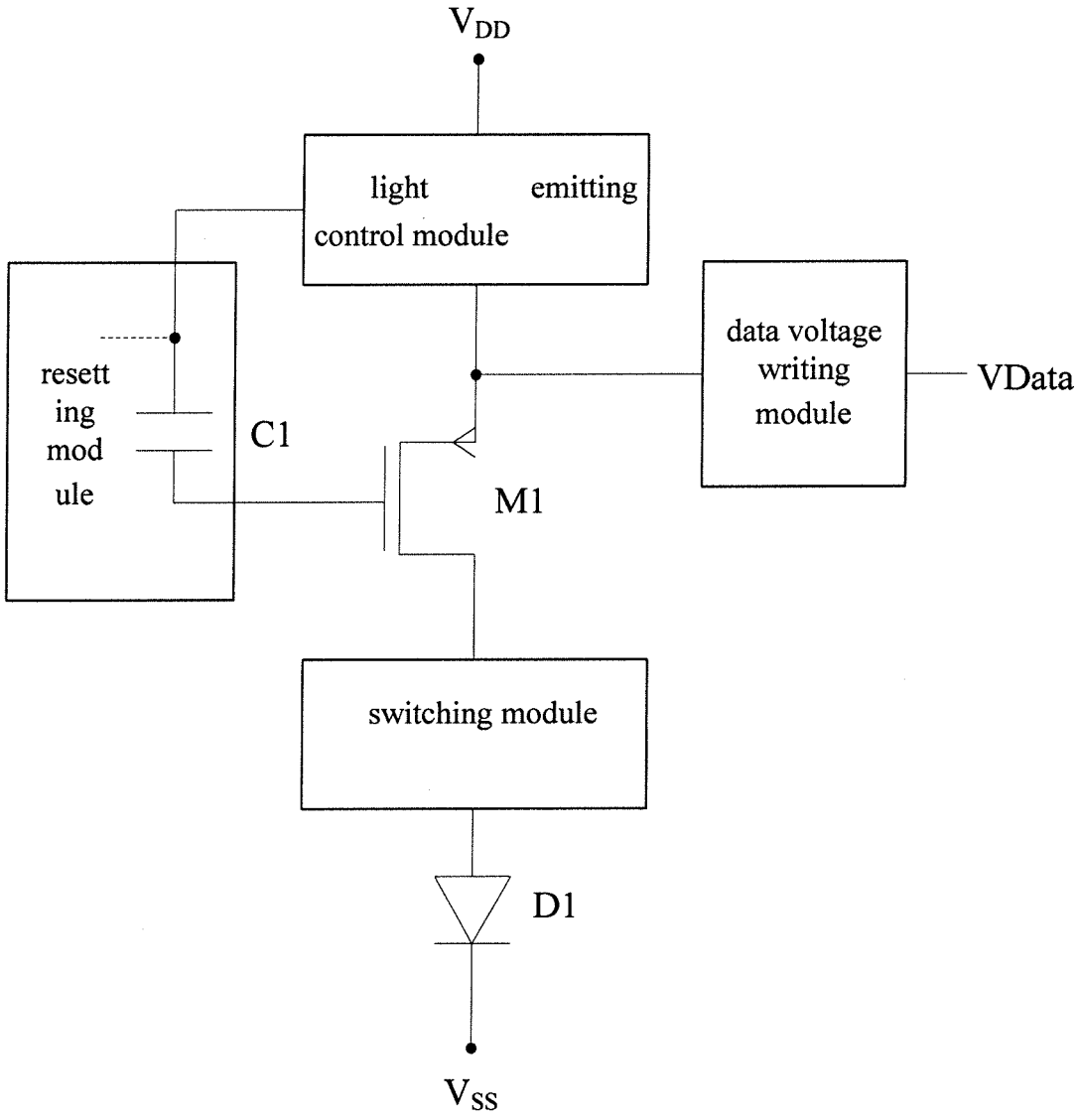
V_{DD}
light emitting control module
resett ing mod ule
C1
M1
data voltage writing module
VData
switching module
D1
V_{SS}

Fig. 1

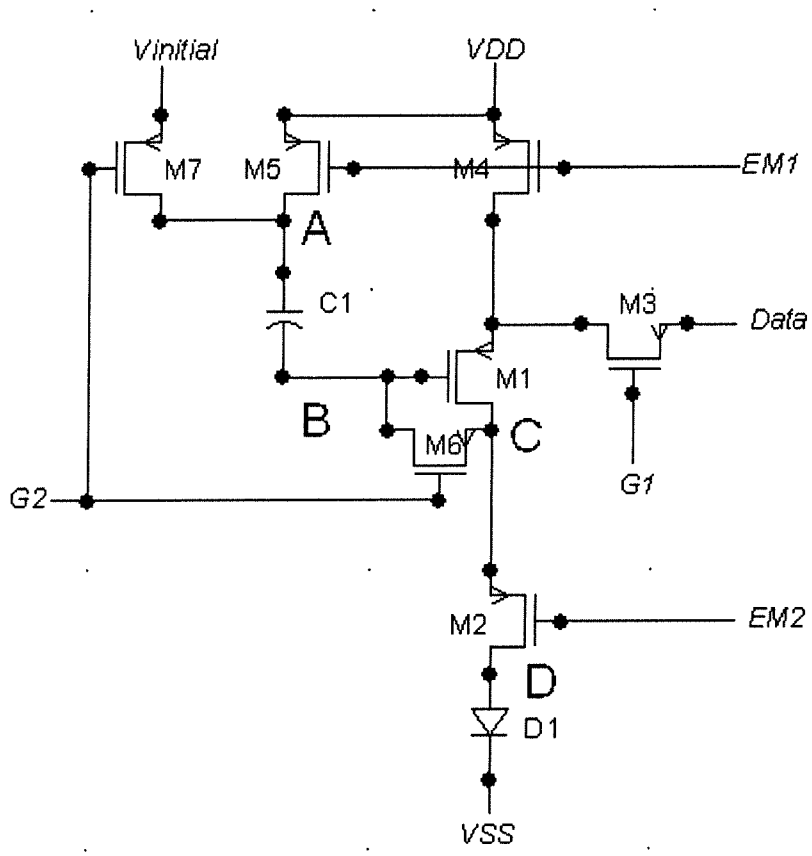
Vinitial
VDD
M7
M5
M4
EM1
A
C1
M3
Data
M1
B
M6
C
G2
G1
M2
EM2
D
D1
VSS

Fig. 2

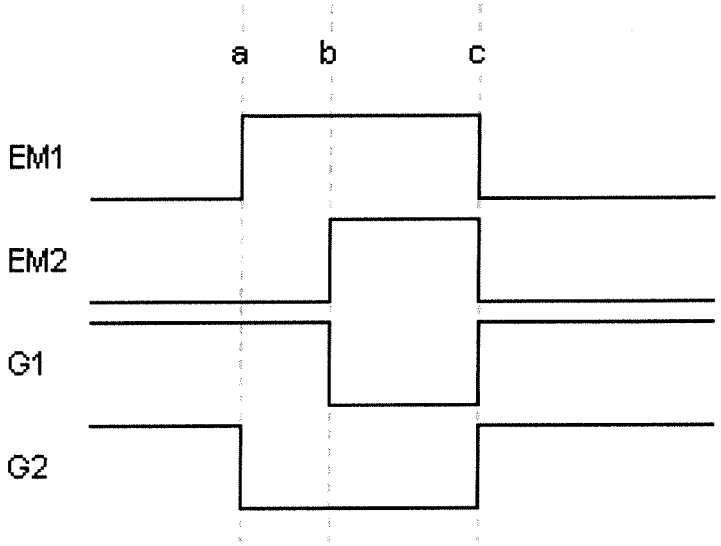
a
b
c
EM1
EM2
G1
G2

Fig. 3

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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- US 2010194716 A1 **[0006]**
- CN 102881253 A **[0007]**
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专利名称(译)	补偿像素电路和显示装置		
公开(公告)号	EP3142099B1	公开(公告)日	2019-07-24
申请号	EP2014861144	申请日	2014-09-30
[标]申请(专利权)人(译)	京东方科技集团股份有限公司		
申请(专利权)人(译)	京东方科技集团股份有限公司.		
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[标]发明人	MA ZHANJIE		
发明人	MA, ZHANJIE		
IPC分类号	G09G3/3233		
CPC分类号	G09G3/3233 G09G2230/00 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2320/045 G09G3/3225 G09G2310/061 G09G2320/0233		
优先权	201410194265.X 2014-05-08 CN		
其他公开文献	EP3142099A1 EP3142099A4		
外部链接	Espacenet		

摘要(译)

提供了补偿像素电路和显示装置。补偿像素电路包括有机发光二极管（D1）和驱动晶体管（M1），驱动晶体管（M1）的第一端连接到有机发光二极管（D1）的阳极。补偿像素电路还包括：复位模块，数据电压写入模块，发光控制模块和开关模块。复位模块包括电容器（C1），其第一端子连接到驱动晶体管（M1）的栅极，并且被配置为使驱动晶体管（M1）的栅极放电，使得栅极电压减小到a的幅度。有机发光二极管（D1）的阈值电压。数据电压写入模块被配置为在驱动晶体管（M1）的栅极放电，以便在栅极电压减小到阈值的大小之后将数据电压连接到驱动晶体管（M1）的第二端子。有机发光二极管（D）的电压。发光控制模块被配置为在完成数据电压写入之后将驱动晶体管（M1）的源极和电容器（C1）的第二端子连接到高电平的工作电压。切换模块被配置为当数据电压连接到驱动晶体管（M1）的第二端子时将驱动晶体管（M1）与有机发光二极管（D1）断开。补偿像素电路可以补偿阈值电压偏移，并且大大降低帧间信号的影响。

$$I_{DS} = \frac{1}{2}K(V_{GS} - Vth)^2$$

$$= \frac{1}{2}K(V_{DD} + Vdata + Vth - Vinitial - V_{DD} - Vth)^2$$

$$= \frac{1}{2}K(Vdata - Vinitial)^2$$