(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 3 121 805 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
06.11.2019 Bulletin 2019/45

(51) Int Cl.:
G09G 3/32 *(2016.01)*

(21) Application number: **16180868.8**

(22) Date of filing: **22.07.2016**

(54) METHOD OF DRIVING ORGANIC LIGHT EMITTING DIODE DISPLAY

VERFAHREN ZUR ANSTEUERUNG EINER OLED-ANZEIGE

PROCÉDÉ DE PILOTAGE D'AFFICHAGE À DIODE ÉLECTROLUMINESCENTE ORGANIQUE

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **23.07.2015 KR 20150104280**

(43) Date of publication of application:
25.01.2017 Bulletin 2017/04

(73) Proprietor: **LG Display Co., Ltd.**
Yeongdeungpo-gu
Seoul 07336 (KR)

(72) Inventors:
- **RYU, Hon-Jin**
  411-737 GYEONGGI-DO (KR)
- **KIM, Seong-Hyun**
  561-805 JEOLLABUK-DO (KR)

(74) Representative: **Ter Meer Steinmeister & Partner Patentanwälte mbB**
Nymphenburger Straße 4
80335 München (DE)

(56) References cited:
US-A1- 2001 003 448
US-A1- 2008 238 897
US-A1- 2009 262 101
US-A1- 2010 091 006
US-A1- 2012 235 973

EP 3 121 805 B1

Description

[0001] The present application claims the priority benefit of Korean Patent Application No. 10-2015-0104280 filed in Republic of Korea on July 23, 2015.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to an organic light emitting diode display (OLED) and a method for driving the OLED display. In particular, the present invention relates to a OLED display device and a method of driving an OLED that can periodically reduce variances of threshold voltages of a driving thin film transistor and a organic light emitting diode.

Discussion of the Related Art

[0003] Recently, flat display devices, such as a plasma display panel (PDP), a liquid crystal display (LCD), and an organic light emitting diode display (OLED), have been researched.

[0004] Among the flat display devices, the OLED is a self-luminescent device and can have a thin profile because the OLED does not need a backlight used for the LCD.

[0005] Further, compared with the LCD, the OLED has advantages of excellent viewing angle and contrast ratio, low power consumption, operation in low DC voltage, fast response speed, being strong to an external impact because of its solid internal components, and wide operating temperature range.

[0006] Particularly, since processes of manufacturing the OLED are simple, production cost of the OLED can be reduced more than that of the LCD.

[0007] FIG. 1 is a view illustrating organic light emitting diodes and driving circuits arranged at respective pixel regions of a display region of an OLED according to the related art, and FIG. 2 is a timing chart of gate pulses and data signals applied to the driving circuits of FIG. 1.

[0008] Referring to FIG. 1, the related art OLED includes first and second organic light emitting diodes D1 and D2 and first and second driving circuits 11 and 12 to operate the first and second organic light emitting diodes D1 and D2, respectively, in a display region 10.

[0009] In detail, the first driving circuit 11 is connected to a first gate line GL1 and each data line DL and operates the first organic light emitting diode D1, and the second driving circuit 12 is connected to a second gate line GL2 and each data line DL and operates the second organic light emitting diode D2.

[0010] For the purpose of explanations, the first and second driving circuits 11 and 12 are shown. However, a plurality of driving circuits may be arranged below the first and second driving circuits 11 and 12, and thus a plurality of gate lines may be arranged below the first and second gate lines GL1 and GL2 connected to the first and second driving circuits 11 and 12.

[0011] A method of driving the OLED is explained below.

[0012] The method of driving the OLED includes sequentially supplying first and second gate pulses g1 and g2 to the first and second gate lines GL1 and GL2, respectively, and sequentially supplying first and second data signals d1 and d2 to each data line DL.

[0013] Referring to FIG. 2, during a frame, the first gate pulse g1 is supplied to the first gate line GL1 and then the second gate pulse g2 is supplied to the second gate line GL2.

[0014] Further, the first and second data signals are sequentially supplied per horizontal period H.

[0015] Further, the first data signal d1 is supplied to the first driving circuit 11 during a overlapping section between the first gate pulse g1 and the first data signal d1, and the second data signal d2 is supplied to the second driving circuit 12 during a overlapping section between the second gate pulse g2 and the second data signal d2.

[0016] Further, the first organic light emitting diode D1 emits light in a section (i.e., a light-emission section) from a falling point of the first gate pulse g1 in the frame to a rising point of a first gate pulse g1 in a next frame, and the second organic light emitting diode D2 emits light in a section (i.e., a light-emission section) from a falling point of the second gate pulse g2 in the frame to a rising point of a second gate pulse g2 in a next frame.

[0017] As shown in FIG. 1, the first driving circuit 11 is supplied with the first data signal d1 by the first gate pulse g1, and the second driving circuit 12 is supplied with the second data signal d2 by the second gate pulse g2.

[0018] In detail, the first driving circuit 11 is supplied with the first gate pulse g1 from the first gate line GL1 and the first data signal d1 from the data line DL to make the first organic light emitting diode D1 emit light.

[0019] Then, the second driving circuit 12 is supplied with the second gate pulse g2 from the second gate line GL2 and the second data signal d2 from the data line DL to make the second organic light emitting diode D2 emit light.

[0020] Unlike an LCD including a thin film transistor which is turned on only during a relatively short time in one frame, the OLED includes a driving thin film transistor which is included in each of the first and second driving circuits 11 and 12 and maintains a turn-on state during a relatively long time in one frame. Accordingly, the driving thin film transistor of the OLED is prone to deterioration.

[0021] Accordingly, a threshold voltage (Vth) of the driving thin film transistor is varied, and this variation negatively affects a display quality of the OLED.

[0022] In other words, because of the variation of the threshold voltage (Vth), a grey level different from a grey level of a data signal is displayed, and thus the display quality of the OLED is deteriorated.

[0023] Further, when the organic light emitting diodes D1 and D2 emit light continuously during a certain time, threshold voltages of the organic light emitting diodes D1 and D2 are also varied. Accordingly, a brightness of a light emitted from the organic light emitting diode is different from a target brightness, and a lifetime of the organic light emitting diode is reduced.

[0024] US 2010/0091006 A1 discloses an organic light emitting display device capable of compensating for the threshold voltage and mobility of a driving transistor. The device includes a pixel unit with a plurality of pixels formed at intersection areas of data and scan lines; a scan driving unit sequentially supplying a scan signal to the scan lines; a data driving unit supplying data signals to the data lines; a power supply unit outputting a high-potential pixel power source, a low-potential compensation power source and a low-potential ground power source to drive the pixels; and a power control unit supplying the compensation power source supplied from the power supply unit to the pixel unit during a first period (black frame period) of each frame, and supplying the pixel power source supplied from the power supply unit to the pixel unit during a second period (display frame period) of each of the frames.

[0025] US 2008/0238897 A1 discloses the prevention of display luminance difference and burning with a line at which the polarity inversion switches when the order of inversion of black and video changes in the middle of the screen by a frame polarity inversion drive in a liquid crystal display device for performing black insertion drive. An enable signal to each gate driver is independently controlled, a start pulse input to write a black signal is performed at an arbitrary timing within one frame period with respect to the gate driver to insert a black image within one frame period, a write polarity of the video signal is inverted in frame cycle with the video display start pulse as a base point, and a write polarity of the black image signal is inverted in frame cycle with the black display start pulse as a base point.

[0026] US 2001/0003448 A1 discloses a liquid crystal display driving process which prevents the appearance of motion blur without any increase in circuit size or any reduction in panel numerical aperture. Thereby a selecting any one of the scanning lines at one time, and altering the state of a liquid crystal via the signal line is provided, wherein an image data selection period and a black display selection period are set within a time frame shorter than the time necessary for scanning any one of the aforementioned scanning lines, and an image corresponding with the aforementioned image data is displayed via the aforementioned signal line during the image data selection period and a monochromatic image is displayed via the aforementioned signal line during the black display selection period.

[0027] US 2009/0262101 A1 discloses a display system. A display includes a plurality of pixels, each having a light emitting device and a driving transistor for driving the light emitting device, the driving transistor and the light emitting device being coupled in series between a first power supply and a second power supply. The method includes: at a first frame, programming a pixel with a first programming voltage different from a programming voltage for a valid image, and charging at least one of the first power supply and the second power supply so that at least one of the driving transistor and the light emitting device is under a negative bias. At a first cycle, an image display operation is implemented with programming the pixel circuit for a valid image and driving the light emitting device; and at a second cycle, a relaxation operation for reducing a stress on the pixel circuit is implemented that includes a selecting of a relaxation switch transistor coupled to the storage capacitor in parallel.

SUMMARY OF THE INVENTION

[0028] Accordingly, the present invention is directed to an OLED and a method of driving an OLED that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0029] An object of the present invention is to periodically reduce variances of threshold voltages of a driving thin film transistor and an organic light emitting diode.

[0030] Additional features and advantages of the disclosure will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the disclosure. The advantages of the disclosure will be realized and attained by the structure particularly pointed out in the written description and claims as well as the appended drawings.

[0031] The object is solved by the features of the independent claims.

[0032] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] The accompanying drawings, which are included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this specification, illustrate embodiments of the disclosure and together with the description serve to explain the principles of the disclosure. In the drawings:

FIG. 1 is a view illustrating organic light emitting diodes and driving circuits arranged at respective pixel regions of a display region of an OLED according to the related art;

FIG. 2 is a timing chart of gate pulses and data signals applied to the driving circuits of FIG. 1;

FIG. 3 is a view illustrating organic light emitting diodes and driving circuits arranged at respective pixel regions of a display region of an OLED according to

an embodiment of the present invention;

FIG. 4 is a timing chart of gate pulses, data signals and compensation signals applied to the driving circuits of FIG. 3;

FIGs. 5A to 5D are views illustrating an organic light emitting diode and a driving circuit of one pixel of an OLED according to the embodiment of the present invention; and

FIG. 6 is a timing chart of signals, including a gate pulse, a data signal and a compensation signal, supplied to the driving circuit of FIGs. 5A to 5D.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0034] Reference will now be made in detail to embodiments, examples of which are illustrated in the accompanying drawings. The same or like reference numbers may be used throughout the drawings to refer to the same or like parts.

[0035] FIG. 3 is a view illustrating organic light emitting diodes and driving circuits arranged at respective pixel regions of a display region of an OLED according to an embodiment of the present invention, and FIG. 4 is a timing chart of gate pulses, data signals and compensation signals applied to the driving circuits of FIG. 3.

[0036] Referring to FIG. 3, the OLED of the embodiment includes first and nth organic light emitting diodes D1 and D(n) and first and nth driving circuits 110 and 120 to operate the first and nth organic light emitting diodes D1 and D(n), respectively, in a display region 100, and n is an integer greater than 1.

[0037] In detail, the first driving circuit 110 is connected to a first gate line GL1 and each data line DL and operates the first organic light emitting diode D1, and the nth driving circuit 120 is connected to an nth gate line GL(n) and each data line DL and operates the nth organic light emitting diode D(n).

[0038] For the purpose of explanations, the first and nth driving circuits 110 and 120 are shown. However, a plurality of driving circuits may be arranged between the first and nth driving circuits 110 and 120, and thus a plurality of gate lines may be arranged between the first and nth gate lines GL1 and GL(n) connected to the first and nth driving circuits 110 and 120.

[0039] Further, a plurality of driving circuits may be arranged below the nth driving circuit 120, and thus a plurality of gate lines may be arranged below the nth gate line GL(n).

[0040] A method of driving the OLED of the embodiment is explained below.

[0041] The method of driving the OLED includes sequentially supplying a first gate pulse g1 and a second gate pulse g2 to the first gate line GL1 connected to the first driving circuit 110, and sequentially supplying a first data signal d1 and a first compensation signal r1 to each data line DL connected to the first driving circuit 110.

[0042] Further, the method further includes sequentially supplying a third gate pulse g3 and a fourth gate pulse g4 to the nth gate line GL(n) connected to the nth driving circuit 120, and sequentially supplying a second compensation signal r2 and a second data signal d2 to each data line DL connected to the nth driving circuit 120.

[0043] Referring to FIG. 4, during a frame, the first gate pulse g1 and the second gate pulse g2 are sequentially supplied to the first gate line GL1, and the third gate pulse g3 and the fourth gate pulse g4 are sequentially supplied to the nth gate line GL(n).

[0044] In other words, during a frame, two gate pulses are sequentially supplied to each gate line.

[0045] Further, the first gate pulse g1 and the third gate pulse g3 are sequentially supplied, and the fourth gate pulse g4 and the second gate pulse g2 are sequentially supplied.

[0046] In detail, the first gate pulse g1 is supplied to the first gate line GL1, and then the third gate pulse g3 is supplied to the nth gate line GL(n).

[0047] Next, the fourth gate pulse g4 is supplied to the nth gate line GL(n), and then the second gate pulse g2 is supplied to the first gate line GL1.

[0048] The first to fourth gate pulses g1 to g4 may have the same pulse width.

[0049] Further, the first data signal d1 and the second compensation signal r2 are sequentially supplied during a horizontal period H, and the second data signal d2 and the first compensation signal r1 are sequentially supplied during another horizontal period H

[0050] In other words, during each horizontal period H, each data signal d1 or d2 and each compensation signal r1 or r2 are sequentially supplied to each data line.

[0051] A ratio of supplying sections of the first data signal d1 and the second compensation signal r2 may be adjusted, and a ratio of supplying sections of the second data signal d2 and the first compensation signal r1 may be adjusted.

[0052] Further, gate pulses supplied to different gate lines may overlap each other, and by sequentially supplying the data signal d1 or d2 and the compensation signal r1 or r2 during one horizontal period H, the data signal d1 or d2 and the compensation signal r1 or r2 interfering with each other can be prevented. In this regard, for example, the third gate signal g3 may be overlap the first gate signal g1, and the third gate signal g3 may overlap the second compensation signal r2 and the first data signal d1 as well during the corresponding horizontal period H.

[0053] In this case, the first and second compensation signals r1 and r2 have voltage levels lower than the first and second data signals d1 and d2.

[0054] For example, because the first and second data signals d1 and d2 generally have a voltage level greater than 0V i.e., a positive polarity, the first and second compensation signals r1 and r2 preferably have a voltage

level of 0V.

[0055] Further, in an overlapping section between the first gate pulse g1 and the first data signal d1, the first data signal d1 is supplied to the first driving circuit 110. In an overlapping section between the second gate pulse g2 and the first compensation signal r1, the first compensation signal r1 is supplied to the first driving circuit 110.

[0056] Further, in an overlapping section between the third gate pulse g3 and the second compensation signal r2, the second compensation signal r2 is supplied to the nth driving circuit 120. In an overlapping section between the fourth gate pulse g4 and the second data signal d2, the second data signal d2 is supplied to the nth driving circuit 120.

[0057] Further, in a section (i.e., a light-emission section) from a falling point of the first gate pulse g1 to a rising point of the second gate pulse g2, the first organic light emitting diode D1 emits light. In a section (i.e., a compensation section) from a falling point of the second gate pulse g2 to a rising point of a first gate pulse g1 of a next frame, the first organic light emitting diode D1 does not emit light.

[0058] Further, in a section (i.e., a compensation section) from a falling point of the third gate pulse g3 to a rising point of the fourth gate pulse g4, the nth organic light emitting diode D(n) does not emit light. In a section (i.e., a light-emission section) from a falling point of the fourth gate pulse g4 to a rising point of a third gate pulse g3 of a next frame, the nth organic light emitting diode D(n) emits light.

[0059] Further, a ratio of the light-emission section and the compensation section may be adjusted according to the ratio of supplying sections of the data signal d1 or d2 and the compensation signal r1 or r2. Further, when adjusting the ratio of the light-emission section and the compensation section, the third gate signal g3 may not overlap the first gate signal g1 (e.g., the third gate signal g3 and the first gate signal g1 may be at different horizontal periods), and the second compensation signal r2 by the third gate signal g3 may not be immediately next to the first data signal d1 by the first gate signal g1 (e.g., the second compensation signal r2 and the first data signal d1 may be at different horizontal periods).

[0060] As shown in FIG. 3, the first driving circuit 110 is supplied with the first data signal d1 and the first compensation signal r1 by the first gate pulse g1 and the second gate pulse g2, and the nth driving circuit 120 is supplied with the second compensation signal r2 and the second data signal d2 by the third gate pulse g3 and the fourth gate signal g4.

[0061] In detail, the first driving circuit 110 is supplied with the first gate pulse g1 from the first gate line GL1 and the first data signal d1 from the data line DL to make the first organic light emitting diode D1 emit light, and then is supplied with the second gate pulse g2 from the first gate line GL1 and the first compensation signal r1 from the data line DL to make the first organic light emitting diode D1 not emit light

[0062] Further, the nth driving circuit 120 is supplied with the third gate pulse g3 from the nth gate line GL(n) and the second compensation signal r2 from the data line DL to make the nth organic light emitting diode D(n) not emit light, and then is supplied with the fourth gate pulse g4 from the nth gate line GL(n) and the second data signal d2 from the data line DL to make the nth organic light emitting diode D(n) emit light.

[0063] Accordingly, the method of driving the OLED of the embodiment substantially divides one frame into the light-emission section when the first or nth organic light emitting diode D1 or D(n) emits light, and the compensation section when the first or nth organic light emitting diode D1 and D(n) does not emit light. In the compensation section, the first or second compensation signal r1 or r2 having a voltage level lower than the first or second data signal d1 or d2 is supplied to the first or nth driving circuit 110 or 120, and thus a variance of a threshold voltage of a driving thin film transistor of the first or nth driving circuit 110 or 120 and a variance of a threshold voltage of the first or nth organic light emitting diodes D1 or D(n), which are caused by a voltage corresponding to the first or second data signal d1 or d2, can be reduced periodically.

[0064] FIGs. 5A to 5D are views illustrating an organic light emitting diode and a driving circuit of one pixel of an OLED according to the embodiment of the present invention.

[0065] For the purpose of explanations, a pixel including a first organic light emitting diode D1 and a first driving circuit 110 are shown. Other pixel including an nth organic light emitting diode (D(n) of FIG. 3) and an nth driving circuit (120 of FIG. 3) have the same configuration as the pixel in FIGs. 5A to 5D.

[0066] Referring to FIGs. 5A to 5D, the first driving circuit 110 includes a driving thin film transistor DT, a switching thin film transistor SWT, a sensing thin film transistor SST and a capacitor C.

[0067] In detail, the first organic light emitting diode D1 includes an anode connected to a first node N1, and a cathode supplied with a low power voltage VSS.

[0068] The first organic light emitting diode D1 generates light having a brightness corresponding to a drain current Ids supplied from the driving thin film transistor DT.

[0069] Further, the driving thin film transistor DT includes a gate electrode G connected to a switching thin film transistor SWT, a source electrode S connected to the first node N1, and a drain electrode D supplied with a high power voltage VDD greater than the low power voltage VSS.

[0070] When the driving thin film transistor DT is supplied with a first data signal d1 from the switching thin film transistor SWT, the drain current Ids generated according to a voltage between the gate electrode G and the source electrode S of the driving thin film transistor DT flows into the first node N1.

[0071] Further, the switching thin film transistor SWT

includes a gate electrode G connected to a first gate line GL1, a source electrode S connected to a data line DL, and a drain electrode D connected to the gate electrode G of the driving thin film transistor DT.

[0072] The switching thin film transistor SWT is supplied with a first or second gate pulses g1 or g2 and turned on, and thus a first data signal d1 or a first compensation signal r1 is supplied to the driving thin film transistor DT.

[0073] Further, the sensing thin film transistor SST includes a gate electrode G connected to a first sensing driving line SL1, a source electrode S connected to the first node N1, and a drain electrode D connected to a sensing sync line SSL.

[0074] The sensing thin film transistor SST functions to reset (or initialize) a current flowing on the first node N1 according to a reference voltage Vref supplied through the sensing sync line SSL.

[0075] Further, the capacitor C is connected between the first node N1 and the gate electrode G of the driving thin film transistor DT.

[0076] The capacitor C stores (i.e., is charged with) voltages corresponding to a first data signal d1 and the first compensation signal r1, respectively, and maintains the stored voltages during a frame.

[0077] Timings of the signals supplied to the first driving circuit 110 are explained below with reference to FIGs. 5A to 5D and FIG. 6.

[0078] FIG. 5A shows signals supplied to the first driving circuit 110 in a charging section of the first data signal d1, FIG. 5B shows signals supplied to the first driving circuit 110 in a light-emission section of the first organic light emitting diode D1, FIG. 5C shows signals supplied to the first driving circuit 110 in a charging section of the first compensation signal r1, and FIG. 5D shows signals supplied to the first driving circuit 110 in a compensation section of the driving thin film transistor.

[0079] FIG. 6 is a timing chart of signals, including a gate pulse, a data signal and a compensation signal, supplied to the driving circuit of FIGs. 5A to 5D.

[0080] First, in the charging section of the first data signal d1, the switching thin film transistor SWT is turned on by the first gate pulse g1 supplied through the first gate line GL1, and the first data signal d1 from the data line DL is supplied to the gate electrode G of the driving thin film transistor DT.

[0081] At the same timing as the first gate pulse g1, the sensing thin film transistor SST is turned on by a sensing signal s1 supplied through the first sensing driving line SL1, and the reference voltage Vref from the sensing sync line SSL is supplied to the first node N1 i.e., the source electrode S of the driving thin film transistor DT.

[0082] By the capacitor C, the gate electrode G and the source electrode S of the driving thin film transistor DT are charged with a voltage corresponding to the first data signal d1 and the reference voltage Vref, respectively.

[0083] Next, in the light-emission section of the first organic light emitting diode D1, the switching thin film transistor SWT and the sensing thin film transistor SST are turned off. The voltage corresponding to the first data signal d1 and the reference voltage Vref at the gate electrode G and the source electrode S of the driving thin film transistor DT are boosted, and the drain current Ids according to the voltages at the gate electrode G and the source electrode S of the driving thin film transistor DT flows onto the first node N1.

[0084] In this case, the first organic light emitting diode D1 emits light having a brightness according to a level of the drain current Ids.

[0085] Next, in the charging section of the first compensation signal r1, the switching thin film transistor SWT is turned on by the second gate pulse g2 supplied through the first gate line GL1, and the first compensation signal r1 from the data line DL is supplied to the gate electrode G of the driving thin film transistor DT.

[0086] In the charging section of the first compensation signal r1, the sensing thin film transistor SST is turned off.

[0087] Accordingly, by the capacitor C, the gate electrode G and the source electrode S of the driving thin film transistor DT are charged with a voltage lower than the voltage corresponding to the first data signal r1 and a voltage lower than the reference voltage Vref, respectively.

[0088] Next, in the compensation section of the driving thin film transistor DT, the switching thin film transistor SWT is turned off. Accordingly, by the capacitor C, the gate electrode G and the source electrode S of the driving thin film transistor DT are charged with a voltage corresponding to the first compensation signal r1 and a voltage lower than the low power voltage VSS, respectively.

[0089] The first compensation signal r1 has a voltage level lower than the first data signal d1.

[0090] Accordingly, the method of driving the OLED of the embodiment divides one frame into the light-emission section when the first organic light emitting diode D1 emit light, and the compensation section when the first organic light emitting diode D1 does not emit light. In the compensation section, the first compensation signal r1 having a voltage level lower than the first data signal d1 is supplied to the first driving circuit 110, and thus a variance of a threshold voltage of the driving thin film transistor DT and a variance of a threshold voltage of the first organic light emitting diode D1, which are caused by the voltage corresponding to the first data signal d1, can be reduced periodically.

[0091] In a preferred embodiment the light emission section is longer than the compensation section.

[0092] It will be apparent to those skilled in the art that various modifications and variations can be made in a display device of the present invention without departing from the scope of the disclosure. Thus, it is intended that the present invention covers the modifications and variations of this disclosure provided they come within the scope of the appended claims.

Claims

1. An organic light emitting diode display, comprising:

a display panel including a first organic light emitting diode (D1), a first driving circuit (110) arranged to operate the first organic light emitting diode (D1), a n^{th} organic light emitting diode (Dn) and a n^{th} driving circuit (120) arranged to operate the n^{th} organic light emitting diode (Dn), a first gate line (GL1) connected to the first driving circuit (110), a n^{th} gate line (GLn) connected to the n^{th} driving circuit (120), a data line (DL) connected to the first driving circuit (110) and to the n^{th} driving circuit (120), where n is an integer of 2 or greater;

a gate driver that is configured to sequentially supply a first gate pulse (g1) and a second gate pulse (g2) to the first gate line (GL1) connected to the first driving circuit (110) during one frame time, and that is configured to sequentially supply a third gate pulse (g3) and a fourth gate pulse (g4) to the n^{th} gate line (GLn) connected to the n^{th} driving circuit (120) during the one frame time such that the first gate pulse (g1) supplied to the first gate line (GL1) and the third gate pulse (g3) supplied to the n^{th} gate line (GLn) partially overlap each other and the second gate pulse (g2) supplied to the first gate line (GL1) and the fourth gate pulse (g4) supplied to the n^{th} gate line (GLn) partially overlap each other;

a data driver that is configured to sequentially supply a first data signal (d1) and a second compensation signal (r2) through the data line (DL) to the first driving circuit (110) and the n^{th} driving circuit (120), respectively, during one horizontal period (1H) of the one frame time, and that is configured to sequentially supply a second data signal (d2) and a first compensation signal (r1) through the data line (DL) to the n^{th} driving circuit (120) and the first driving circuit (110), respectively, during another horizontal period of the one frame time;

wherein the first compensation signal (r1) has a voltage level lower than the first data signals (d1),

wherein the second compensation signal (r2) has a voltage level lower than the second data signals (d2);

wherein the gate driver and data driver are arranged to supply the gate pulses, data and compensation signals such that

the first gate pulse (g1) and the first data signal (d1) have an overlapping period during which the first data signal (d1) is supplied to the first driving circuit (110) such that, from a falling point of the first gate pulse (g1) to the rising point of the second gate pulse (g2), the first driving circuit is adapted to operate the first organic light emitting diode (D1) according to the first data signal,

the second gate pulse (g2) and the first compensation signal (r1) have an overlapping period during which the first compensation signal (r1) is supplied to the first driving circuit (110), such that, from a falling point of the second gate pulse (g2) to a rising point of a first gate pulse (g1) of a next frame time, the first driving circuit is adapted to switch off the first light emitting diode (D1),

the third gate pulse (g3) and the second compensation signal (r2) have an overlapping period during which the second compensation signal (r2) is supplied to the n^{th} driving circuit (120), such that, from a falling point of the third gate pulse (g3) to the rising point of the fourth gate pulse (g4), the n^{th} driving circuit is adapted to switch off the n^{th} light emitting diode (Dn), and

the fourth gate pulse (g4) and the second data signal (d2) have an overlapping period during which the second data signal (d2) is supplied to the n^{th} driving circuit (120), such that, from a falling point of the fourth gate pulse (g4) to a rising point of a third gate pulse (g3) of a next frame time, the n^{th} driving circuit is adapted to operate the n^{th} organic light emitting diode (Dn) according to the second data signal.

2. A method of driving the organic light emitting diode display of claim 1, the method comprising:

sequentially supplying, by the gate driver, a first gate pulse (g1) and a second gate pulse (g2) to the first gate line (GL1) connected to the first driving circuit (110) during one frame time and sequentially supplying, by the gate driver, a third gate pulse (g3) and a fourth gate pulse (g4) to the n^{th} gate line (GLn) connected to the n^{th} driving circuit (120) during the one frame time such that the first gate pulse (g1) supplied to the first gate line (GL1) and the third gate pulse (g3) supplied to the n^{th} gate line (GLn) are sequentially supplied and partially overlap each other and the second gate pulse (g2) supplied to the first gate line (GL1) and the fourth gate pulse (g4) supplied to the n^{th} gate line (GLn) are sequentially supplied and partially overlap each other;

sequentially supplying, by the data driver, a first data signal (d1) and a second compensation signal (r2) through the data line (DL) to the first driving circuit (110) and the n^{th} driving circuit (120), respectively, during one horizontal period (1H) of the one frame time;

sequentially supplying, by the data driver, a second data signal (d2) and a first compensation signal (r1) through the data line (DL) to the n^{th} driving circuit (120) and the first driving circuit

(110), respectively, during another horizontal period of the one frame time;
wherein the first compensation signal (r1) has a voltage level lower than the first data signals (d1, wherein the second compensation signals (r2) has a voltage level lower than the second data signals (d2);
wherein the first gate pulse (g1) and the first data signal (d1) are supplied with an overlapping period during which the first data signal (d1) is supplied to the first driving circuit (110) such that, from a falling point of the first gate pulse (g1) to the rising point of the second gate pulse (g2), the first driving circuit is adapted to operate the first organic light emitting diode (D1) according to the first data signal;
wherein the second gate pulse (g2) and the first compensation signal (r1) are supplied with an overlapping period during which the first compensation signal (r1) is supplied to the first driving circuit (110) such that, from a falling point of the second gate pulse (g2) to a rising point of a first gate pulse (g1) of a next frame time, the first driving circuit is adapted to switch off the first light emitting diode (D1);
wherein the third gate pulse (g3) and the second compensation signal (r2) are supplied with an overlapping period during which the second compensation signal (r2) is supplied to the n^{th} driving circuit (120) such that, from a falling point of the third gate pulse (g3) to the rising point of the fourth gate pulse (g4), the n^{th} driving circuit is adapted to switch off the n^{th} light emitting diode (Dn);
wherein the fourth gate pulse (g4) and the second data signal (d2) are supplied with an overlapping period during which the second data signal (d2) is supplied to the n^{th} driving circuit (120) such that, from a falling point of the fourth gate pulse (g4) to a rising point of a third gate pulse (g3) of a next frame time, the n^{th} driving circuit is adapted to operate the n^{th} organic light emitting diode (Dn) according to the second data signal.

Patentansprüche

1. Anzeige mit organischen Leuchtdioden, umfassend:

eine Anzeigetafel, die eine erste organische Leuchtdiode (D1) umfasst, eine erste Ansteuerungsschaltung (110), die dazu angeordnet ist, die erste organische Leuchtdiode (D1) zu betreiben, eine n-te organische Leuchtdiode (Dn) und eine n-te Ansteuerungsschaltung (120), die dazu angeordnet ist, die n-te organische Leuchtdiode (Dn) zu betreiben, eine erste Gate-Leitung (GL1), die mit der ersten Ansteuerungsschaltung (110) verbunden ist, eine n-te Gate-Leitung (GLn), die mit der n-ten Ansteuerungsschaltung (120) verbunden ist, eine Datenleitung (DL), die mit der ersten Ansteuerungsschaltung (110) und mit der n-ten Ansteuerungsschaltung (120) verbunden ist, worin n eine Ganzzahl von 2 oder größer ist;
einen Gate-Treiber, der dazu ausgelegt ist, sequenziell einen ersten Gate-Impuls (g1) und einen zweiten Gate-Impuls (g2) an die erste Gate-Leitung (GL1), die mit der ersten Ansteuerungsschaltung (110) verbunden ist, während einer Rahmenzeit zu liefern, und der dazu ausgelegt ist, sequenziell einen dritten Gate-Impuls (g3) und einen vierten Gate-Impuls (g4) an die n-te Gate-Leitung (GLn), die mit der n-ten Ansteuerungsschaltung (120) verbunden ist, während der einen Rahmenzeit zu liefern, sodass der erste Gate-Impuls (g1), der an die erste Gate-Leitung (GL1) geliefert wird, und der dritte Gate-Impuls (g3), der an die n-te Gate-Leitung (GLn) geliefert wird, einander teilweise überlagern, und der zweite Gate-Impuls (g2), der an die erste Gate-Leitung (GL1) geliefert wird, und der vierte Gate-Impuls (g4), der an die n-te Gate-Leitung (GLn) geliefert wird, einander teilweise überlagern;
einen Datentreiber, der dazu ausgelegt ist, sequenziell ein erstes Datensignal (d1) und ein zweites Kompensationssignal (r2) über die Datenleitung (DL) an die erste Ansteuerungsschaltung (110) bzw. die n-te Ansteuerungsschaltung (120) während einer horizontalen Periode (1H) der einen Rahmenzeit zu liefern, und der dazu ausgelegt ist, sequenziell ein zweites Datensignal (d2) und ein erstes Kompensationssignal (r1) über die Datenleitung (DL) an die n-te Ansteuerungsschaltung (120) bzw. die erste Ansteuerungsschaltung (110) während einer anderen horizontalen Periode der einen Rahmenzeit zu liefern;
wobei das erste Kompensationssignal (r1) einen Spannungspegel aufweist, der niedriger ist als die ersten Datensignale (d1),
wobei das zweite Kompensationssignal (r2) einen Spannungspegel aufweist, der niedriger ist als die zweiten Datensignale (d2);
wobei der Gate-Treiber und der Datentreiber dazu angeordnet sind, die Gate-Impulse, Daten und Kompensationssignale zu liefern, sodass der erste Gate-Impuls (g1) und das erste Datensignal (d1) einen Überlagerungszeitraum aufweisen, in dem das erste Datensignal (d1) an die erste Ansteuerungsschaltung (110) geliefert wird, sodass von einem Abfallpunkt des ersten Gate-Impulses (g1) bis zum Anstiegspunkt des zweiten Gate-Impulses (g2) die erste Ansteue-

rungsschaltung dazu angepasst ist, die erste organische Leuchtdiode (D1)gemäß dem ersten Datensignal zu betreiben,
der zweite Gate-Impuls (g2) und das erste Kompensationssignal (r1) einen Überlagerungszeitraum aufweisen, in dem das erste Kompensationssignal (r1) an die erste Ansteuerungsschaltung (110) geliefert wird, sodass von einem Abfallpunkt des zweiten Gate-Impulses (g2) bis zum Anstiegspunkt des ersten Gate-Impulses (g1) einer nächsten Rahmenzeit, die erste Ansteuerungsschaltung dazu angepasst ist, die erste Leuchtdiode (D1) auszuschalten,
der dritte Gate-Impuls (g3) und das zweite Kompensationssignal (r2) einen Überlagerungszeitraum aufweisen, in dem das zweite Kompensationssignal (r2) an die n-te Ansteuerungsschaltung (120) geliefert wird, sodass von einem Abfallpunkt des dritten Gate-Impulses (g3) bis zu dem Anstiegspunkt des vierten Gate-Impulses (g4) die n-te Ansteuerungsschaltung dazu angepasst ist, die n-te Leuchtdiode (Dn) auszuschalten, und der vierte Gate-Impuls (g4) und das zweite Datensignal (d2) einen Überlagerungszeitraum aufweisen, in dem das zweite Datensignal (d2) an die n-te Ansteuerungsschaltung (120) geliefert wird, sodass von einem Abfallpunkt des vierten Gate-Impulses (g4) bis zu einem Anstiegspunkt eines dritten Gate-Impulses (g3) einer nächsten Rahmenzeit die n-te Ansteuerungsschaltung dazu angepasst ist, die n-te organische Leuchtdiode (Dn) gemäß dem zweiten Datensignal zu betreiben.

2. Verfahren zur Ansteuerung der Anzeige mit organischen Leuchtdioden nach Anspruch 1, wobei das Verfahren umfasst:

sequenzielles Liefern eines ersten Gate-Impulses (g1) und eines zweiten Gate-Impulses (g2) durch den Gate-Treiber an die erste Gate-Leitung (GL1), die mit der ersten Ansteuerungsschaltung (110) verbunden ist, während einer Rahmenzeit und sequenzielles Liefern eines dritten Gate-Impulses (g3) und eines vierten Gate-Impulses (g4) durch den Gate-Treiber an die n-te Gate-Leitung (GLn), die mit der n-ten Ansteuerungsschaltung (120) verbunden ist, während der einen Rahmenzeit, sodass der erste Gate-Impuls (g1), der an die erste Gate-Leitung (GL1) geliefert wurde, und der dritte Gate-Impuls (g3), der an die n-te Gate-Leitung (GLn) geliefert wurde, sequenziell geliefert werden und einander teilweise überlagern, und der zweite Gate-Impuls (g2), der an die erste Gate-Leitung (GL1) geliefert wurde, und der vierte Gate-Impuls (g4), der an die n-te Gate-Leitung (GLn) geliefert wurde, sequenziell geliefert werden und einander teilweise überlagern;
sequenzielles Liefern eines ersten Datensignals (d1) und eines zweiten Kompensationssignals (r2) durch den Datentreiber über die Datenleitung (DL) an die erste Ansteuerungsschaltung (110) bzw. die n-te Ansteuerungsschaltung während einer horizontalen Periode (1H) der einen Rahmenzeit;
sequenzielles Liefern eines zweiten Datensignals (d2) und eines ersten Kompensationssignals (r1) durch den Datentreiber über die Datenleitung (DL) an die n-te Ansteuerungsschaltung (120) bzw. die erste Ansteuerungsschaltung (110) während einer anderen horizontalen Periode der einen Rahmenzeit;
wobei das erste Kompensationssignal (r1) einen Spannungspegel aufweist, der niedriger ist als die ersten Datensignale (d1), wobei das zweite Kompensationssignal (r2) einen Spannungspegel aufweist, der niedriger ist als die zweiten Datensignale (d2);
wobei der erste Gate-Impuls (g1) und das erste Datensignal (d1) mit einem Überlagerungszeitraum geliefert werden, in dem das erste Datensignal (d1) an die erste Ansteuerungsschaltung (110) geliefert wird, sodass von einem Abfallpunkt des ersten Gate-Impulses (g1) bis zum Anstiegspunkt des zweiten Gate-Impulses (g2) die erste Ansteuerungsschaltung dazu angepasst ist, die erste organische Leuchtdiode (D1) gemäß dem ersten Datensignal zu betreiben;
wobei der zweite Gate-Impuls (g2) und das erste Kompensationssignal (r1) mit einem Überlagerungszeitraum geliefert werden, in dem das erste Kompensationssignal (r1) an die erste Ansteuerungsschaltung (110) geliefert wird, sodass von einem Abfallpunkt des zweiten Gate-Impulses (g2) bis zum Anstiegspunkt eines ersten Gate-Impulses (g1) einer nächsten Rahmenzeit die erste Ansteuerungsschaltung dazu angepasst ist, die erste Leuchtdiode (D1) auszuschalten;
wobei der dritte Gate-Impuls (g3) und das zweite Kompensationssignal (r2) mit einem Überlagerungszeitraum geliefert werden, in dem das zweite Kompensationssignal (r2) an die n-te Ansteuerungsschaltung (120) geliefert wird, sodass von einem Abfallpunkt des dritten Gate-Impulses (g3) bis zum Anstiegspunkt des vierten Gate-Impulses (g4) die n-te Ansteuerungsschaltung dazu angepasst ist, die n-te organische Leuchtdiode (Dn) auszuschalten;
wobei der vierte Gate-Impuls (g4) und das zweite Datensignal (d2) mit einem Überlagerungszeitraum geliefert werden, in dem das zweite Datensignal (d2) an die n-te Ansteuerungsschaltung (120) geliefert wird, sodass von einem Abfallpunkt des vierten Gate-Impulses (g4) bis

zu einem Anstiegspunkt des dritten Gate-Impulses (g3) einer nächsten Rahmenzeit die n-te Ansteuerungsschaltung dazu angepasst ist, die n-te organische Leuchtdiode (Dn) gemäß dem zweiten Datensignal zu betreiben.

Revendications

1. Affichage à diodes électroluminescentes organiques, comportant :

un panneau d'affichage incluant une première diode électroluminescente organique (D1), un premier circuit d'attaque (110) conçu pour faire fonctionner la première diode électroluminescente organique (D1), une $n^{ème}$ diode électroluminescente organique (Dn) et un $n^{ème}$ circuit d'attaque (120) conçu pour faire fonctionner la $n^{ème}$ diode électroluminescente organique (Dn), une première ligne de grille (GL1) reliée au premier circuit d'attaque (110), une $n^{ème}$ ligne de grille (GLn) reliée au $n^{ème}$ circuit d'attaque (120), une ligne de données (DL) reliée au premier circuit d'attaque (110) et au $n^{ème}$ circuit d'attaque (120), où n est un entier supérieur ou égal à 2 ;
un circuit d'attaque de grille qui est configuré pour délivrer séquentiellement une première impulsion de grille (g1) et une deuxième impulsion de grille (g2) à la première ligne de grille (GL1) reliée au premier circuit d'attaque (110) pendant un temps de trame, et qui est configuré pour délivrer séquentiellement une troisième impulsion de grille (g3) et une quatrième impulsion de grille (g4) à la $n^{ème}$ ligne de grille (GLn) reliée au $n^{ème}$ circuit d'attaque (120) pendant le temps de trame de telle sorte que la première impulsion de grille (g1) délivrée à la première ligne de grille (GL1) et la troisième impulsion de grille (g3) délivrée à la $n^{ème}$ ligne de grille (GLn) se chevauchent partiellement et la deuxième impulsion de grille (g2) délivrée à la première ligne de grille (GL1) et la quatrième impulsion de grille (g4) délivrée à la $n^{ème}$ ligne de grille (GLn) se chevauchent partiellement ;
un circuit d'attaque de données qui est configuré pour délivrer séquentiellement un premier signal de données (d1) et un second signal de compensation (r2) via la ligne de données (DL) au premier circuit d'attaque (110) et au $n^{ème}$ circuit d'attaque (120), respectivement, pendant une période horizontale (1H) du temps de trame, et qui est configuré pour délivrer séquentiellement un second signal de données (d2) et un premier signal de compensation (r1) via la ligne de données (DL) au $n^{ème}$ circuit d'attaque (120) et au premier circuit d'attaque (110), respectivement, pendant une autre période horizontale du temps de trame ;
dans lequel le premier signal de compensation (r1) a un niveau de tension inférieur aux premiers signaux de données (D1),
dans lequel le second signal de compensation (r2) a un niveau de tension inférieur aux seconds signaux de données (d2) ;
dans lequel le circuit d'attaque de grille et le circuit d'attaque de données sont conçus pour délivrer les impulsions de grille, les signaux de données et les signaux de compensation de telle sorte que
la première impulsion de grille (g1) et le premier signal de données (d1) ont une période de chevauchement pendant laquelle le premier signal de données (d1) est délivré au premier circuit d'attaque (110) de telle sorte que, à partir d'un point de descente de la première impulsion de grille (g1) jusqu'au point de montée de la deuxième impulsion de grille (g2), le premier circuit d'attaque est adapté pour faire fonctionner la première diode électroluminescente organique (D1) en fonction du premier signal de données,
la deuxième impulsion de grille (g2) et le premier signal de compensation (r1) ont une période de chevauchement pendant laquelle le premier signal de compensation (r1) est délivré au premier circuit d'attaque (110), de telle sorte que, à partir d'un point de descente de la deuxième impulsion de grille (g2) jusqu'à un point de montée d'une première impulsion de grille (g1) d'un temps de trame suivant, le premier circuit d'attaque est adapté pour éteindre la première diode électroluminescente (D1),
la troisième impulsion de grille (g3) et le second signal de compensation (r2) ont une période de chevauchement pendant laquelle le second signal de compensation (r2) est délivré au $n^{ème}$ circuit d'attaque (120), de telle sorte que, à partir d'un point de descente de la troisième impulsion de grille (g3) jusqu'au point de montée de la quatrième impulsion de grille (g4), le $n^{ème}$ circuit d'attaque est adapté pour éteindre la $n^{ème}$ diode électroluminescente (Dn), et
la quatrième impulsion de grille (g4) et le second signal de données (d2) ont une période de chevauchement pendant laquelle le second signal de données (d2) est délivré au $n^{ème}$ circuit d'attaque (120), de telle sorte que, à partir d'un point de descente de la quatrième impulsion de grille (g4) jusqu'à un point de montée d'une troisième impulsion de grille (g3) d'un temps de trame suivant, le $n^{ème}$ circuit d'attaque est adapté pour faire fonctionner la $n^{ème}$ diode électroluminescente organique (Dn) en fonction du second signal de données.

2. Procédé de commande d'un affichage à diodes élec-

troluminescentes organiques selon la revendication 1, le procédé comportant les étapes consistant à :

délivrer séquentiellement, par le circuit d'attaque de grille, une première impulsion de grille (g1) et une deuxième impulsion de grille (g2) à la première ligne de grille (GL1) reliée au premier circuit d'attaque (110) pendant un temps de trame, et délivrer séquentiellement, par le circuit d'attaque de grille, une troisième impulsion de grille (g3) et une quatrième impulsion de grille (g4) à la $n^{ème}$ ligne de grille (GLn) reliée au $n^{ème}$ circuit d'attaque (120) pendant le temps de trame de telle sorte que la première impulsion de grille (g1) délivrée à la première ligne de grille (GL1) et la troisième impulsion de grille (g3) délivrée à la $n^{ème}$ ligne de grille (GLn) sont délivrées séquentiellement et se chevauchent partiellement et la deuxième impulsion de grille (g2) délivrée à la première ligne de grille (GL1) et la quatrième impulsion de grille (g4) délivrée à la $n^{ème}$ ligne de grille (GLn) sont délivrées séquentiellement et se chevauchent partiellement ;

délivrer séquentiellement, par le circuit d'attaque de données, un premier signal de données (d1) et un second signal de compensation (r2) via la ligne de données (DL) au premier circuit d'attaque (110) et au $n^{ème}$ circuit d'attaque (120), respectivement, pendant une période horizontale (1H) du temps de trame ;

délivrer séquentiellement, par le circuit d'attaque de données, un second signal de données (d2) et un premier signal de compensation (r1) via la ligne de données (DL) au $n^{ème}$ circuit d'attaque (120) et au premier circuit d'attaque (110), respectivement, pendant une autre période horizontale du temps de trame ;

dans lequel le premier signal de compensation (r1) a un niveau de tension inférieur aux premiers signaux de données (d1), dans lequel les seconds signaux de compensation (r2) ont un niveau de tension inférieur aux seconds signaux de données (d2) ;

dans lequel la première impulsion de grille (g1) et le premier signal de données (d1) sont délivrés avec une période de chevauchement pendant laquelle le premier signal de données (d1) est délivré au premier circuit d'attaque (110) de telle sorte que, à partir d'un point de descente de la première impulsion de grille (g1) jusqu'au point de montée de la deuxième impulsion de grille (g2), le premier circuit d'attaque est adapté pour faire fonctionner la première diode électroluminescente organique (D1) en fonction du premier signal de données ;

dans lequel la deuxième impulsion de grille (g2) et le premier signal de compensation (r1) sont délivrés avec une période de chevauchement pendant laquelle le premier signal de compensation (r1) est délivré au premier circuit d'attaque (110) de telle sorte que, à partir d'un point de descente de la deuxième impulsion de grille (g2) jusqu'à un point de montée d'une première impulsion de grille (g1) d'un temps de trame suivant, le premier circuit d'attaque est adapté pour éteindre la première diode électroluminescente (D1);

dans lequel la troisième impulsion de grille (g3) et le second signal de compensation (r2) sont délivrés avec une période de chevauchement pendant laquelle le second signal de compensation (r2) est délivré au $n^{ème}$ circuit d'attaque (120), de telle sorte que, à partir d'un point de descente de la troisième impulsion de grille (g3) jusqu'au point de montée de la quatrième impulsion de grille (g4), le $n^{ème}$ circuit d'attaque est adapté pour éteindre la $n^{ème}$ diode électroluminescente (Dn) ;

dans lequel la quatrième impulsion de grille (g4) et le second signal de données (d2) sont délivrés avec une période de chevauchement pendant laquelle le second signal de données (d2) est délivré au $n^{ème}$ circuit d'attaque (120), de telle sorte que, à partir d'un point de descente de la quatrième impulsion de grille (g4) jusqu'à un point de montée d'une troisième impulsion de grille (g3) d'un temps de trame suivant, le $n^{ème}$ circuit d'attaque est adapté pour faire fonctionner la $n^{ème}$ diode électroluminescente organique (Dn) en fonction du second signal de données.

FIG. 1 (RELATED ART)

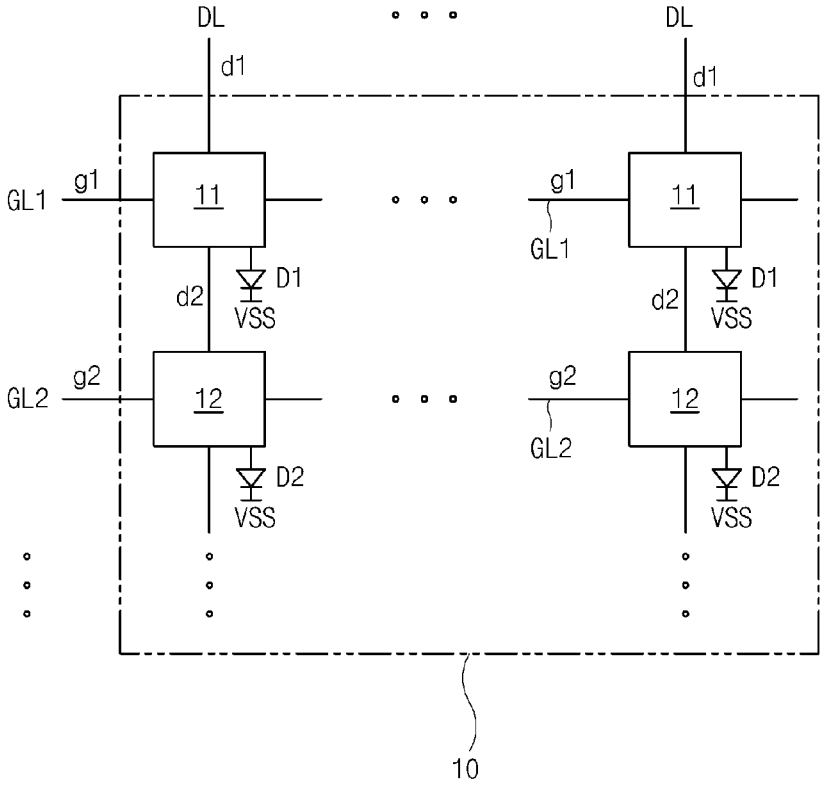


FIG. 2 (RELATED ART)

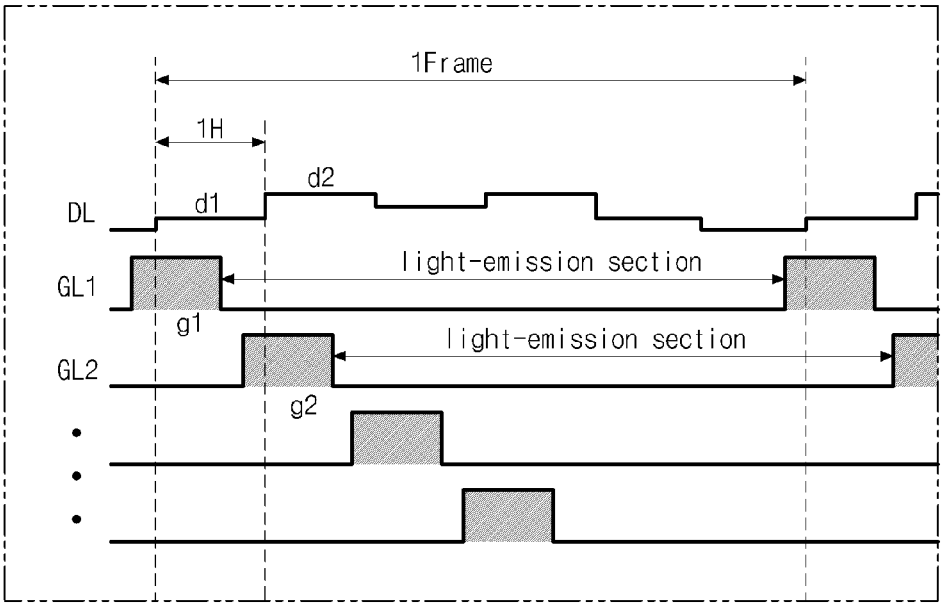


FIG. 3

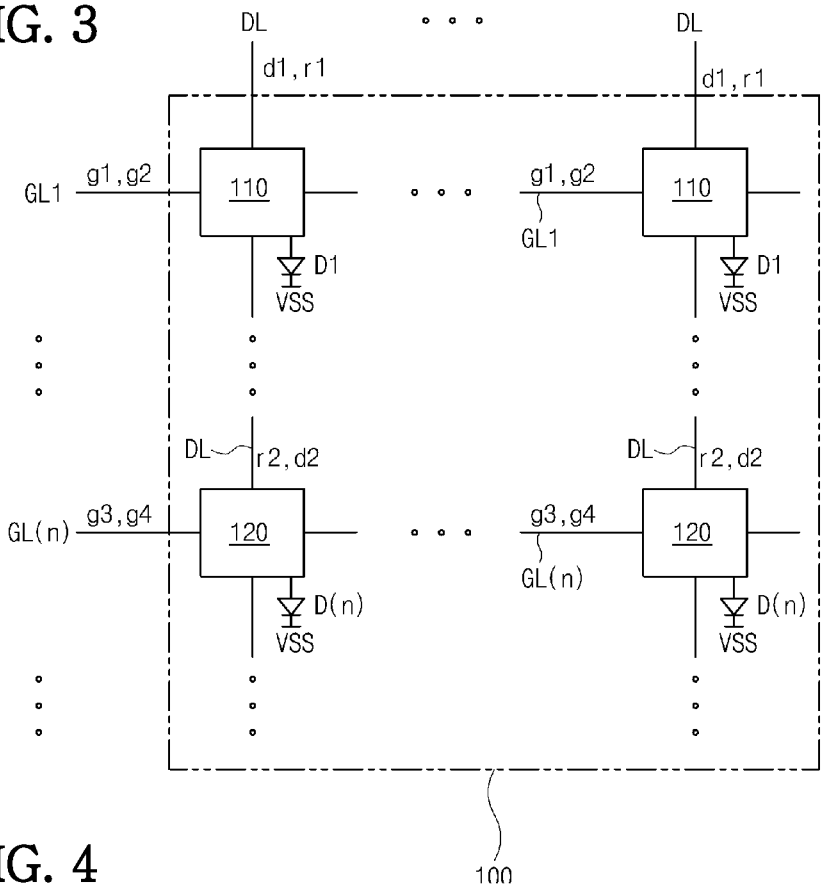

DL
d1,r1
GL1
g1,g2
110
D1
VSS
GL(n)
g3,g4
120
D(n)
r2,d2
100

FIG. 4

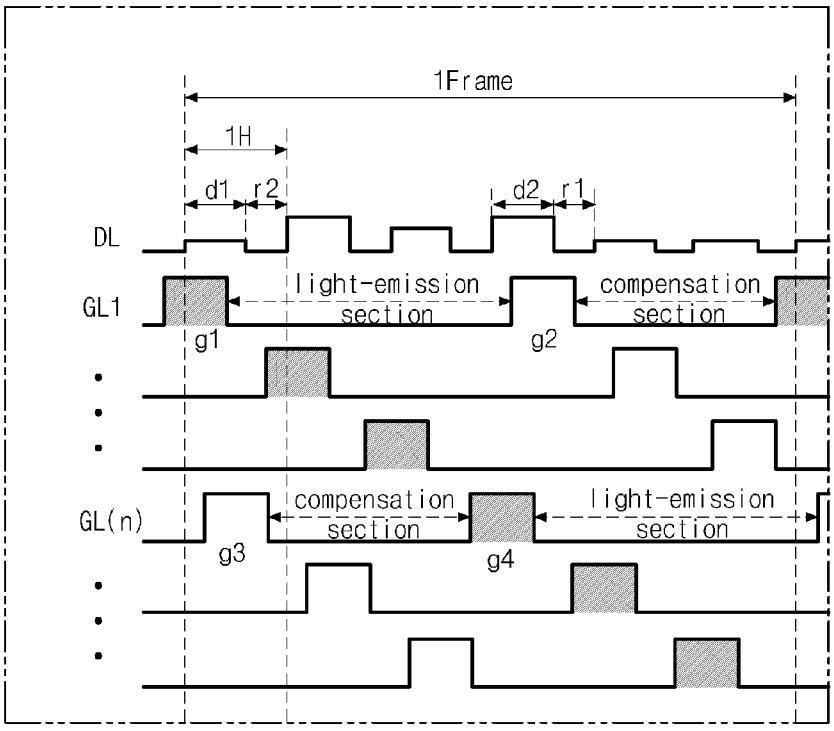

1Frame
1H
d1
r2
d2
r1
DL
GL1
light-emission section
compensation section
g1
g2
GL(n)
g3
g4

FIG. 5A

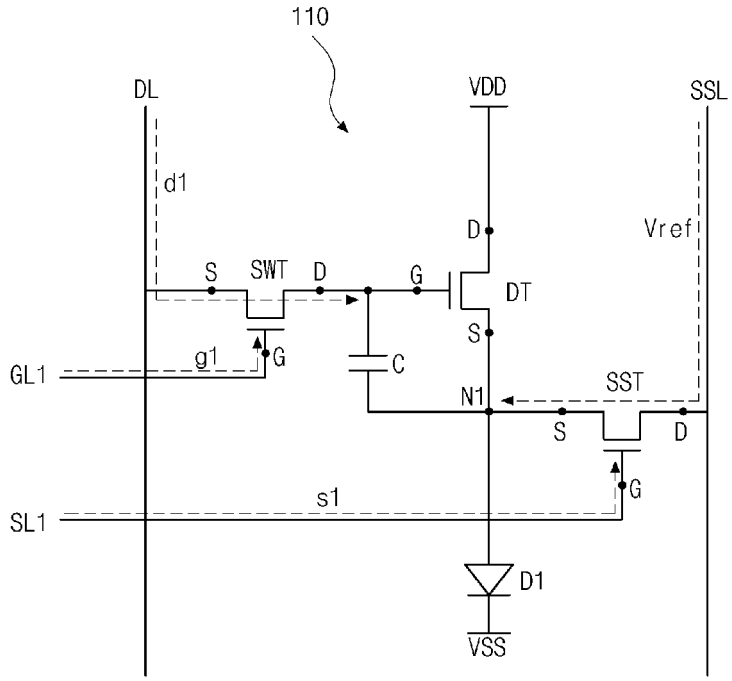

110
DL
VDD
SSL
d1
D
Vref
S
SWT
D
G
DT
S
g1
G
C
GL1
N1
SST
S
D
G
s1
SL1
D1
VSS

FIG. 5B

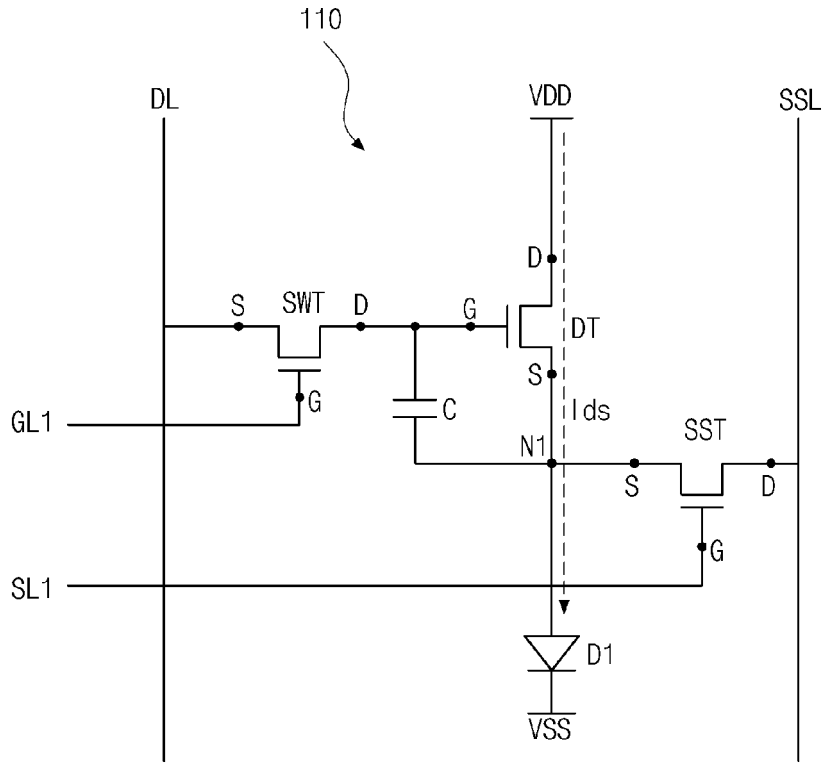

110
DL
VDD
SSL
D
S
SWT
D
G
DT
S
G
C
Ids
GL1
N1
SST
S
D
G
SL1
D1
VSS

FIG. 5C

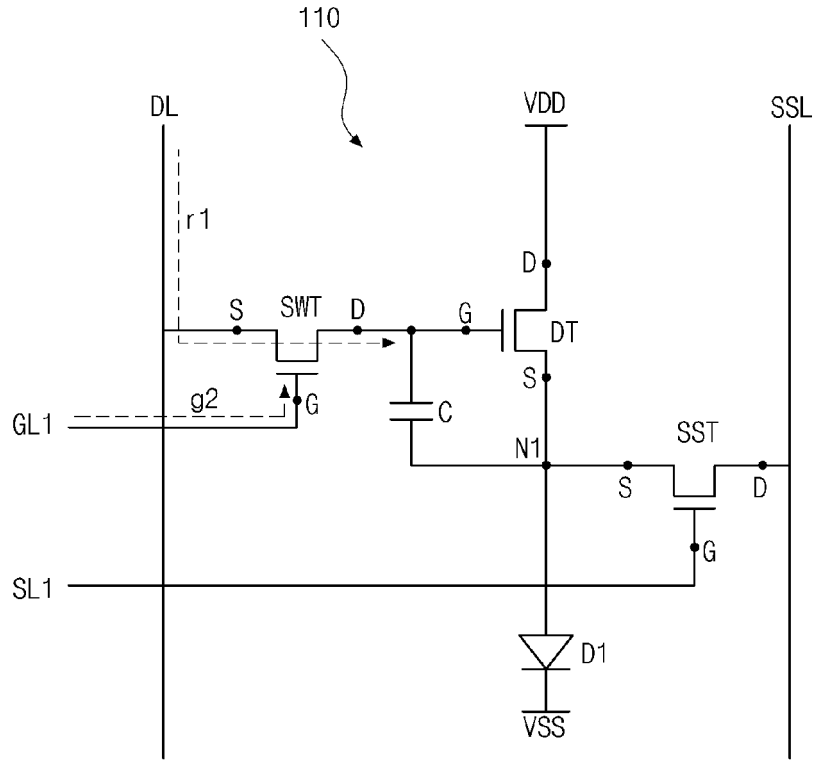

110
DL
VDD
SSL
r1
D
S
SWT
D
G
DT
S
g2
G
C
GL1
N1
SST
S
D
G
SL1
D1
VSS

FIG. 5D

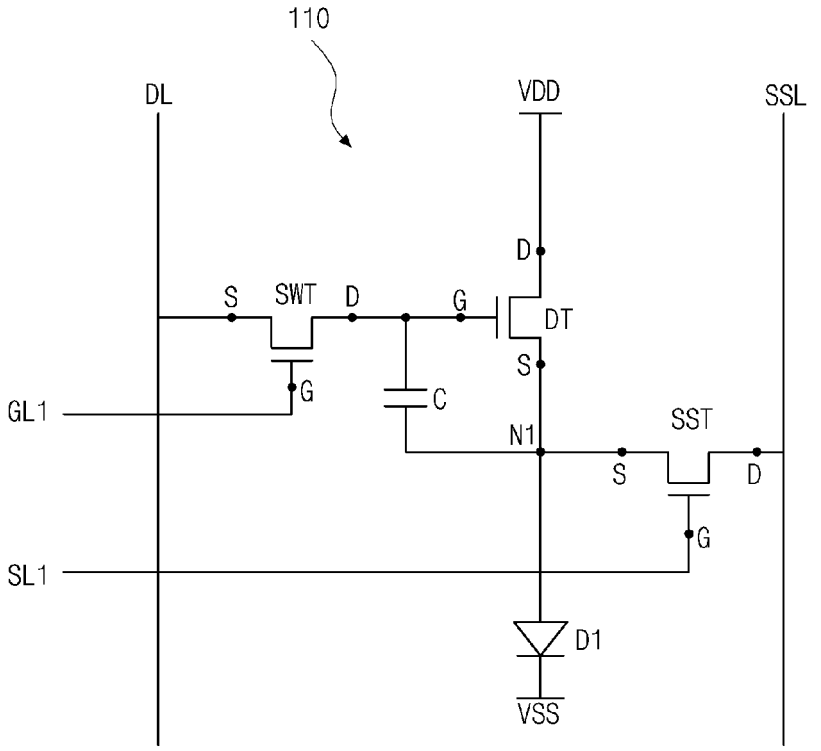
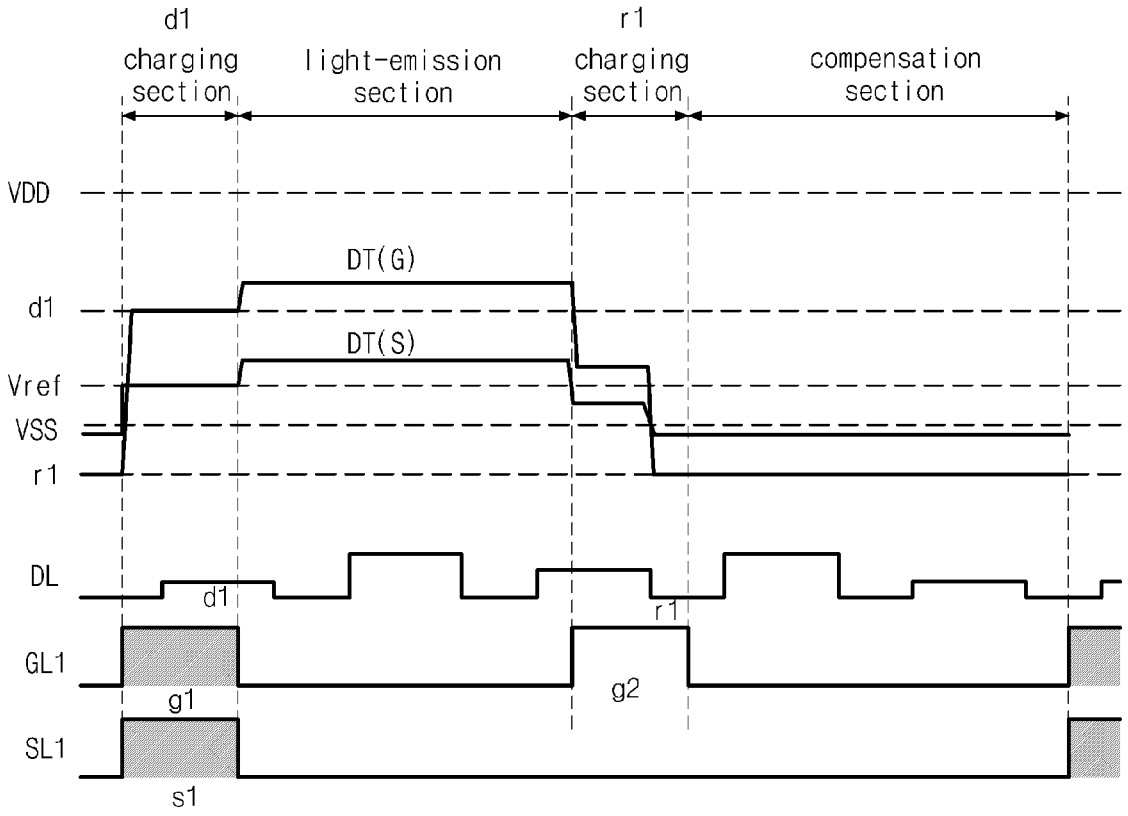

110
DL
VDD
SSL
D
S
SWT
D
G
DT
S
G
C
GL1
N1
SST
S
D
G
SL1
D1
VSS

FIG. 6


d1
charging
section
light-emission
section
r1
charging
section
compensation
section
VDD
DT(G)
d1
DT(S)
Vref
VSS
r1
DL
d1
r1
GL1
g1
g2
SL1
s1

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- KR 1020150104280 **[0001]**
- US 20100091006 A1 **[0024]**
- US 20080238897 A1 **[0025]**
- US 20010003448 A1 **[0026]**
- US 20090262101 A1 **[0027]**

专利名称(译)	控制OLED显示的过程		
公开(公告)号	EP3121805B1	公开(公告)日	2019-11-06
申请号	EP2016180868	申请日	2016-07-22
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	RYU HON JIN KIM SEONG HYUN		
发明人	RYU, HON-JIN KIM, SEONG-HYUN		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3208 G09G3/2081 G09G3/3233 G09G2310/0205 G09G2310/0251 G09G2320/045 G09G3/3266 G09G3/3291		
优先权	1020150104280 2015-07-23 KR		
其他公开文献	EP3121805A1		
外部链接	Espacenet		

摘要(译)

公开了一种有机发光二极管显示器以及驱动该有机发光二极管显示器的方法，该方法包括第一有机发光二极管（D1）和用于操作该第一有机发光二极管的第一驱动电路（110）。包括向连接到第一驱动电路（110）的第一栅极线（GL1）提供第一栅极脉冲（g1）和第二栅极脉冲（g1）；以及提供第一数据信号（d1）和第一补偿信号（ r1）到连接到第一驱动电路（110）的数据线（DL）。

FIG. 1 (RELATED ART)

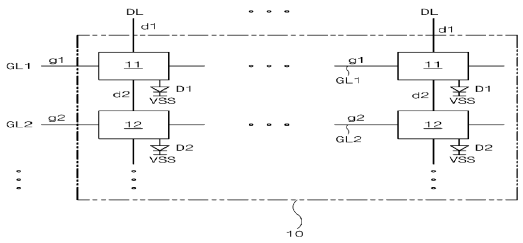


FIG. 2 (RELATED ART)