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(54) **Organic light emitting display device having compensation pixel structure**

Organische lichtemittierende Anzeigevorrichtung mit Kompensationpixelstruktur

Dispositif d'affichage électroluminescent organique ayant une structure de pixel de compensation

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Description

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from Korean Patent Application Number 10-2013-0155542 filed on December 13, 2013.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to an organic light-emitting display device.

Description of Related Art

[0003] Organic light-emitting display devices that are recently in the spotlight as next generation display devices have advantages, such as relatively fast response speeds, high light emitting efficiency and luminance and wide viewing angles, since they use organic light-emitting diodes (OLEDs) that emit light by themselves.

[0004] Organic light-emitting display devices have a matrix structure in which pixels including organic light-emitting diodes are arranged, in which the brightness of each pixel selected by a scanning signal is controlled according to the grayscale of data.

[0005] Each pixel in such an organic light-emitting display device includes an organic light-emitting diode (OLED) as well as a driving transistor for driving the OLED. The driving transistor has unique characteristics such as a threshold voltage and mobility. A difference in the characteristic value between the driving transistors of adjacent pixels may reduce the luminance quality of the corresponding pixels.

[0006] Therefore, the development of pixel structures for compensating for the threshold voltage and mobility of the driving transistor is underway.

[0007] However, in spite of such compensation technology, information about the threshold voltage is lost by a parasitic capacitor component at the gate node of the driving transistor, which is problematic. The loss in the information about the threshold voltage may lead to a severe non-uniform image quality.

[0008] US 2010/289830 describes a display device including a pixel circuit for generating a signal value for display by synthesizing signal values input within one horizontal period, and making display at a gradation corresponding to the signal value for display, a signal line disposed in a form of a column on a pixel array where the pixel circuit is arranged in a form of a matrix, a scanning line disposed in a form of a row on the pixel array, a signal line driving section configured to output signal values as a signal value to be supplied to each pixel circuit to the signal line within one horizontal period, and a scanning line driving section configured to sequentially introduce the signal values within one horizontal period, the signal values being generated in the signal line, into the pixel circuit in each row by driving the scanning line. US 2010/289830 further describes that the pixel circuit includes a light emitting element, a driving transistor for applying a current corresponding to said signal value for display, said signal value for display being input to the driving transistor, to said light emitting element, a capacitance having one end as a point of input of said signal value for display to a gate node of said driving transistor, a first switch element connected between said one end of said capacitance and said signal line, and conduction-controlled by a potential of a first scanning line, and a second switch element connected between another end of said capacitance and said signal line, and conduction-controlled by a potential of a second scanning line, and when said first signal value is output to said signal line, said scanning line driving section makes said first switch element and said second switch element conduct to input said first signal value to both ends of said capacitance, and when said second signal value is output to said signal line, said scanning line driving section makes only said second switch element conduct to input said second signal value to said other end of said capacitance, whereby said signal value for display resulting from synthesis of said first signal value and said second signal value is obtained at said input point.

[0009] US 2013/249857 describes a semiconductor device (e.g., a light-emitting device, a display device) including a first wiring, a first capacitor, a second capacitor, a first switch having a function of controlling electrical connection between the first wiring and one of a pair of electrodes of the first capacitor and between the first wiring and one of a pair of electrodes of the second capacitor, a second wiring, a transistor one of a source and a drain of which is electrically connected to the second wiring and a gate of which is electrically connected to the other of the pair of electrodes of the first capacitor, a second switch having a function of controlling electrical connection between the gate of the transistor and the one of the source and the drain of the transistor, and a third switch having a function of controlling electrical connection between the other of the source and the drain of the transistor and the one of the pair of electrodes of the first capacitor and between the other of the source and the drain of the transistor and the one of the pair of electrodes

of the second capacitor.

[0010] WO 2013/021623 and US 2014/022288 describe a driving method of a display apparatus including a plurality of arrayed pixel circuits. Each of the pixel circuits includes a current light emitting device, a driving transistor supplying current to the current light emitting device, a first capacitor having a first terminal connected to a gate of the driving transistor, a second capacitor connected between a second terminal of the first capacitor and a source of the driving transistor, a first switch applying a reference voltage to the gate of the driving transistor, a second switch supplying an image signal voltage to a node at which the first and the second capacitors are connected, a third switch supplying an initialization voltage to the source of the driving transistor, and a fourth switch configured to short circuit the first capacitor. The driving method includes: (a) dividing one-frame period into an initializing period, a threshold detection period, a writing period, and a luminescence period, (b) applying, in the initializing period, a differential voltage between the reference voltage and the initializing voltage to the second capacitor by setting the second switch OFF, and setting the first, third and fourth switches ON, (c) reducing, in the threshold detection period, the voltage of the second capacitor by closing a current path formed of the second capacitor and the driving transistor, where the current path is closed by setting second and third switches OFF and first and fourth switches ON, (d) applying, in the writing period, a differential voltage between the reference voltage and the image signal voltage to the first capacitor by setting the third and fourth switches OFF and first and second switches ON, and (e) applying, in the luminescence period, a current to the driving transistor and the current light emitting device corresponding to the image signal voltage, by setting first, second, third and fourth switches OFF.

[0011] US 2005/057182 describes an active matrix type display apparatus including a self-luminescent element which is connected to a first voltage power source line and which emits light in accordance with a supplied electric current, a driving transistor which is connected between a second voltage power source line and the self-luminescent element and which controls an electric current amount supplied to the self-luminescent element in accordance with a gate control voltage, a first switch formed of a transistor and connected between a gate and a drain of the driving transistor, a first capacitance connected to the gate, a second switch formed of a transistor and connected between the drain of the driving transistor and the self-luminescent element, and a second capacitance connected between the second switch and the gate of the driving transistor.

BRIEF SUMMARY OF THE INVENTION

[0012] Various aspects of the present invention provide an organic light-emitting display device having a pixel structure able to significantly improve threshold voltage compensation capability and range by compensating for a loss in a threshold voltage that would occur during operation.

[0013] Also provided is an organic light-emitting display device having a pixel structure able to compensate for mobility and control a mobility compensation time based on a capacitor design within the pixel structure, thereby achieving a sufficient data writing time.

[0014] Also provided is an organic light-emitting display device having a pixel structure that has superior global uniformity characteristics.

[0015] In an aspect of the present invention, provided is an organic light-emitting display device according to claim 1.

[0016] In one or more embodiments, each of the pixels further comprises: a third transistor controlled by a third scanning signal, the third transistor being connected between the first node of the driving transistor and the hold node.

[0017] In one or more embodiments, a capacitance of the second storage capacitor is smaller than a capacitance of the first storage capacitor or a capacitance of the boost capacitor.

[0018] In one or more embodiments, a driving voltage supplied through the driving voltage line is an alternating current voltage, and each of the number of pixels performs an initialization operation, a threshold voltage sensing operation, a data writing and mobility compensation operation and an emission operation.

[0019] In one or more embodiments, at the initialization operation, a low level driving voltage is applied to the third node of the driving transistor, the first and third transistors are turned on, and the second transistor is turned off, such that the hold node and the first node of the driving transistor are initialized by a source voltage, and the second node of the driving transistor is initialized by the low level driving voltage.

[0020] In one or more embodiments, at the threshold voltage sensing operation, a high level driving voltage is applied to the third node of the driving transistor, the first transistor is maintained in a turned-on state, the second transistor is turned off, and the third transistor is maintained in a turned-off state, such that the first node of the driving transistor is maintained at the source voltage, a voltage at the second node of the driving transistor increases, and a voltage at the hold node increases according to a voltage change at the second node of the driving voltage and a first capacitance ratio.

[0021] In one or more embodiments, the voltage at the hold node increases to a voltage obtained by multiplying the voltage change at the second node of the driving voltage with the first capacitance ratio, and the first capacitance ratio is a value obtained by dividing the capacitance of the second storage capacitor with a total of the capacitance of the boost capacitor and the capacitance of the second storage capacitor.

[0022] In one or more embodiments, at the data writing and mobility sensing operation, a data voltage is applied to the second transistor through the corresponding data line, a high level driving voltage is applied to the third node of the driving transistor, the first transistor is turned off, and the second transistor is turned on, such that a voltage at the hold node increases, a voltage at the second node of the driving transistor increases according to the mobility sensing operation, and a voltage at the first node of the driving transistor increases according to a voltage change at the hold node, a voltage change at the second node of the driving transistor, a second capacitance ratio and a third capacitance ratio.

[0023] In one or more embodiments, the voltage at the first node of the driving transistor increases by a total of a voltage obtained by multiplying the voltage change at the hold node with the second capacitance ratio and a voltage obtained by multiplying the voltage change at the second node of the driving transistor with the third capacitance ratio.

[0024] In one or more embodiments, the second capacitance ratio is a value obtained by dividing the capacitance of the boost capacitor with a total of the capacitance of the first storage capacitor and the capacitance of the boost capacitor, and the third capacitance ratio is a value obtained by dividing the capacitance of the first storage capacitor with the total of the capacitance of the first storage capacitor and the capacitance of the boost capacitor.

[0025] In one or more embodiments, the third capacitance ratio determines a rate at which a voltage difference between the first node and the second node of the driving transistor decreases.

[0026] In one or more embodiments, at the emission operation, the driving transistor, the first transistor, the second transistor and the third transistor are turned off, and the organic light-emitting diode emits light while the voltage at the second node of the driving transistor increases.

[0027] In one or more embodiments, the capacitance of the second storage capacitor determines an amount to control at compensation for a loss in threshold voltage information caused by a parasitic capacitor of the first node of the driving transistor.

[0028] In one or more embodiments, a driving voltage supplied through the driving voltage line is a direct current voltage, and each of the number of pixels performs an initialization operation, a threshold voltage sensing operation, a data writing and mobility compensation operation and an emission operation, each of the number of pixels further comprising a fourth transistor connected between the second node of the driving transistor and an initialization voltage line, the fourth transistor being controlled by the third scanning signal by which the third transistor is controlled.

[0029] In one or more embodiments, at the initialization operation, the driving voltage is applied to the third node of the driving transistor, and the first transistor, the third transistor and the fourth transistor are turned on, and the second transistor is turned off, such that the hold node and the first node of the driving transistor are initialized by a source voltage, and the second node of the driving transistor is initialized by an initialization voltage.

[0030] In one or more embodiments, a driving voltage supplied through the driving voltage line is an alternating current voltage.

[0031] In one or more embodiments, the hold node is initialized by a voltage applied through the corresponding data line, the voltage applied through the data line comprises a low level initialization data voltage and a high level data voltage alternating with the low level initialization data voltage, and the second transistor repeats turning on and off by a horizontal time.

[0032] In one or more embodiments, each of the pixels further comprises a third transistor connected between the second node of the driving transistor and an initialization voltage line, the third transistor being controlled by the second scanning signal by which the second transistor is controlled, a driving voltage supplied through the driving voltage line being a direct current voltage.

[0033] In another aspect of the present invention, provided is an organic light-emitting display device according to claim 10.

[0034] In another aspect of the present invention, provided is an organic light-emitting display device according to claim 12.

[0035] In another aspect of the present invention, provided is an organic light-emitting display device according to claim 13.

[0036] Preferred embodiments are described in the dependent claims.

[0037] According to the present invention as set forth above, the organic light-emitting display device has the pixel structure able to significantly improve threshold voltage compensation capability and range by compensating for a loss in a threshold voltage that would occur during operation.

[0038] In addition, the organic light-emitting display device has the pixel structure able to compensate for mobility and control a mobility compensation time based on a capacitor design within the pixel structure, thereby achieving a sufficient data writing time.

[0039] Furthermore, the organic light-emitting display device has the pixel structure having superior global uniformity characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

[0040] The above and other objects, features and advantages of the present invention will be more clearly understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a schematic system configuration view illustrating an organic light-emitting display device according to exemplary embodiments of the present invention;

FIG. 2 is an equivalent circuit diagram illustrating a pixel structure of an organic light-emitting display device according to a comparative example ;

FIG. 3 is an operation timing diagram of a pixel having the pixel structure of the organic light-emitting display device according to the comparative example;

FIG. 4 is a circuit diagram illustrating a parasitic capacitor component of the pixel structure of the organic light-emitting display device according to the comparative example;

FIG. 5 is an equivalent circuit diagram illustrating a pixel structure of an organic light-emitting display device according to a first exemplary embodiment of the present invention;

FIG. 6 is an operation timing diagram of a pixel having the pixel structure of the organic light-emitting display device according to the first exemplary embodiment;

FIG. 7A, FIG. 7B, FIG. 8A, FIG. 8B, FIG. 9, FIG. 10A, FIG. 10B, FIG. 11, FIG. 12A and FIG. 12B are circuit diagrams illustrating the operation according to process steps and graphs illustrating voltage changes at major nodes in the pixel structure of the organic light-emitting display device according to the first exemplary embodiment;

FIG. 13A, FIG. 13B, FIG. 14A, FIG. 14B, FIG. 15A, FIG. 15B and FIG. 16 are graphs illustrating a variety of simulations on the pixel structure of the organic light-emitting display device according to the first exemplary embodiment;

FIG. 17 is an equivalent circuit diagram illustrating a pixel structure of an organic light-emitting display device according to a second exemplary embodiment of the present invention;

FIG. 18 is an operation timing diagram of a pixel having the pixel structure of the organic light-emitting display device according to the second exemplary embodiment;

FIG. 19 is an equivalent circuit diagram illustrating a pixel structure of an organic light-emitting display device according to a third exemplary embodiment of the present invention;

FIG. 20 and FIG. 21 are an operation timing diagram and a voltage change graph at major nodes in the pixel structure of the organic light-emitting display device according to the third exemplary embodiment;

FIG. 22 is an equivalent circuit diagram illustrating a pixel structure of an organic light-emitting display device according to a fourth exemplary embodiment of the present invention; and

FIG. 23 is an operation diagram of a pixel having the pixel structure of the organic light-emitting display device according to the fourth exemplary embodiment.

DETAILED DESCRIPTION OF THE INVENTION

[0041] Reference will now be made in detail to the present invention, embodiments of which are illustrated in the accompanying drawings. Throughout this document, reference should be made to the drawings, in which the same reference numerals and signs may be used throughout the different drawings to designate the same or similar components. In the following description of the present invention, detailed descriptions of known functions and components incorporated herein will be omitted in the case that the subject matter of the present invention may be rendered unclear thereby.

[0042] It will also be understood that, although terms such as "first," "second," "A," "B," "(a)" and "(b)" may be used herein to describe various elements, such terms are only used to distinguish one element from another element. The

substance, sequence, order or number of these elements is not limited by these terms. It will be understood that when an element is referred to as being "connected to" or "coupled to" another element, not only can it be "directly connected" or "coupled to" the other element, but also can it be "indirectly connected or coupled to" the other element via an "intervening" element. In the same context, it will be understood that when an element is referred to as being formed "on" or "under" another element, not only can it be directly formed on or under another element, but also can it be indirectly formed on or under another element via an intervening element.

[0043] FIG. 1 is a schematic system configuration view illustrating an organic light-emitting display device 100 according to exemplary embodiments of the present invention.

[0044] Referring to FIG. 1, the organic light-emitting display device 100 includes a display panel 110 on which a plurality of data lines DL1 to DLm and a plurality of gate lines GL1 to GLn are disposed such that a number of pixels P are defined, a data driver 120 for driving the data lines LD1 to DLm, a gate driver 130 for driving the gate lines GL1 to GLn, and a timing controller 140 for controlling the data driver 120 and the gate driver 130.

[0045] The data driver 120 may include a plurality of data driver integrated circuits (also referred to as source driver integrated circuits) that may be connected to the bonding pads of the display panel 110 by a tape automated bonding (TAB) method or a chip-on-glass (COG) method, may be directly formed on the display panel 110 by a gate-in-panel (GIP) method, or may be integrated on the display panel 110.

[0046] The gate driver 130 may be positioned only at one side of the display panel 110 as illustrated in FIG. 1 or may be divided into two sections each of which is positioned on either side of the display panel 110.

[0047] The gate driver 130 can provide each of the pixels with one or more scanning signals according to several pixel structures, which will be described later.

[0048] In addition, the gate driver 130 may include a plurality of gate driver integrated circuits that may be connected to the bonding pads of the display panel by a tape automated bonding (TAB) method or a chip-on-glass (COG) method, may be directly formed on the display panel 110 by a gate-in-panel (GIP) method, or may integrated on the display panel 110.

[0049] The timing controller 140 controls the operation timing of the data driver 120 and the gate driver 130, and outputs a variety of control signals for this purpose.

[0050] Each of the pixels of the organic light-emitting display device 100 includes an organic light-emitting diode (OLED) and a circuit for driving the OLED.

[0051] The circuit for driving the OLED includes a driving transistor for supplying a current to the OLED, a switching transistor for applying a data voltage to a gate node of the driving transistor, and a storage capacitor for maintaining a data voltage for the period of one frame. The circuit can further include at least one transistor for compensating for the threshold voltage Vth and the mobility of the driving transistor.

[0052] The pixel structures may vary according to the numbers and the connecting structures of the transistors and the capacitors included in the circuit.

[0053] Reference will be made to five pixel structures according to a comparative example and four exemplary embodiments of the present invention.

[0054] First, a pixel structure including four transistors and one capacitor according to a comparative example will be described with reference to FIG. 2 to FIG. 4.

[0055] FIG. 2 is an equivalent circuit diagram illustrating the pixel structure of an organic light-emitting display device 100 according to the comparative example.

[0056] Referring to FIG. 2, each pixel of the organic light-emitting display device 100 according to the comparative example has a pixel structure including an organic light-emitting diode (OLED), a first transistor T1 connected between a driving voltage line DVL through which a driving voltage EVDD is supplied and the OLED, a second transistor T2 connected between a data line DL and a gate node DTG of the first transistor T1, a third transistor T3 connected between a source node DTS of the first transistor T1 and an initialization voltage line IVL through which an initialization voltage Vini is supplied, a fourth transistor T4 connected between a reference voltage line through which a reference voltage Vref is supplied and the gate node DTG of the first transistor T1, and a storage capacitor Cstg connected between the gate node DTG and the source node DTS of the first transistor T1.

[0057] The first transistor T1 is a driving transistor for driving the OLED.

[0058] Although the four transistors T1 to T4 are illustrated as being an N type, this is merely an illustrative example, and the four transistors may be designed to be a P type.

[0059] A description will be given of an operation method of each pixel having this pixel structure with reference to an operation timing diagram illustrated in FIG. 3.

[0060] FIG. 3 is the operation timing diagram of a pixel having the pixel structure of the organic light-emitting display device according to the comparative example.

[0061] Referring to FIG. 3, the pixel having the pixel structure of the organic light-emitting display device 100 according to the comparative example carries out an operation, including an initialization step, a threshold voltage sensing step, a data writing and mobility compensation step and an emission step.

[0062] Referring to FIG. 3, at the initialization step, the second transistor T2 is turned off, and the fourth transistor T4 and the third transistor T3 are turned on, such that the gate node DTG and the source node DTS of the first transistor T1 are respectively initialized with a reference voltage Vref and an initialization voltage Vini.

[0063] Referring to FIG. 3, at the threshold voltage sensing step, the third transistor T3 is turned off, and the source node DTS of the first transistor T1 senses a threshold voltage of the first transistor T1. That is, the voltage Vs at the source node DTS of the first transistor T1 can be expressed including the threshold voltage (Vs = Vref-Vth).

[0064] At this time, information about the threshold voltage Vth of the first transistor T1 is stored in the storage capacitor Cstg. That is, the difference in the voltage between both ends of the storage capacitor Cstg is identical to the threshold voltage Vth of the first transistor T1.

[0065] Referring to FIG. 3, at the data writing and mobility compensation step, the third transistor T3 and the fourth transistor T4 are turned off, and the second transistor T2 is turned on, such that a data voltage Vdata is applied to (or written in) the gate node DTG of the first transistor T1.

[0066] At this time, the first transistor T1 is turned on, and the voltage at the source node DTS of the first transistor T1 increases.

[0067] The increase in the voltage at the source node DTS of the first transistor T1 is proportional to the mobility of the first transistor T1.

[0068] For example, assuming that the mobility of the first transistor T1 is $\mu 1$ or $\mu 2$, where $\mu 1 > \mu 2$, a voltage change ΔDTS1 at the source node DTS when the mobility of the first transistor T1 is μl is greater than a voltage change ΔDTS2 at the source node DTS when the mobility of the first transistor T1 is $\mu 2$. Accordingly, the voltage difference Vgs1 between the gate node DTG and the source node DTS when the mobility of the first transistor T1 is $\mu 1$ is smaller than the voltage difference Vgs2 between the gate node DTG and the source node DTS at the mobility of the first transistor T1 is $\mu 2$.

[0069] Based on the degree in a voltage increase (or voltage change) at the source node DTS of the first transistor T1, the mobility of the first transistor T1 can be sensed, and variations in the mobility can be compensated by negative feedback.

[0070] Referring to FIG. 3, at the emission step, all of the transistors T2 to T4 except for the first transistor T1 serving as the driving transistor are turned off. The OLED starts emitting light while the voltage at the source node DTS of the first transistor T1 increases such that the current of the first transistor T1 is identical to that of the OLED.

[0071] At this time, information about the threshold voltage that has been present at the source node DTS of the first transistor T1 is transferred to the gate node DTG of the first transistor T1, thereby compensating for the threshold voltage of the first transistor T1.

[0072] Specifically, the voltage at the source node DTS of the first transistor T1 is expressed without the threshold voltage, and the voltage of the gate node DTG of the first transistor T1 is expressed including the threshold voltage. The first transistor T1 can drive the OLED free from the influence of the threshold voltage.

[0073] The pixel structure of the organic light-emitting display device 100 according to the first embodiment makes possible the threshold voltage sensing, the mobility compensation and the like that have been problematic in the related art.

[0074] As described above, in the pixel structure of the organic light-emitting display device 100 according to the comparative example, at the threshold voltage sensing step, the threshold voltage Vth of the first transistor T1 serving as the driving transistor is stored in the source node DTS of the first transistor T1. The threshold voltage Vth stored in the source node DTS of the first transistor T1 in this fashion is transferred to the gate node DTG of the first transistor T1 serving as the driving transistor at the emission step.

[0075] Here, storing the threshold voltage in the source node DTS of the first transistor T1 indicates that the voltage at the source node DTS of the first transistor T1 can be expressed by the threshold voltage. In addition, the transfer of the threshold voltage Vth stored in the source node DTS of the first transistor T1 to the gate node DTG of the first transistor T1 indicates that the threshold voltage included in a voltage formula of the source node DTS of the first transistor T1 is included in a voltage formula of the gate node DTG of the first transistor T1.

[0076] In the process of storing and transferring the threshold voltage, as illustrated in FIG. 4, a parasitic capacitor Cpara formed at the gate node DTG of the first transistor T1 serving as the driving transistor may cause a loss in the threshold voltage.

[0077] In particular, the loss in the threshold voltage caused by the parasitic capacitor Cpara formed at the gate node DTG of the first transistor T1 may create a relatively-large gate source voltage at a low grayscale that is controlled based on a small gate source voltage of the driving transistor T1, thereby leading to a severe non-uniform image quality at the threshold voltage.

[0078] In addition, the compensation range for the threshold voltage may be significantly reduced, thereby lowering the yield of transistors.

[0079] Furthermore, it is difficult to obtain a sufficient data writing time due to a short mobility compensation time.

[0080] Therefore, reference will now be made to exemplary embodiments (first to fourth embodiments) of the pixel structure that can significantly improve threshold voltage compensation capability and range by compensating for a loss

in a threshold voltage that would occur during operation, can compensate for mobility and control a mobility compensation time based on a capacitor design within the pixel structure, thereby achieving a sufficient data writing time, and has superior global uniformity characteristics.

[0081] First, a description will be given of a 4T3C pixel structure including four transistors (T) and three capacitors (C) according to a first exemplary embodiment with reference to FIG. 5 to FIG. 16.

[0082] FIG. 5 is an equivalent circuit diagram illustrating the pixel structure of the organic light-emitting display device 100 according to the first exemplary embodiment of the present invention.

[0083] Referring to FIG. 5, each of pixels defined on the display plane 110 of the organic light-emitting display device 100 according to the first embodiment includes: an organic light-emitting diode (OLED); four transistors including a driving transistor DT, a first transistor T1, a second transistor T2 and a third transistor T3; and three capacitors including a first storage capacitor Cstg1, a second storage capacitors Cstg2 and a boost capacitor Cboost.

[0084] The driving transistor DT drives the OLED, and includes a first node N1 forming a gate node, a second node N2 connected to the OLED and a third node N3 connected to a driving voltage line DVL through which a driving voltage EVDD is supplied.

[0085] The first transistor T1 is controlled by a first scanning signal SCAN1, and is connected between a source voltage line SVL and the first node N1 of the driving transistor DT.

[0086] The first storage capacitor Cstg1 is connected between the first node N1 and the second node N2 of the driving transistor DT.

[0087] The second storage capacitor Cstg2 and the boost capacitor Cboost are connected between the first node N1 and the second node N2 of the driving transistor DT.

[0088] The second transistor T2 is controlled by a second scanning signal SCAN2, and is connected between a hold node Nh to which the second storage capacitor Cstg2 and the booster capacitor Cboost are connected and a data line DL.

[0089] The third transistor T3 is controlled by a third scanning signal SCAN3, and is connected between the first node N1 of the driving transistor DT and the hold node Nh.

[0090] In the pixel structure of the organic light-emitting display device 100 according to the first embodiment, a driving voltage VDD applied to the third node N3 of the driving transistor DT through the driving voltage line DVL is an AC voltage, which is shifted by 1 H.

[0091] Here, the driving voltage VDD at a low level can be indicated by VDD(-), and the driving voltage VDD at a high level can be indicated by VDD(+).

[0092] In the pixel structure of the organic light-emitting display device 100 according to the first embodiment, the three capacitors have their own capacitances. Comparing the capacitances of the first storage capacitor Cstg1, the boost capacitor Cboost and the second storage capacitor Cstg2, the capacitance of the second storage capacitor Cstg2 is designed smallest. The capacitances of the first storage capacitor Cstg1 and the boost capacitor Cboost are designed similar to each other.

[0093] A description will be given below of the operation of the pixel having the above-described 4T3C pixel structure.

[0094] FIG. 6 is an operation timing diagram of a pixel having the pixel structure of the organic light-emitting display device 100 according to the first exemplary embodiment.

[0095] Referring to FIG. 6, the pixel having the pixel structure of the organic light-emitting display device 100 according to the first embodiment carries out an operation, including an initialization step, a threshold voltage sensing step, a data writing and mobility compensation step and an emission step.

[0096] A description will be given below of the respective steps of the operation with reference to FIG. 7A, FIG. 7B, FIG. 8A, FIG. 8B, FIG. 9, FIG. 10A, FIG. 10B, FIG. 11, FIG. 12A and FIG. 12B.

[0097] First, referring to FIG. 7A and FIG. 7B, at the initialization step, a low level driving voltage VDD(-) is applied to the third node N3 of the driving transistor DT, the first transistor T1 and the third transistor T3 are turned on by a first scanning signal SCAN1 and a third scanning signal SCAN3 that are high level scanning signals, and the second transistor T2 is turned off by a second scanning signal SCAN2 that is a low level scanning signal.

[0098] Accordingly, the hold node Nh and the first node N1 of the driving transistor DT are initialized using a source voltage Vss, and the second node N2 of the driving transistor DT is initialized using the low level driving voltage VDD(-).

[0099] At this initialization step, voltages at the first node N1 of the driving transistor DT, the second node N2 of the driving transistor DT and the hold node Nh can be expressed as in following Formula 1:

$$\text{Voltage of } N1 = \text{VSS}$$

$$\text{Voltage of } N2 = \text{VDD(-)}$$

$$\text{Voltage of } Nh = \text{VSS} \qquad \ldots\ldots \text{ Formula 1}$$

[0100] In Formula 1, VSS indicates a source voltage, and VDD(-) indicates a low level driving voltage.

[0101] Afterwards, referring to FIG. 8A and FIG. 8B, at the threshold voltage sensing step, a high level driving voltage VDD(+) is applied to the third node N3 of the driving transistor DT, the first transistor T1 is maintained at the turned-on state by a high level first scanning signal SCAN1, the second transistor T2 is turned off by a low level second voltage signal SCAN2, and the third transistor T3 is turned off by a low level third scanning signal SCAN3.

[0102] At this threshold voltage sensing step, changes in voltages at the first node N1 of the driving transistor DT, the second node N2 of the driving transistor DT and the hold node Nh will be discussed with reference to FIG. 9.

[0103] Referring to FIG. 9, at the threshold voltage sensing step, the first node N1 of the driving transistor DT is maintained at the source voltage VSS.

[0104] In addition, at the threshold voltage sensing step, the voltage at the second node N2 of the driving transistor DT increases from the initialized voltage VDD(-). The voltage increases from VDD(-) to VSS-Vth, which is less than the source voltage Vss, i.e. the voltage at the first node N1 of the driving transistor DT, subtracted by the threshold voltage Vth.

[0105] Therefore, at the threshold voltage sensing step, a voltage change at the second node N2 of the driving transistor DT is VSS-Vth-VDD(-).

[0106] In addition, at the threshold voltage sensing step, the voltage at the hold node Nh increases according to the voltage change VSS-Vth-VDD(-) at the second node N2 of the driving transistor DT and a first capacitance ratio A.

[0107] More specifically, the voltage at the hold node Nh increases by a value obtained by multiplying the voltage change VSS-Vth-VDD(-) at the second node N2 of the driving transistor DT with the first capacitance ratio A. Here, the first capacitance ratio A is a value obtained by dividing the capacitance of the second storage capacitor Cstg2 with a total of the capacitance of the boost capacitor Cboost and the capacitance of the second storage capacitor Cstg2.

[0108] At the threshold voltage sensing step, the voltages at the first node N1 of the driving transistor DT, the second node N2 of the driving transistor DT and the hold node Nh can be expressed by following Formula 2 and Formula 3:

$$\text{Voltage of } N1 = \text{VSS}$$

$$\text{Voltage of } N2 = \text{VSS-Vth}$$

$$\text{Voltage of } Nh = \text{VSS+A*(VSS-Vth-VDD(-))},$$

$$\text{where A} = \text{Cstg2}/(Cboost+Cstg2) \quad \ldots\ldots \text{ Formula 2}$$

If VSS = 0,

$$\text{Voltage of } N1 = 0$$

$$\text{Voltage of } N2 = \text{-Vth}$$

$$\text{Voltage of } Nh = \text{-A*(VDD(-)+Vth)} \quad \ldots\ldots \text{ Formula 3}$$

[0109] In Formula 2 and Formula 3, VSS indicates a source voltage, Vth indicates a threshold voltage of the driving transistor DT, VDD(-) indicates a low level driving voltage, A indicates a first capacitance ratio, *Cstg2* indicates a capacitance of the second storage capacitor Cstg2, and *Cboost* indicates a capacitance of the boost capacitor Cboost.

[0110] Afterwards, referring to FIG. 10A and FIG. 10B, at the data writing and mobility sensing step, the second transistor T2 is turned on by a high level second scanning signal SCAN2, a data voltage Vdata is applied through the data line DL to turn on second transistor T2, a high level driving voltage VDD(+) is applied to the third node N3 of the driving transistor DT, and the first transistor T1 is turned off by a low level first scanning signal SCAN1.

[0111] At the data writing and mobility sensing step, the second transistor T2 is turned on, by which the data voltage Vdata supplied through the data line DL is applied to the hold node Nh.

[0112] Consequently, the voltage at the hold node Nh increases to the data voltage Vdata.

[0113] A voltage change at the hold node Nh is expressed by Vdata-[VSS+A*(VSS-Vth-VDD(-))].

[0114] In response to the mobility sensing, the voltage at the second node N2 of the driving transistor DT increases further from the voltage VSS-Vth that has increased at the threshold voltage sensing step.

[0115] A voltage change ΔVu at the second node N2 of the driving transistor DT due to this voltage increase may vary according to a voltage change ΔVp at the hold node Nh.

[0116] In response to a coupled data being applied to the first node N1 of the driving transistor DT and, simultaneously, the mobility sensing, the voltage at the first node N1 of the driving transistor DT increases from the source voltage VSS that has been maintained through the threshold voltage sensing step.

[0117] The voltage at the first node N1 of the driving transistor DT can increase according to the voltage change ΔVp at the hold node Nh, the voltage change ΔVu at the second node N2 of the driving transistor DT in response to the

mobility sensing operation, a second capacitance ratio B and a third capacitance ratio C.

[0118] More specifically, the voltage at the first node N1 of the driving transistor DT increases further by a voltage value B*ΔVp+C*ΔVu, i.e. a total of a voltage obtained by multiplying the voltage change ΔVp at the hold node Nh with the second capacitance ratio B and a voltage obtained by multiplying the voltage change ΔVu at the second node N2 of the driving transistor DT in response to the mobility sensing operation with the third capacitance ratio C.

[0119] Here, the second capacitance ratio B is a value obtained by dividing the capacitance of the boost capacitor Cboost with a total of the capacitance of the first storage capacitor Cstg1 and the capacitance of the boost capacitor Cboost.

[0120] The third capacitance ratio C is a value obtained by dividing the capacitance of the first storage capacitor Cstg1 with a total of the capacitance of the boost capacitor Cboost and the capacitance of the first storage capacitor Cstg1.

[0121] This third capacitance ratio C can determine the rate at which the difference in the voltage between the first node N1 and the second node N2 of the driving transistor DT decreases.

[0122] At the data writing and mobility sensing step, voltages at the first node N1 of the driving transistor DT, the second node N2 of the driving transistor DT and the hold node Nh can be expressed by following Formula 4 and Formula 5 (VSS = 0):

$$\text{Voltage of } N1 = \text{VSS}+B*\Delta Vp+C*\Delta Vu$$

$$\text{Voltage of } N2 = \text{VSS}-\text{Vth}+\Delta Vu$$

$$\text{Voltage of } Nh = \text{Vdata}-\text{VSS}+A*(\text{VSS}-\text{Vth}-\text{VDD}(-))+\Delta Vp$$

$$\text{where } B = \text{Cboost}/(\text{Cstg1}+\text{Cboost})$$

$$C = \text{Cstg1}/(\text{Cboost}+\text{Cstg1}) \quad \ldots\ldots \text{ Formula 4}$$

$$\text{If VSS} = 0,$$

$$\text{Voltage of } N1 = B*\Delta Vp+C*\Delta Vu$$

$$\text{Voltage of } N2 = -\text{Vth}+\Delta Vu$$

$$\text{Voltage of } Nh = \text{Vdata} = -A*(\text{VDD}(-)+\text{Vth})+\Delta Vp \quad \ldots\ldots \text{ Formula 5}$$

[0123] In Formula 4 and Formula 5, VSS indicates a source voltage, Vth indicates a threshold voltage of the driving transistor DT, VDD(-) indicates a low level driving voltage, Vdata indicates a data voltage, ΔVp indicates a voltage change at the hold node Nh, ΔVu indicates a voltage change at the second node N2 of the driving transistor DT, B indicates a second capacitance, C indicates a third capacitance, Cstg1 indicates a capacitance of the first storage capacitor Cstg1, and Cboost indicates a capacitance of the boost capacitor.

[0124] In sequence, referring to FIG. 12A and FIG. 12B, at the emission step, all of the first transistor T1, the second transistor T2 and the third transistor T3 are turned off.

[0125] Consequently, the voltage at the second node N2 of the driving transistor DT increases, and the OLED emits light.

[0126] At this time, a threshold voltage of the driving voltage DT is transferred.

[0127] A current Ids flowing between the drain node N3 and the source node N2 of the driving transistor DT can be expressed by following Formula 6:

$$Ids = k(Vgs - Vth)^2, \ \ where\ k = \frac{1}{2}\mu Cox\frac{W}{L} \quad \ldots\ldots \text{ Formula 6}$$

[0128] In Formula 6, Ids indicates a current flowing between the drain node N3 and the source node N1 of the driving transistor DT, Vgs indicates a difference in the voltage between the first node N1 and the second node N2 of the driving transistor DT, and Vth is a threshold voltage of the driving transistor DT. k is a component about the mobility of the driving transistor DT, and is defined by mobility μ, an oxide capacitance Cox, a channel width W and a channel length L.

[0129] When the OLED emits light, the current flowing between the drain node N3 and the source node N2 of the driving transistor DT is identical to a current Ioled flowing through the OLED.

[0130] Therefore, it is possible to determine whether or not the threshold voltage Vth of the driving transistor DT has an effect on a corresponding pixel, i.e. whether or not the threshold voltage Vth of the driving transistor DT has an effect

on the current Ioled flowing through the OLED, by evaluating "Vgs-Vth."

[0131] Based on the voltages at the first node N1 of the driving transistor DT, the second node N2 of the driving transistor DT and the hold node Nh according to the above-described steps, Vgs-Vth can be expressed by following Formula 7:

$$\begin{aligned} \text{Vgs-Vth} &= B*\Delta Vp+C*\Delta Vu-(-Vth+\Delta Vu)-Vth \\ &= B(Data+A(VDD(-)+Vth))+C*\Delta Vu+Vth-\Delta Vu-Vth \\ &= B*Data+B*A*VDD(-)+B*A*Vth-\Delta Vu\ *(1-C), \\ \text{where}\ \ A &= Cstg2/(Cboost+Cstg2) \\ B &= (Cboost/Cstg1+Cboost) \\ C &= Cstg1/(Cboost+Cstg1) \end{aligned} \qquad \ldots\ldots \text{ Formula 7}$$

[0132] In Formula 7, VSS indicates a source voltage, Vth indicates a threshold voltage of the driving transistor DT, VDD(-) indicates a low level driving voltage, Vdata indicates a data voltage, ΔVp indicates a voltage change at the hold node Nh, ΔVu indicates a voltage change at the second node N2 of the driving transistor DT, A indicates a first capacitance ratio, B indicates a second capacitance ratio, C indicates a third capacitance ratio, *Cstg1* indicates a capacitance of the first storage capacitor Cstg1, *Cboost* indicates a capacitance of the boost capacitor Cboost, and *Cstg2* indicates a capacitance of the second storage capacitor Cstg2.

[0133] In Formula 7, "B*A*Vth" is a part that cancels a loss in the threshold voltage. If the capacitances of the three capacitors Cstg1, Cstg2 and Cboost are determined such that B*A is very small, B*A*Vth in Vgs-Vth becomes a negligibly small value. It is possible to make a current flow through the OLED without a significant effect on the threshold voltage Vth of the driving transistor DT.

[0134] Considering this, it is possible to control the part that cancels the loss through the second storage capacitor Cstg2.

[0135] Specifically, the capacitance of the capacitor Cstg2 makes it possible to determine the amount to control at compensation for the loss in the information about the threshold voltage caused by the parasitic capacitor Cpara of the first node N1 of the driving transistor DT.

[0136] In addition, in Formula 7, ΔVu*(1-C) indicates a decrease in the voltage difference Vgs between the first node N1 and the second node N2 of the driving transistor DT at the mobility sensing step.

[0137] Here, the third capacitance ratio C can reduce the rate at which the voltage difference Vgs decreases. Specifically, the third capacitance ratio C determines the reduction rate of the voltage difference Vgs between the first node N1 and the second node N2 of the driving transistor DT.

[0138] FIG. 13A, FIG. 13B, FIG. 14A, FIG. 14B, FIG. 15A, FIG. 15B and FIG. 16 are graphs illustrating a variety of simulations on the pixel structure of the organic light-emitting display device 100 according to the first exemplary embodiment.

[0139] FIG. 13A and FIG. 13B illustrate the results of simulations on the threshold voltage compensation capability of the pixel structure according to the first embodiment, performed by changing the second capacitor Cstg2 in order to compensate for a loss in the threshold voltage caused by the parasitic capacitor Cpara.

[0140] Referring to FIG. 13A and FIG. 13B, the pixel structure has the capacitance value of the second capacitor Cstg2 that has optimum performance at both a low gray level (63 Gray) and a high gray level (255 Gray).

[0141] FIG. 14A and FIG. 14B illustrate the results of simulations on the complex compensation capability of the pixel structure according to the first embodiment when both the threshold voltage Vth and the mobility of the driving transistor DT deviate from a reference.

[0142] Referring to FIG. 14A and FIG. 14B, it is appreciated that there are wide compensation ranges for the threshold voltage Vth and the mobility at either a low gray level (63 Gray) or a high gray level (255 Gray) when Δloled is within 5%.

[0143] FIG. 15A and FIG. 15B illustrate the global uniformity of the pixel structure according to the first embodiment at a low gray level (63 Gray) and a high gray level (255 Gray).

[0144] Referring to FIG. 15A and FIG. 15B, it is appreciated that the pixel structure according to the first embodiment has superior global uniformity at either the low gray level (63 Gray) or the high gray level (255 Gray).

[0145] FIG. 16 illustrates variations in a current (Y axis) flowing through the OLED according to data voltages (X axis) in the pixel structure according to the first embodiment.

[0146] Referring to FIG. 16, steps 1.5, 1.0, 0.5 and 0 pF indicate the capacitances between a first electrode (e.g. an anode) of the OLED and the source voltage VSS.

[0147] Referring to FIG. 16, it is possible to design a capacitor to control current capacity when the current capacity

is insufficient although the OLED operates like a capacitor. Specifically, even in the case that the data voltage is the same, it is possible to increase the amount of current flowing through the OLED by increasing the designed capacitance of the capacitor component of the OLED.

[0148] The 4T3C pixel structure according to the first embodiment and the operation of the pixel having the 4T3C pixel structure were described hereinabove.

[0149] Reference will now be made to a modified embodiment (second embodiment) of the 4T3C pixel structure according to the first embodiment and the operation thereof in conjunction with FIG. 17 and FIG. 18.

[0150] FIG. 17 is an equivalent circuit diagram illustrating a pixel structure of an organic light-emitting display device 100 according to a second exemplary embodiment of the present invention.

[0151] Referring to FIG. 17, each of pixels of the organic light-emitting display device 100 according to the second embodiment has a pixel structure including: an organic light-emitting diode (OLED); five transistors including a driving transistor DT, a first transistor T1, a second transistor T2, a third transistor T3 and a fourth transistor T4; and three capacitors including a first storage capacitor Cstg1, a second storage capacitor Cstg2 and a boost capacitor Cboost.

[0152] The driving transistor DT includes a first node N1 forming a gate node, a second node N2 connected to the OLED and a third node N3 connected to a driving voltage line DVL through which a driving voltage VDD is supplied.

[0153] The first transistor T1 is controlled by a first scanning signal SCAN1, and is connected between a source voltage line SVL and the first node N1 of the driving transistor DT.

[0154] The first storage capacitor Cstg1 is connected between the first node N1 and the second node N2 of the driving transistor DT.

[0155] The second storage capacitor Cstg2 and the boost capacitor Cboost are connected between the first node N1 and the second node N2 of the driving transistor DT.

[0156] The second transistor T2 is controlled by a second scanning signal SCAN2, and is connected between a hold node Nh and a data line DL.

[0157] The third transistor T3 is controlled by a third scanning signal SCAN3, and is connected between the first node N1 of the driving transistor DT and the hold node Nh.

[0158] The fourth transistor T4 is connected between the second node N2 of the driving transistor DT and an initialization voltage line IVL through which an initialization voltage Vini is supplied.

[0159] The fourth transistor T4 is commonly controlled by the third scanning signal SCAN3 by which the third transistor T3 is controlled.

[0160] The 5T3C pixel structure according to the second embodiment illustrated in FIG. 17 is substantially identical to the 4T3C pixel structure according to the first embodiment illustrated in FIG. 5, except that the driving voltage VDD supplied through a driving voltage line DVL is a DC voltage, and that the fourth transistor T4 is added.

[0161] Accordingly, the second node N2 of the driving transistor DT is initialized by an initialization voltage IVL supplied through the initialization voltage line IVL in the pixel structure according to the second embodiment illustrated in FIG. 17, whereas the second node N2 of the driving transistor DT is initialized by VDD(-) in the 4T3C pixel structure according to the first embodiment illustrated in FIG. 5.

[0162] As described above, the operation system and operating characteristics of the 5T3C pixel structure according to the second embodiment illustrated in FIG. 17 are substantially identical to those of the 4T3C pixel structure according to the first embodiment illustrated in FIG. 5, except for the initialization of the second node N2 of the driving transistor DT.

[0163] Therefore, the operation timing of a pixel having the 5T3C pixel structure according to the second embodiment illustrated in FIG. 17 is identical to the operation timing of a pixel having the 4T3C pixel structure according to the first embodiment illustrated in FIG. 5.

[0164] The operation timing of the pixel having the 5T3C pixel structure according to the second embodiment illustrated in FIG. 17 will be described in brief with reference to FIG. 18.

[0165] Referring to FIG. 18, the pixel having the 5T3C pixel structure according to the second embodiment also carries out an operation, including an initialization step, a threshold voltage sensing step, a data writing and mobility compensation step and an emission step, as in the first embodiment.

[0166] Comparing the operation timing of a pixel having the 5T3C pixel structure according to the second embodiment illustrated in FIG. 17 with the operation timing of a pixel having the 4T3C pixel structure according to the first embodiment illustrated in FIG. 5, the operation system and operating characteristics thereof are identical except that the driving voltage VDD is a DC voltage in the 5T3C pixel structure.

[0167] Since the DC driving voltage VDD is supplied, the fourth transistor T4 is added to initialize the second node N2 of the driving transistor DT.

[0168] Therefore, at the initialization step, the DC driving voltage VDD is applied to the third node N3 of the driving transistor DT, the first transistor T1 is turned on by a high level first scanning signal SCAN1, the third transistor T3 and the fourth transistor T4 are turned on by a high level third scanning signal, and the second transistor T2 is turned on by a low level second scanning signal SCAN2.

[0169] Consequently, the hold node Nh and the first node N1 of the driving transistor DT are initialized by a source

voltage VSS supplied through the first transistor T1, and the second node N2 of the driving transistor DT is initialized by the initialization voltage Vini supplied through the fourth transistor T4.

[0170] Descriptions of the threshold voltage sensing step, the data writing and mobility compensation step and the emission step will be omitted since they are identical to those of the operation of the 4T3C pixel structure according to the first embodiment.

[0171] The 4T3C pixel structure according to the first embodiment and the 5T3C pixel structure including one more transistor (the fourth transistor T4) according to the second embodiment were described hereinabove.

[0172] Reference will now be made to a 3T3C pixel structure according to a third embodiment corresponding to a modified embodiment of the 4T3C pixel structure according to the first embodiment in conjunction with FIG. 19 to FIG. 21.

[0173] FIG. 19 is an equivalent circuit diagram illustrating the pixel structure of an organic light-emitting display device 100 according to the third exemplary embodiment of the present invention.

[0174] The organic light-emitting display device 100 according to the third embodiment includes a display panel 110 on which a plurality of data lines DL1 to DLm and a plurality of gate lines GL1 to GLn are disposed such that a number of pixels P are defined, a data driver 120 for driving the data lines LD1 to DLm, a gate driver 130 for driving the gate lines GL1 to GLn, and a timing controller 140 for controlling the data driver 120 and the gate driver 130.

[0175] Referring to FIG. 19, each of a plurality of pixels of the organic light-emitting display device 100 according to the third embodiment has a 3T3C pixel structure including an organic light-emitting diode (OLED), a driving transistor DT, a first transistor T1, a second transistor T2, a first storage capacitor Cstg1, a second storage capacitor Cstg2 and a boost capacitor Cboost.

[0176] Here, the driving transistor DT serves to drive the OLED, and includes a first node N1 forming a gate node, a second node N2 connected to the OLED and a third node N3 connected to a driving voltage line DVL.

[0177] The first transistor T1 is controlled by a first scanning signal SCAN1, and is connected between a source voltage line SVL and the first node N1 of the driving transistor DT.

[0178] The first storage capacitor Cstg1 is connected between the first node N1 and the second node N2 of the driving transistor DT.

[0179] The second storage capacitor Cstg2 and the boost capacitor Cboost are connected between the first node N1 and the second node N2 of the driving transistor DT. The connecting node between the second storage capacitor and the boost capacitor forms a hold node Nh.

[0180] The second transistor T2 is controlled by a second scanning signal SCAN2, and is connected between the hold node Nh to which the second storage capacitor Cstg2 and the boost capacitor Cboost are connected and a data line DL.

[0181] Referring to FIG. 19, in each of the plurality of pixels of the organic light-emitting display device 100 according to the third embodiment, an AC driving voltage VDD is supplied to the third node N3 of the driving transistor DT through the driving voltage line DVL.

[0182] The operation of a pixel having the 3T3C pixel structure according to the third embodiment illustrated in FIG. 19 will be described with reference to FIG. 20 and FIG. 21.

[0183] FIG. 20 and FIG. 21 are an operation timing diagram and a voltage change graph at major nodes in the pixel structure of the organic light-emitting display device 100 according to the third exemplary embodiment.

[0184] Referring to FIG. 20, the operation of a pixel having the 3T3C pixel structure according to the third embodiment is identical to the operation of a pixel having the 4T3C pixel structure according to the first embodiment.

[0185] In addition, referring to FIG. 20, the operation of the pixel having the 3T3C pixel structure according to the third embodiment includes an initialization step, a threshold voltage sensing step, a data writing and mobility compensation step and an emission step, like the operation of the pixel having the 4T3C pixel structure according to the first embodiment.

[0186] The operation of the pixel having the 3T3C pixel structure according to the third embodiment differs from the operation of the pixel having the 4T3C pixel structure according to the first embodiment in that the hold node Nh is initialized by a data voltage supplied through the data line DL, since the transistor (T3 in FIG. 5) for initializing the hold node Nh is not provided.

[0187] Therefore, input data voltages are divided into a low level initialization data voltage Vo and a high level data voltage Vdata, and the hold node Nh is initialized by the initialization data voltage Vo.

[0188] In the pixel having the 3T3C pixel structure according to the third embodiment, the hold node Nh is initialized by a voltage applied through the data line DL. The voltage applied through the data line DL is a voltage in which the low level initialization data voltage Vo and the high level data voltage Vdata alternate with each other.

[0189] Accordingly, the transistor (T3 in FIG. 5) connected between the hold node Nh and the first node N1 of the driving transistor DT, as well as a scanning signal for controlling the transistor (T3 in FIG. 5), can be precluded.

[0190] In addition, referring to the operation timing of the initialization step in FIG. 20, since the hold node Nh is initialized by the low level initialization data voltage Vo, an initialization time may be insufficient when performing the initialization through the data line DL.

[0191] Therefore, it is possible to supplement the insufficient time by turning on the second scanning signal SCAN2

in a multiple fashion by a horizontal time (HT). Consequently, the second transistor T2 repeats turning on and off by the horizontal time (HT).

[0192] In this manner, at the initialization step, the hold node Nh is initialized to be in the shape of teeth by the low level initialization data voltage Vo, as illustrated in FIG. 21, according to the type of the data voltage Vdata+Vo and the type of the second scanning signal SCAN2.

[0193] Except for this initialization step, the other operation (at the threshold voltage sensing step, the data writing and mobility compensation step and the emission step) and the timing thereof are identical to those of the pixel having the 4T3C pixel structure according to the first embodiment.

[0194] Accordingly, voltage changes at the first node N1, the second node N2 and the hold node Nh in the pixel having the 3T3C pixel structure according to the third embodiment illustrated in FIG. 21 are identical to voltage changes at the first node N1, the second node N2 and the hold node Nh in the pixel having the 4T3C pixel structure according to the first embodiment illustrated in FIG. 11, except for a voltage change at the hold node at the initialization step.

[0195] Descriptions of the other operation of the pixel having the 3T3C pixel structure according to the third embodiment at the threshold voltage sensing step, the data writing and mobility compensation step and the emission step and voltage changes at the nodes N1, N2 and Nh at these steps will be omitted since they are identical to those of the pixel having the 4T3C pixel structure according to the first embodiment.

[0196] Reference will now be made to a 4T3C pixel structure according to a fourth embodiment corresponding to a modified embodiment of the third embodiment and the operation of a pixel having the 3T3C pixel structure in conjunction with FIG. 22 and 23.

[0197] FIG. 22 is an equivalent circuit diagram illustrating the pixel structure of an organic light-emitting display device 100 according to the fourth exemplary embodiment of the present invention.

[0198] Referring to FIG. 22, the pixel structure of each of a plurality of pixels of the organic light-emitting display device 100 according to the fourth embodiment is substantially identical to the 3T3C pixel structure according to the third embodiment illustrated in FIG. 19, except that a DC driving voltage VDD is applied to a third node N3 of a driving transistor DT and, for this, a third transistor T3 connected between a second node N2 of a driving transistor DT and an initialization voltage line IVL is added.

[0199] Specifically, the driving transistor DT drives an organic light-emitting diode (OLED), and includes a first node N1 forming a gate node, a second node N2 connected to the OLED and the third node N3 connected to the driving voltage line DVL. The first transistor T1 is controlled by a first scanning signal SCAN1, and is connected between a source voltage line SVL and the first node N1 of the driving transistor DT. The first storage capacitor Cstg1 is connected between the first node N1 and the second node N2 of the driving transistor DT. The second storage capacitor Cstg2 and the boost capacitor Cboost are connected between the first node N1 and the second node N2 of the driving transistor DT. The connecting node between the second storage capacitor and the boost capacitor forms a hold node Nh. The second transistor T2 is controlled by a second scanning signal SCAN2, and is connected between the hold node Nh to which the second storage capacitor Cstg2 and the boost capacitor Cboost are connected and a data line DL.

[0200] The pixel structure of each of the plurality of pixels of the organic light-emitting display device 100 according to the fourth embodiment illustrated in FIG. 22 forms a 4T3C pixel structure, since this pixel structure has one more transistor (i.e. the third transistor T3) than the 3T3C pixel structure according to the third embodiment illustrated in FIG. 19.

[0201] The third transistor T3 added to the 4T3C pixel structure according to the fourth embodiment is commonly controlled by the second scanning signal SCAN2 by which the second transistor T2 is controlled.

[0202] With reference to FIG. 23, a description will be given below of the operation of a pixel having the 4T3C pixel structure according to the fourth embodiment illustrated in FIG. 22.

[0203] Referring to FIG. 23, the operation timing of the pixel having the 4T3C pixel structure according to the fourth embodiment is substantially identical to the operation timing of the pixel having the 3T3C pixel structure according to the third embodiment illustrated in FIG. 20, except that a DC driving voltage VDD is supplied and, consequently, an initialization voltage Vini is applied to the second node N2 of the driving transistor DT through the third transistor T3 connected to the second node N2 of the driving transistor DT.

[0204] According to the present invention as set forth above, the organic light-emitting display device has the pixel structure able to significantly improve threshold voltage compensation capability and range by compensating for a loss in a threshold voltage that would occur during operation.

[0205] That is, the use of the pixel structure according to the certain embodiments of the present invention makes it possible to store a relative threshold voltage in addition to an absolute threshold voltage, thereby compensating for a loss in the threshold voltage.

[0206] The organic light-emitting display device has the pixel structure able to compensate for mobility and control a mobility compensation time based on a capacitor design within the pixel structure, thereby achieving a sufficient data writing time.

[0207] That is, the use of the pixel structure according to the certain embodiments of the invention makes it possible to control a mobility sensing time to a desirable time using an internal capacitor, thereby achieving a sufficient data

writing time.

[0208] The organic light-emitting display device has the pixel structure having superior global uniformity characteristics.

[0209] The foregoing descriptions and the accompanying drawings have been presented in order to explain the certain principles of the present invention. A person skilled in the art to which the invention relates can make many modifications and variations by combining, dividing, substituting for or changing elements without departing from the principle of the invention. The foregoing embodiments disclosed herein shall be interpreted as illustrative only not as limitative of the principle and scope of the invention. It should be understood that the scope of the invention shall be defined by the appended Claims and all of their equivalents fall within the scope of the invention

Claims

1. An organic light-emitting display device (100) comprising:

a display panel (110) on which data lines (DL1 to DLm) and gate lines (GL1 to GLn) are arranged to define a number of pixels (P);
a data driver (120) driving the data lines (DL1 to DLm);
a gate driver (130) driving the gate lines (GL1 to GLn); and
a timing controller (140) controlling the data driver (120) and the gate driver (130),
wherein each of the pixels (P) comprises:

an organic light-emitting diode (OLED);
a driving transistor (DT) driving the organic light-emitting diode (OLED), wherein the driving transistor (DT) includes a first node (N1) forming a gate node, a second node (N2) connected to the organic light-emitting diode (OLED) and a third node (N3) connected to a driving voltage line (DVL);
a first transistor (T1) controlled by a first scanning signal (SCAN1), the first transistor (T1) being connected between a source voltage line (SVL) and the first node (N1) of the driving transistor (DT);
a first storage capacitor (Cstg1) connected between the first node (N1) and the second node (N2) of the driving transistor (DT);
a second storage capacitor (Cstg2) and a boost capacitor (Cboost) between the first node (N1) and the second node (N2) of the driving transistor (DT);
a second transistor (T2) controlled by a second scanning signal (SCAN2), the second transistor (T2) being connected between a hold node (Nh) to which the second storage capacitor (Cstg2) and the boost capacitor (Cboost) are connected and a corresponding data line DL of the data lines (DL1 to DLm); and
a third transistor (T3) controlled by a third scanning signal (SCAN3), the third transistor (T3) being connected between the first node (N1) of the driving transistor (DT) and the hold node (Nh),

wherein a driving voltage (VDD) supplied through the driving voltage line (DVL) is an alternating current (AC) voltage, and each of the number of pixels (P) performs an initialization operation, a threshold voltage sensing operation, a data writing and mobility compensation operation and an emission operation,
wherein, at the initialization operation, a low level driving voltage (VDD(-)) is applied to the third node (N3) of the driving transistor (DT), the first (T1) and third (T3) transistors are turned on, and the second transistor (T2) is turned off, such that the hold node (Nh) and the first node (N1) of the driving transistor (DT) are initialized by a source voltage (Vss), and the second node (N2) of the driving transistor (DT) is initialized by the low level driving voltage (VDD(-)),
characterised in that,
at the threshold voltage sensing operation, a high level driving voltage (VDD(+)) is applied to the third node (N3) of the driving transistor (DT), the first transistor (T1) is maintained in a turned-on state, the second transistor (T2) is maintained in a turned-off state, and the third transistor (T3) is turned off, such that the first node (N1) of the driving transistor (DT) is maintained at the source voltage (VSS), a voltage at the second node (N2) of the driving transistor (DT) increases from the low level driving voltage (VDD(-)) to a voltage equal to the source voltage (Vss) subtracted by a threshold voltage (Vth) of the driving transistor (DT), and a voltage at the hold node (Nh) increases according to a voltage change at the second node (N2) of the driving transistor (DT) and a first capacitance ratio (A).

2. The organic light-emitting display device (100) according to claim 1, wherein
the voltage at the hold node (Nh) increases to a voltage obtained by multiplying the voltage change at the second node (N2) of the driving transistor (DT) with the first capacitance ratio (A), and

the first capacitance ratio (A) is a value obtained by dividing the capacitance of the second storage capacitor (Cstg2) with a total of the capacitance of the boost capacitor (Cboost) and the capacitance of the second storage capacitor (Cstg2).

3. The organic light-emitting display device (100) according to claim 1 or 2, wherein a capacitance of the second storage capacitor (Cstg2) is smaller than a capacitance of the first storage capacitor (Cstg1) or a capacitance of the boost capacitor (Cboost).

4. The organic light-emitting display device (100) according to claim 1 or 2, wherein, at the data writing and mobility sensing operation, a data voltage (Vdata) is applied to the second transistor (T2) through the corresponding data line (DL), a high level driving voltage (VDD(+)) is applied to the third node (N3) of the driving transistor (DT), the first transistor (T1) is turned off, and the second transistor (T2) is turned on, such that a voltage at the hold node (Nh) increases, a voltage at the second node (N2) of the driving transistor (DT) increases according to the mobility sensing operation, and a voltage at the first node (N1) of the driving transistor (DT) increases according to a voltage change at the hold node (Nh), a voltage change at the second node (N2) of the driving transistor (DT), a second capacitance ratio (B) and a third capacitance ratio (C).

5. The organic light-emitting display device (100) according to claim 3, wherein the voltage at the first node (N1) of the driving transistor (DT) increases by a total of a voltage obtained by multiplying the voltage change at the hold node (Nh) with the second capacitance ratio (B) and a voltage obtained by multiplying the voltage change at the second node (N2) of the driving transistor (DT) with the third capacitance ratio (C).

6. The organic light-emitting display device (100) according to claim 5, wherein
the second capacitance ratio (B) is a value obtained by dividing the capacitance of the boost capacitor (Cboost) with a total of the capacitance of the first storage capacitor (Cstg1) and the capacitance of the boost capacitor (Cboost), and
the third capacitance ratio (C) is a value obtained by dividing the capacitance of the first storage capacitor (Cstg1) with the total of the capacitance of the first storage capacitor (Cstg1) and the capacitance of the boost capacitor (Cboost).

7. The organic light-emitting display device (100) according to any one of claims 4 to 6, wherein the third capacitance ratio (C) determines a rate at which a voltage difference between the first node (N1) and the second node (N2) of the driving transistor (DT) decreases.

8. The organic light-emitting display device (100) according to any one of claims 4 to 7, wherein, at the emission operation, the driving transistor (DT), the first transistor (T1), the second transistor (T2) and the third transistor (T3) are turned off, and the organic light-emitting diode (OLED) emits light while the voltage at the second node (N2) of the driving transistor (DT) increases.

9. The organic light-emitting display device (100) according to claim 8, wherein the capacitance of the second storage capacitor (Cstg2) determines an amount to control at compensation for a loss in threshold voltage information caused by a parasitic capacitor (Cpara) of the first node (N1) of the driving transistor (DT).

10. An organic light-emitting display device (100) comprising:

a display panel (110) on which data lines (DL1 to DLm) and gate lines (GL1 to GLn) are arranged to define a number of pixels (P);
a data driver (120) driving the data lines (DL1 to DLm);
a gate driver (130) driving the gate lines (GL1 to GLn); and
a timing controller (140) controlling the data driver (120) and the gate driver (130),
wherein each of the pixels (P) comprises:

an organic light-emitting diode (OLED);
a driving transistor (DT) driving the organic light-emitting diode (OLED), wherein the driving transistor (DT) includes a first node (N1) forming a gate node, a second node (N2) connected to the organic light-emitting diode (OLED) and a third node (N3) connected to a driving voltage line (DVL);
a first transistor (T1) controlled by a first scanning signal (SCAN1), the first transistor (T1) being connected between a source voltage line (SVL) and the first node (N1) of the driving transistor (DT);

a first storage capacitor (Cstg1) connected between the first node (N1) and the second node (N2) of the driving transistor (DT);
a second storage capacitor (Cstg2) and a boost capacitor (Cboost) between the first node (N1) and the second node (N2) of the driving transistor (DT);
a second transistor (T2) controlled by a second scanning signal (SCAN2), the second transistor (T2) being connected between a hold node (Nh) to which the second storage capacitor (Cstg2) and the boost capacitor (Cboost) are connected and a corresponding data line DL of the data lines (DL1 to DLm); and
a third transistor (T3) controlled by a third scanning signal (SCAN3), the third transistor (T3) being connected between the first node (N1) of the driving transistor (DT) and the hold node (Nh),

characterised in that,
a driving voltage (VDD) supplied through the driving voltage line (DVL) is a direct current (DC) voltage, and each of the number of pixels (P) performs an initialization operation, a threshold voltage sensing operation, a data writing and mobility compensation operation and an emission operation,
each of the number of pixels (P) further comprising a fourth transistor (T4) connected between the second node (N2) of the driving transistor (DT) and an initialization voltage line (IVL), the fourth transistor (T4) being controlled by the third scanning signal (SCAN3) by which the third transistor (T3) is controlled.

11. The organic light-emitting display device (100) according to claim 10, wherein, at the initialization operation, the driving voltage (VDD) is applied to the third node (N3) of the driving transistor (DT), and the first transistor (T1), the third transistor (T3) and the fourth transistor (T4) are turned on, and the second transistor (T2) is turned off, such that the hold node (Nh) and the first node (N1) of the driving transistor (DT) are initialized by a source voltage (VSS), and the second node (N2) of the driving transistor (DT) is initialized by an initialization voltage (Vini).

12. An organic light-emitting display device (100) comprising:

a display panel (110) on which data lines (DL1 to DLm) and gate lines (GL1 to GLn) are arranged to define a number of pixels (P);
a data driver (120) driving the data lines (DL1 to DLm);
a gate driver (130) driving the gate lines (GL1 to GLn); and
a timing controller (140) controlling the data driver (120) and the gate driver (130),
wherein each of the pixels (P) comprises:

an organic light-emitting diode (OLED);
a driving transistor (DT) driving the organic light-emitting diode (OLED), wherein the driving transistor (DT) includes a first node (N1) forming a gate node, a second node (N2) connected to the organic light-emitting diode (OLED) and a third node (N3) connected to a driving voltage line (DVL);
a first transistor (T1) controlled by a first scanning signal (SCAN1), the first transistor (T1) being connected between a source voltage line (SVL) and the first node (N1) of the driving transistor (DT);
a first storage capacitor (Cstg1) connected between the first node (N1) and the second node (N2) of the driving transistor (DT);
a second storage capacitor (Cstg2) and a boost capacitor (Cboost) between the first node (N1) and the second node (N2) of the driving transistor (DT); and
a second transistor (T2) controlled by a second scanning signal (SCAN2), the second transistor (T2) being connected between a hold node (Nh) to which the second storage capacitor (Cstg2) and the boost capacitor (Cboost) are connected and a corresponding data line DL of the data lines (DL1 to DLm),

characterised in that,
a driving voltage (VDD) supplied through the driving voltage line (DVL) is an alternating current (AC) voltage, wherein the hold node (Nh) is initialized by a voltage applied through the corresponding data line (DL), the voltage applied through the data line (DL) comprises a low level initialization data voltage (Vo) and a high level data voltage (Vdata) alternating with the low level initialization data voltage (Vo), and the second transistor (T2) repeats turning on and off by a horizontal time (HT).

13. An organic light-emitting display device (100) comprising:

a display panel (110) on which data lines (DL1 to DLm) and gate lines (GL1 to GLn) are arranged to define a number of pixels (P);

a data driver (120) driving the data lines (DL1 to DLm);
a gate driver (130) driving the gate lines (GL1 to GLn); and
a timing controller (140) controlling the data driver (120) and the gate driver (130),
wherein each of the pixels (P) comprises:

an organic light-emitting diode (OLED);
a driving transistor (DT) driving the organic light-emitting diode (OLED), wherein the driving transistor (DT) includes a first node (N1) forming a gate node, a second node (N2) connected to the organic light-emitting diode (OLED) and a third node (N3) connected to a driving voltage line (DVL);
a first transistor (T1) controlled by a first scanning signal (SCAN1), the first transistor (T1) being connected between a source voltage line (SVL) and the first node (N1) of the driving transistor (DT);
a first storage capacitor (Cstg1) connected between the first node (N1) and the second node (N2) of the driving transistor (DT);
a second storage capacitor (Cstg2) and a boost capacitor (Cboost) between the first node (N1) and the second node (N2) of the driving transistor (DT); and
a second transistor (T2) controlled by a second scanning signal (SCAN2), the second transistor (T2) being connected between a hold node (Nh) to which the second storage capacitor (Cstg2) and the boost capacitor (Cboost) are connected and a corresponding data line DL of the data lines (DL1 to DLm),

characterised in that,
each of the pixels (P) further comprises a third transistor (T3) connected between the second node (N2) of the driving transistor (DT) and an initialization voltage line (IVL), the third transistor (T3) being controlled by the second scanning signal (SCAN2) by which the second transistor (T2) is controlled, a driving voltage (VDD) supplied through the driving voltage line (DVL) being a direct current (DC) voltage.

Patentansprüche

1. Eine organische lichtemittierende Anzeigevorrichtung (100), aufweisend:

ein Anzeigepanel (110), auf dem Datenleitungen (DL1 bis DLm) und Gate-Leitungen (GL1 bis GLn) zum Definieren einer Anzahl von Pixeln (P) angeordnet sind;
einen Daten-Treiber (120), der die Datenleitungen (DL1 bis DLm) ansteuert;
einen Gate-Treiber (130), der die Gate-Leitungen (GL1 bis GLn) ansteuert; und
eine Zeitablaufsteuerung (140), die den Daten-Treiber (120) und den Gate-Treiber (130) steuert,
wobei jedes der Pixel (P) aufweist:

eine organische lichtemittierende Diode (OLED);
einen Ansteuerungstransistor (DT), der die organische lichtemittierende Diode (OLED) ansteuert, wobei der Ansteuerungstransistor (DT) einen ersten Knoten (N1), der einen Gate-Knoten bildet, einen zweiten Knoten (N2), der mit der organischen lichtemittierenden Diode (OLED) verbunden ist, und einen dritten Knoten (N3), der mit einer Ansteuerungsspannungs-Leitung (DVL) verbunden ist, aufweist;
einen ersten Transistor (T1), der mittels eines ersten Abtastsignals (SCAN1) gesteuert wird, wobei der erste Transistor (T1) zwischen eine Sourcespannungsleitung (SVL) und den ersten Knoten (N1) des Ansteuerungstransistors (DT) geschaltet ist;
einen ersten Speicherkondensator (Cstg1), der zwischen den ersten Knoten (N1) und den zweiten Knoten (N2) des Ansteuerungstransistors (DT) geschaltet ist;
einen zweiten Speicherkondensator (Cstg2) und einen Boost-Kondensator (Cboost) zwischen dem ersten Knoten (N1) und dem zweiten Knoten (N2) des Ansteuerungstransistors (DT);
einen zweiten Transistor (T2), der mittels eines zweiten Abtastsignals (SCAN2) gesteuert wird, wobei der zweite Transistor (T2) zwischen einen Halte-Knoten (Nh), mit dem der zweite Speicherkondensator (Cstg2) und der Boost-Kondensator (Cboost) verbunden sind, und eine entsprechende Datenleitung (DL) der Datenleitungen (DL1 bis DLm) geschaltet ist; und
einen dritten Transistor (T3), der mittels eines dritten Abtastsignals (SCAN3) gesteuert wird, wobei der dritte Transistor (T3) zwischen den ersten Knoten (N1) des Ansteuerungstransistors (DT) und den Halte-Knoten (Nh) geschaltet ist,
wobei eine Ansteuerungsspannung (VDD), die durch die Ansteuerungsspannungsleitung (DVL) zugeführt wird, eine Wechselstrom (AC)-Spannung ist und jedes der Anzahl von Pixeln (P) einen Initialisierungs-

Vorgang, einen Schwellenspannung-Messvorgang, einen Daten-Schreibe-und-Beweglichkeitskompensations-Vorgang und einen Emissions-Vorgang durchführt,
wobei bei dem Initialisierungs-Vorgang eine Ansteuerungsspannung mit niedrigem Pegel (VDD(-)) an den dritten Knoten (N3) des Ansteuerungstransistors (DT) angelegt wird, der erste (T1) und der dritte (T3) Transistor angeschaltet werden und der zweite Transistor (T2) ausgeschaltet wird, derart, dass der Halte-Knoten (Nh) und der erste Knoten (N1) des Ansteuerungstransistors (DT) mittels einer Source-Spannung (Vss) initialisiert werden und der zweite Knoten (N2) des Ansteuerungstransistors (DT) mittels der Ansteuerungsspannung mit niedrigem Pegel (VDD(-)) initialisiert wird,

dadurch gekennzeichnet, dass
bei dem Schwellenspannung-Messvorgang eine Ansteuerungsspannung mit hohem Pegel (VDD(+)) an den dritten Knoten (N3) des Ansteuerungstransistors (DT) angelegt wird, der erste Transistor (T1) in einem eingeschalteten Zustand beibehalten wird, der zweite Transistor (D2) in einem ausgeschalteten Zustand beibehalten wird und der dritte Transistor (T3) ausgeschaltet wird, derart, dass der erste Knoten (N1) des Ansteuerungstransistors (DT) bei der Source-Spannung (VSS) beibehalten wird, eine Spannung an dem zweiten Knoten (N2) des Ansteuerungstransistors (DT) von der Ansteuerungsspannung mit niedrigem Pegel (VDD(-)) bis zu einer Spannung, die gleich der Source-Spannung (Vss), von der eine Schwellenspannung (Vth) des Ansteuerungstransistors (DT) abgezogen ist, zunimmt, und eine Spannung an dem Halte-Knoten (Nh) entsprechend einer Spannungsänderung an dem zweiten Knoten (N2) des Ansteuerungstransistors (DT) und einem ersten Kapazitätsverhältnis (A) zunimmt.

2. Die organische lichtemittierende Anzeigevorrichtung (100) gemäß Anspruch 1, wobei
die Spannung an dem Halte-Knoten (Nh) auf eine Spannung ansteigt, die mittels Multiplizierens der Spannungsänderung an dem zweiten Knoten (N2) des Ansteuerungstransistors (DT) mit dem ersten Kapazitätsverhältnis (A) erhalten wird, und
das erste Kapazitätsverhältnis (A) ein Wert ist, der mittels Teilens der Kapazität des zweiten Speicherkondensators (Cstg2) durch einen Gesamtwert aus der Kapazität des Boost-Kondensators (Cboost) und der Kapazität des zweiten Speicherkondensators (Cstg2) erhalten wird.

3. Die organische lichtemittierende Anzeigevorrichtung (100) gemäß Anspruch 1 oder 2, wobei eine Kapazität des zweiten Speicherkondensators (Cstg2) kleiner ist als eine Kapazität des ersten Speicherkondensators (Cstg1) oder eine Kapazität des Boost-Kondensators (Cboost).

4. Die organische lichtemittierende Anzeigevorrichtung (100) gemäß Anspruch 1 oder 2, wobei bei dem Daten-Schreibe-und-Beweglichkeits-Messvorgang eine Datenspannung (Vdata) an den zweiten Transistor (T2) durch die entsprechende Datenleitung (DL) hindurch angelegt wird, eine Ansteuerungsspannung mit hohem Pegel (VDD(+)) an den dritten Knoten (N3) des Ansteuerungstransistors (DT) angelegt wird, der erste Transistor (T1) ausgeschaltet wird und der zweite Transistor (T2) eingeschaltet wird, derart, dass eine Spannung an dem Halte-Knoten (Nh) zunimmt, eine Spannung an dem zweiten Knoten (N2) des Ansteuerungstransistors (DT) entsprechend dem Beweglichkeits-Messvorgang zunimmt und eine Spannung an dem ersten Knoten (N1) des Ansteuerungstransistors (DT) entsprechend einer Spannungsänderung an dem Halte-Knoten (Nh), einer Spannungsänderung an dem zweiten Knoten (N2) des Ansteuerungstransistors (DT), einem zweiten Kapazitätsverhältnis (B) und einem dritten Kapazitätsverhältnis (C) zunimmt.

5. Die organische lichtemittierende Anzeigevorrichtung (100) gemäß Anspruch 3, wobei die Spannung an dem ersten Knoten (N1) des Ansteuerungstransistors (DT) um einen Gesamtwert aus einer Spannung, die mittels Multiplizierens der Spannungsänderung an dem Halte-Knoten (Nh) mit dem zweiten Kapazitätsverhältnis (B) erhalten wird, und einer Spannung, die mittels Multiplizierens der Spannungsänderung an dem zweiten Knoten (N2) des Ansteuerungstransistors (DT) mit dem dritten Kapazitätsverhältnis (C) erhalten wird, zunimmt.

6. Die organische lichtemittierende Anzeigevorrichtung (100) gemäß Anspruch 5, wobei
das zweite Kapazitätsverhältnis (B) ein Wert ist, der mittels Teilens der Kapazität des Boost-Kondensators (Cboost) durch einen Gesamtwert aus der Kapazität des ersten Speicherkondensators (Cstg1) und der Kapazität des Boost-Kondensators (Cboost) erhalten wird, und
das dritte Kapazitätsverhältnis (C) ein Wert ist, der mittels Teilens der Kapazität des ersten Speicherkondensators (Cstg1) durch den Gesamtwert aus der Kapazität des ersten Speicherkondensators (Cstg1) und der Kapazität des Boost-Kondensators (Cboost) erhalten wird.

7. Die organische lichtemittierende Anzeigevorrichtung (100) gemäß einem der Ansprüche 4 bis 6, wobei das dritte Kapazitätsverhältnis (C) eine Rate bestimmt, mit der eine Spannungsdifferenz zwischen dem ersten Knoten (N1) und dem zweiten Knoten (N2) des Ansteuerungstransistors (DT) abnimmt.

8. Die organische lichtemittierende Anzeigevorrichtung (100) gemäß einem der Ansprüche 4 bis 7, wobei bei dem Emissions-Vorgang der Ansteuerungstransistor (DT), der erste Transistor (T1), der zweite Transistor (T2) und der dritte Transistor (T3) ausgeschaltet werden und die organische lichtemittierende Diode (OLED) Licht emittiert, während die Spannung an dem zweiten Knoten (N2) des Ansteuerungstransistors (DT) ansteigt.

9. Die organische lichtemittierende Anzeigevorrichtung (100) gemäß Anspruch 8, wobei die Kapazität des zweiten Speicherkondensators (Cstg2) eine Menge zum Steuern bei Kompensation eines Verlustes an Schwellenspannungs-Information, die mittels eines parasitären Kondensators (Cpara) des ersten Knotens (N1) des Ansteuerungstransistors (DT) hervorgerufen wird, bestimmt.

10. Eine organische lichtemittierende Anzeigevorrichtung (100), aufweisend:

ein Anzeigepanel (110), auf dem Datenleitungen (DL1 bis DLm) und Gate-Leitungen (GL1 bis GLn) zum Definieren einer Anzahl von Pixeln (P) angeordnet sind;
einen Daten-Treiber (120), der die Datenleitungen (DL1 bis DLm) ansteuert;
einen Gate-Treiber (130), der die Gate-Leitungen (GL1 bis GLn) ansteuert; und
eine Zeitablaufsteuerung (140), die den Daten-Treiber (120) und den Gate-Treiber (130) steuert,
wobei jedes der Pixel (P) aufweist:

eine organische lichtemittierende Diode (OLED);
einen Ansteuerungstransistor (DT), der die organische lichtemittierende Diode (OLED) ansteuert, wobei der Ansteuerungstransistor (DT) einen ersten Knoten (N1), der einen Gate-Knoten bildet, einen zweiten Knoten (N2), der mit der organischen lichtemittierenden Diode (OLED) verbunden ist, und einen dritten Knoten (N3), der mit einer Ansteuerungsspannungs-Leitung (DVL) verbunden ist, aufweist;
einen ersten Transistor (T1), der mittels eines ersten Abtastsignals (SCAN1) gesteuert wird, wobei der erste Transistor (T1) zwischen eine Sourcespannungsleitung (SVL) und den ersten Knoten (N1) des Ansteuerungstransistors (DT) geschaltet ist;
einen ersten Speicherkondensator (Cstg1), der zwischen den ersten Knoten (N1) und den zweiten Knoten (N2) des Ansteuerungstransistors (DT) geschaltet ist;
einen zweiten Speicherkondensator (Cstg2) und einen Boost-Kondensator (Cboost) zwischen dem ersten Knoten (N1) und dem zweiten Knoten (N2) des Ansteuerungstransistors (DT);
einen zweiten Transistor (T2), der mittels eines zweiten Abtastsignals (SCAN2) gesteuert wird, wobei der zweite Transistor (T2) zwischen einen Halte-Knoten (Nh), mit dem der zweite Speicherkondensator (Cstg2) und der Boost-Kondensator (Cboost) verbunden sind, und eine entsprechende Datenleitung (DL) der Datenleitungen (DL1 bis DLm) geschaltet ist; und
einen dritten Transistor (T3), der mittels eines dritten Abtastsignals (SCAN3) gesteuert wird, wobei der dritte Transistor (T3) zwischen den ersten Knoten (N1) des Ansteuerungstransistors (DT) und den Halte-Knoten (Nh) geschaltet ist,
dadurch gekennzeichnet, dass
eine Ansteuerungsspannung (VDD), die durch die Ansteuerungsspannungsleitung (DVL) zugeführt wird, eine Gleichstrom (DC)-Spannung ist und jedes der Anzahl von Pixeln (P) einen Initialisierungs-Vorgang, einen Schwellenspannung-Messvorgang, einen Daten-Schreibe-und-Beweglichkeitskompensations-Vorgang und einen Emissions-Vorgang durchführt,
jedes der Anzahl von Pixeln (P) ferner einen vierten Transistor (T4) aufweist, der zwischen den zweiten Knoten (N2) des Ansteuerungstransistors (DT) und eine Initialisierungsspannungs-Leitung (IVL) geschaltet ist, wobei der vierte Transistor (T4) mittels des dritten AbtastSignals (SCAN3), mittels dessen der dritte Transistor (T3) gesteuert wird, gesteuert wird.

11. Die organische lichtemittierende Anzeigevorrichtung (100) gemäß Anspruch 10, wobei bei dem Initialisierungs-Vorgang die Ansteuerungsspannung (VDD) an den dritten Knoten (N3) des Ansteuerungstransistors (DT) angelegt wird und der erste Transistor (T1), der dritte Transistor (T3) und der vierte Transistor (T4) eingeschaltet werden und der zweite Transistor (T2) ausgeschaltet wird, derart, dass der Halte-Knoten (Nh) und der erste Knoten (N1) des Ansteuerungstransistors (DT) mittels einer Source-Spannung (VSS) initialisiert werden und der zweite Knoten (N2) des Ansteuerungstransistors (DT) mittels einer Initialisierungsspannung (Vini) initialisiert wird.

12. Eine organische lichtemittierende Anzeigevorrichtung (100), aufweisend:

ein Anzeigepanel (110), auf dem Datenleitungen (DL1 bis DLm) und Gate-Leitungen (GL1 bis GLn) zum Definieren einer Anzahl von Pixeln (P) angeordnet sind;
einen Daten-Treiber (120), der die Datenleitungen (DL1 bis DLm) ansteuert;
einen Gate-Treiber (130), der die Gate-Leitungen (GL1 bis GLn) ansteuert; und
eine Zeitablaufsteuerung (140), die den Daten-Treiber (120) und den Gate-Treiber (130) steuert,
wobei jedes der Pixel (P) aufweist:

eine organische lichtemittierende Diode (OLED);
einen Ansteuerungstransistor (DT), der die organische lichtemittierende Diode (OLED) ansteuert, wobei der Ansteuerungstransistor (DT) einen ersten Knoten (N1), der einen Gate-Knoten bildet, einen zweiten Knoten (N2), der mit der organischen lichtemittierenden Diode (OLED) verbunden ist, und einen dritten Knoten (N3), der mit einer Ansteuerungsspannungs-Leitung (DVL) verbunden ist, aufweist;
einen ersten Transistor (T1), der mittels eines ersten Abtastsignals (SCAN1) gesteuert wird, wobei der erste Transistor (T1) zwischen eine Sourcespannungsleitung (SVL) und den ersten Knoten (N1) des Ansteuerungstransistors (DT) geschaltet ist;
einen ersten Speicherkondensator (Cstg1), der zwischen den ersten Knoten (N1) und den zweiten Knoten (N2) des Ansteuerungstransistors (DT) geschaltet ist;
einen zweiten Speicherkondensator (Cstg2) und einen Boost-Kondensator (Cboost) zwischen dem ersten Knoten (N1) und dem zweiten Knoten (N2) des Ansteuerungstransistors (DT); und
einen zweiten Transistor (T2), der mittels eines zweiten Abtastsignals (SCAN2) gesteuert wird, wobei der zweite Transistor (T2) zwischen einen Halte-Knoten (Nh), mit dem der zweite Speicherkondensator (Cstg2) und der Boost-Kondensator (Cboost) verbunden sind, und eine entsprechende Datenleitung (DL) der Datenleitungen (DL1 bis DLm) geschaltet ist,
dadurch gekennzeichnet, dass
eine Ansteuerungsspannung (VDD), die durch die Ansteuerungsspannungsleitung (DVL) zugeführt wird, eine Wechselstrom (AC)-Spannung ist, wobei der Halte-Knoten (Nh) mittels einer durch die entsprechende Datenleitung (DL) hindurch angelegte Spannung initialisiert wird, wobei die durch die Datenleitung (DL) hindurch angelegte Spannung eine Initialisierungs-Datenspannung mit niedrigem Pegel (Vo) und eine Datenspannung mit hohem Pegel (Vdata), die mit der Initialisierungs-Datenspannung mit niedrigem Pegel (Vo) abwechselt, aufweist und der zweite Transistor (T2) Ein- und Ausschalten mittels einer horizontalen Zeitspanne (HT) wiederholt.

13. Eine organische lichtemittierende Anzeigevorrichtung (100), aufweisend:

ein Anzeigepanel (110), auf dem Datenleitungen (DL1 bis DLm) und Gate-Leitungen (GL1 bis GLn) zum Definieren einer Anzahl von Pixeln (P) angeordnet sind;
einen Daten-Treiber (120), der die Datenleitungen (DL1 bis DLm) ansteuert;
einen Gate-Treiber (130), der die Gate-Leitungen (GL1 bis GLn) ansteuert; und
eine Zeitablaufsteuerung (140), die den Daten-Treiber (120) und den Gate-Treiber (130) steuert,
wobei jedes der Pixel (P) aufweist:

eine organische lichtemittierende Diode (OLED);
einen Ansteuerungstransistor (DT), der die organische lichtemittierende Diode (OLED) ansteuert, wobei der Ansteuerungstransistor (DT) einen ersten Knoten (N1), der einen Gate-Knoten bildet, einen zweiten Knoten (N2), der mit der organischen lichtemittierenden Diode (OLED) verbunden ist, und einen dritten Knoten (N3), der mit einer Ansteuerungsspannungs-Leitung (DVL) verbunden ist, aufweist;
einen ersten Transistor (T1), der mittels eines ersten Abtastsignals (SCAN1) gesteuert wird, wobei der erste Transistor (T1) zwischen eine Sourcespannungsleitung (SVL) und den ersten Knoten (N1) des Ansteuerungstransistors (DT) geschaltet ist;
einen ersten Speicherkondensator (Cstg1), der zwischen den ersten Knoten (N1) und den zweiten Knoten (N2) des Ansteuerungstransistors (DT) geschaltet ist;
einen zweiten Speicherkondensator (Cstg2) und einen Boost-Kondensator (Cboost) zwischen dem ersten Knoten (N1) und dem zweiten Knoten (N2) des Ansteuerungstransistors (DT); und
einen zweiten Transistor (T2), der mittels eines zweiten Abtastsignals (SCAN2) gesteuert wird, wobei der zweite Transistor (T2) zwischen einen Halte-Knoten (Nh), mit dem der zweite Speicherkondensator (Cstg2) und der Boost-Kondensator (Cboost) verbunden sind, und eine entsprechende Datenleitung (DL) der Da-

tenleitungen (DL1 bis DLm) geschaltet ist,
dadurch gekennzeichnet, dass
jedes der Pixel ferner einen dritten Transistor (T3) aufweist, der zwischen den zweiten Knoten (N2) des Ansteuerungstransistors (DT) und eine Initialisierungsspannungs-Leitung (IVL) geschaltet ist, wobei der dritte Transistor (T3) mittels des zweiten AbtastSignals (SCAN2), mittels dessen der zweite Transistor (T2) gesteuert wird, gesteuert wird, wobei eine Ansteuerungsspannung (VDD), die durch die Ansteuerungsspannungs-Leitung (DVL) zugeführt wird, eine Gleichstrom (DC)-Spannung ist.

Revendications

1. Dispositif d'affichage électroluminescent organique (100) comprenant :

un panneau d'affichage (110) sur lequel des lignes de données (DL1 à DLm) et des lignes de grille (GL1 à GLn) sont agencées en vue de définir un nombre de pixels (P) ;
un pilote de données (120) pilotant les lignes de données (DL1 à DLm) ;
un pilote de grille (130) pilotant les lignes de grille (GL1 à GLn) ; et
un contrôleur de temporisation (140) commandant le pilote de données (120) et le pilote de grille (130), dans lequel chacun des pixels (P) comprend :

une diode électroluminescente organique (OLED) ;
un transistor de commande (DT) commandant la diode électroluminescente organique (OLED), dans lequel le transistor de commande (DT) inclut un premier noeud (N1) formant un noeud de grille, un deuxième noeud (N2) connecté à la diode électroluminescente organique (OLED) et un troisième noeud (N3) connecté à une ligne de tension de commande (DVL) ;
un premier transistor (T1) commandé par un premier signal de balayage (SCAN1), le premier transistor (T1) étant connecté entre une ligne de tension de source (SVL) et le premier noeud (N1) du transistor de commande (DT) ;
un premier condensateur de stockage (Cstg1) connecté entre le premier noeud (N1) et le deuxième noeud (N2) du transistor de commande (DT) ;
un second condensateur de stockage (Cstg2) et un condensateur d'amplification (Cboost) entre le premier noeud (N1) et le deuxième noeud (N2) du transistor de commande (DT) ;
un deuxième transistor (T2) commandé par un deuxième signal de balayage (SCAN2), le deuxième transistor (T2) étant connecté entre un noeud de maintien (Nh) auquel le second condensateur de stockage (Cstg2) et le condensateur d'amplification (Cboost) sont connectés et une ligne de données correspondante (DL) des lignes de données (DL1 à DLm) ; et
un troisième transistor (T3) commandé par un troisième signal de balayage (SCAN3), le troisième transistor (T3) étant connecté entre le premier noeud (N1) du transistor de commande (DT) et le noeud de maintien (Nh) ;

dans lequel une tension de commande (VDD) fournie par le biais de la ligne de tension de commande (DVL) correspond à une tension en courant alternatif (AC), et chacun du nombre de pixels (P) met en oeuvre une opération d'initialisation, une opération de détection de tension de seuil, une opération de compensation de mobilité et d'écriture de données et une opération d'émission,
dans lequel, au cours de l'opération d'initialisation, une tension de commande de niveau faible (VDD(-)) est appliquée au troisième noeud (N3) du transistor de commande (DT), les premier (T1) et troisième (T3) transistors sont activés, et le deuxième transistor (T2) est désactivé, de sorte que le noeud de maintien (Nh) et le premier noeud (N1) du transistor de commande (DT) sont initialisés par une tension de source (Vss), et que le deuxième noeud (N2) du transistor de commande (DT) est initialisé par la tension de commande de niveau faible (VDD(-)) ;
caractérisé en ce que,
au cours de l'opération de détection de tension de seuil, une tension de commande de niveau élevé (VDD(+)) est appliquée au troisième noeud (N3) du transistor de commande (DT), le premier transistor (T1) est maintenu dans un état activé, le deuxième transistor (T2) est maintenu dans un état désactivé, et le troisième transistor (T3) est désactivé, de sorte que le premier noeud (N1) du transistor de commande (DT) est maintenu à la tension de source (VSS), une tension au niveau du deuxième noeud (N2) du transistor de commande (DT) augmente, en passant de la tension de commande de niveau faible (VDD(-)) à une tension égale à la tension de source (Vss) moins une tension de seuil (vth) du transistor de commande (DT), et une tension au niveau du noeud de maintien (Nh) augmente selon une modification de tension au niveau du deuxième noeud (N2) du

transistor de commande (DT) et un premier rapport de capacité (A).

2. Dispositif d'affichage électroluminescent organique (100) selon la revendication 1, dans lequel
la tension au niveau du noeud de maintien (Nh) augmente jusqu'à une tension obtenue en multipliant la modification de tension au niveau du deuxième noeud (N2) du transistor de commande (DT) par le premier rapport de capacité (A) ; et
le premier rapport de capacité (A) correspond à une valeur obtenue en divisant la capacité du second condensateur de stockage (Cstg2) par un total de la capacité du condensateur d'amplification (Cboost) et de la capacité du second condensateur de stockage (Cstg2).

3. Dispositif d'affichage électroluminescent organique (100) selon la revendication 1 ou 2, dans lequel une capacité du second condensateur de stockage (Cstg2) est inférieure à une capacité du premier condensateur de stockage (Cstg1) ou à une capacité du condensateur d'amplification (Cboost).

4. Dispositif d'affichage électroluminescent organique (100) selon la revendication 1 ou 2, dans lequel, au cours de l'opération de détection de mobilité et d'écriture de données, une tension de données (Vdata) est appliquée au deuxième transistor (T2) à travers la ligne de données correspondante (DL), une tension de commande de niveau élevé (VDD(+)) est appliquée au troisième noeud (N3) du transistor de commande (DT), le premier transistor (T1) est désactivé, et le deuxième transistor (T2) est activé, de sorte qu'une tension au niveau du noeud de maintien (Nh) augmente, une tension au niveau du deuxième noeud (N2) du transistor de commande (DT) augmente selon l'opération de détection de mobilité, et une tension au niveau du premier noeud (N1) du transistor de commande (DT) augmente selon une modification de tension au niveau du noeud de maintien (Nh), selon une modification de tension au niveau du deuxième noeud (N2) du transistor de commande (DT), selon un deuxième rapport de capacité (B) et selon un troisième rapport de capacité (C).

5. Dispositif d'affichage électroluminescent organique (100) selon la revendication 3, dans lequel la tension au niveau du premier noeud (N1) du transistor de commande (DT) augmente d'un total d'une tension obtenue en multipliant la modification de tension au niveau du noeud de maintien (Nh) par le deuxième rapport de capacité (B) et d'une tension obtenue en multipliant la modification de tension au niveau du deuxième noeud (N2) du transistor de commande (DT) par le troisième rapport de capacité (C).

6. Dispositif d'affichage électroluminescent organique (100) selon la revendication 5, dans lequel
le deuxième rapport de capacité (B) correspond à une valeur obtenue en divisant la capacité du condensateur d'amplification (Cboost) par un total de la capacité du premier condensateur de stockage (Cstg1) et de la capacité du condensateur d'amplification (Cboost) ; et
le troisième rapport de capacité (C) correspond à une valeur obtenue en divisant la capacité du premier condensateur de stockage (Cstg1) par le total de la capacité du premier condensateur de stockage (Cstg1) et de la capacité du condensateur d'amplification (Cboost).

7. Dispositif d'affichage électroluminescent organique (100) selon l'une quelconque des revendications 4 à 6, dans lequel le troisième rapport de capacité (C) détermine un rapport auquel une différence de tension entre le premier noeud (N1) et le deuxième noeud (N2) du transistor de commande (DT) diminue.

8. Dispositif d'affichage électroluminescent organique (100) selon l'une quelconque des revendications 4 à 7, dans lequel, au cours de l'opération d'émission, le transistor de commande (DT), le premier transistor (T1), le deuxième transistor (T2) et le troisième transistor (T3) sont désactivés, et la diode électroluminescente organique (OLED) émet de la lumière tandis que la tension au niveau du deuxième noeud (N2) du transistor de commande (DT) augmente.

9. Dispositif d'affichage électroluminescent organique (100) selon la revendication 8, dans lequel la capacité du second condensateur de stockage (Cstg2) détermine une quantité à commander lors d'une compensation pour une perte d'informations de tension de seuil occasionnée par un condensateur parasite (Cpara) du premier noeud (N1) du transistor de commande (DT).

10. Dispositif d'affichage électroluminescent organique (100) comprenant :

un panneau d'affichage (110) sur lequel des lignes de données (DL1 à DLm) et des lignes de grille (GL1 à GLn) sont agencées de manière à définir un nombre de pixels (P) ;

un pilote de données (120) pilotant les lignes de données (DL1 à DLm) ;
un pilote de grille (130) pilotant les lignes de grille (GL1 à GLn) ; et
un contrôleur de temporisation (140) commandant le pilote de données (120) et le pilote de grille (130), dans lequel chacun des pixels (P) comporte :

une diode électroluminescente organique (OLED) ;
un transistor de commande (DT) commandant la diode électroluminescente organique (OLED), dans lequel le transistor de commande (DT) inclut un premier noeud (N1) formant un noeud de grille, un deuxième noeud (N2) connecté à la diode électroluminescente organique (OLED) et un troisième noeud (N3) connecté à une ligne de tension de commande (DVL) ;
un premier transistor (T1) commandé par un premier signal de balayage (SCAN1), le premier transistor (T1) étant connecté entre une ligne de tension de source (SVL) et le premier noeud (N1) du transistor de commande (DT) ;
un premier condensateur de stockage (Cstg1) connecté entre le premier noeud (N1) et le deuxième noeud (N2) du transistor de commande (DT) ;
un second condensateur de stockage (Cstg2) et un condensateur d'amplification (Cboost) entre le premier noeud (N1) et le deuxième noeud (N2) du transistor de commande (DT) ;
un deuxième transistor (T2) commandé par un deuxième signal de balayage (SCAN2), le deuxième transistor (T2) étant connecté entre un noeud de maintien (Nh) auquel le second condensateur de stockage (Cstg2) et le condensateur d'amplification (Cboost) sont connectés et une ligne de données correspondante (DL) des lignes de données (DL1 à DLm) ; et
un troisième transistor (T3) commandé par un troisième signal de balayage (SCAN3), le troisième transistor (T3) étant connecté entre le premier noeud (N1) du transistor de commande (DT) et le noeud de maintien (Nh) ;

caractérisé en ce que,
une tension de commande (VDD) fournie à travers la ligne de tension de commande (DVL) correspond à une tension en courant continu (DC), et chacun du nombre de pixels (P) met en oeuvre une opération d'initialisation, une opération de détection de tension de seuil, une opération de compensation de mobilité et d'écriture de données et une opération d'émission ;
chacun du nombre de pixels (P) comportant en outre un quatrième transistor (T4) connecté entre le deuxième noeud (N2) du transistor de commande (DT) et une ligne de tension d'initialisation (IVL), le quatrième transistor (T4) étant commandé par le troisième signal de balayage (SCAN3) par lequel est commandé le troisième transistor (T3).

11. Dispositif d'affichage électroluminescent organique (100) selon la revendication 10, dans lequel, au cours de l'opération d'initialisation, la tension de commande (VDD) est appliquée au troisième noeud (N3) du transistor de commande (DT), et le premier transistor (T1), le troisième transistor (T3) et le quatrième transistor (T4) sont activés, et le deuxième transistor (T2) est désactivé, de sorte que le noeud de maintien (Nh) et le premier noeud (N1) du transistor de commande (DT) sont initialisés par une tension de source (VSS), et le deuxième noeud (N2) du transistor de commande (DT) est initialisé par une tension d'initialisation (Vini).

12. Dispositif d'affichage électroluminescent organique (100) comprenant :

un panneau d'affichage (110) sur lequel des lignes de données (DL1 à DLm) et des lignes de grille (GL1 à GLn) sont agencées en vue de définir un nombre de pixels (P) ;
un pilote de données (120) pilotant les lignes de données (DL1 à DLm) ;
un pilote de grille (130) pilotant les lignes de grille (GL1 à GLn) ; et
un contrôleur de temporisation (140) commandant le pilote de données (120) et le pilote de grille (130), dans lequel chacun des pixels (P) comprend :

une diode électroluminescente organique (OLED) ;
un transistor de commande (DT) commandant la diode électroluminescente organique (OLED), dans lequel le transistor de commande (DT) inclut un premier noeud (N1) formant un noeud de grille, un deuxième noeud (N2) connecté à la diode électroluminescente organique (OLED) et un troisième noeud (N3) connecté à une ligne de tension de commande (DVL) ;
un premier transistor (T1) commandé par un premier signal de balayage (SCAN1), le premier transistor (T1) étant connecté entre une ligne de tension de source (SVL) et le premier noeud (N1) du transistor de

commande (DT) ;
un premier condensateur de stockage (Cstg1) connecté entre le premier noeud (N1) et le deuxième noeud (N2) du transistor de commande (DT) ;
un second condensateur de stockage (Cstg2) et un condensateur d'amplification (Cboost) entre le premier noeud (N1) et le deuxième noeud (N2) du transistor de commande (DT) ; et
un deuxième transistor (T2) commandé par un deuxième signal de balayage (SCAN2), le deuxième transistor (T2) étant connecté entre un noeud de maintien (Nh) auquel le second condensateur de stockage (Cstg2) et le condensateur d'amplification (Cboost) sont connectés et une ligne de données correspondante (DL) des lignes de données (DL1 à DLm) ;

caractérisé en ce que,
une tension de commande (VDD) fournie à travers la ligne de tension de commande (DVL) correspond à une tension en courant alternatif (AC), dans lequel le noeud de maintien (Nh) est initialisé par une tension appliquée à travers la ligne de données correspondante (DL), la tension appliquée à travers la ligne de données (DL) comporte une tension de données d'initialisation de niveau faible (Vo) et une tension de données de niveau élevé (Vdata) alternant avec la tension de données d'initialisation de niveau faible (Vo), et le deuxième transistor (T2) répète l'activation et la désactivation par un temps horizontal (HT).

13. Dispositif d'affichage électroluminescent organique (100) comportant :

un panneau d'affichage (110) sur lequel des lignes de données (DL1 à DLm) et des lignes de grille (GL1 à GLn) sont agencées en vue de définir un nombre de pixels (P) ;
un pilote de données (120) pilotant les lignes de données (DL1 à DLm) ;
un pilote de grille (130) pilotant les lignes de grille (GL1 à GLn) ; et
un contrôleur de temporisation (140) commandant le pilote de données (120) et le pilote de grille (130), dans lequel chacun des pixels (P) comprend :

une diode électroluminescente organique (OLED) ;
un transistor de commande (DT) commandant la diode électroluminescente organique (OLED), dans lequel le transistor de commande (DT) inclut un premier noeud (N1) formant un noeud de grille, un deuxième noeud (N2) connecté à la diode électroluminescente organique (OLED) et un troisième noeud (N3) connecté à une ligne de tension de commande (DVL) ;
un premier transistor (T1) commandé par un premier signal de balayage (SCAN1), le premier transistor (T1) étant connecté entre une ligne de tension de source (SVL) et le premier noeud (N1) du transistor de commande (DT) ;
un premier condensateur de stockage (Cstg1) connecté entre le premier noeud (N1) et le deuxième noeud (N2) du transistor de commande (DT) ;
un second condensateur de stockage (Cstg2) et un condensateur d'amplification (Cboost) entre le premier noeud (N1) et le deuxième noeud (N2) du transistor de commande (DT) ; et
un deuxième transistor (T2) commandé par un deuxième signal de balayage (SCAN2), le deuxième transistor (T2) étant connecté entre un noeud de maintien (Nh) auquel le second condensateur de stockage (Cstg2) et le condensateur d'amplification (Cboost) sont connectés et une ligne de données correspondante (DL) des lignes de données (DL1 à DLm) ;

caractérisé en ce que,
chacun des pixels (P) comporte en outre un troisième transistor (T3) connecté entre le deuxième noeud (N2) du transistor de commande (DT) et une ligne de tension d'initialisation (IVL), le troisième transistor (T3) étant commandé par le deuxième signal de balayage (SCAN2) par lequel est commandé le deuxième transistor (T2), une tension de commande (VDD) fournie à travers la ligne de tension de commande (DVL) correspondant à une tension en courant continu (DC).

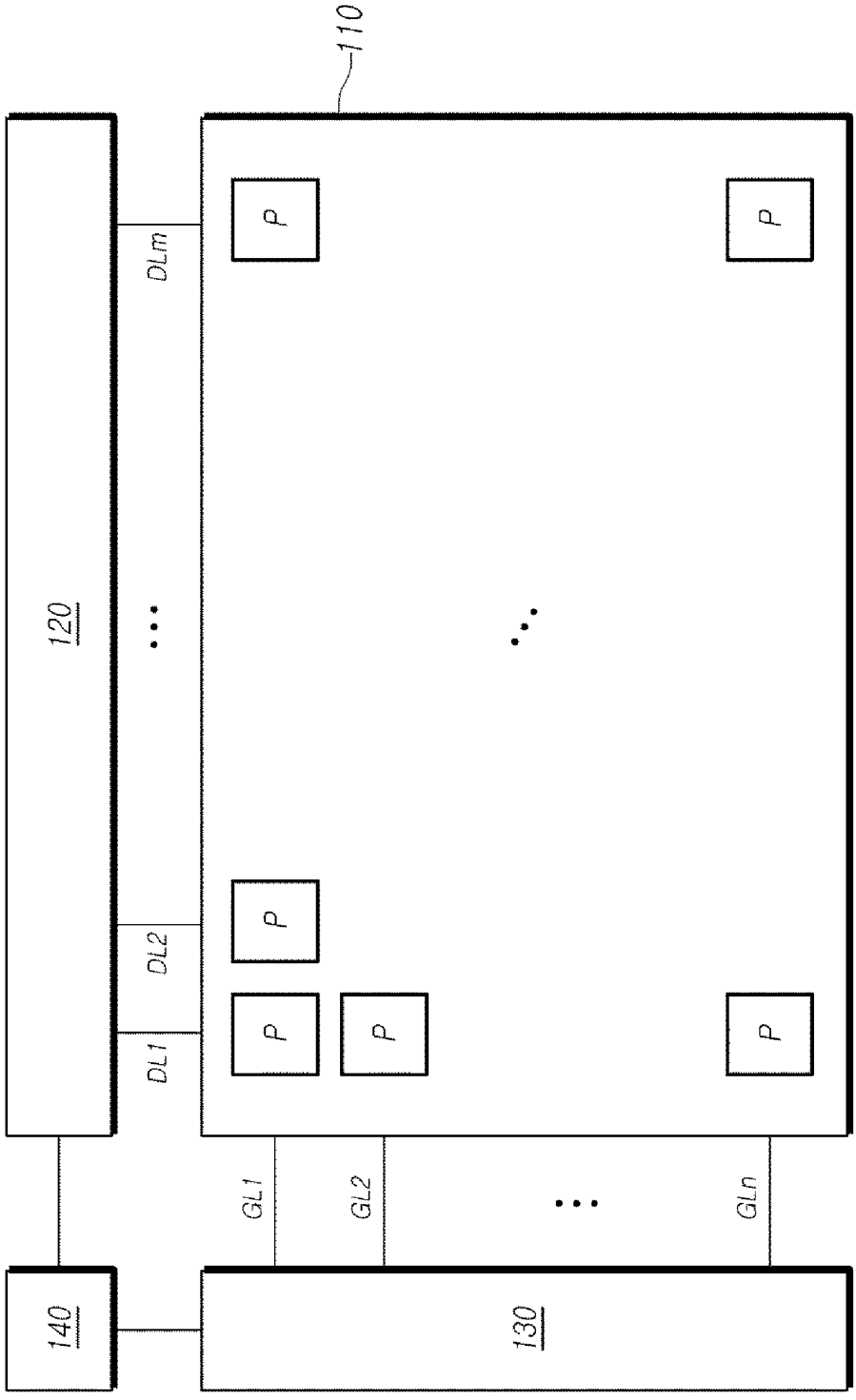


FIG. 1

FIG.2

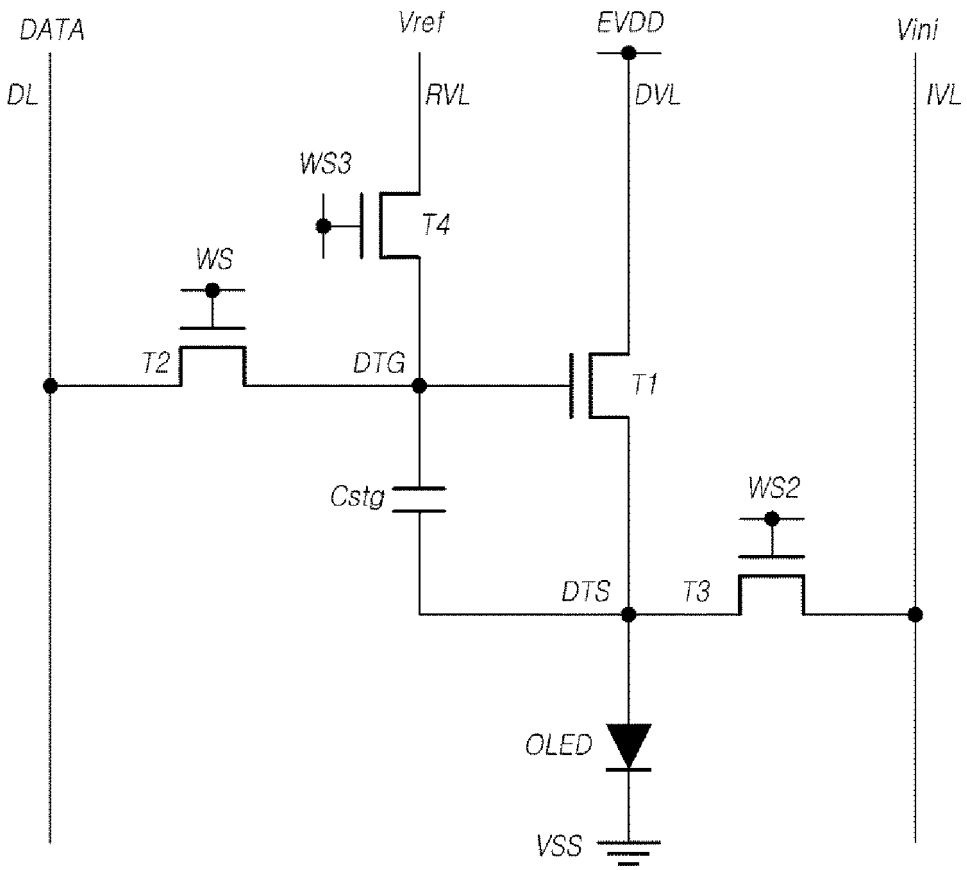

DATA
DL
Vref
RVL
EVDD
DVL
Vini
IVL
WS3
T4
WS
T2
DTG
T1
Cstg
WS2
DTS
T3
OLED
VSS

FIG.3

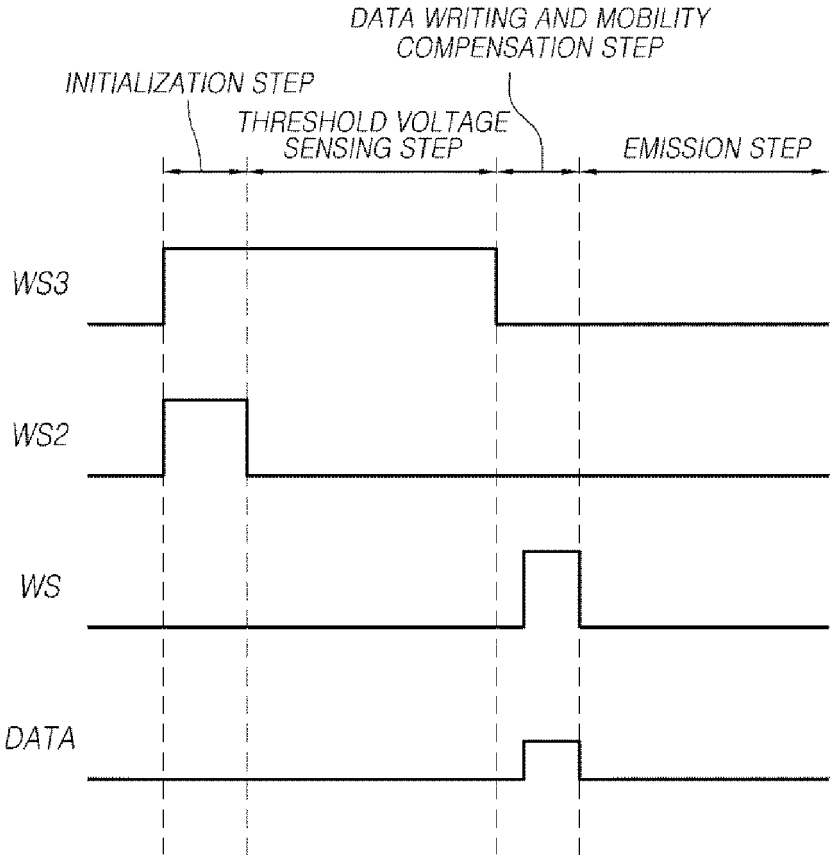

DATA WRITING AND MOBILITY COMPENSATION STEP
INITIALIZATION STEP
THRESHOLD VOLTAGE SENSING STEP
EMISSION STEP
WS3
WS2
WS
DATA

FIG.4

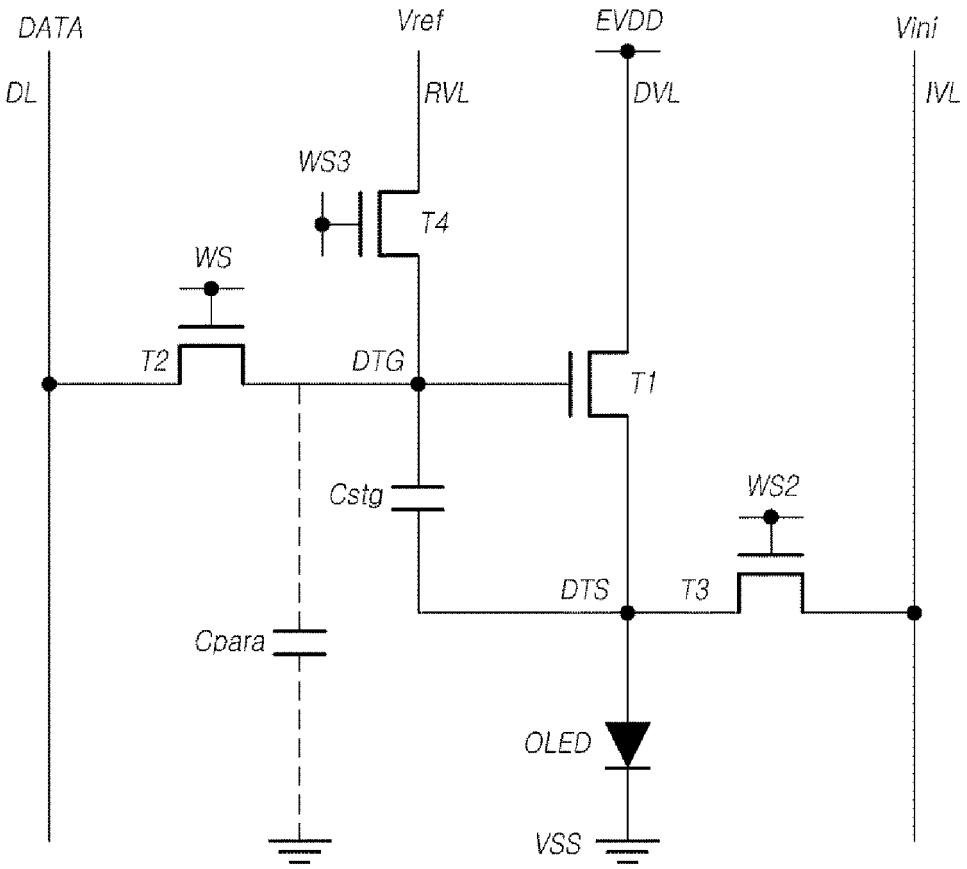

DATA
DL
Vref
RVL
EVDD
DVL
Vini
IVL
WS3
T4
WS
T2
DTG
T1
Cstg
WS2
DTS
T3
Cpara
OLED
VSS

FIG.5

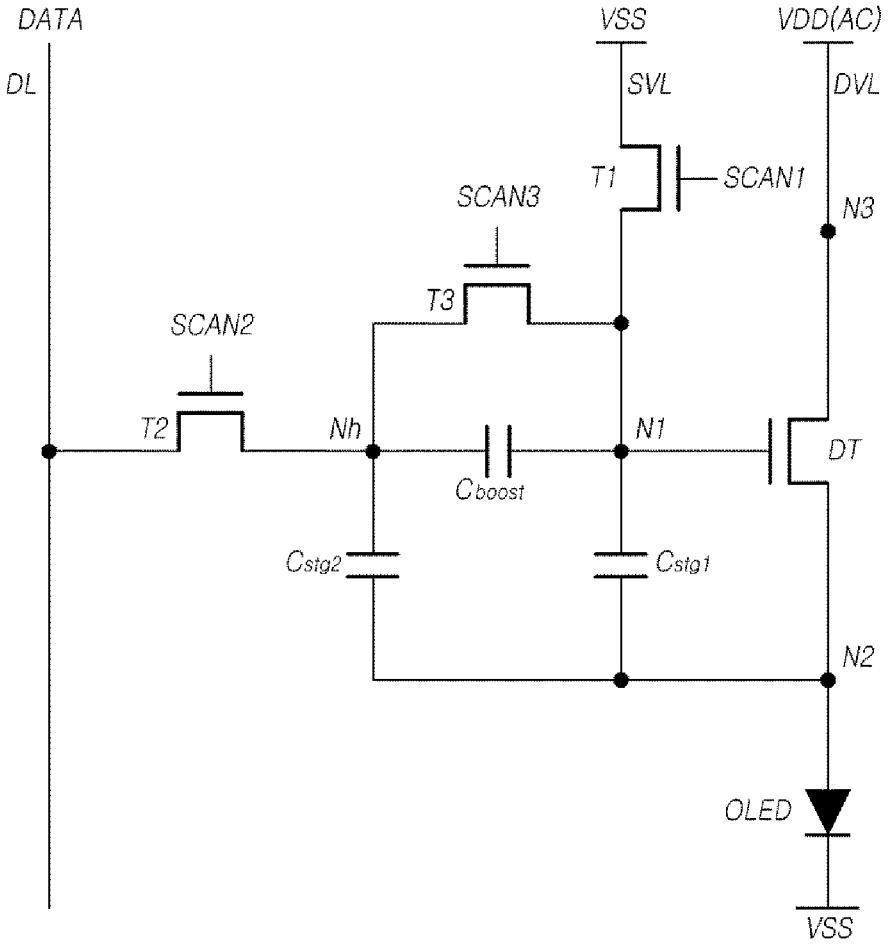

DATA
DL
VSS
SVL
VDD(AC)
DVL
T1
SCAN1
N3
SCAN3
T3
SCAN2
T2
Nh
N1
DT
Cboost
Cstg2
Cstg1
N2
OLED
VSS

FIG.6

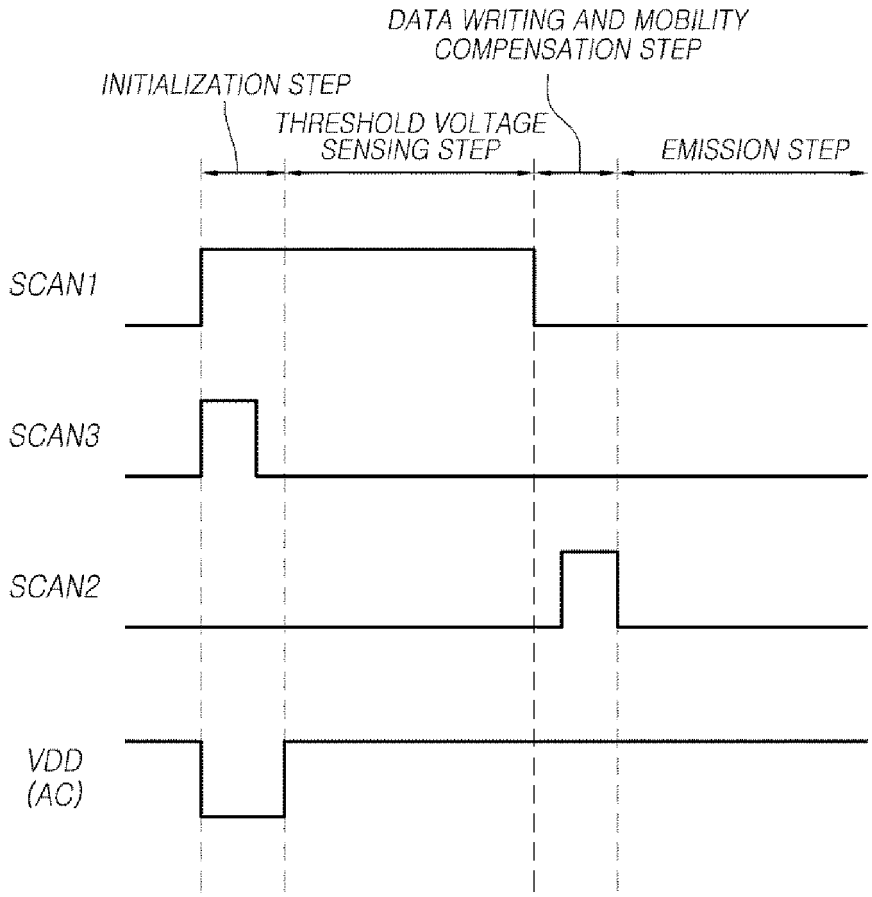

DATA WRITING AND MOBILITY COMPENSATION STEP
INITIALIZATION STEP
THRESHOLD VOLTAGE SENSING STEP
EMISSION STEP
SCAN1
SCAN3
SCAN2
VDD (AC)

FIG. 7A

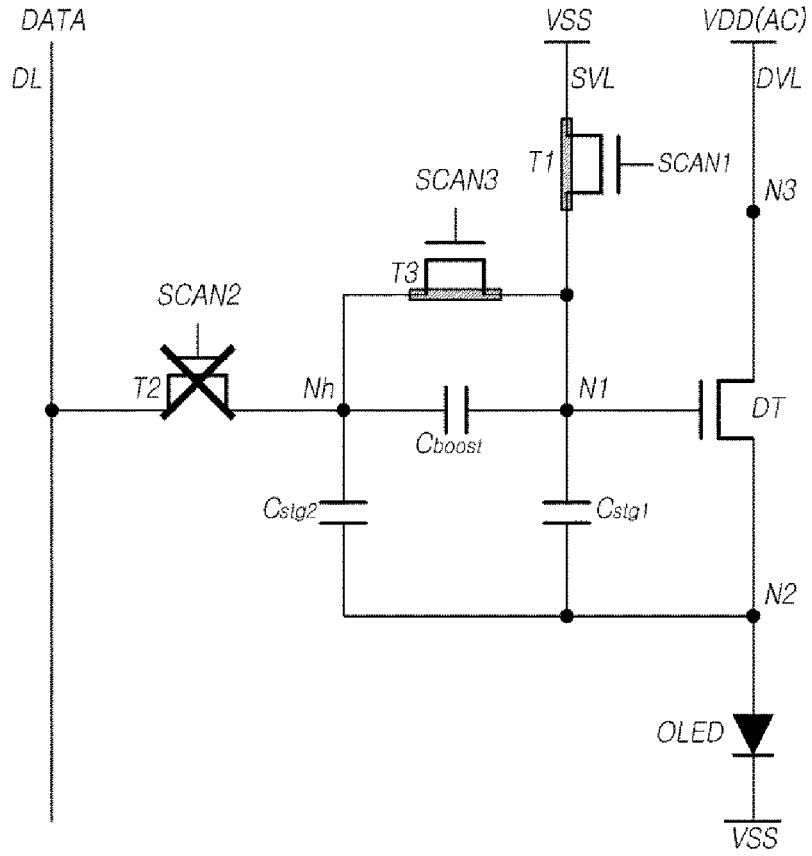

DATA
DL
VSS
SVL
VDD(AC)
DVL
T1
SCAN1
N3
SCAN3
T3
SCAN2
T2
Nh
N1
DT
Cboost
Cstg2
Cstg1
N2
OLED
VSS

FIG. 7B

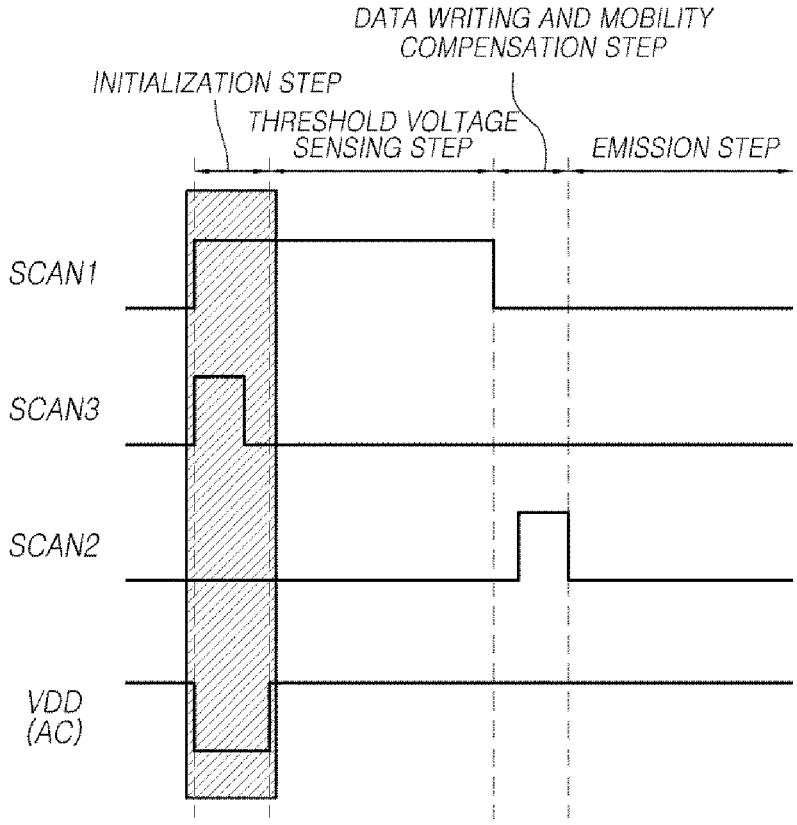

DATA WRITING AND MOBILITY COMPENSATION STEP
INITIALIZATION STEP
THRESHOLD VOLTAGE SENSING STEP
EMISSION STEP
SCAN1
SCAN3
SCAN2
VDD (AC)

FIG.8A

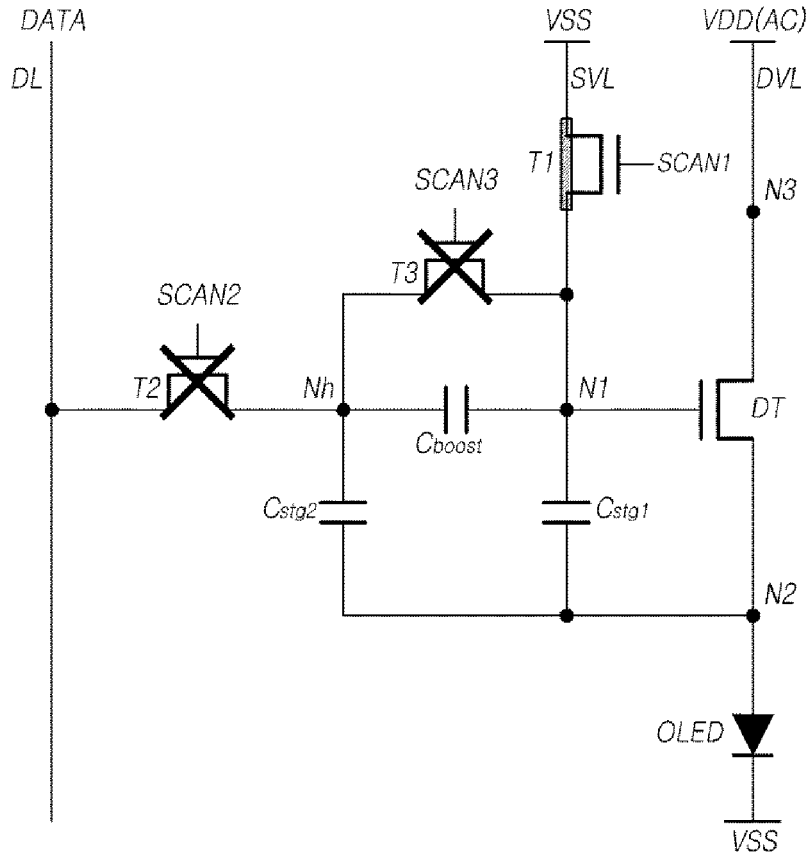

DATA
DL
VSS
SVL
VDD(AC)
DVL
T1
SCAN1
N3
SCAN3
T3
SCAN2
T2
Nh
N1
DT
Cboost
Cstg2
Cstg1
N2
OLED
VSS

FIG. 8B

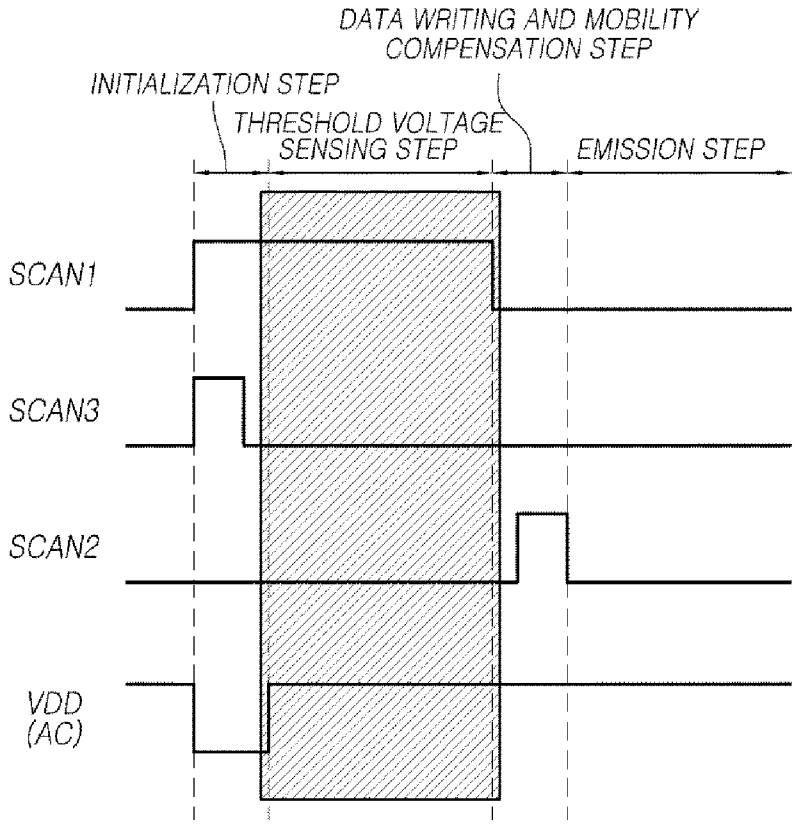

DATA WRITING AND MOBILITY COMPENSATION STEP
INITIALIZATION STEP
THRESHOLD VOLTAGE SENSING STEP
EMISSION STEP
SCAN1
SCAN3
SCAN2
VDD (AC)

FIG.9

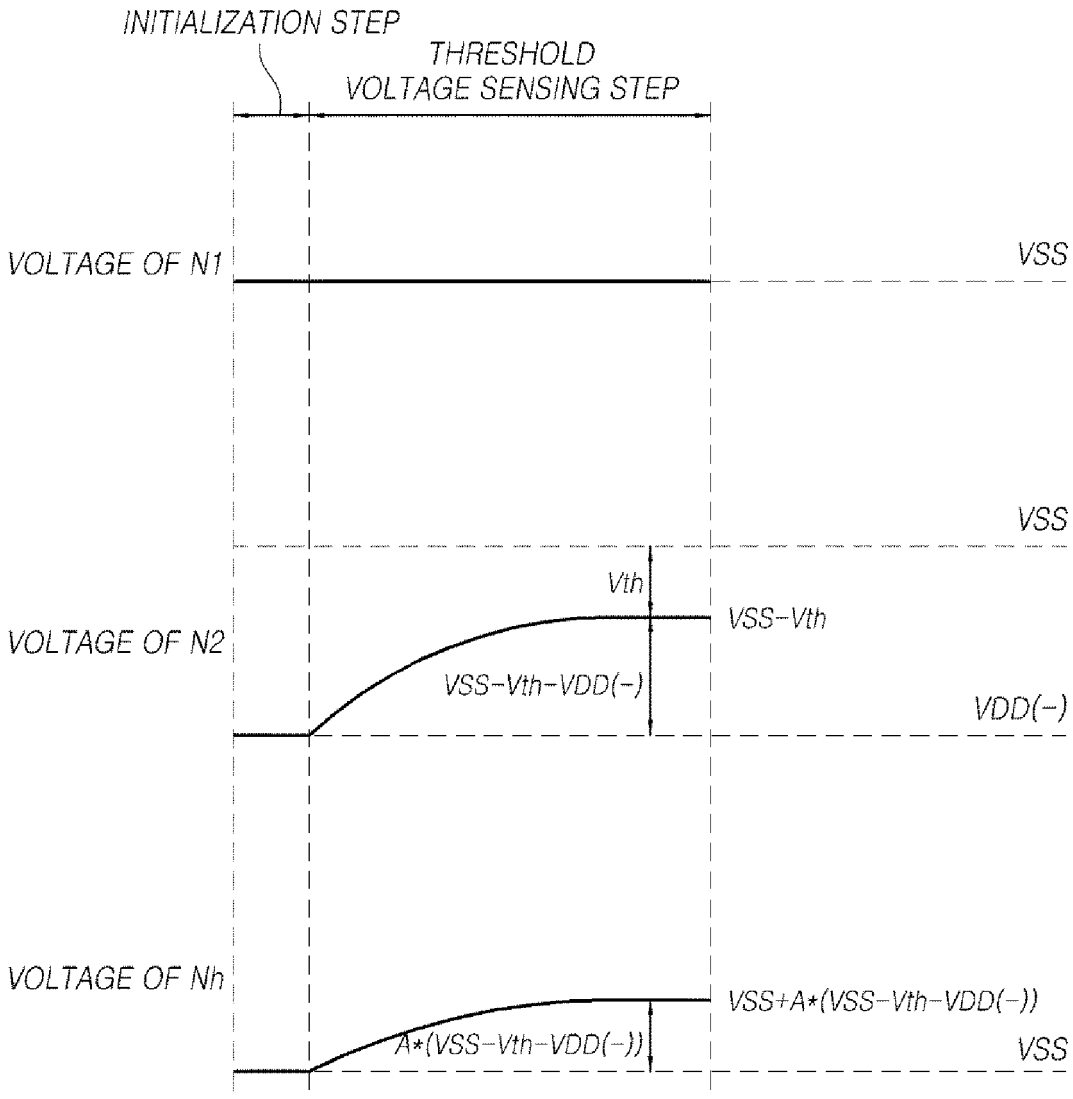

INITIALIZATION STEP
THRESHOLD VOLTAGE SENSING STEP
VOLTAGE OF N1
VSS
VSS
Vth
VOLTAGE OF N2
VSS-Vth
VSS-Vth-VDD(-)
VDD(-)
VOLTAGE OF Nh
VSS+A*(VSS-Vth-VDD(-))
A*(VSS-Vth-VDD(-))
VSS

FIG. 10A

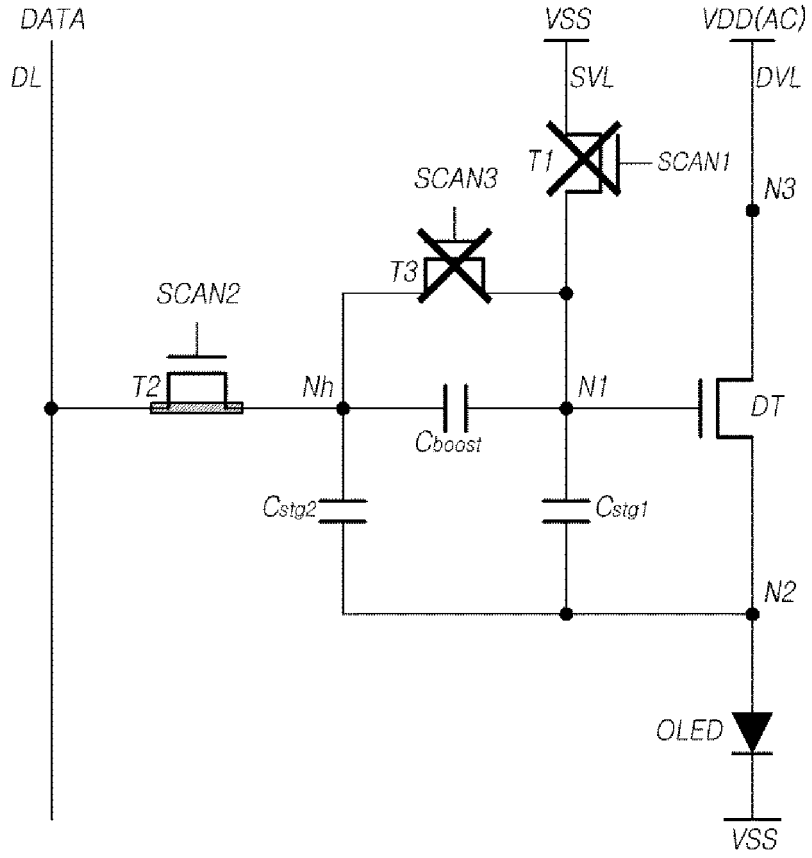

DATA
DL
VSS
SVL
VDD(AC)
DVL
T1
SCAN1
N3
SCAN3
T3
SCAN2
T2
Nh
N1
DT
Cboost
Cstg2
Cstg1
N2
OLED
VSS

FIG. 10B

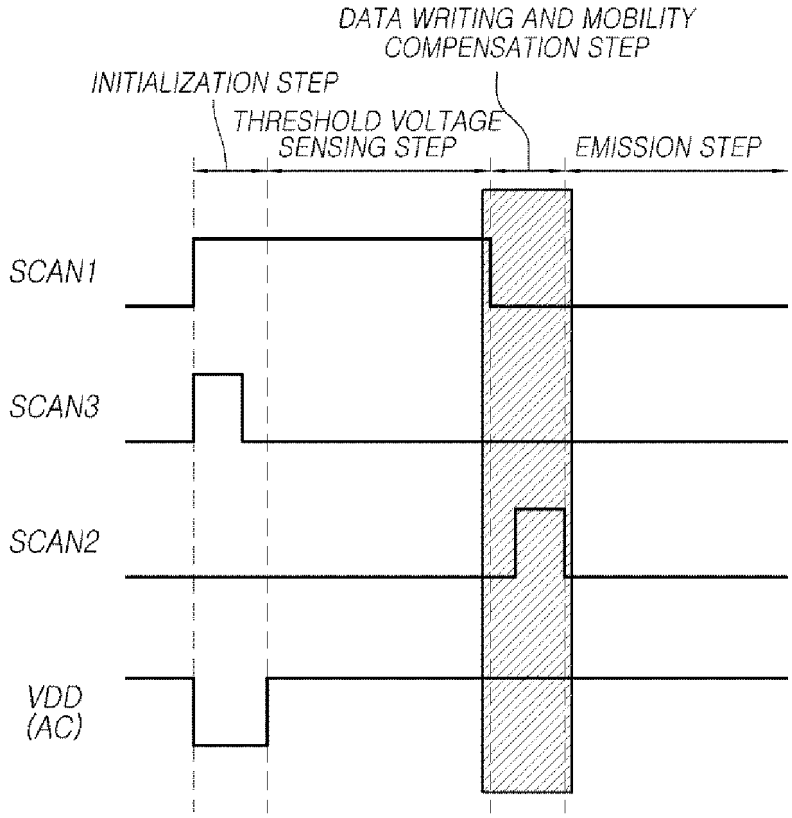

DATA WRITING AND MOBILITY COMPENSATION STEP
INITIALIZATION STEP
THRESHOLD VOLTAGE SENSING STEP
EMISSION STEP
SCAN1
SCAN3
SCAN2
VDD (AC)

FIG. 11

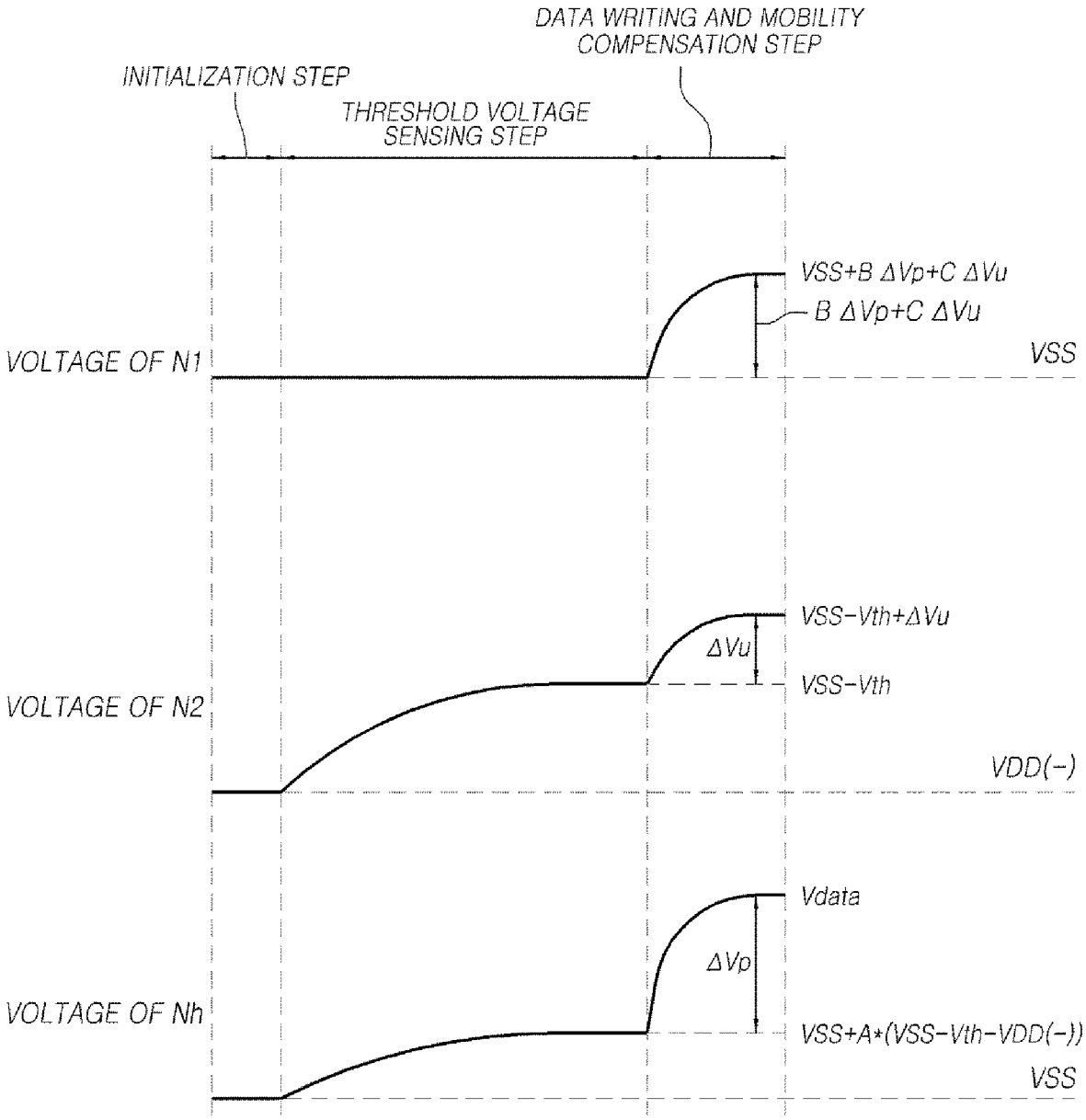

DATA WRITING AND MOBILITY COMPENSATION STEP
INITIALIZATION STEP
THRESHOLD VOLTAGE SENSING STEP
VOLTAGE OF N1
VSS+B ΔVp+C ΔVu
B ΔVp+C ΔVu
VSS
VOLTAGE OF N2
VSS-Vth+ΔVu
ΔVu
VSS-Vth
VDD(-)
VOLTAGE OF Nh
Vdata
ΔVp
VSS+A*(VSS-Vth-VDD(-))
VSS

FIG. 12A

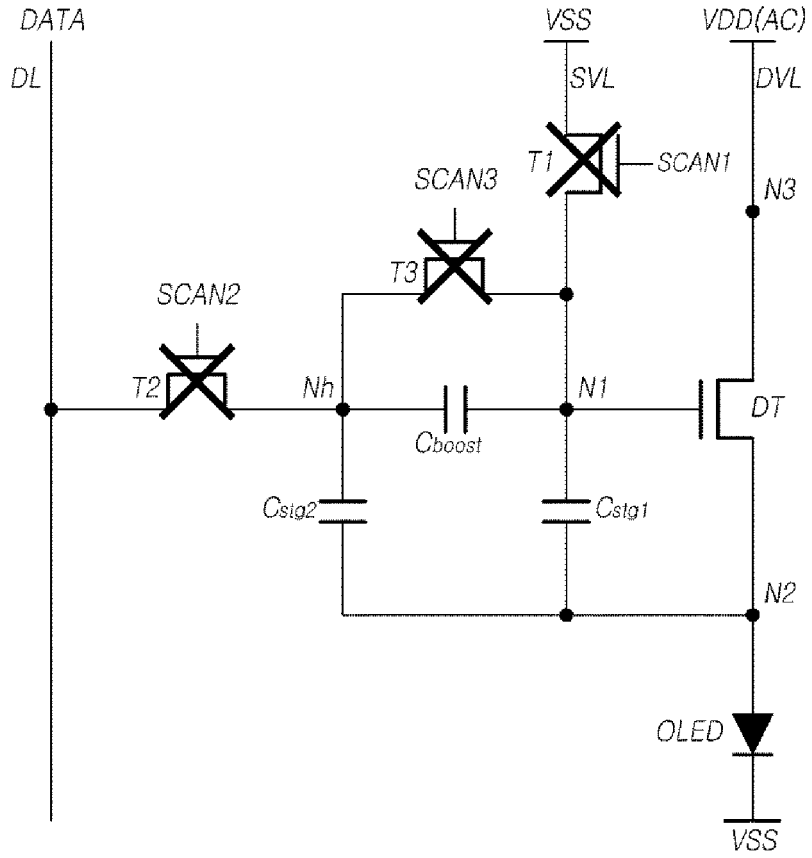

DATA
DL
VSS
SVL
VDD(AC)
DVL
T1
SCAN1
N3
SCAN3
T3
SCAN2
T2
Nh
N1
DT
Cboost
Csig2
Cstg1
N2
OLED
VSS

FIG. 12B

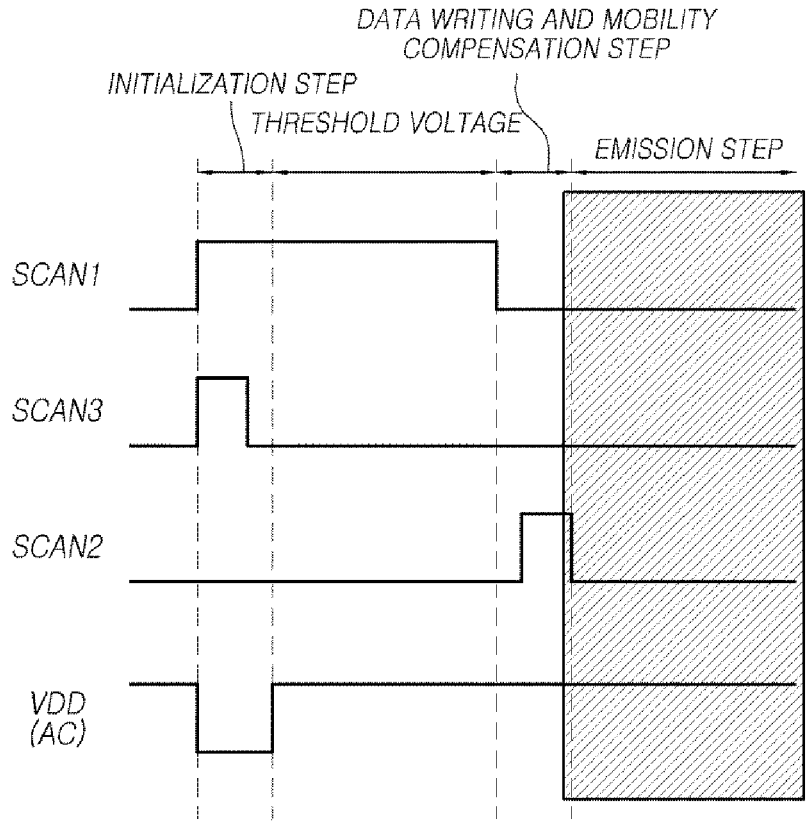

DATA WRITING AND MOBILITY COMPENSATION STEP
INITIALIZATION STEP
THRESHOLD VOLTAGE
EMISSION STEP
SCAN1
SCAN3
SCAN2
VDD (AC)

FIG. 13A

63GRAY

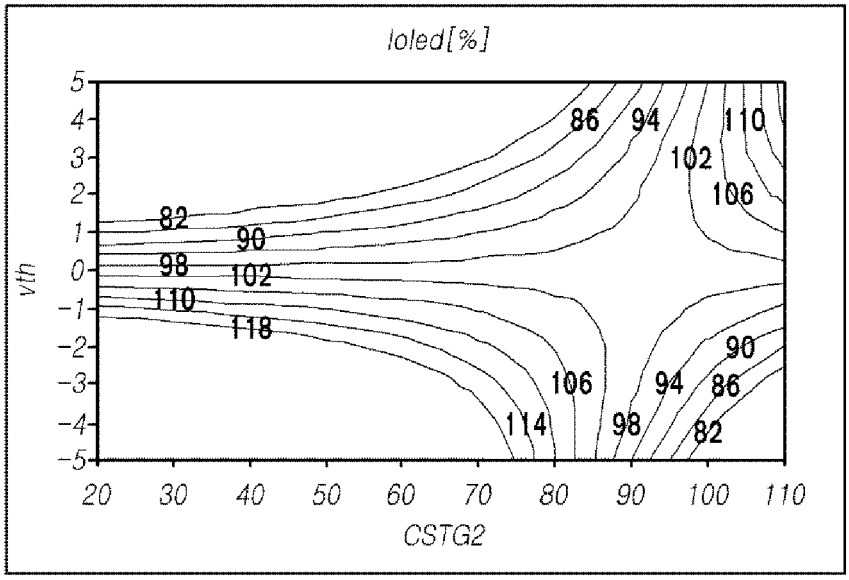


FIG. 13B

255GRAY

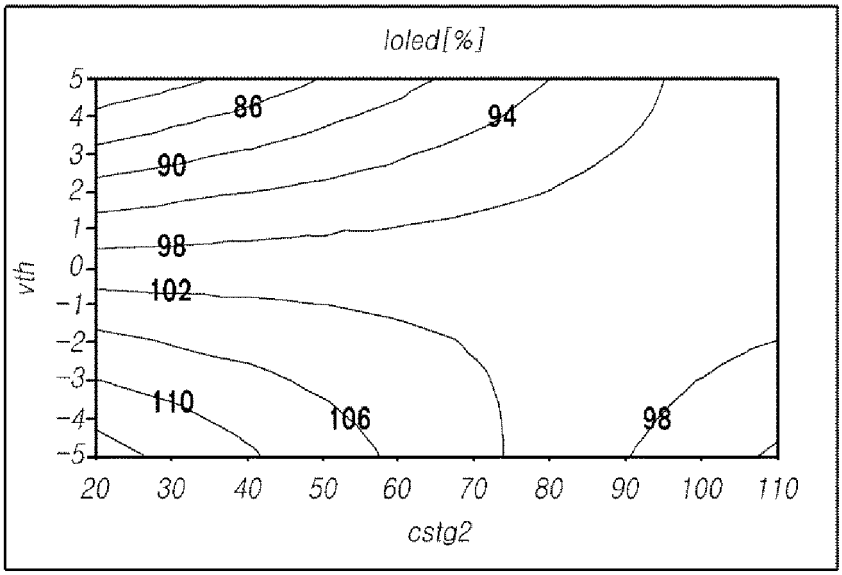


FIG.14A

63GRAY

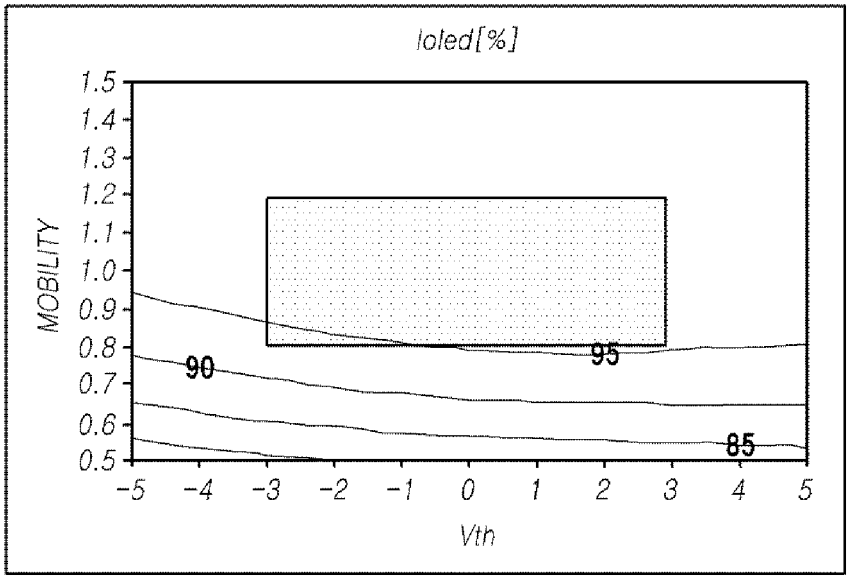


FIG. 14B

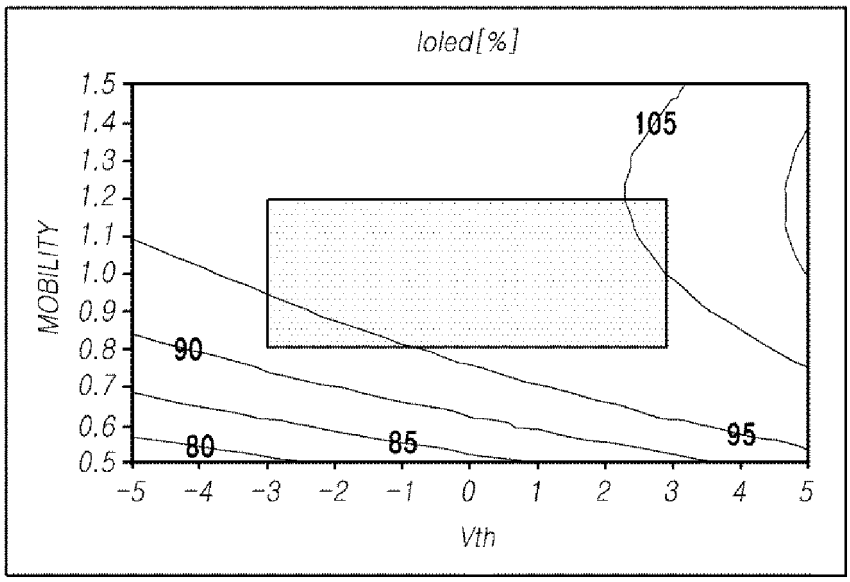

255GRAY
Ioled[%]
MOBILITY
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
105
90
80
85
95
−5
−4
−3
−2
−1
0
1
2
3
4
5
Vth

FIG. 15A

63GRAY

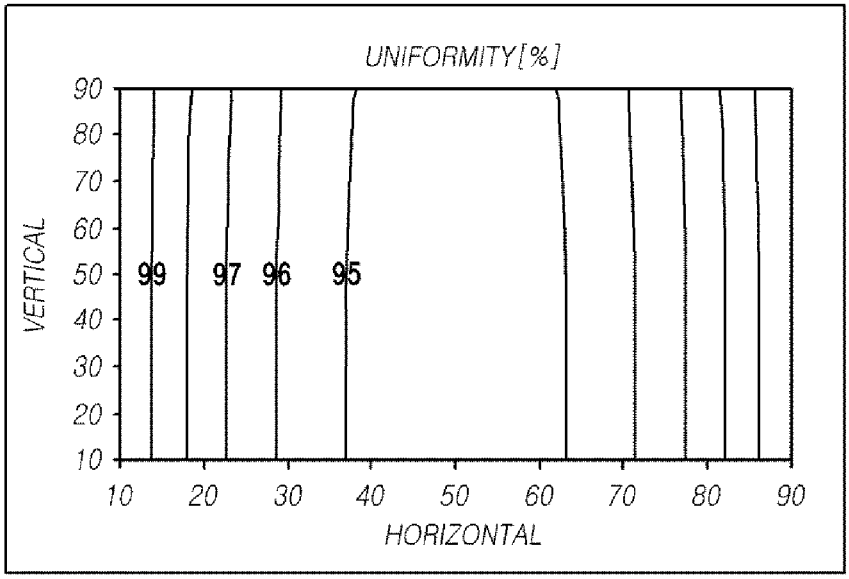


FIG. 15B

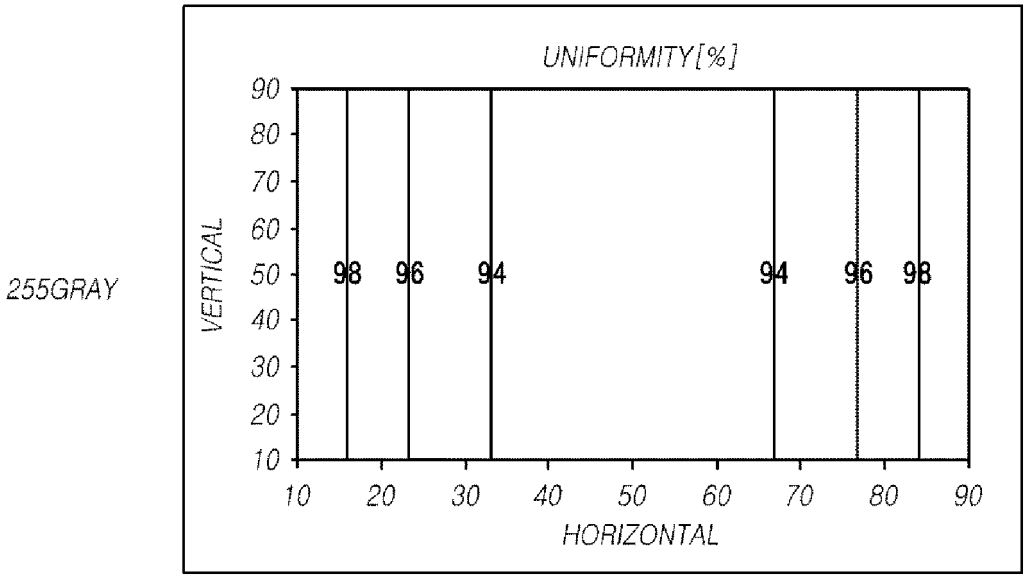

255GRAY
UNIFORMITY[%]
VERTICAL
HORIZONTAL
90
80
70
60
50
40
30
20
10
98
96
94
94
96
98

FIG. 16

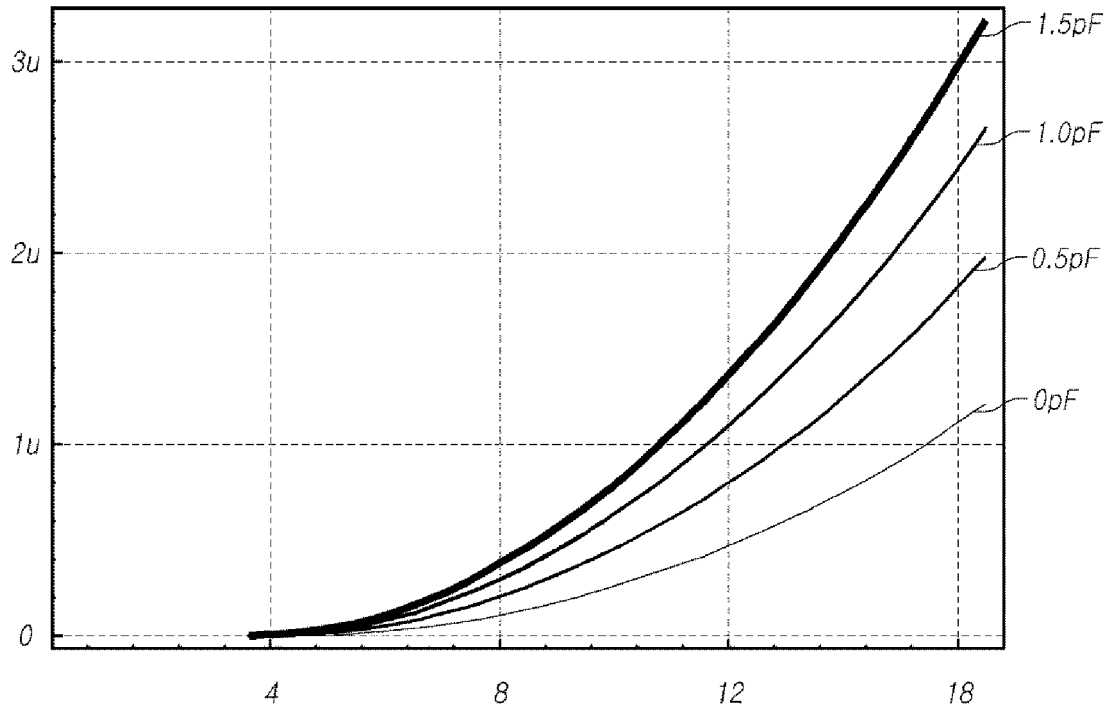


FIG. 17

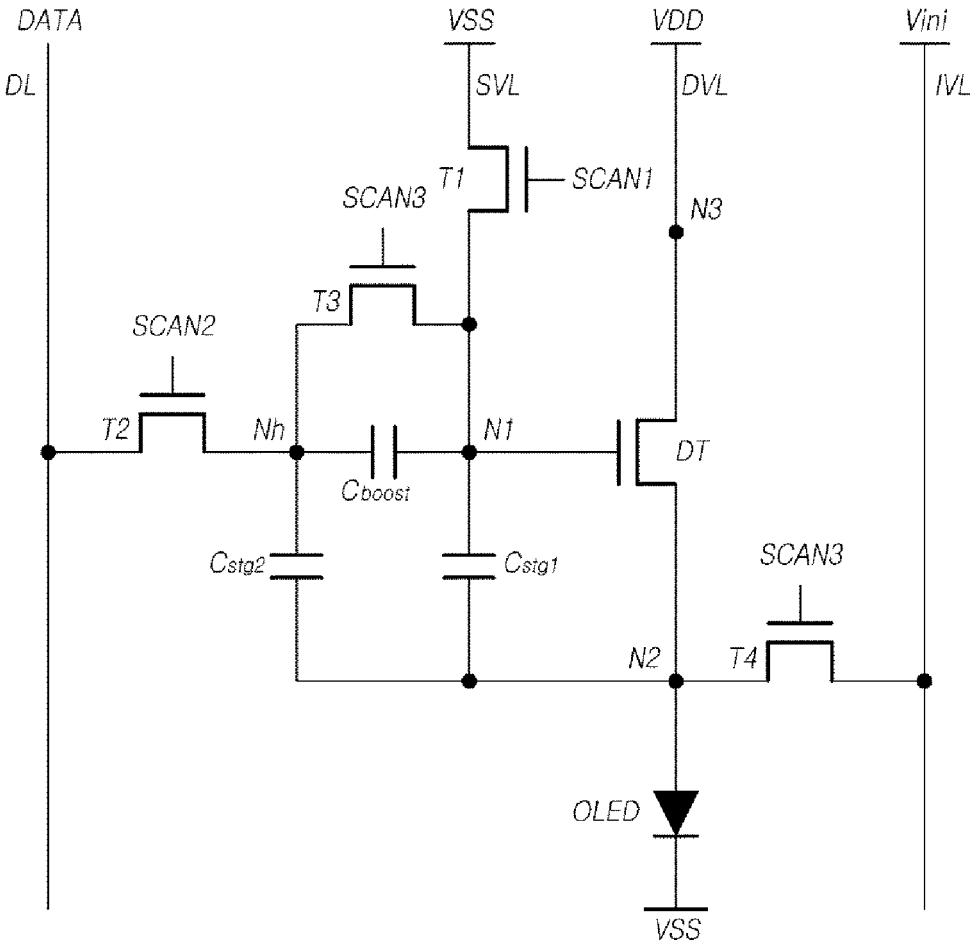

DATA
VSS
VDD
Vini
DL
SVL
DVL
IVL
T1
SCAN1
SCAN3
N3
T3
SCAN2
T2
Nh
N1
DT
Cboost
Cstg2
Cstg1
SCAN3
N2
T4
OLED
VSS

FIG. 18

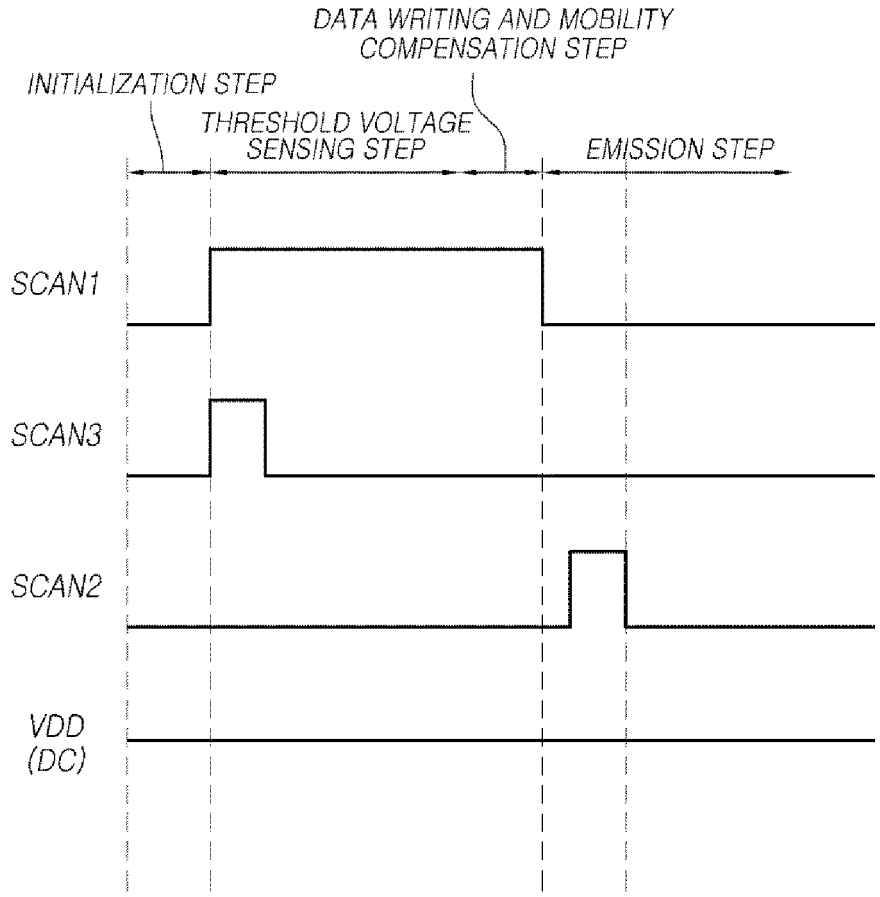

DATA WRITING AND MOBILITY COMPENSATION STEP
INITIALIZATION STEP
THRESHOLD VOLTAGE SENSING STEP
EMISSION STEP
SCAN1
SCAN3
SCAN2
VDD (DC)

FIG. 19

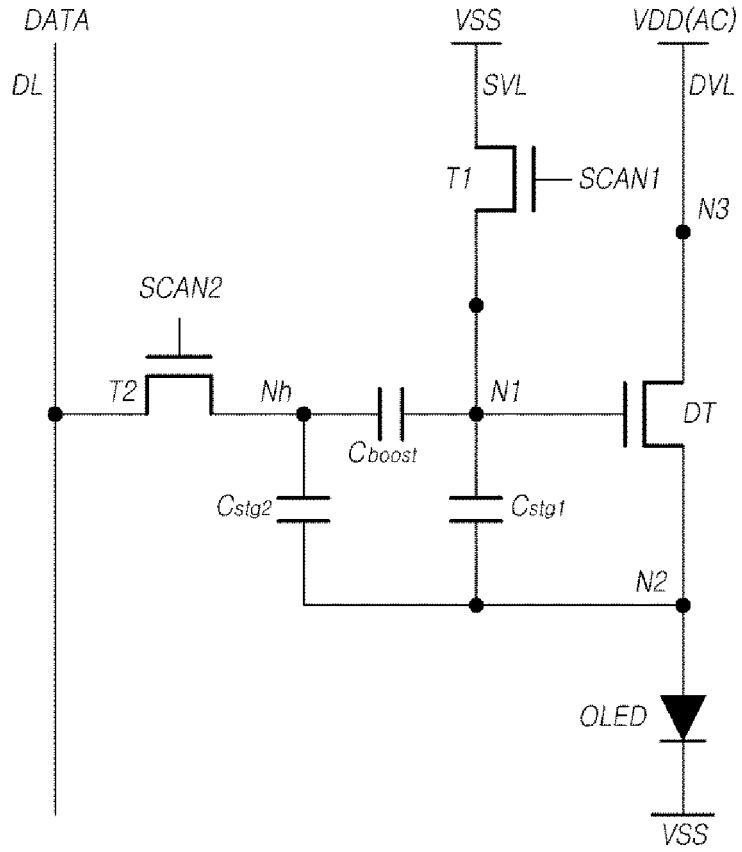

DATA
DL
VSS
SVL
VDD(AC)
DVL
T1
SCAN1
N3
SCAN2
T2
Nh
N1
DT
Cboost
Cstg2
Cstg1
N2
OLED
VSS

FIG.20

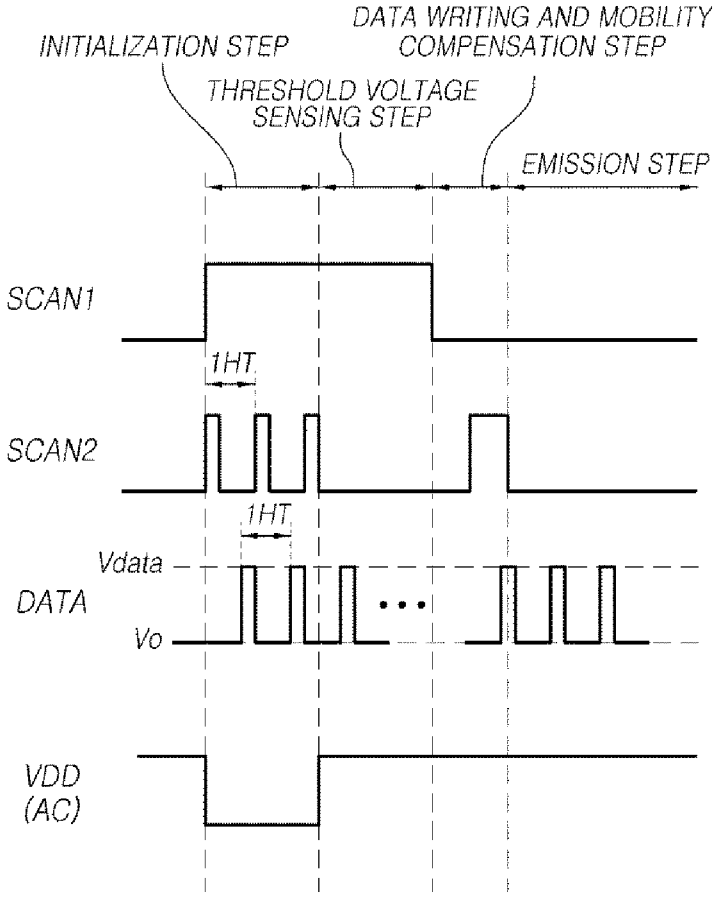

INITIALIZATION STEP
DATA WRITING AND MOBILITY COMPENSATION STEP
THRESHOLD VOLTAGE SENSING STEP
EMISSION STEP
SCAN1
1HT
SCAN2
1HT
Vdata
DATA
Vo
VDD (AC)

FIG.21

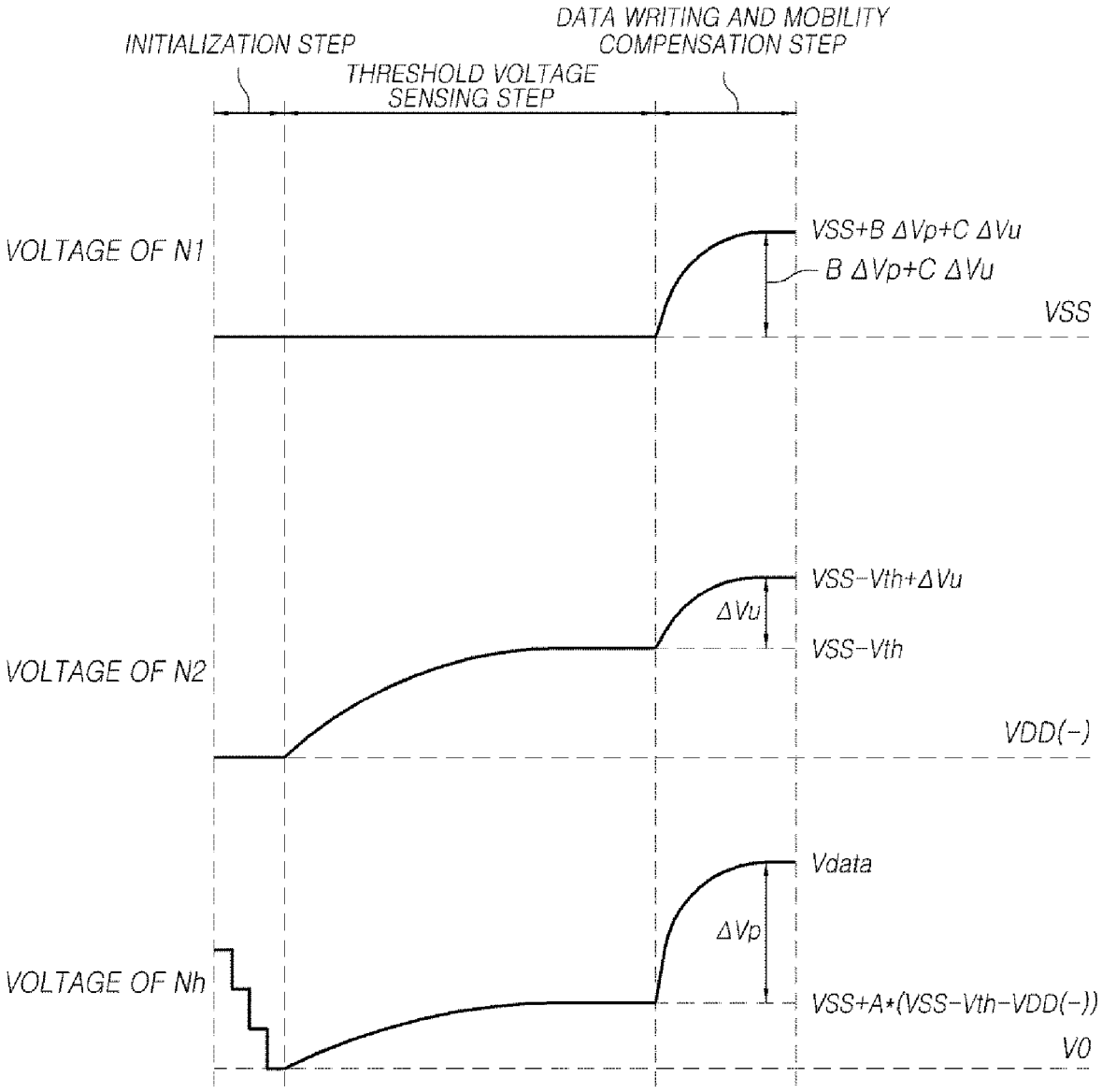

INITIALIZATION STEP
THRESHOLD VOLTAGE SENSING STEP
DATA WRITING AND MOBILITY COMPENSATION STEP
VOLTAGE OF N1
VSS+B ΔVp+C ΔVu
B ΔVp+C ΔVu
VSS
VOLTAGE OF N2
VSS-Vth+ΔVu
ΔVu
VSS-Vth
VDD(-)
VOLTAGE OF Nh
Vdata
ΔVp
VSS+A*(VSS-Vth-VDD(-))
V0

FIG.22

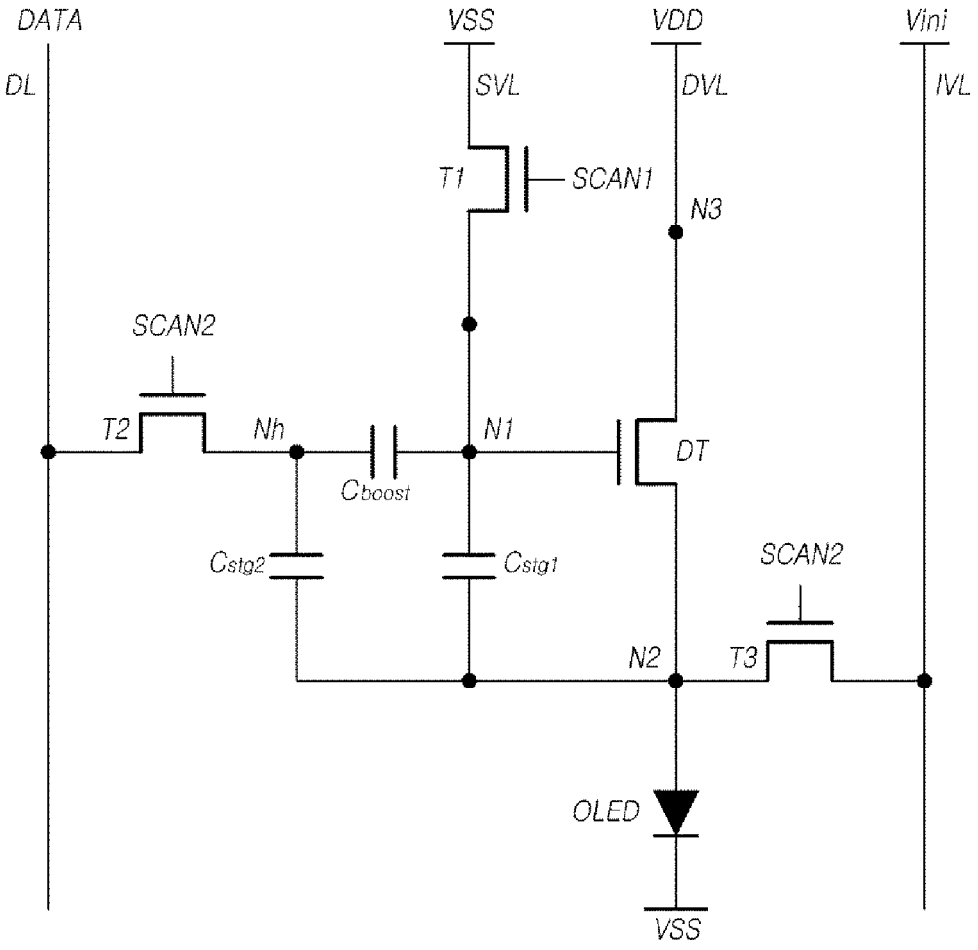
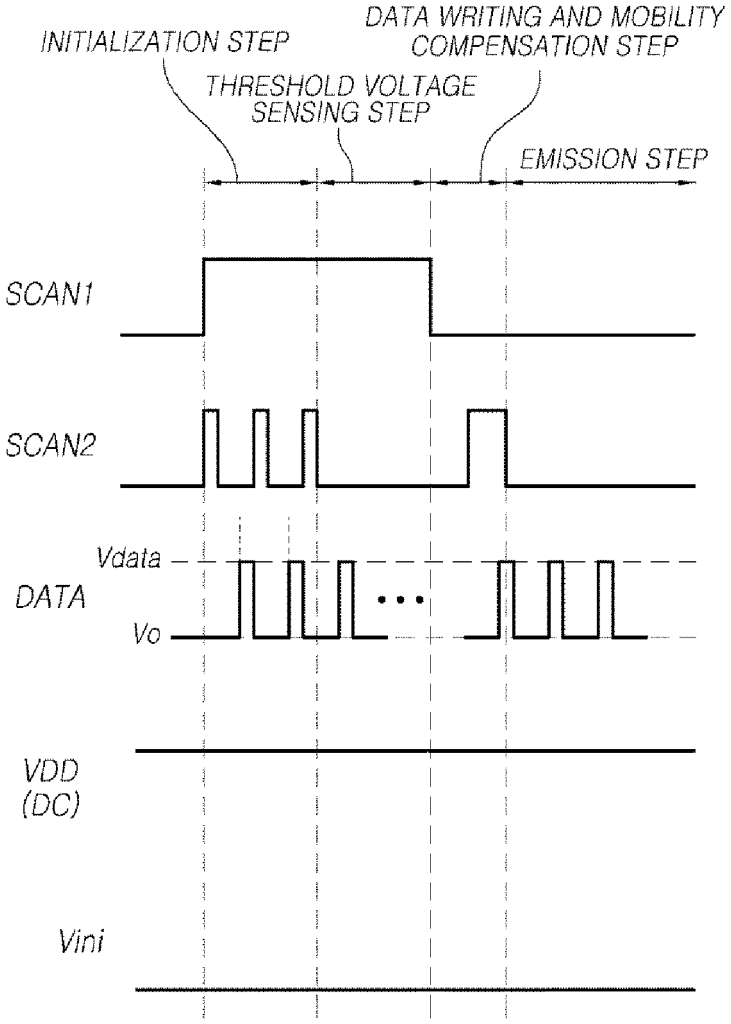

DATA
VSS
VDD
Vini
DL
SVL
DVL
IVL
T1
SCAN1
N3
SCAN2
T2
Nh
N1
DT
Cboost
Cstg2
Cstg1
SCAN2
N2
T3
OLED
VSS

FIG.23


INITIALIZATION STEP
DATA WRITING AND MOBILITY COMPENSATION STEP
THRESHOLD VOLTAGE SENSING STEP
EMISSION STEP
SCAN1
SCAN2
Vdata
DATA
Vo
VDD (DC)
Vini

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 1020130155542 **[0001]**
- US 2010289830 A **[0008]**
- US 2013249857 A **[0009]**
- WO 2013021623 A **[0010]**
- US 2014022288 A **[0010]**
- US 2005057182 A **[0011]**

专利名称(译)	具有补偿像素结构的有机发光显示装置		
公开(公告)号	EP2884484B1	公开(公告)日	2017-08-16
申请号	EP2014191844	申请日	2014-11-05
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	HAN INHYO YUN SANGUK		
发明人	HAN, INHYO YUN, SANGUK		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G2300/0819 G09G2300/0852 G09G2300/0866 G09G2320/0219 G09G3/32 G09G3/3258 G09G3/3266 G09G3/3291 G09G2300/0876 G09G2320/0204		
优先权	1020130155542 2013-12-13 KR		
其他公开文献	EP2884484A1		
外部链接	Espacenet		

摘要(译)

一种有机发光显示装置，具有能够通过补偿在操作期间将发生的阈值电压的损失来显着改善阈值电压补偿能力和范围的像素结构。

$$\text{Voltage of } N1 = VSS$$

$$\text{Voltage of } N2 = VDD(-)$$

$$\text{Voltage of } Nh = VSS \qquad \text{.....Formula 1}$$