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(71) Applicant: **LG Display Co., Ltd.**
Seoul 150-721 (KR)

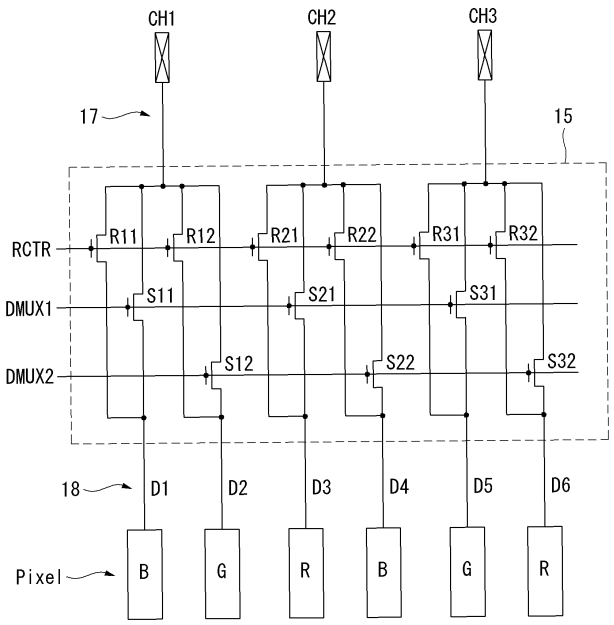
(72) Inventors:
- **Lee, Jungmin**
  413-783 Paju-si, Gyeonggi-do (KR)
- **Kang, Changheon**
  413-833 Paju-si, Gyeonggi-do (KR)

(74) Representative: **Viering, Jentschura & Partner**
Patent- und Rechtsanwälte
Am Brauhaus 8
01099 Dresden (DE)

(54) Organic light emitting display

(57) An organic light emitting display includes a display panel including first pixels displaying a first color, second pixels displaying a second color, and third pixels displaying a third color, a data driving circuit generating a data voltage, a demultiplexer (demux) switching circuit, which includes first to Nth demux switches connected to each output channel of the data driving circuit, where N is a positive integer equal to or greater than 2, and time-division supplies the data voltage to N data lines of the display panel, and a control signal generator generating first to Nth demux control signals for controlling operations of the first to Nth demux switches. The first to Nth demux control signals sequentially rise to an on-level and then sequentially fall to an off-level in a programming period, in which a scan signal is held at the on-level.

FIG. 6



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the invention relate to an active matrix organic light emitting display.

Discussion of the Related Art

[0002] An active matrix organic light emitting display includes organic light emitting diodes (hereinafter, abbreviated to "OLEDs") capable of emitting light by itself and has advantages of a fast response time, a high light emitting efficiency, a high luminance, a wide viewing angle, and the like.

[0003] The OLED serving as a self-emitting element has a structure shown in FIG. 1. The OLED includes an anode electrode, a cathode electrode, and an organic compound layer formed between the anode electrode and the cathode electrode. The organic compound layer includes a hole injection layer HIL, a hole transport layer HTL, an emission layer EML, an electron transport layer ETL, and an electron injection layer EIL. When a driving voltage is applied to the anode electrode and the cathode electrode, holes passing through the hole transport layer HTL and electrons passing through the electron transport layer ETL move to the emission layer EML and form excitons. As a result, the emission layer EML generates visible light.

[0004] The organic light emitting display arranges pixels each including the OLED in a matrix form and adjusts a luminance of the pixels depending on grayscale of video data. Each pixel includes a driving thin film transistor (TFT) which controls a driving current flowing in the OLED depending on a gate-source voltage of the driving TFT, a capacitor which holds a gate potential of the driving TFT constant during one frame, and a switching TFT which stores a data voltage in the capacitor in response to a gate signal. The luminance of the pixel is proportional to a magnitude of the driving current flowing in the OLED.

[0005] The organic light emitting display includes a data driving circuit which converts digital video data into analog data voltages and supplies the analog data voltages to data lines of a display panel. Because the data driving circuit generally has as many output channels as the data lines of the display panel, the size of the data driving circuit increases. Hence, the cost of the data driving circuit is expensive. In a related art, a demultiplexer (demux) driving method using a demux switching circuit was proposed to reduce the number of output channels of the data driving circuit to 1/2 or more.

[0006] FIG. 2 shows an existing 1 to 2 demux driving method. A demux switching circuit shown in FIG. 2 connects output channels CH1, CH2, and CH3 of a data driving circuit with data lines D1 to D6 of a display panel at 1:2. The demux switching circuit time-divides a data voltage input through one output channel and supplies the data voltage to the two data lines. A time-division operation of the demux switching circuit is performed by switching operations of demux switches S11, S21, S31, S12, S22, and S32 driven in response to demux control signals DMUX1 and DMUX2. The first demux switches S11, S21, and S31 are simultaneously turned on in response to the first demux control signal DMUX1, and the second demux switches S12, S22, and S32 are simultaneously turned on in response to the second demux control signal DMUX2. In this instance, the first demux switches S11, S21, and S31 and the second demux switches S12, S22, and S32 are turned on at different timings.

[0007] When the demux switch connected to the pixel changes from a turn-on state to a turn-off state, a parasitic capacitor may reduce a voltage applied to the pixel by a kickback voltage. Thus, first pixels connected to the first demux switches S11, S21, and S31 and second pixels connected to the second demux switches S12, S22, and S32 may be affected by the kickback voltage. In this instance, because the first demux switches S11, S21, and S31 and the second demux switches S12, S22, and S32 are turned on at different timings, the number of times of influence of the kickback voltage on the first pixels and the number of times of influence of the kickback voltage on the second pixels may be different from each other. An unwanted current deviation is generated between the first pixels and the second pixels because of a difference between the number of times of influence of the kickback voltage on the first pixels and the second pixels. FIG. 3 shows a current deviation between adjacent pixels resulting from a difference between the number of times of influence of the kickback voltage on the adjacent pixels. The current deviation generates a longitudinal dim and thus reduces image quality.

[0008] Each of pixels displaying red (R) includes a red OLED, each of pixels displaying green (G) includes a green OLED, and each of pixels displaying blue (B) includes a blue OLED. The R OLED, the G OLED, and the B OLED have different emission efficiencies. Thus, when the pixels generating the unwanted current deviation display different colors, the unwanted current deviation is displayed as the longitudinal dim, but is not conspicuous. However, when the pixels generating the unwanted current deviation display the same color, the unwanted current deviation is displayed as the longitudinal dim and is very conspicuous. In other words, the problem of the current deviation further increases when the pixels displaying the same color are selectively connected to the first demux switches S11, S21, and S31 and the second demux switches S12, S22, and S32 as shown in FIG. 2.

SUMMARY OF THE INVENTION

[0009] Embodiments of the invention provide an organic light emitting display capable of preventing a current deviation from being generated between pixels dis-

playing the same color by designing a demultiplexer (demux) switching circuit and a demux switching control signal so that the number of times of influence of a kickback voltage on the pixels displaying the same color are equal to each other in a demux driving method.

[0010] In one aspect, there is an organic light emitting display comprising a display panel including first pixels displaying a first color, second pixels displaying a second color, and third pixels displaying a third color, a data driving circuit configured to generate a data voltage, a demultiplexer (demux) switching circuit including first to Nth demux switches connected to each output channel of the data driving circuit, where N is a positive integer equal to or greater than 2, the demux switching circuit configured to time-division supply the data voltage received from one output channel of the data driving circuit to N data lines of the display panel, and a control signal generator configured to generate first to Nth demux control signals for controlling operations of the first to Nth demux switches, wherein the first to Nth demux control signals sequentially rise to an on-level and then sequentially fall to an off-level in a programming period, in which a first scan signal used to apply the data voltage to the pixels is held at the on-level.

[0011] In one or more embodiments, the first scan signal falls to the off-level for an emission period following the programming period, wherein all of the first to Nth demux control signals fall earlier than the first scan signal.

[0012] In one or more embodiments, N is 2, and pixels, on one horizontal pixel line, displaying the same color are selectively connected to first demux switches simultaneously operating in response to a first demux control signal and second demux switches simultaneously operating in response to a second demux control signal.

[0013] In one or more embodiments, an initialization period, which is arranged prior to the programming period and initializes the first to third pixels, and a sensing period, which is arranged between the initialization period and the programming period and senses threshold voltages of driving elements included in the first to third pixels, are assigned so as to drive pixels disposed on one horizontal pixel line, wherein the initialization period is selected as one horizontal period, which is defined as a value obtained by dividing one frame period by a vertical resolution of the display panel, and a sum of lengths of the sensing period and the programming period is selected as one horizontal period, wherein the initialization period of pixels disposed on an Nth horizontal pixel line overlaps the sensing period and the programming period of pixels disposed on an (N-1)th horizontal pixel line.

[0014] In one or more embodiments, the data driving circuit further generates a reference voltage required in the initialization period and the sensing period and supplies the reference voltage to the demux switching circuit, wherein the demux switching circuit further includes first auxiliary switches respectively connected in parallel to the first demux switches and second auxiliary switches respectively connected in parallel to the second demux switches, wherein the first and second auxiliary switches are simultaneously turned on in response to an auxiliary control signal, which is held at the on-level in the initialization period and the sensing period.

[0015] In one or more embodiments, an initialization period, which is arranged prior to the programming period and initializes the first to third pixels, and a sensing period, which is arranged between the initialization period and the programming period and senses threshold voltages of driving elements included in the first to third pixels, are assigned so as to drive pixels disposed on one horizontal pixel line, wherein a sum of lengths of the initialization period, the sensing period, and the programming period is selected as one horizontal period, which is defined as a value obtained by dividing one frame period by a vertical resolution of the display panel.

[0016] In one or more embodiments, the data driving circuit further generates a reference voltage required in the initialization period and the sensing period and supplies the reference voltage to the demux switching circuit, wherein the first and second demux switches are simultaneously turned on in response to the first and second demux control signals, which are synchronized with each other at the on-level in the initialization period and the sensing period.

[0017] In one or more embodiments, N is 3, and the first pixels displaying the first color are connected to first demux switches simultaneously operating in response to a first demux control signal, wherein the second pixels displaying the second color are connected to second demux switches simultaneously operating in response to a second demux control signal, wherein the third pixels displaying the third color are connected to third demux switches simultaneously operating in response to a third demux control signal.

[0018] In one or more embodiments, an initialization period, which is arranged prior to the programming period and initializes the first to third pixels, and a sensing period, which is arranged between the initialization period and the programming period and senses threshold voltages of driving elements included in the first to third pixels, are assigned so as to drive pixels disposed on one horizontal pixel line, wherein a sum of lengths of the initialization period, the sensing period, and the programming period is selected as one horizontal period, which is defined as a value obtained by dividing one frame period by a vertical resolution of the display panel.

[0019] In one or more embodiments, the data driving circuit further generates a reference voltage required in the initialization period and the sensing period and supplies the reference voltage to the demux switching circuit, wherein the demux switching circuit further includes first auxiliary switches respectively connected in parallel to the first demux switches, second auxiliary switches respectively connected in parallel to the second demux switches, and third auxiliary switches respectively connected in parallel to the third demux switches, wherein the first to third auxiliary switches are simultaneously

turned on in response to an auxiliary control signal, which is held at the on-level in the initialization period and the sensing period.

[0020] In one or more embodiments, the data driving circuit further generates a reference voltage required in the initialization period and the sensing period and supplies the reference voltage to the demux switching circuit, wherein the first to third demux switches are simultaneously turned on in response to the first to third demux control signals, which are synchronized with each other at the on-level in the initialization period and the sensing period.

[0021] In another aspect, there is an organic light emitting display comprising a display panel including first pixels displaying a first color, second pixels displaying a second color, and third pixels displaying a third color, a data driving circuit configured to generate a data voltage, a demultiplexer (demux) switching circuit including first and second demux switches connected to each of some output channels of the data driving circuit, the demux switching circuit configured to time-division supply the data voltage received from the some output channels of the data driving circuit to two data lines of the display panel, and a control signal generator configured to generate first and second demux control signals for controlling operations of the first and second demux switches, wherein the first pixels displaying the first color are connected to the some output channels of the data driving circuit through the first demux switches, the second pixels displaying the second color are connected to the some output channels of the data driving circuit through the second demux switches, and the third pixels displaying the third color are directly connected to remaining output channels except the some output channels of the data driving circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1 shows an organic light emitting diode and its emission principle;
FIG. 2 shows an existing 1 to 2 demultiplexer (demux) driving method;
FIG. 3 shows a current deviation between adjacent pixels resulting from a difference between the number of times of influence of a kickback voltage on the adjacent pixels;
FIG. 4 shows an organic light emitting display according to an exemplary embodiment of the invention;
FIG. 5 shows an example of a pixel;
FIG. 6 shows an example of a demux switching circuit for 1 to 2 demux drive;
FIG. 7 shows driving timing of a pixel shown in FIG. 5 and a demux switching circuit shown in FIG. 6;
FIGS. 8A to 8D show an operation state of a pixel in each of driving stages;
FIG. 9 shows another example of a demux switching circuit for 1 to 2 demux drive;
FIG. 10 shows driving timing of a pixel shown in FIG. 5 and a demux switching circuit shown in FIG. 9;
FIG. 11 shows an example of a demux switching circuit for 1 to 3 demux drive;
FIG. 12 shows driving timing of a pixel shown in FIG. 5 and a demux switching circuit shown in FIG. 11;
FIG. 13 shows another example of a demux switching circuit for 1 to 3 demux drive;
FIG. 14 shows driving timing of a pixel shown in FIG. 5 and a demux switching circuit shown in FIG. 13.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0023] Reference will now be made in detail to embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts. It will be paid attention that detailed description of known arts will be omitted if it is determined that the arts can mislead the embodiments of the invention.

[0024] Exemplary embodiments of the invention will be described with reference to FIGS. 4 to 16.

[0025] FIG. 4 shows an organic light emitting display according to an exemplary embodiment of the invention. FIG. 5 shows an example of a pixel.

[0026] As shown in FIGS. 4 and 5, an organic light emitting display according to an exemplary embodiment of the invention includes a display panel 10 including a plurality of pixels, a data driving circuit 12 generating a data voltage Vdata which will be applied to the pixels, a gate driving circuit 13 generating a gate signal which will be applied to the pixels, a timing controller 11 for controlling operation timing of the data driving circuit 12 and the gate driving circuit 13, a demultiplexer (demux) switching circuit 15 which demultiplexes the data voltage Vdata received from the data driving circuit 12 and divides the demultiplexed data voltage Vdata into data lines 18, and a control signal generator 16 generating a demux switching control signal DCTR.

[0027] The display panel 10 includes a pixel array 14, on which an image is displayed. The pixel array 14 includes the plurality of data lines 18, a plurality of gate lines 19 crossing the data lines 18, and a plurality of pixels positioned at crossings of the data lines 18 and the gate lines 19. The pixels include a plurality of red (R) pixels, each of which includes a red organic light emitting diode (OLED) and displays red, a plurality of green (G) pixels, each of which includes a green OLED and displays green, a plurality of blue (B) pixels, each of which includes a

blue OLED and displays blue. Each gate line 19 includes a first scan line 191, a second scan line 192, and an emission line 193. Each pixel is connected to one data line 18 and the three signal lines 191, 192, and 193 constituting one gate line 19. Each pixel may receive the data voltage Vdata and a reference voltage Vref through the data line 18. Each pixel receives a first scan signal SCAN1 through the first scan line 191, receives a second scan signal SCAN2 through the second scan line 192, and receives an emission signal EM through the emission line 193. Each pixel may receive a high potential cell driving voltage VDD, a low potential cell driving voltage VSS, and an initialization voltage Vinit from a power generator (not shown).

[0028] Each pixel includes an OLED, a driving thin film transistor (TFT) DT, a first switching TFT ST1, a second switching TFT ST2, a third switching TFT ST3, a first capacitor C1, and a second capacitor C2.

[0029] The OLED emits light using a driving current supplied from the driving TFT DT. An organic compound layer having a multi-layered structure is formed between an anode electrode and a cathode electrode of the OLED as shown in FIG. 1. The anode electrode of the OLED is connected to a second node N2 of the driving TFT DT, and the cathode electrode of the OLED is connected to an input terminal of the low potential cell driving voltage VSS.

[0030] The driving TFT DT controls the driving current applied to the OLED using a gate-source voltage of the driving TFT DT. A gate electrode of the driving TFT DT is connected to a first node N1, a drain electrode of the driving TFT DT is connected to a source electrode of the third switching TFT ST3, and a source electrode of the driving TFT DT is connected to the second node N2.

[0031] The first switching TFT ST1 switches on a current path between the data line 18 and the first node N1 in response to the first scan signal SCAN1. The first switching TFT ST1 is turned on and thus supplies the reference voltage Vref and the data voltage Vdata, which are alternately applied to the data line 18, to the first node N1. A gate electrode of the first switching TFT ST1 is connected to the first scan line 191, a drain electrode of the first switching TFT ST1 is connected to the data line 18, and a source electrode of the first switching TFT ST1 is connected to the first node N1.

[0032] The second switching TFT ST2 switches on a current path between an input terminal of the initialization voltage Vinit and the second node N2 in response to the second scan signal SCAN2. The second switching TFT ST2 is turned on and thus supplies the initialization voltage Vinit to the second node N2. A gate electrode of the second switching TFT ST2 is connected to the second scan line 192, a drain electrode of the second switching TFT ST2 is connected to the input terminal of the initialization voltage Vinit, and a source electrode of the second switching TFT ST2 is connected to the second node N2.

[0033] The third switching TFT ST3 switches on a current path between an input terminal of the high potential cell driving voltage VDD and the drain electrode of the driving TFT DT in response to the emission signal EM. The third switching TFT ST3 is turned on and thus supplies the high potential cell driving voltage VDD to the drain electrode of the driving TFT DT. A gate electrode of the third switching TFT ST3 is connected to the emission line 193, a drain electrode of the third switching TFT ST3 is connected to the input terminal of the high potential cell driving voltage VDD, and a source electrode of the third switching TFT ST3 is connected to the drain electrode of the driving TFT DT.

[0034] The first capacitor C1 is connected between the first node N1 and the second node N2, and the second capacitor C2 is connected between the second node N2 and the input terminal of the initialization voltage Vinit.

[0035] The TFTs included in each pixel may be implemented as an oxide TFT including an oxide semiconductor layer. The oxide TFT is advantageous to the large-sized display panel when considering all of electron mobility, process deviation, etc. The embodiment of the invention is not limited thereto. The semiconductor layer of the TFT may be formed of amorphous silicon, polycrystalline silicon, etc. The embodiment of the invention describes an n-type TFT as an example of the TFT, but may use a p-type TFT.

[0036] The timing controller 11 rearranges digital video data RGB received from the outside in conformity with a resolution of the display panel 10 and supplies the rearranged digital video data RGB to the data driving circuit 12. The timing controller 11 generates a data control signal DDC for controlling operation timing of the data driving circuit 12 and a gate control signal GDC for controlling operation timing of the gate driving circuit 13 based on timing signals, such as a vertical sync signal Vsync, a horizontal sync signal Hsync, a dot clock DCLK, and a data enable signal DE.

[0037] The data driving circuit 12 converts the digital video data RGB received from the timing controller 11 into an analog signal based on the data control signal DDC and generates the data voltage Vdata. The data driving circuit 12 generates the reference voltage Vref of a constant level. The data driving circuit 12 alternately outputs the reference voltage Vref and the data voltage Vdata in one horizontal period 1H as indicated by driving timings shown in FIGS. 7, 10, 12, 14, and 16. The data driving circuit 12 has output channels, of which the number is less than the number of data lines 18 of the display panel 10. The data driving circuit 12 simultaneously outputs the reference voltage Vref through all of the output channels during a portion of one horizontal period 1H and simultaneously outputs the data voltage Vdata through all of the output channels during the remaining period of the one horizontal period 1H. In the embodiment disclosed herein, one horizontal period 1H is defined as a value obtained by dividing one frame period by a vertical resolution of the display panel.

[0038] The gate driving circuit 13 generates the gate signal, namely the first and second scan signals SCAN1

and SCAN2 and the emission signal EM based on the gate control signal GDC. The gate driving circuit 13 supplies the first scan signal SCAN1 to the first scan lines 191 while shifting a phase of the first scan signal SCAN1 in a line sequential manner and supplies the second scan signal SCAN2 to the second scan lines 192 while shifting a phase of the second scan signal SCAN2 in the line sequential manner. In the same manner as the first and second scan signals SCAN1 and SCAN2, the gate driving circuit 13 supplies the emission signal EM to the emission lines 193 while shifting a phase of the emission signal EM in the line sequential manner. The first scan signal SCAN1 may be implemented as a single waveform having one on-level period in one frame period as shown in FIGS. 10, 12, 14, and 16, or may be implemented as a double waveform having two on-level periods in one frame period as shown in FIG. 7. The second scan signal SCAN2 may be implemented as a single waveform in one frame period, and the emission signal EM may be implemented as a double waveform in one frame period. The gate driving circuit 13 may be directly formed on the display panel 10 through a gate driver-in panel (GIP) process.

[0039] The demux switching circuit 15 is connected to the data driving circuit 12 through source bus lines 17 and also is connected to the pixels through the data lines 18. The demux switching circuit 15 may time-division supply the data voltage Vdata received from one output channel of the data driving circuit 12 to N data lines 18 of the display panel 10, or may time-division supply the reference voltage Vref received from one output channel of the data driving circuit 12 to the N data lines 18 of the display panel 10. For this, the demux switching circuit 15 may include first to Nth demux switches connected to each output channel of the data driving circuit 12, where N is a positive integer equal to or greater than 2. The first to Nth demux switches are turned on in response to first to Nth demux control signals, respectively. The demux switching circuit 15 may further include first to Nth auxiliary switches for switching on only the supply of the reference voltage Vref as shown in FIGS. 6 and 11. The first to Nth demux switches may be designed to switch on only the supply of the data voltage Vdata. The first to Nth auxiliary switches are simultaneously turned on in response to an auxiliary control signal.

[0040] The control signal generator 16 generates the demux switching control signal DCTR. The demux switching control signal DCTR includes the first to Nth demux control signals and the auxiliary control signal. The control signal generator 16 may be mounted inside the timing controller 11.

[0041] In the following description, the invention describes various embodiments about the design of the demux switching circuit and the demux switching control signal, so that the pixels displaying the same color have the same number of times of influence of a kickback voltage in a demux driving method.

[First embodiment]

[0042] An organic light emitting display according to a first embodiment of the invention includes a demux switching circuit for 1 to N demux drive, so that pixels displaying the same color have the same number of times of influence of a kickback voltage in a demux driving method. Further, the organic light emitting display according to the first embodiment of the invention designs first to Nth demux control signals, which sequentially rise to an on-level and then sequentially fall to an off-level in a programming period, in which a first scan signal is held at an on-level, so as to apply a data voltage to pixels.

[0043] FIG. 6 shows an example of the demux switching circuit for 1 to 2 demux drive in the organic light emitting display according to the first embodiment of the invention. FIG. 7 shows driving timing of the pixel shown in FIG. 5 and the demux switching circuit shown in FIG. 6. FIGS. 8A to 8D show an operation state of a pixel in each of driving stages.

[0044] The demux switching circuit 15 shown in FIG. 6 includes first demux switches S11, S21, and S31 and second demux switches S12, S22, and S32, which are connected to each of output channels CH1, CH2, and CH3 of the data driving circuit. The demux switching circuit 15 divides a signal received from the data driving circuit using 1 to 2 demultiplexing method and outputs the divided signals to data lines D1 to D6. Because the 1 to 2 demux drive is applied to pixels displaying three colors, pixels of the same color are selectively connected to the first demux switches S11, S21, and S31 simultaneously operating in response to a first demux control signal DMUX1 and the second demux switches S12, S22, and S32 simultaneously operating in response to a second demux control signal DMUX2. For example, a B pixel is connected to the first demux switch S11 through the first data line D1, and another B pixel is connected to the second demux switch S22 through the fourth data line D4. Further, a G pixel is connected to the second demux switch S12 through the second data line D2, and another G pixel is connected to the first demux switch S31 through the fifth data line D5. Further, an R pixel is connected to the first demux switch S21 through the third data line D3, and another R pixel is connected to the second demux switch S32 through the sixth data line D6.

[0045] If a current deviation is generated between the pixels of the same color in the 1 to 2 demux drive, the current deviation may become a problem as described in a related art. To solve the problem, as shown in FIG. 7, the embodiment of the invention designs the first and second demux control signals DMUX1 and DMUX2, so that they sequentially rise to an on-level and then sequentially fall to an off-level in a programming period P3. Hence, pixels connected to the first demux switches S11, S21, and S31 and pixels connected to the second demux switches S12, S22, and S32 have the same number of times of influence of the kickback voltage. In other words, the first scan signal SCAN1 falls to the off-level for an

emission period P4 following the programming period P3, and both the first and second demux control signals DMUX1 and DMUX2 fall earlier than the first scan signal SCAN1.

[0046] Accordingly, each pixel irrespective of the color is affected by the kickback voltage once at a time when the demux switch connected to the pixel is turned off in response to one of the first and second demux control signals DMUX1 and DMUX2, and is again affected by the kickback voltage at a time when the first switching TFT ST1 of the pixel is turned off in response to the first scan signal SCAN1. Namely, because each pixel is affected by the kickback voltage twice irrespective of the color of the pixel, the embodiment of the invention prevents the current deviation from being generated by a difference between the number of times of influence of the kickback voltage.

[0047] To drive the pixels disposed on one horizontal pixel line, an initialization period P1 for initializing the pixels may be assigned before the programming period P3, and a sensing period P2 for sensing threshold voltages of the driving TFTs DT included in the pixels may be assigned between the initialization period P1 and the programming period P3. The initialization period P1 may be selected as one horizontal period 1H, and a sum of a length of the sensing period P2 and a length of the programming period P3 may be selected as one horizontal period 1H. The initialization period P1 of the pixels disposed on an Nth horizontal pixel line may overlap the sensing period P2 and the programming period P3 of the pixels disposed on an (N-1)th horizontal pixel line, so as to secure a margin of the driving timing.

[0048] The reference voltage Vref and the data voltage are alternately input to the demux switching circuit 15 on a per horizontal period (1H) basis. The reference voltage Vref is input in the initialization period P1 and the sensing period P2, and the requirable data voltage is input in the programming period P3. The demux switching circuit 15 may further include first auxiliary switches R11, R21, and R31 respectively connected in parallel to the first demux switches S11, S21, and S31 and second auxiliary switches R12, R22, and R32 respectively connected in parallel to the second demux switches S12, S22, and S32, so as to time-divide the supply timings of the reference voltage Vref and the data voltage. The first and second auxiliary switches are simultaneously turned on in the initialization period P1 and the sensing period P2 in response to an auxiliary control signal RCTR supplied from the control signal generator 16 and may supply the reference voltage Vref to all of the data lines D1 to D6. The first demux switches S11, S21, and S31 are turned on in response to the first demux control signal DMUX1 and supplies a data voltage Vdata1 to some data lines D1, D3, and D5 in the programming period P3. The second demux switches S12, S22, and S32 are turned on in response to the second demux control signal DMUX2 and supplies a data voltage Vdata2 to some data lines D2, D4, and D6 in the programming period P3.

[0049] The first scan signal SCAN1 is implemented as a double waveform having two on-level periods and may have an on-level Lon in a portion of the initialization period P1, the sensing period P2, and the programming period P3. The second scan signal SCAN2 is implemented as a single waveform having one on-level period and may have the on-level Lon in synchronization with the first scan signal SCAN1 in a portion of the initialization period P1. The emission signal EM is implemented as a double waveform having two on-level periods and may have the on-level Lon in the sensing period P2 and the emission period P4. The auxiliary control signal RCTR may have the on-level Lon in synchronization with the supply timing of the reference voltage Vref.

[0050] An operation state of a pixel in each of driving stages is described with reference to FIGS. 8A to 8D.

[0051] In the initialization period P1 shown in FIG. 8A, the first and second switching TFTs ST1 and ST2 are turned on. Hence, the first node N1 is initialized to the reference voltage Vref, and the second node N2 is initialized to the initialization voltage Vinit. In the sensing period P2 shown in FIG. 8B, the first and third switching TFTs ST1 and ST3 are turned on. Hence, a potential of the second node N2 is sampled to a voltage (Vref-Vth), where 'Vth' is a threshold voltage of the driving TFT DT. In the initialization period P1 and the sensing period P2, the data line is charged to the reference voltage Vref by a turn-on operation of the auxiliary switch.

[0052] In the programming period P3 shown in FIG. 8C, the first switching TFT ST1 is turned on, and thus the data voltage Vdata is applied to the first node N1. In this instance, the potential of the second node N2 is changed to a voltage (Vref-Vth+C'(Vdata-Vref)) because of capacitance coupling resulting from a capacitance distribution ratio (C'=C1/(C1+C2+Coled)) of the first and second capacitors C1 and C2. In particular, in the programming period P3, first and second demux switches alternately operate, and the data voltage is charged to each data line. According to the embodiment of the invention, because all of the pixels have the same number of times of influence of the kickback voltage irrespective of operation order of the first and second demux switches, the current deviation between the pixels is not generated.

[0053] In the emission period P4 shown in FIG. 8D, the third switching TFT ST3 is turned on, and the high potential cell driving voltage VDD is supplied to the pixel. Hence, the OLED is turned on and emits light during one frame period. In the emission period P4, a driving current Ioled flowing in the OLED is calculated as k(Vdata-Vref-C'(Vdata-Vref))2. According to the above equation, a deviation between the threshold voltages Vth of the pixels and a deviation between the high potential cell driving voltages VDD of the pixels are compensated. In the above equation, 'k' is a constant value determined by a current mobility, a parasitic capacitance, and a channel capacitance, etc. of the driving TFT DT.

[0054] FIG. 9 shows another example of the demux switching circuit for the 1 to 2 demux drive in the organic

light emitting display according to the first embodiment of the invention. FIG. 10 shows driving timing of the pixel shown in FIG. 5 and the demux switching circuit shown in FIG. 9.

[0055] The demux switching circuit 15 shown in FIG. 9 includes first demux switches S11, S21, and S31 and second demux switches S12, S22, and S32 connected to each of output channels CH1, CH2, and CH3 of the data driving circuit. The demux switching circuit 15 divides a signal received from the data driving circuit using 1 to 2 demultiplexing method and outputs the divided signals to data lines D1 to D6. Because the 1 to 2 demux drive is applied to pixels of three colors, pixels of the same color are selectively connected to the first demux switches S11, S21, and S31 simultaneously operating in response to the first demux control signal DMUX1 and the second demux switches S12, S22, and S32 simultaneously operating in response to the second demux control signal DMUX2.

[0056] The demux switching circuit 15 shown in FIG. 9 is different from the demux switching circuit 15 shown in FIG. 6 in that it does not include separate auxiliary switches. Further, the demux switching circuit 15 shown in FIG. 9 is characterized in that the first and second demux control signals DMUX1 and DMUX2 are designed as shown in FIG. 10 so that the reference voltage Vref and the data voltage are time-division supplied through demux switches. More specifically, the first and second demux control signals DMUX1 and DMUX2 shown in FIG. 10 are different from those shown in FIG. 7 in that they are held at the on-level Lon in the initialization period P1 and the sensing period P2. The first and second demux switches S11, S21, S31, S12, S22, and S32 are simultaneously turned on in response to the first and second demux control signals DMUX1 and DMUX2, which are synchronized with each other at the on-level Lon in the initialization period P1 and the sensing period P2, and thus supply the reference voltage Vref to the data lines D1 to D6.

[0057] As shown in FIG. 10, the initialization periods P1, the sensing periods P2, and the programming periods P3 of the adjacent horizontal pixel lines do not overlap each other unlike FIG. 7 and are independent. In FIG. 10, a sum of lengths of the initialization period P1, the sensing period P2, and the programming period P3 may be selected as one horizontal period. The first scan signal SCAN1 may be implemented as a single waveform having the on-level Lon in the initialization period P1, the sensing period P2, and the programming period P3.

[0058] The embodiment of the invention shown in FIGS. 9 and 10 has substantially the same operation effect as the embodiment of the invention shown in FIGS. 6 and 7. The embodiment of the invention shown in FIGS. 9 and 10 is characterized in that the pixels connected to the first demux switches S11, S21, and S31 and the pixels connected to the second demux switches S12, S22, and S32 have the same number of times of influence of the kickback voltage by designing the first and second demux control signals DMUX1 and DMUX2 so that they sequentially rise to the on-level Lon and then sequentially fall to an off-level Loff in the programming period P3 in the same manner as FIG. 7. In other words, the first scan signal SCAN1 falls to the off-level Loff for an emission period P4 following the programming period P3, and both the first and second demux control signals DMUX1 and DMUX2 fall earlier than the first scan signal SCAN1.

[0059] Accordingly, each pixel irrespective of the color is affected by the kickback voltage once at a time when the demux switch connected to the pixel is turned off in response to one of the first and second demux control signals DMUX1 and DMUX2, and is again affected by the kickback voltage at a time when the first switching TFT ST1 of the pixel is turned off in response to the first scan signal SCAN1. Namely, because each pixel is affected by the kickback voltage twice irrespective of the color of the pixel, the embodiment of the invention prevents the current deviation from being generated by a difference between the number of times of influence of the kickback voltage.

[0060] FIG. 11 shows an example of the demux switching circuit for 1 to 3 demux drive in the organic light emitting display according to the first embodiment of the invention. FIG. 12 shows driving timing of the pixel shown in FIG. 5 and the demux switching circuit shown in FIG. 11.

[0061] The demux switching circuit 15 shown in FIG. 11 includes a first demux switch (for example, S11), a second demux switch (for example, S12), and a third demux switch (for example, S13) connected to an output channel (for example, CH1) of the data driving circuit. The demux switching circuit 15 divides a signal received from the data driving circuit using 1 to 3 demultiplexing method and outputs the divided signals to data lines D1, D2, and D3. Because the 1 to 3 demux drive is applied to pixels of three colors, first pixels displaying a first color may be connected to the first demux switches (for example, S11, etc.) simultaneously operating in response to a first demux control signal DMUX1, and second pixels displaying a second color may be connected to the second demux switches (for example, S12, etc.) simultaneously operating in response to a second demux control signal DMUX2. Further, third pixels displaying a third color may be connected to the third demux switches (for example, S13, etc.) simultaneously operating in response to a third demux control signal DMUX3.

[0062] Because the pixels of the same color correspond to one demux switch in the 1 to 3 demux drive, the current deviation between the pixels of the same color is not generated without intentionally modulating the first to third demux control signals DMUX1 to DMUX3 as shown in FIG. 12. However, when the first to third demux control signals DMUX1 to DMUX3 are designed as shown in FIG. 12, a current deviation between the pixels of different colors may be previously prevented. The current deviation between the pixels of different colors is not conspicuously visible as a longitudinal dim. However, the

image quality of the organic light emitting display may be further improved by previously preventing the current deviation between the pixels of different colors.

[0063] As shown in FIGS. 11 and 12, the embodiment of the invention is characterized in that the pixels connected to the first to third demux switches S11, S12, and S13 have the same number of times of influence of the kickback voltage by designing the first to third demux control signals DMUX1 to DMUX3 so that they sequentially rise to the on-level Lon and then sequentially fall to the off-level Loff in the programming period P3. In other words, the first scan signal SCAN1 falls to the off-level Loff for the emission period P4 following the programming period P3, and all of the first to third demux control signals DMUX1 to DMUX3 fall earlier than the first scan signal SCAN1. The first scan signal SCAN1 may be implemented as a single waveform having the on-level Lon in the initialization period P1, the sensing period P2, and the programming period P3.

[0064] Accordingly, each pixel irrespective of the color is affected by the kickback voltage once at a time when the demux switch connected to the pixel is turned off in response to the demux control signal, and is again affected by the kickback voltage at a time when the first switching TFT ST1 of the pixel is turned off in response to the first scan signal SCAN1. Namely, because each pixel is affected by the kickback voltage twice irrespective of the color of the pixel, the embodiment of the invention prevents the current deviation from being generated by a difference between the number of times of influence of the kickback voltage.

[0065] In FIG. 12, a sum of lengths of the initialization period P1, the sensing period P2, and the programming period P3 may be selected as one horizontal period. The reference voltage Vref and the data voltage are alternately input to the demux switching circuit 15 on a per horizontal period (1H) basis. The reference voltage Vref is input in the initialization period P1 and the sensing period P2, and the data voltage is input in the programming period P3. The demux switching circuit 15 may further include a first auxiliary switch R11 connected in parallel to the first demux switch S11, a second auxiliary switch R12 connected in parallel to the second demux switch S12, and a third auxiliary switch R13 connected in parallel to the third demux switch S13, so as to time-divide the supply timings of the reference voltage Vref and the data voltage. The first to third auxiliary switches R11, R12, and R13 are simultaneously turned on in the initialization period P1 and the sensing period P2 in response to an auxiliary control signal RCTR supplied from the control signal generator 16 and may supply the reference voltage Vref to all of the data lines D1 to D3. The first demux switch S11 is turned on in response to the first demux control signal DMUX1 and supplies a data voltage Vdata1 to some data line D1 in the programming period P3. The second demux switch S12 is turned on in response to the second demux control signal DMUX2 and supplies a data voltage Vdata2 to some data line D2 in the programming period P3. The third demux switch S13 is turned on in response to the third demux control signal DMUX3 and supplies a data voltage Vdata3 to some data line D3 in the programming period P3.

[0066] FIG. 13 shows another example of the demux switching circuit for the 1 to 3 demux drive in the organic light emitting display according to the first embodiment of the invention. FIG. 14 shows driving timing of the pixel shown in FIG. 5 and the demux switching circuit shown in FIG. 13.

[0067] The demux switching circuit 15 shown in FIG. 13 is different from the demux switching circuit 15 shown in FIG. 11 in that it does not include separate auxiliary switches. Further, the demux switching circuit 15 shown in FIG. 13 is characterized in that the first to third demux control signals DMUX1 to DMUX3 are designed as shown in FIG. 14 so that the reference voltage Vref and the data voltage are time-division supplied through demux switches. More specifically, the first to third demux control signals DMUX1 to DMUX3 shown in FIG. 14 are different from those shown in FIG. 12 in that they are held at the on-level Lon in the initialization period P1 and the sensing period P2. The first to third demux switches S11, S12, and S13 are simultaneously turned on in response to the first to third demux control signals DMUX1 to DMUX3, which are synchronized with each other at the on-level Lon in the initialization period P1 and the sensing period P2, and thus supply the reference voltage Vref to the data lines D1 to D3.

[0068] The embodiment of the invention shown in FIGS. 13 and 14 has substantially the same operation effect as the embodiment of the invention shown in FIGS. 11 and 12.

[0069] As described above, the embodiment of the invention designs the demux switching circuit and the demux switching control signal so that the pixels displaying the same color have the same number of times of influence of the kickback voltage in the demux driving method, thereby preventing the generation of the unwanted current deviation between the pixels of the same color.

[0070] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Claims

1. An organic light emitting display comprising:

a display panel including first pixels displaying a first color, second pixels displaying a second color, and third pixels displaying a third color;
a data driving circuit configured to generate a data voltage;
a demultiplexer (demux) switching circuit including first to Nth demux switches connected to each output channel of the data driving circuit, where N is a positive integer equal to or greater than 2, the demux switching circuit configured to time-division supply the data voltage received from one output channel of the data driving circuit to N data lines of the display panel; and
a control signal generator configured to generate first to Nth demux control signals for controlling operations of the first to Nth demux switches,
wherein the first to Nth demux control signals sequentially rise to an on-level and then sequentially fall to an off-level in a programming period, in which a first scan signal used to apply the data voltage to the pixels is held at the on-level.

2. The organic light emitting display of claim 1, wherein the first scan signal falls to the off-level for an emission period following the programming period,
wherein all of the first to Nth demux control signals fall earlier than the first scan signal.

3. The organic light emitting display of claim 1 or 2, wherein N is 2,
wherein pixels, on one horizontal pixel line, displaying the same color are selectively connected to first demux switches simultaneously operating in response to a first demux control signal and second demux switches simultaneously operating in response to a second demux control signal.

4. The organic light emitting display of claim 3, wherein an initialization period, which is arranged prior to the programming period and initializes the first to third pixels, and a sensing period, which is arranged between the initialization period and the programming period and senses threshold voltages of driving elements included in the first to third pixels, are assigned so as to drive pixels disposed on one horizontal pixel line,
wherein the initialization period is selected as one horizontal period, which is defined as a value obtained by dividing one frame period by a vertical resolution of the display panel, and a sum of lengths of the sensing period and the programming period is selected as one horizontal period,
wherein the initialization period of pixels disposed on an Nth horizontal pixel line overlaps the sensing period and the programming period of pixels disposed on an (N-1)th horizontal pixel line.

5. The organic light emitting display of claim 4, wherein the data driving circuit further generates a reference voltage required in the initialization period and the sensing period and supplies the reference voltage to the demux switching circuit,
wherein the demux switching circuit further includes first auxiliary switches respectively connected in parallel to the first demux switches and second auxiliary switches respectively connected in parallel to the second demux switches,
wherein the first and second auxiliary switches are simultaneously turned on in response to an auxiliary control signal, which is held at the on-level in the initialization period and the sensing period.

6. The organic light emitting display of claim 3, wherein an initialization period, which is arranged prior to the programming period and initializes the first to third pixels, and a sensing period, which is arranged between the initialization period and the programming period and senses threshold voltages of driving elements included in the first to third pixels, are assigned so as to drive pixels disposed on one horizontal pixel line,
wherein a sum of lengths of the initialization period, the sensing period, and the programming period is selected as one horizontal period, which is defined as a value obtained by dividing one frame period by a vertical resolution of the display panel.

7. The organic light emitting display of claim 4 or 6, wherein the data driving circuit further generates a reference voltage required in the initialization period and the sensing period and supplies the reference voltage to the demux switching circuit,
wherein the first and second demux switches are simultaneously turned on in response to the first and second demux control signals, which are synchronized with each other at the on-level in the initialization period and the sensing period.

8. The organic light emitting display of claim 1 or 2, wherein N is 3,
wherein the first pixels displaying the first color are connected to first demux switches simultaneously operating in response to a first demux control signal,
wherein the second pixels displaying the second color are connected to second demux switches simultaneously operating in response to a second demux control signal,
wherein the third pixels displaying the third color are connected to third demux switches simultaneously operating in response to a third demux control signal.

9. The organic light emitting display of claim 8, wherein an initialization period, which is arranged prior to the programming period and initializes the first to third pixels, and a sensing period, which is arranged be-

tween the initialization period and the programming period and senses threshold voltages of driving elements included in the first to third pixels, are assigned so as to drive pixels disposed on one horizontal pixel line,
wherein a sum of lengths of the initialization period, the sensing period, and the programming period is selected as one horizontal period, which is defined as a value obtained by dividing one frame period by a vertical resolution of the display panel.

10. The organic light emitting display of claim 9, wherein the data driving circuit further generates a reference voltage required in the initialization period and the sensing period and supplies the reference voltage to the demux switching circuit,
wherein the demux switching circuit further includes first auxiliary switches respectively connected in parallel to the first demux switches, second auxiliary switches respectively connected in parallel to the second demux switches, and third auxiliary switches respectively connected in parallel to the third demux switches,
wherein the first to third auxiliary switches are simultaneously turned on in response to an auxiliary control signal, which is held at the on-level in the initialization period and the sensing period.

11. The organic light emitting display of claim 9 or 10, wherein the data driving circuit further generates a reference voltage required in the initialization period and the sensing period and supplies the reference voltage to the demux switching circuit,
wherein the first to third demux switches are simultaneously turned on in response to the first to third demux control signals, which are synchronized with each other at the on-level in the initialization period and the sensing period.

FIG. 1

(RELATED ART)

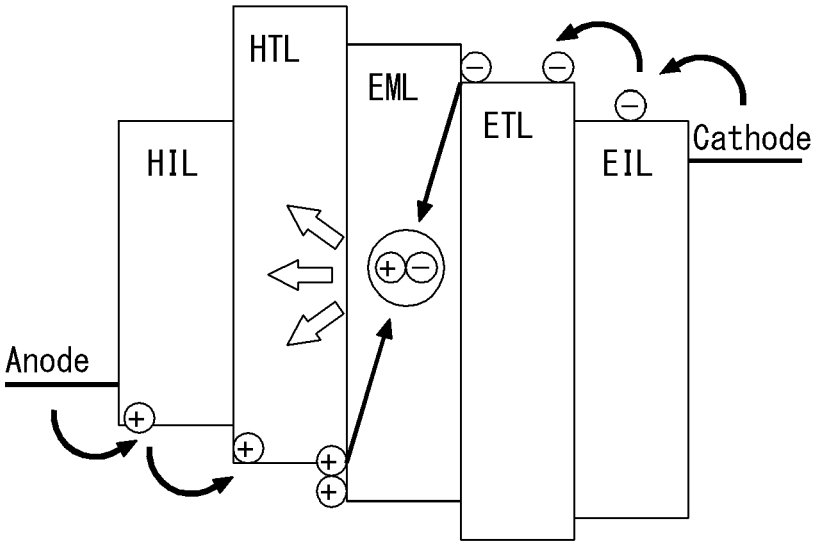


FIG. 2

(RELATED ART)

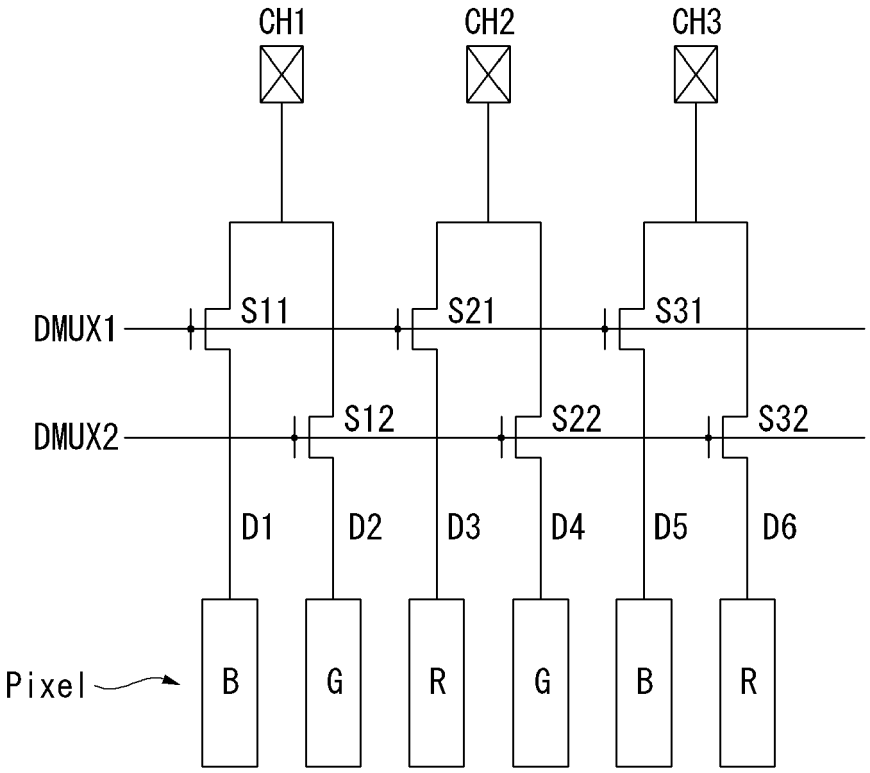


FIG. 3

(RELATED ART)

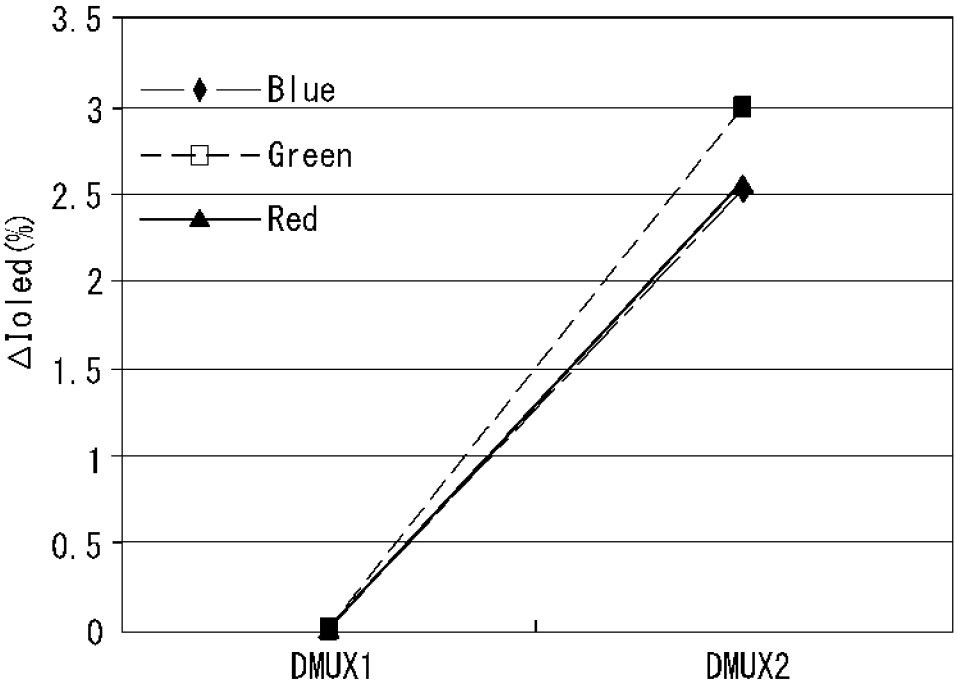


FIG. 4

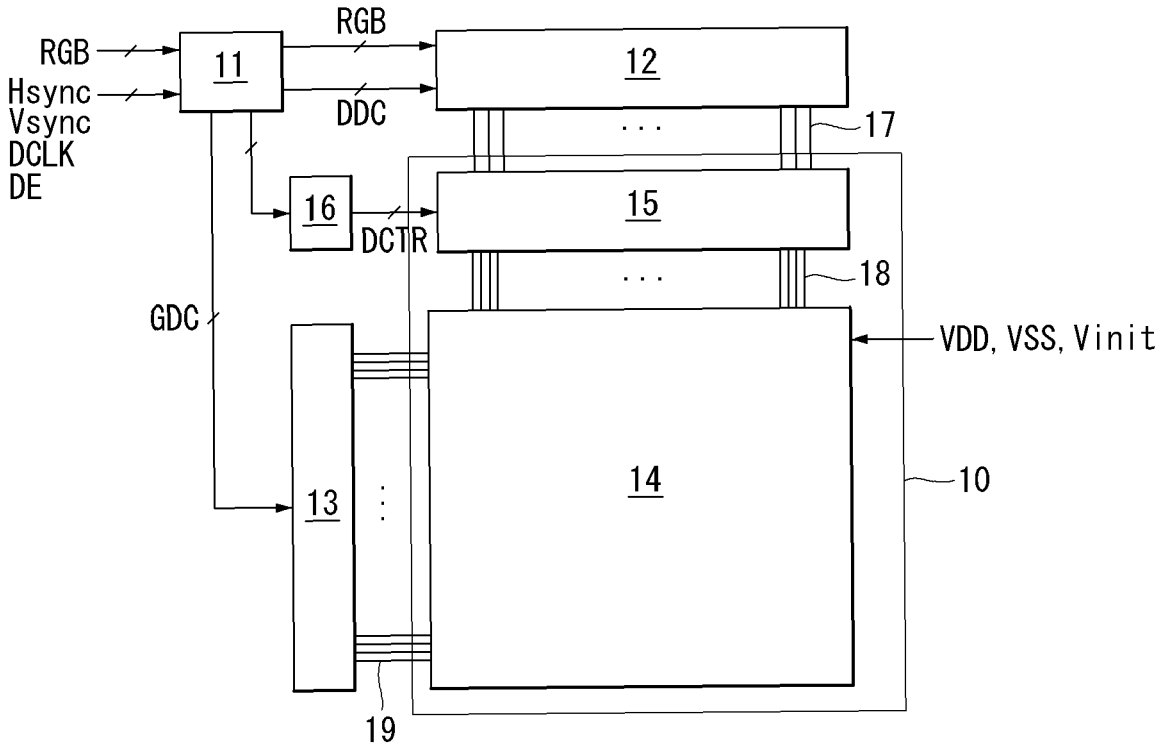

RGB
Hsync
Vsync
DCLK
DE
11
RGB
DDC
12
17
16
DCTR
15
18
GDC
VDD, VSS, Vinit
13
14
10
19

FIG. 5

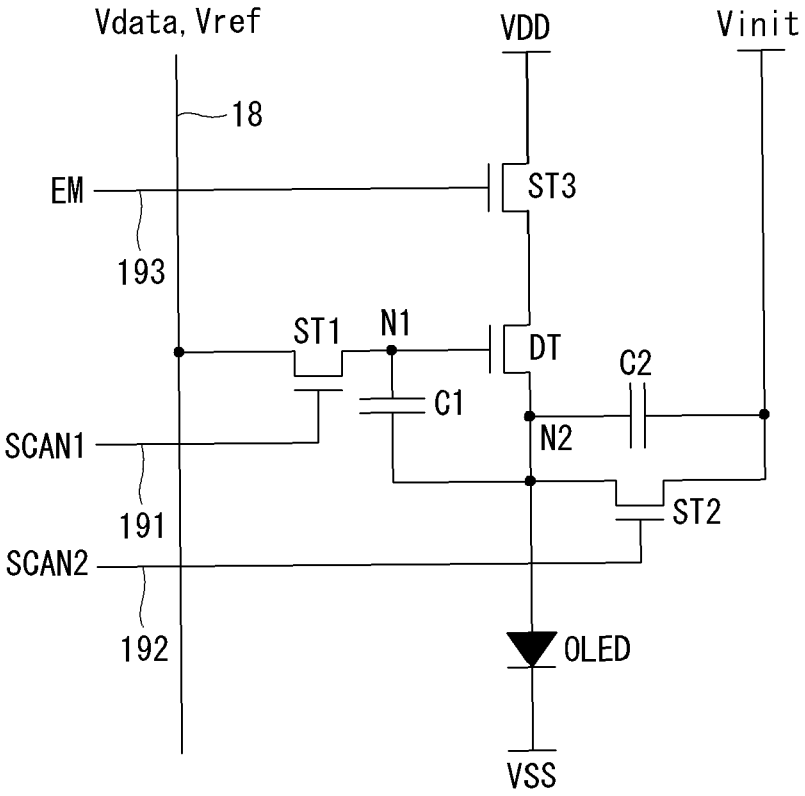

Vdata, Vref
VDD
Vinit
18
EM
ST3
193
ST1
N1
DT
C2
C1
SCAN1
N2
ST2
191
SCAN2
192
OLED
VSS

FIG. 6

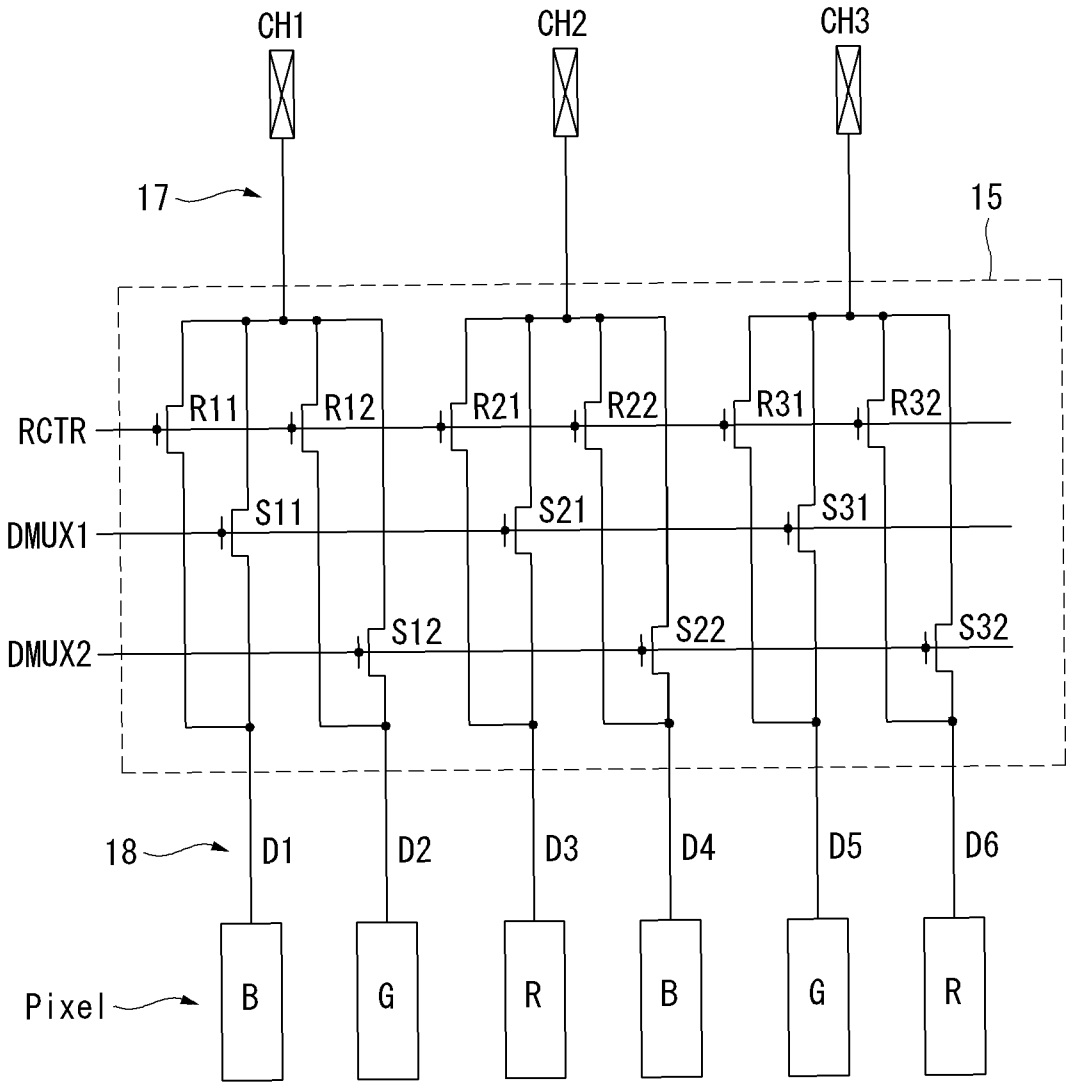

CH1
CH2
CH3
17
15
RCTR
DMUX1
DMUX2
R11
R12
R21
R22
R31
R32
S11
S21
S31
S12
S22
S32
18
D1
D2
D3
D4
D5
D6
Pixel
B
G
R
B
G
R

FIG. 7

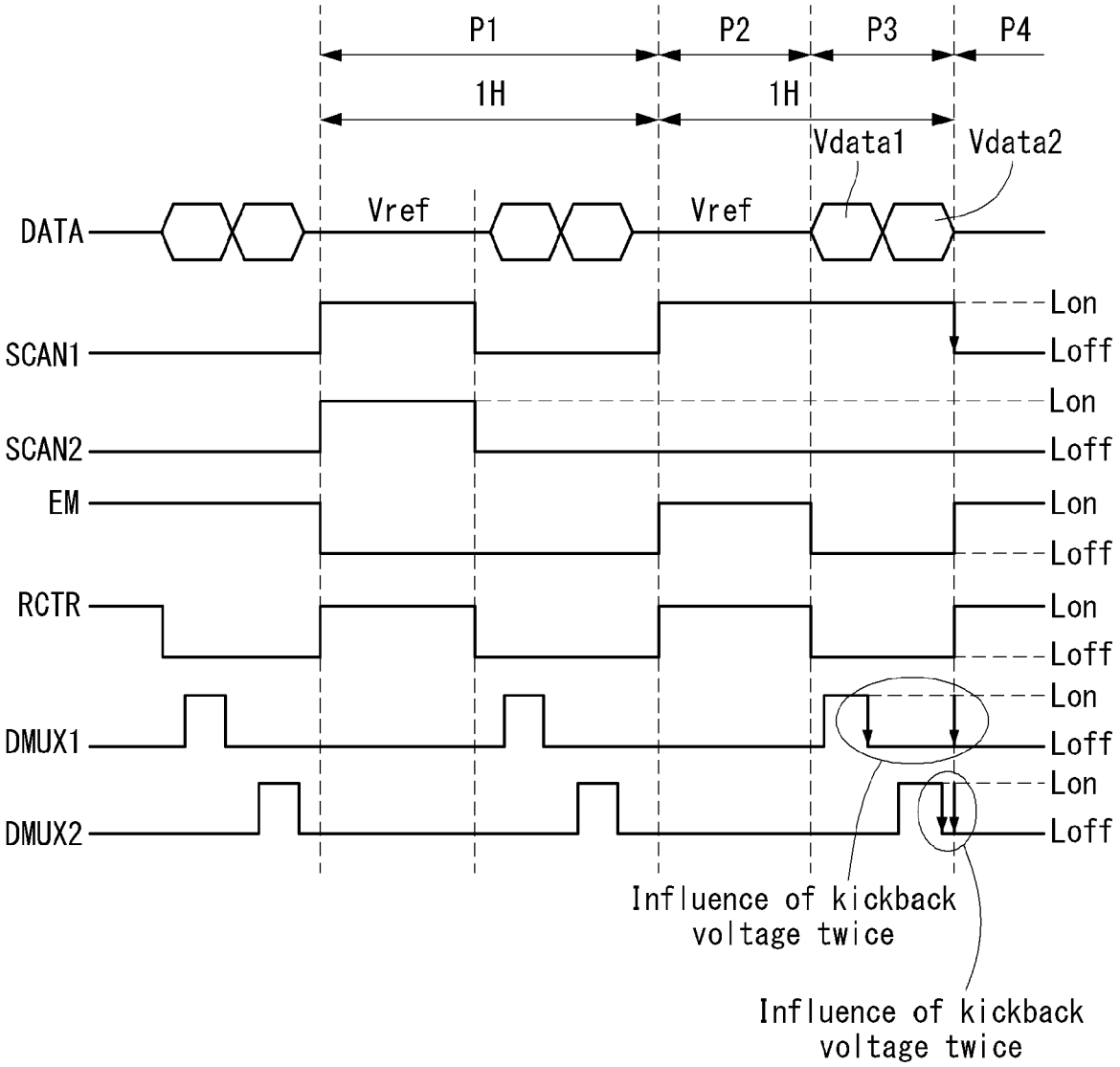

P1
P2
P3
P4
1H
1H
Vdata1
Vdata2
DATA
Vref
Vref
SCAN1
SCAN2
EM
RCTR
DMUX1
DMUX2
Lon
Loff
Lon
Loff
Lon
Loff
Lon
Loff
Lon
Loff
Lon
Loff
Influence of kickback voltage twice
Influence of kickback voltage twice

FIG. 8A

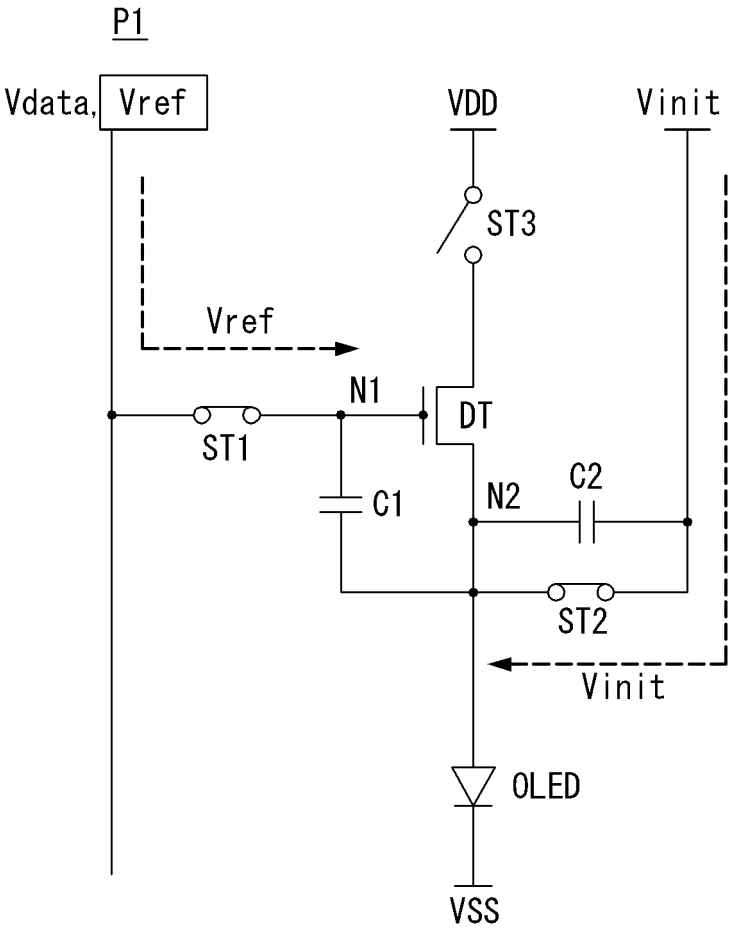

P1
Vdata,
Vref
VDD
Vinit
ST3
Vref
N1
DT
ST1
C1
N2
C2
ST2
Vinit
OLED
VSS

FIG. 8B

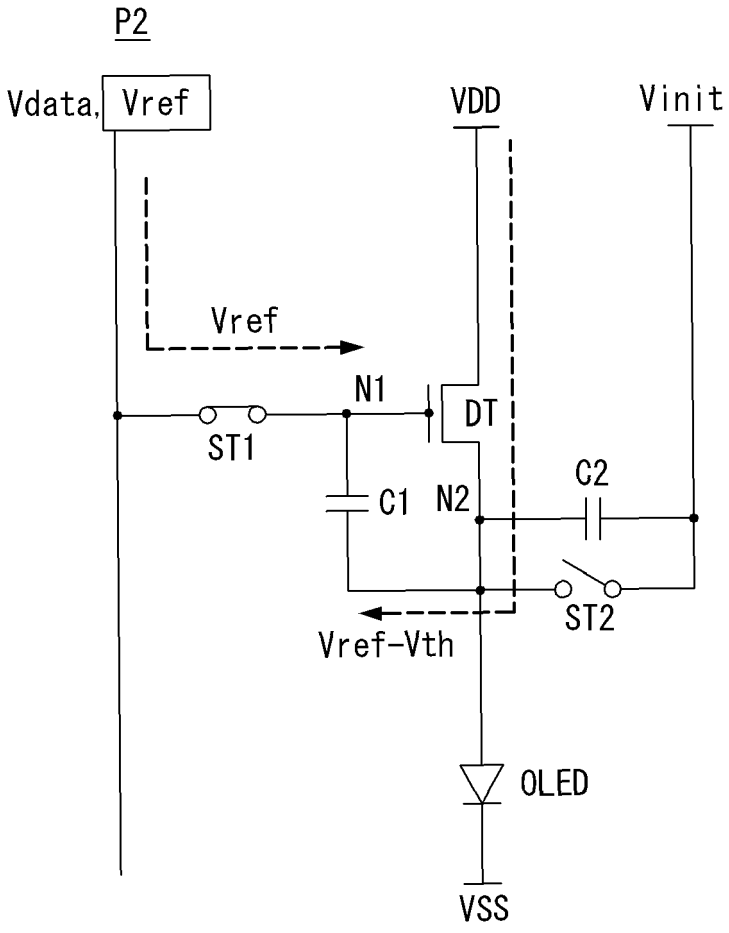

P2
Vdata,
Vref
VDD
Vinit
Vref
N1
DT
ST1
C1
N2
C2
ST2
Vref-Vth
OLED
VSS

FIG. 8C

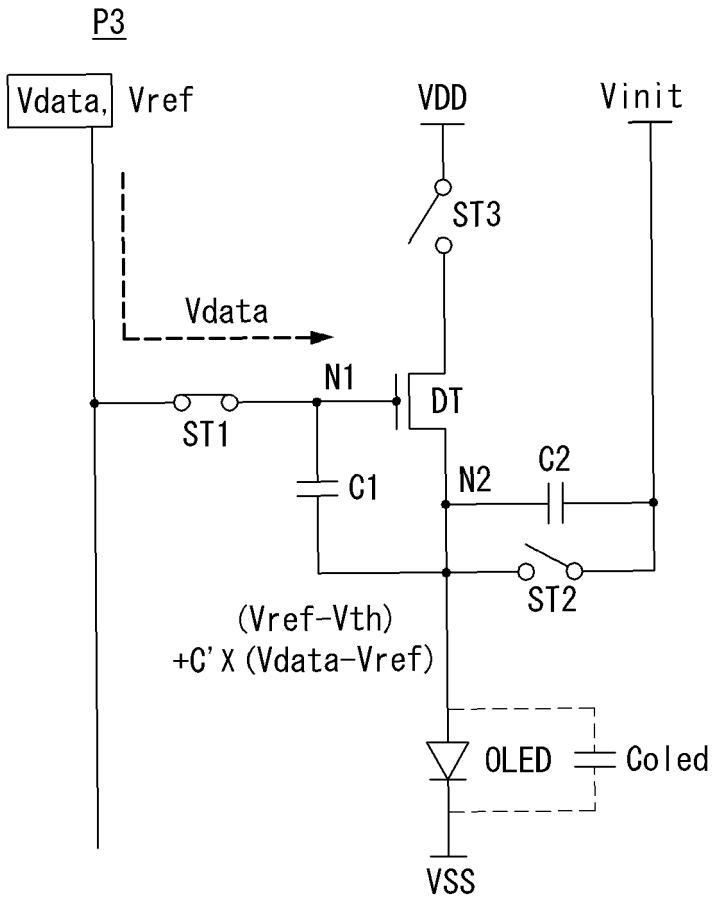

P3
Vdata, Vref
VDD
Vinit
ST3
Vdata
N1
DT
ST1
C1
N2
C2
ST2
(Vref-Vth)
+C'X(Vdata-Vref)
OLED
Coled
VSS

FIG. 8D

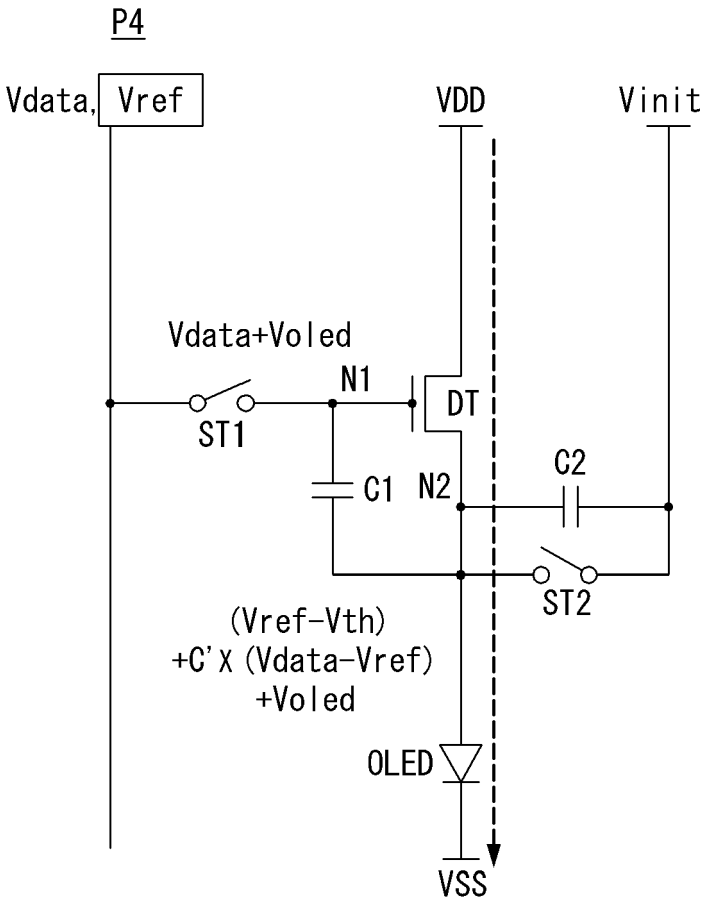

P4
Vdata,
Vref
VDD
Vinit
Vdata+Voled
N1
DT
ST1
C1
N2
C2
ST2
(Vref-Vth)
+C'X (Vdata-Vref)
+Voled
OLED
VSS

FIG. 9

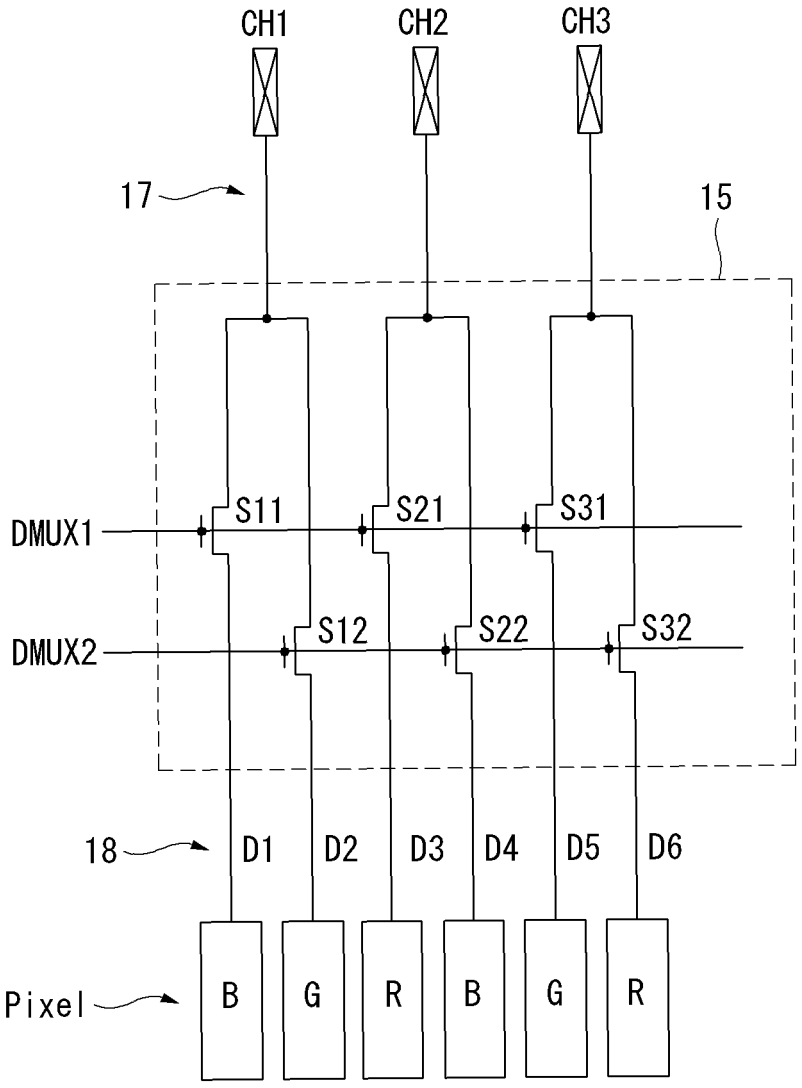

CH1
CH2
CH3
17
15
DMUX1
DMUX2
S11
S21
S31
S12
S22
S32
18
D1
D2
D3
D4
D5
D6
Pixel
B
G
R
B
G
R

FIG. 10

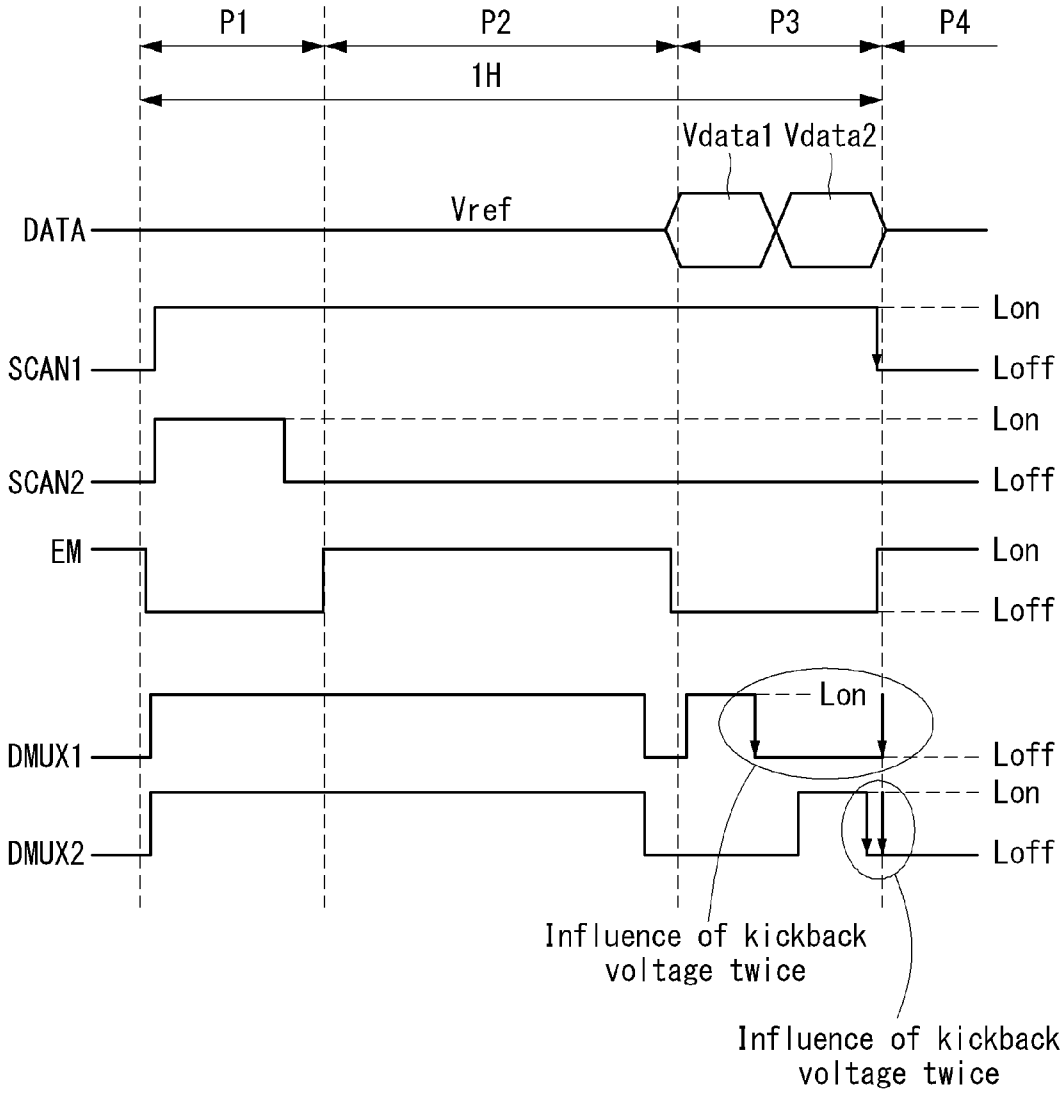

P1
P2
P3
P4
1H
Vdata1 Vdata2
Vref
DATA
Lon
Loff
SCAN1
Lon
Loff
SCAN2
Lon
Loff
EM
Lon
Loff
DMUX1
Lon
Loff
DMUX2
Influence of kickback voltage twice
Influence of kickback voltage twice

FIG. 11

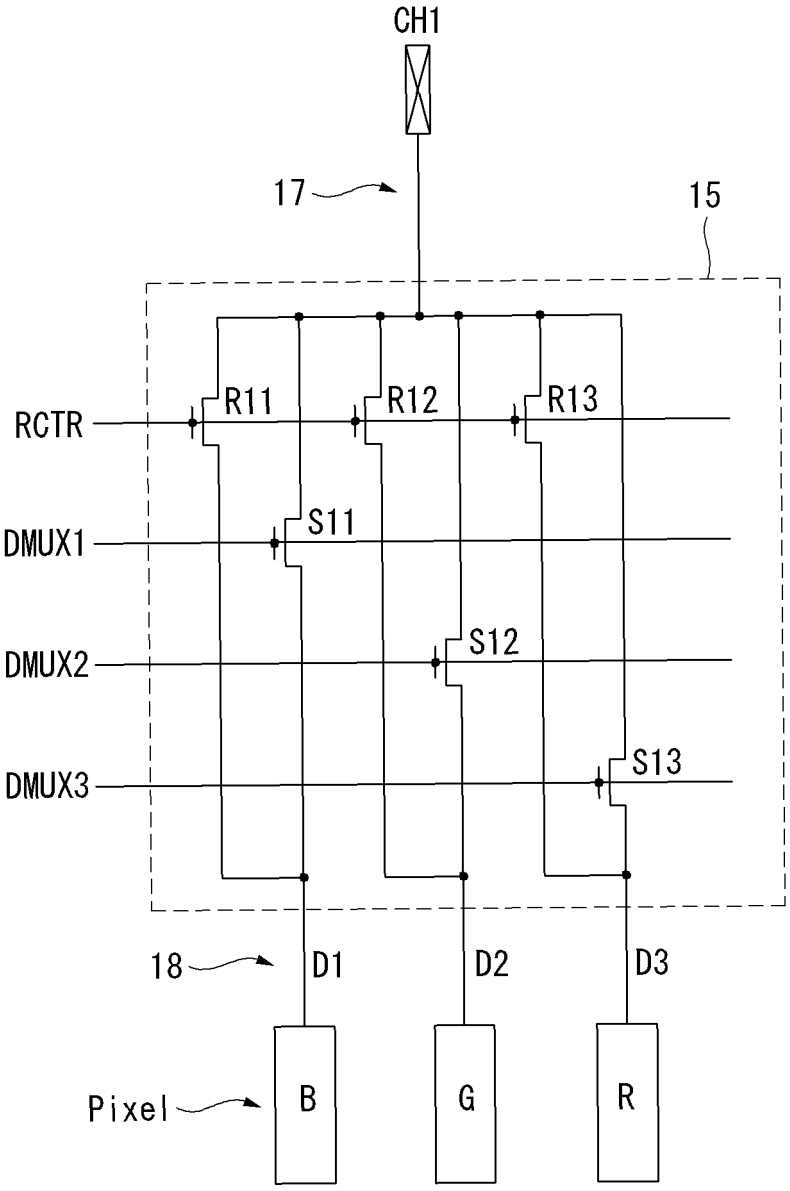

CH1
17
15
R11
R12
R13
RCTR
DMUX1
S11
DMUX2
S12
DMUX3
S13
18
D1
D2
D3
Pixel
B
G
R

FIG. 12

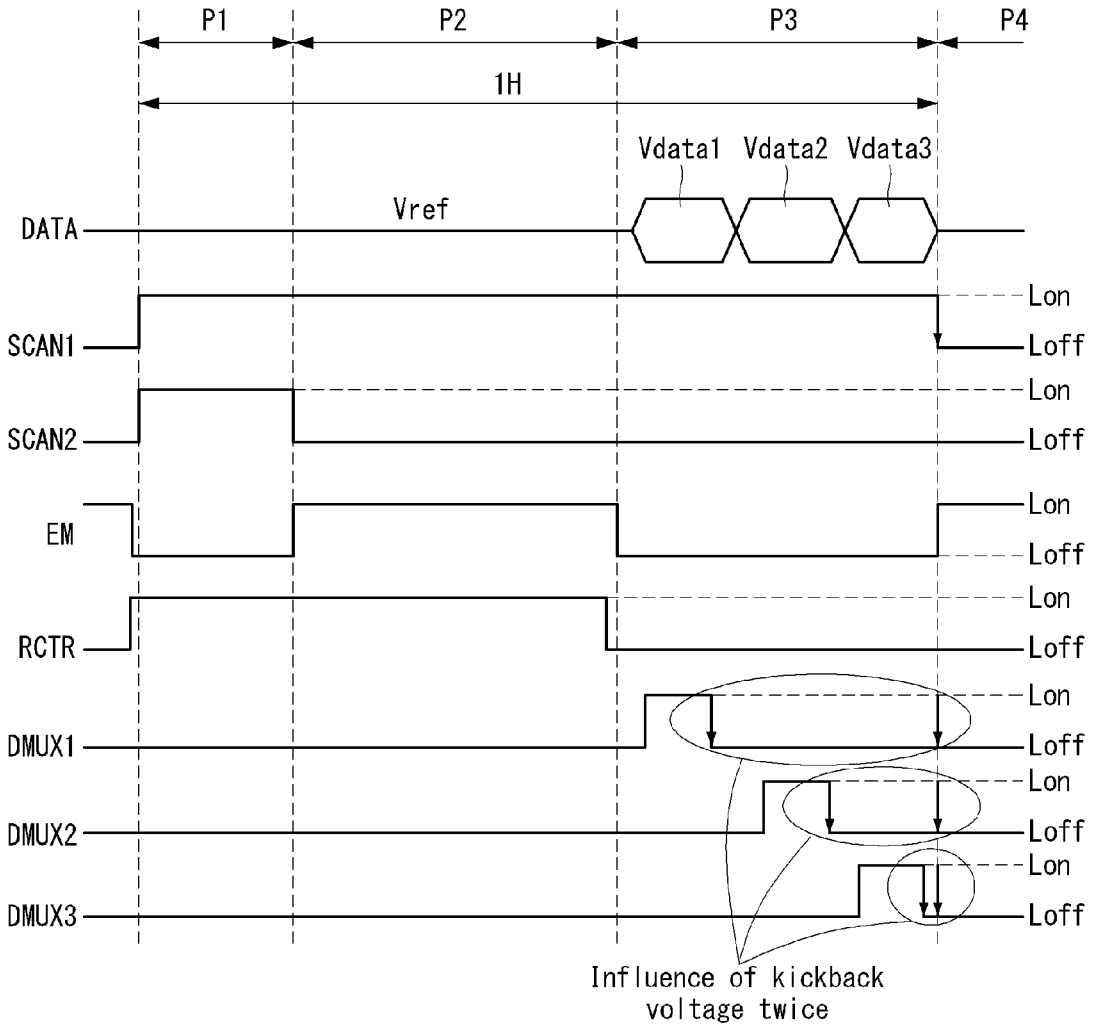

P1
P2
P3
P4
1H
Vdata1
Vdata2
Vdata3
DATA
Vref
SCAN1
SCAN2
EM
RCTR
DMUX1
DMUX2
DMUX3
Lon
Loff
Influence of kickback voltage twice

FIG. 13

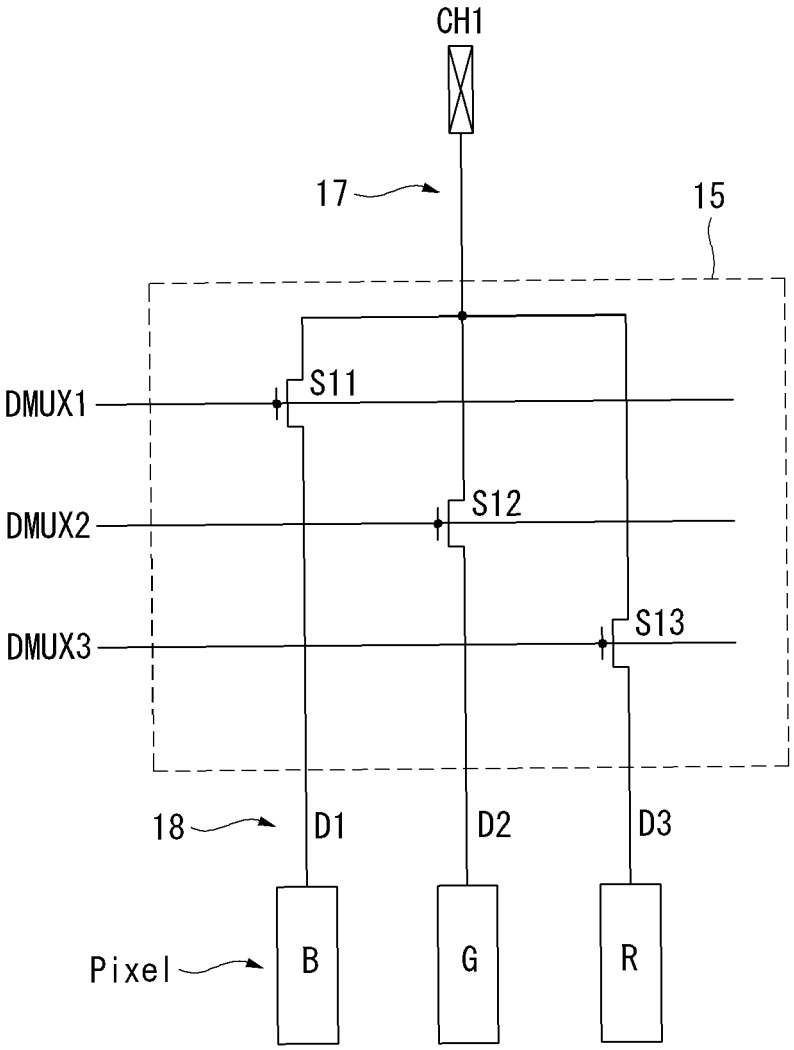
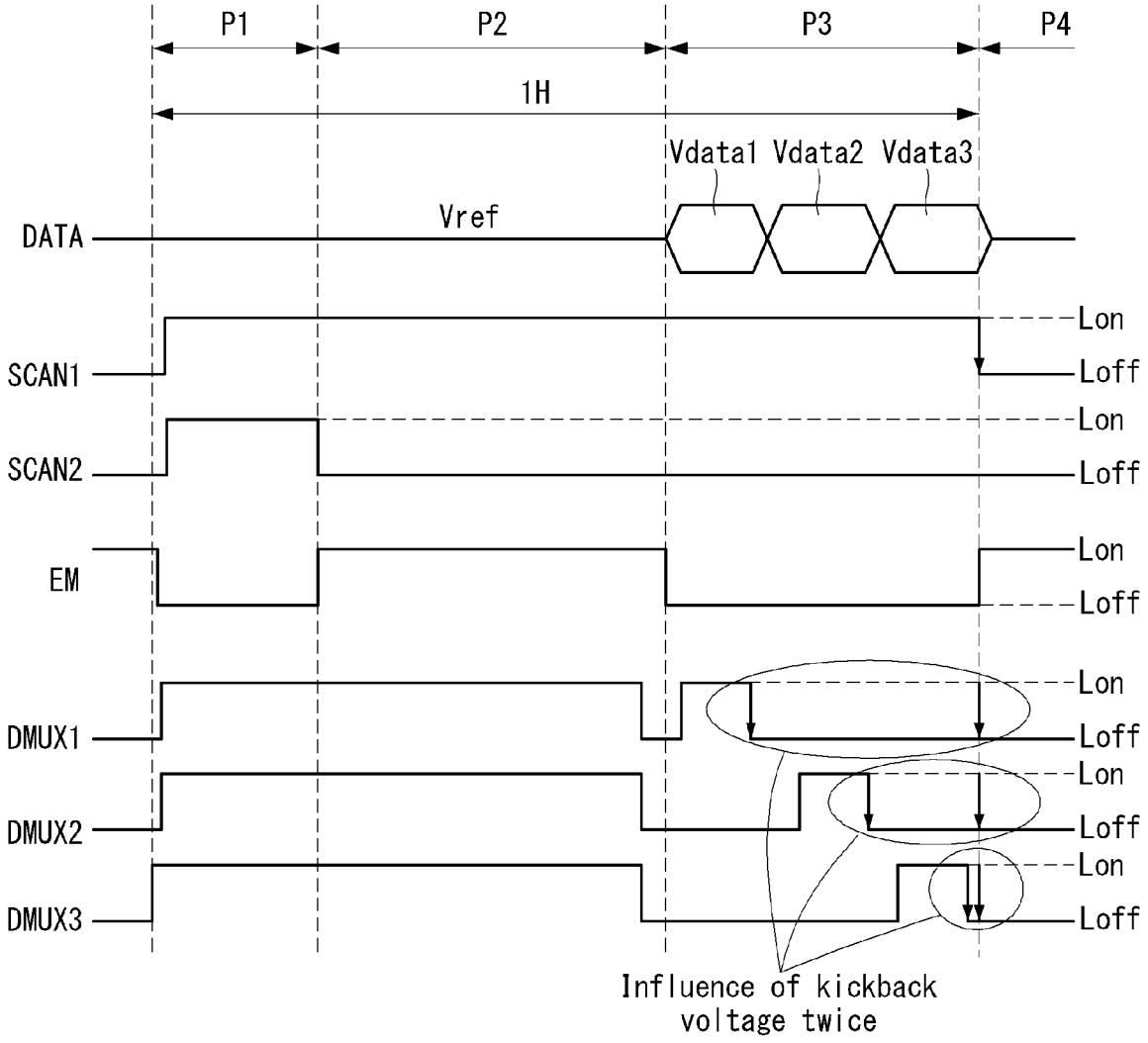


FIG. 14


P1
P2
P3
P4
1H
Vdata1 Vdata2 Vdata3
DATA
Vref
SCAN1
SCAN2
EM
DMUX1
DMUX2
DMUX3
Lon
Loff
Influence of kickback voltage twice

专利名称(译)	有机发光显示器		
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[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	LEE JUNGMIN KANG CHANGHEON		
发明人	LEE, JUNGMIN KANG, CHANGHEON		
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摘要(译)

有机发光显示器包括显示面板，该显示面板包括显示第一颜色的第一像素，显示第二颜色的第二像素，显示第三颜色的第三像素，产生数据电压的数据驱动电路，多路分解器（demux）切换电路，包括连接到数据驱动电路的每个输出通道的第一至第N解复用开关，其中N是等于或大于2的正整数，并且时分将数据电压提供给显示面板的N条数据线，以及控制信号发生器产生第一至第N解复用控制信号，用于控制第一至第N解复用开关的操作。第一至第N解复用控制信号顺序地上升到接通电平，然后在编程周期中顺序地下降到关断电平，其中扫描信号保持在接通电平。

FIG. 6