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(54) **Organic light emitting display device**

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Description

BACKGROUND

1. Field

[0001] The following description relates to an organic light emitting display device.

2. Description of the Related Art

[0002] An organic light emitting display device displays images using organic light emitting diodes as luminescent elements. The organic light emitting display device is considered one of the next-generation display devices because of its excellent luminance and color purity.

[0003] In such an organic light emitting display device, a plurality of pixels are formed by using red, green and blue sub-pixels and, accordingly, various color images are displayed.

[0004] The perception of colors is influenced by a process known as assimilation or the Von Bezold color blending effect.

[0005] Therefore, an arrangement structure of pixels is optimized when using the process so that high resolution can be realized.

[0006] Accordingly, the organic light emitting display device may have a structure in which first and second sub-pixels for emitting light of different colors in one column are alternately arranged.

[0007] U.S. patent application 2009/0021534 A1 discloses an organic light emitting display, wherein each pixel comprises a first sub-pixel, a second sub-pixel and two third sub-pixels arranged in a repeating pattern, wherein first and second sub-pixels are alternately arranged in a first column, and third sub-pixels having a width approximately the half of the width of the first and second sub-pixels are arranged in a second column adjacent to the first column.

[0008] However, in such a data driver, data of first and second colors would be alternately supplied to one data line. If additional data lines are utilized and the data driver is directly connected to those data lines, the number of output lines of the data driver is increased, and therefore, it is more difficult to develop a driving integrated circuit (IC) with such a data driver. Further, a design space necessary for the arrangement of output lines of the driving IC is increased, and therefore, a dead space or size of a non-display region is increased.

[0009] U.S. patent application 2009/0167648 A1 and European patent applications 1 764 771 A2 and 1 635 324 A1 disclose organic light emitting displays comprising a demultiplexer between the output lines of the data driver and the data lines connected to the sub-pixels for reducing the number of output lines, wherein the demultiplexer sequentially supplies the data voltages to the corresponding data lines, and wherein each of the data lines is connected to one of the three sub-pixels.

SUMMARY OF THE INVENTION

[0010] Accordingly, exemplary embodiments of the present invention provide an organic light emitting display device having a data driver with a decreased number of output lines by utilizing a data distributor and employing an arrangement structure of pixels for improving resolution.

[0011] According to an aspect of an exemplary embodiment of the present invention, there is provided an organic light emitting display device according to claim 1.

[0012] The organic light emitting display device may further include a third column adjacent to the second column in which other ones of the first and second sub-pixels are alternately arranged, and a fourth column adjacent to the third column in which other ones of the third sub-pixels are arranged, wherein the first and second sub-pixels in the first and third columns may be respectively arranged diagonally about the second column in a substantially checkerboard arrangement. Preferably, the first column does not include third sub-pixels, and the second column does not include first or second sub-pixels.

[0013] A width of the third sub-pixels may be narrower along a horizontal axis than a width of each of the first and second sub-pixels, and a number of the third sub-pixels may be twice a number of each of the first and second sub-pixels.

[0014] The repeating pattern may be divided into sub-pixel groups each including two first sub-pixels, two second sub-pixels and four third sub-pixels, arranged in two adjacent rows and four adjacent columns. Each of the sub-pixel groups may include one first sub-pixel and one second sub-pixel sequentially arranged in the first column; two third sub-pixels arranged in the second column; one second sub-pixel and one first sub-pixel sequentially arranged in a third column adjacent to the second column; and two third sub-pixels arranged in a fourth column adjacent to the third column. The repeating pattern may be repeated at least once in a row direction and at least once in a column direction Preferably, the third sub-pixels have a width that is half of a width of each of the first and second sub-pixels along the horizontal axis.

[0015] The first sub-pixels may be red sub-pixels, the second sub-pixels may be blue sub-pixels, and the third sub-pixels may be green sub-pixels.

[0016] The data distributor includes a plurality of first transistors for connecting data lines connected to the third sub-pixels from among the data lines to corresponding ones of the output lines of the data driver when a first clock signal is supplied; a plurality of second transistors for connecting data lines connected to the first and second sub-pixels in odd-numbered rows from among the data lines to the corresponding ones of the output lines of the data driver when a second clock signal is supplied; and a plurality of third transistors for connecting data lines connected to the first and second sub-pixels in even-numbered rows from among the data lines to the corre-

sponding ones of the output lines of the data driver when a third clock signal is supplied, wherein the first, second and third clock signals do not overlap with one another.

[0017] The scan signals are sequentially supplied to the scan lines, the first clock signal is supplied to the data distributor after each of the scan signals is supplied, and the second and third clock signals are alternately supplied to the data distributor after each of the scan signals is supplied.

[0018] The first and second clock signals are sequentially supplied during a period between when a scan signal of the scan signals is supplied to an (i-1)-th scan line of the scan lines ("i" is a natural number) and when a scan signal of the scan signals is supplied to an i-th scan line of the scan lines. The first and third clock signals are sequentially supplied during a period between when the scan signal is supplied to the i-th scan line and when a scan signal of the scan signals is supplied to an (i+1)-th scan line of the scan lines.

[0019] The data lines may include a plurality of first data lines for respectively connecting the first sub-pixels in corresponding columns to the data distributor; a plurality of second data lines for respectively connecting the second sub-pixels in corresponding columns to the data distributor; and a plurality of third data lines for respectively connecting the third sub-pixels in corresponding columns to the data distributor.

[0020] A number of the first data lines, a number of the second data lines, and a number of the third data lines may be the same.

[0021] A number of the third sub-pixels may correspond to a resolution of the display region, and a number of the first sub-pixels and a number of the second sub-pixels may correspond to half of the resolution of the display region.

[0022] According to another aspect of the present invention, there is provided a method of driving an organic light emitting display device according to claim 12.

[0023] According to exemplary embodiments of the present invention, high resolution can be implemented by employing the above described arrangement structure of pixels, in which the first and second sub-pixels are arranged in a substantially checkerboard arrangement, and where the third sub-pixels are arranged between columns in which the first and second sub-pixels are arranged.

[0024] Further, the data distributor is applied so that first and second sub-pixels positioned on the same column do not share one data line with each other but are separately coupled to first and second data lines, respectively. Accordingly, a driving IC can be more readily developed, the range of applications can be increased, and the number of output lines of the data driver can be decreased.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The accompanying drawings, together with the specification, illustrate exemplary embodiments of the present invention, and, together with the description, serve to explain the principles of the present invention.

[0026] FIG. 1 is a plan view schematically illustrating an organic light emitting display device according to an embodiment of the present invention.

[0027] FIG. 2 is an enlarged plan view schematically illustrating a sub-pixel group illustrated in FIG. 1.

[0028] FIG. 3 is a waveform diagram illustrating a driving method of the organic light emitting display device illustrated in FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

[0029] Hereinafter, certain exemplary embodiments according to the present invention will be described with reference to the accompanying drawings. Here, when a first element is described as being coupled to a second element, the first element may be directly coupled to the second element, or may be indirectly coupled to the second element via one or more additional elements. Further, some of the elements that are not essential to the complete understanding of the invention are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0030] FIG. 1 is a plan view schematically illustrating an organic light emitting display device according to an embodiment of the present invention. FIG. 2 is an enlarged plan view schematically illustrating a sub-pixel group illustrated in FIG. 1.

[0031] Referring to FIGS. 1 and 2, the organic light emitting display device according to the embodiment of the present invention includes a display region 100, a scan driver 200, a data driver 300, a data distributor 400 and a timing controller 500.

[0032] The display region 100 includes first sub-pixels R, second sub-pixels B and third sub-pixels G, positioned at crossing regions of scan lines S1 to Sn and data lines D1 to D3m. The first, second and third sub-pixels R, B and G emit light of different colors.

[0033] For example, the first sub-pixels R are red sub-pixels for emitting red light, the second sub-pixels B are blue sub-pixels for emitting blue light, and the third sub-pixels G are green sub-pixels for emitting green light.

[0034] In the embodiment of the present invention, the first, second and third sub-pixels R, B and G are repeatedly arranged in a pattern in the display region 100. Here, the pattern is divided into sub-pixel groups 110 each having two first sub-pixels R, two second sub-pixels B and four third sub-pixels G.

[0035] Specifically, the first and second sub-pixels R and B are alternately arranged along a same column, and the third sub-pixels G are arranged in a column adjacent to the column in which the first and second sub-pixels R and B are arranged.

[0036] The first sub-pixels R are diagonally positioned around columns in which the third sub-pixels G are arranged, and the second sub-pixels B are also diagonally

positioned around columns in which the third sub-pixels G are arranged. The first and second sub-pixels R and B are arranged in a substantially checkerboard arrangement. That is, the first sub-pixels R are alternately arranged in two adjacent rows. The second sub-pixels B are also alternately arranged in two adjacent rows.

[0037] In one embodiment, the width of the third sub-pixels G may be narrower along a horizontal axis than that of each of the first and second sub-pixels R and B, but the number of the third sub-pixels G may be twice the number of each of the first and second sub-pixels R and B.

[0038] For example, the third sub-pixels G may have a "separated" form. In the "separated" form, the third sub-pixels G are formed along the horizontal axis to have half of the width of each of the first and second sub-pixels R and B, but the number of the third sub-pixels G may be twice the number of each of the first and second sub-pixels R and B. The third sub-pixels G in such a "separated" form may have a color that may be more sensitive to resolution (e.g., green sub-pixels), so that higher-quality images can be displayed.

[0039] The arrangement of the first, second and third sub-pixels R, B and G in a sub-pixel group 110 will be described in detail. As illustrated in FIG. 2, the sub-pixel group 110 includes two first sub-pixels R, two second sub-pixels B and four third sub-pixels G, which are arranged in two consecutive rows and four consecutive columns.

[0040] More specifically, one first sub-pixel R and one second sub-pixel B are sequentially arranged in adjacent rows of a first column, and two third sub-pixels G are sequentially arranged in a second column adjacent to the first column. One second sub-pixel B and one first sub-pixel R are sequentially arranged in a third column adjacent to the second column, and two third sub-pixels G are sequentially arranged in a fourth column adjacent to the third column.

[0041] By employing the arrangement structure of pixels as described above, high resolution with respect to the number of sub-pixels R, G and B provided in the display region 100 can be implemented by a "sub-pixel rendering" technique. That is, a number of third sub-pixels may correspond to a resolution of the display device. Here, a number of first and second sub-pixels R and B may each correspond to half of the resolution of the display device.

[0042] In the embodiment of the present invention, the first and second sub-pixels R and B positioned in the same column do not share a same data line. That is, first data lines coupled to first sub-pixels R by column and second data lines coupled to second sub-pixels B by column are independent from each other.

[0043] The data lines D include a plurality of first data lines for connecting the first sub-pixels R to the data distributor 400 by column; a plurality of second data lines for connecting the second sub-pixels B to the data distributor 400 by column; and a plurality of third data lines for connecting the third sub-pixels G to the data distributor 400 by column. Therefore, the number of first, second and third data lines are the same.

[0044] As described above, if first and second sub-pixels R and B positioned in the same column do not share one data line, but are separately coupled to first and second data lines, respectively, the data distributor 400 may be employed between the data lines and the data driver 300. Accordingly, the number of output lines of the data driver 300 can be decreased, and a driving integrated circuit (IC) including the data driver 300 can be more easily developed.

[0045] The scan driver 200 generates scan signals corresponding to scan driving control signals SCS supplied from the timing controller 500. The scan signals generated from the scan driver 200 are sequentially supplied to the scan lines S1 to Sn.

[0046] The data driver 300 generates data signals corresponding to data Data and data driving control signals DCS, supplied from the timing controller 500. The data signals generated from the data driver 300 are supplied to the data distributor 400 through output lines O1 to Om of the data driver 300.

[0047] The data distributor 400 is coupled between the data driver 300 and the data lines D1 to D3m. The data distributor 400 distributes data signals respectively supplied from the output lines O1 to Om of the data driver 300 to the plurality of data lines D1 to D3m, corresponding to clock signals CLA, CLB, CLC supplied from the timing controller 500.

[0048] For example, the data distributor 400 may distribute data signals respectively outputted from the output lines O1 to Om of the data driver 300 to first, second and third data lines associated with each of the output lines.

[0049] To this end, the data distributor 400 includes a plurality of first transistors MA1, MA2, ..., MAm, a plurality of second transistors MB1, MB2, ..., MBm, and a plurality of third transistors MC1, MC2, ..., MCm.

[0050] The first transistors MA1, MA2, ..., MAm are coupled between the output lines O1 to Om of the data driver 300 and the third data lines corresponding to the third sub-pixels G, respectively. Gate electrodes of the first transistors MA1, MA2, ..., MAm are coupled to an input line of the first clock signal CLA supplied from the timing controller 500.

[0051] The first transistors MA1, MA2, ..., MAm are turned on during a period where the first clock signal CLA is supplied, to couple the output lines O1 to Om of the data driver 300 to the third data lines corresponding to the third sub-pixels G, respectively.

[0052] The second transistors MB1, MB2, ..., MBm are coupled between the output lines O1 to Om of the data driver 300 and the first and second data lines corresponding to the first and second sub-pixels R and B positioned in odd-numbered rows, respectively. Gate electrodes of the second transistors MB1, MB2, ..., MBm are coupled to an input line of the second clock signal CLB supplied from the timing controller 500.

[0053] The second transistors MB1, MB2, ..., MBm are turned on during a period where the second clock signal CLB is supplied, to couple the output lines O1 to Om of the data driver 300 to the first and second data lines corresponding to the first and second sub-pixels R and B positioned in the odd-numbered rows, respectively.

[0054] The third transistors MC1, MC2, ..., MCm are coupled between the output lines O1 to Om of the data driver 300 and the first and second data lines corresponding to the first and second sub-pixels R and B positioned in even-numbered rows, respectively. Gate electrodes of the third transistors MC1, MC2, ..., MCm are coupled to an input line of the third clock signal CLC supplied from the timing controller 500.

[0055] The third transistors MC1, MC2, ..., MCm are turned on during a period where the third clock signal CLC is supplied, to couple the output lines O1 to Om of the data driver 300 to the first and second data lines corresponding to the first and second sub-pixels R and B positioned in the even-numbered row, respectively.

[0056] Here, the first, second and third clock signals CLA, CLB and CLC for respectively turning on the first transistors MA1, MA2, ..., MAm, the second transistors MB1, MB2, ..., MBm, and the third transistors MC1, MC2, ..., MCm are supplied during different periods which do not overlap with one another.

[0057] The first clock signal CLA is supplied to the data distributor 400 for every horizontal period where scan signals are sequentially supplied to the scan lines S1 to Sn. The second and third clock signals CLB and CLC are alternately supplied to the data distributor 400 corresponding to the horizontal period. In some embodiments, the period of the second and third clock signals CLB and CLC may be set to be twice the period of the first clock signal CLA.

[0058] For example, the first and second clock signals CLA and CLB may be sequentially supplied during the period between when a scan signal is supplied to an (i-1)-th scan line Si-1 ("i" is a natural number) and when a scan signal is supplied to an i-th scan line Si. During a subsequent horizontal period after the horizontal period where the first and second clock signals CLA and CLB are supplied, the first and third clock signals CLA and CLC may be supplied during, for example, the period between when the scan signal is supplied to the i-th scan line Si and when a scan signal is supplied to an (i+1)-th scan line Si+1.

[0059] The operation of the data distributor 400 will be described in greater detail below.

[0060] The timing controller 500 generates scan driving control signals SCS, data driving control signals DCS and clock signals CLA, CLB and CLC, corresponding to synchronization signals supplied from the outside.

[0061] The scan driving control signals SCS, the data driving control signals DCS and the clock signals CLA, CLB and CLC are supplied to the scan driver 200, the data driver 300 and the data distributor 400, respectively. The timing controller 500 also supplies data Data supplied from the outside to the data driver 300.

[0062] According to the embodiment of the present invention, high resolution can be implemented by employing the above described arrangement structure of pixels, in which the first and second sub-pixels R and B are arranged in substantially a checkerboard arrangement, and the third sub-pixels G are arranged between columns in which the first and second sub-pixels R and B are arranged.

[0063] Further, the data distributor 400 is applied so that first and second sub-pixels R and B positioned in a same column do not share a same data line, but are instead separately coupled to first and second data lines, respectively. Accordingly, a driving IC can be more easily developed, the range of applications can be increased, and the number of output lines of the data driver 300 can be decreased. Furthermore, as the number of output lines of the data driver 300 is decreased, a dead space or non-display region located approximate a lower portion of a panel can also be reduced.

[0064] Meanwhile, it has been described in this embodiment that the area of one first or second sub-pixel R or B is twice as wide as that of one third sub-pixel G. However, the present invention is not limited thereto. That is, the areas of the first, second and third sub-pixels R, B and G may be modified, based on, for example, the lifetime of associated materials and/or various other factors.

[0065] Although it has been described in this embodiment that the data distributor 400 is a 3:1 demultiplexer, the present invention is not limited thereto. That is, it will be apparent that the data distributor 400 may be, for example, a 6:1 demultiplexer, a 9:1 demultiplexer, or the like.

[0066] FIG. 3 is a waveform diagram illustrating a driving method of the organic light emitting display device illustrated in FIG. 1. For convenience of illustration, only two scan signals sequentially supplied to consecutive rows are illustrated in FIG. 3.

[0067] Referring to FIG. 3, clock signals CLA, CLB and CLC are supplied during the periods between supply of the scan signals. Here, the first clock signal CLA is supplied for every horizontal period after a scan signal is supplied, and the second and third clock signals CLB and CLC are alternately supplied corresponding to the horizontal period.

[0068] Here, the scan signals are sequentially supplied to the scan lines corresponding to the horizontal period.

[0069] For example, a scan signal is supplied to an (i-1)-th scan line Si-1 ("i" is a natural number) during a horizontal period for selecting pixels (or sub-pixels) on an (i-1)-th row, and a scan signal is supplied to an i-th scan line Si during a subsequent horizontal period, i.e., a horizontal period for selecting pixels on an i-th row.

[0070] During the period between when the scan signal is supplied to the (i-1)-th scan line Si-1 and when the scan signal is supplied to the i-th scan line Si, a first clock signal CLA and either a second or third clock signal CLB

or CLC are supplied to the data distributor 400. Here, the first clock signal CLA and either the second or third clock signal CLB or CLC are used to pre-charge data lines of pixels selected by an i-th scan signal to receive data signals.

[0071] For example, it is assumed that the "i" is an odd number. After a scan signal is supplied to the scan line Si-1 on the (i-1)-th row, the first and second clock signals CLA and CLB are sequentially supplied to the data distributor 400. At this time, the third clock signal CLC maintains a high-level state so that the third transistors MC1, MC2, ..., MCm maintain a turned-off state.

[0072] When the first clock signal CLA is supplied, the third data lines corresponding to the third sub-pixels G are coupled to the output lines O1 to Om of the data driver 300, and data signals are supplied to the third data lines. At this time, the data driver 300 outputs data signals to be supplied to third sub-pixels G in the i-th row, and the third data lines corresponding to the third sub-pixels G are pre-charged with data signals for the third sub-pixels G in the i-th row.

[0073] When the second clock signal CLB is supplied, the first and second data lines corresponding to the first and second sub-pixels R and B positioned in the odd-numbered rows are coupled to the output lines O1 to Om of the data driver 300, and data signals are supplied to those first and second data lines. At this time, the data driver 300 outputs data signals to be supplied to first and second sub-pixels R and B in the i-th row, and the first and second data lines corresponding to the first and second sub-pixels R and B in the odd-numbered rows are pre-charged with data signals for the first and second sub-pixels R and B in the i-th row, respectively.

[0074] Thereafter, when a scan signal is supplied to the i-th scan line Si, the data signals pre-charged in the first to third data lines are supplied to the first to third sub-pixels R, B and G positioned in the i-th row, respectively.

[0075] Meanwhile, after the scan signal is supplied to the i-th scan line, first and third clock signals CLA and CLC are sequentially supplied to the data distributor 400. At this time, the second clock signal CLB maintains a high-level state so that the second transistors MB1, MB2, ..., MBm maintain a turned-off state.

[0076] When the first clock signal CLA is supplied, the third data lines corresponding to the third sub-pixels G are coupled to the output lines O1 to Om of the data driver 300, and data signals are supplied to the third data lines. At this time, the data driver 300 outputs data signals to be supplied to third sub-pixels G in the (i+1)-th row, and the third data lines corresponding to the third sub-pixels G are pre-charged with data signals for the third sub-pixels G in the (i+1)-th row.

[0077] When the third clock signal CLC is supplied, the first and second data lines corresponding to the first and second sub-pixels R and B positioned in the even-numbered rows are coupled to the output lines O1 to Om of the data driver 300, and data signals are supplied to those first and second data lines. At this time, the data driver 300 outputs data signals to be supplied to first and second sub-pixels R and B in the (i+1)-th row, and the first and second data lines corresponding to the first and second sub-pixels R and B on the even-numbered rows are pre-charged with data signals for the first and second sub-pixels R and B in the (i+1)-th row, respectively.

[0078] Meanwhile, although not shown in this figure for convenience of illustration, when a scan signal is supplied to an (i+1)-th scan line Si+1, the data signals pre-charged in the first to third data lines are supplied to the first to third sub-pixels R, G and B positioned in the (i+1)-th row, respectively.

[0079] In the same manner as described above, data signals are sequentially supplied to the first to third sub-pixels R, G and B by row during the horizontal periods.

[0080] Accordingly, each of the sub-pixels R, G and B stores a data signal corresponding to the respective sub-pixel and emits light having luminance corresponding to the respective data signal, thereby displaying an image in the display region 100.

[0081] While the present invention has been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but is instead intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

Claims

1. An organic light emitting display device, comprising:

a display region (100) comprising first sub-pixels (R), second sub-pixels (B) and third sub-pixels (G) at crossing regions of scan lines (S1, S2, Sn-1, Sn) and data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) and arranged in a repeating pattern, the first, second and third sub-pixels (R, B, G) emitting light of different colors;

a scan driver (200) for sequentially supplying scan signals to the scan lines (S1, S2, Sn-1, Sn);

a data driver (300) for supplying data signals to the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m);

a data distributor (400) between the data driver (300) and the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) for distributing the data signals from output lines (O1 02, Om-1, Om) of the data driver (300) to the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m); and

a timing controller (500) adapted to supply first, second and third clock signals (CLA, CLB, CLC) not overlapping with one another,

wherein first and second sub-pixels (R, B) are alternately arranged in a first column, and third sub-pixels (G) are arranged in a second column

adjacent to the first column,
wherein a first data line (D1) of the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) connects the first sub-pixels (R) in the first column to the data distributor (400) and a second data line (D2) of the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) connects the second sub-pixels (B) in the first column to the data distributor (400),
wherein the data distributor (400) comprises:

a plurality of first transistors (MA1, MA2, MAm-1, MAm) coupled between data lines (D3, D6, D3m-3, D3m) connected to the third sub-pixels (G) from among the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) and corresponding ones of the output lines (O1 02, Om-1, Om) of the data driver (300), wherein the gate electrodes of the first transistors (MA1, MA2, MAm-1, MAm) are coupled to the first clock signal (CLA);
a plurality of second transistors (MB1, MB2, MBm-1, MBm) coupled between data lines (D1, D4, D3m-5, D3m-2) connected to the first and second sub-pixels (R, B) in odd-numbered rows from among the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) and the corresponding ones of the output lines (O1, 02, Om-1, Om) of the data driver (300), wherein the gate electrodes of the second transistors (MB1, MB2, MBm-1, MBm) are coupled to the second clock signal (CLB); and
a plurality of third transistors (MC1, MC2, MCm-1, MCm) coupled between data lines (D2, D5, D3m-4, D3m-1) connected to the first and second sub-pixels (R, B) in even-numbered rows from among the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) and the corresponding ones of the output lines (O1, 02, Om-1, Om) of the data driver (300), wherein the gate electrodes of the third transistors (MC1, MC2, MCm-1, MCm) are coupled to the third clock signal (CLC); and wherein
the timing controller (500) is further adapted to supply the first clock signal (CLA) to the data distributor (400) during each period between two subsequent scan signals, and to alternately supply one of the second and third clock signals (CLB, CLC) to the data distributor (400) during the periods between two subsequent scan signals.

2. The organic light emitting display device according to claim 1, further comprising a third column adjacent to the second column in which first and second sub-pixels (R, B) are alternately arranged, and a fourth column adjacent to the third column in which third sub-pixels (G) are arranged, wherein the first and second sub-pixels (R; B) in the first and third columns are respectively arranged diagonally about the second column in a checkerboard arrangement.

3. The organic light emitting display device according to one of the preceding claims, wherein a width of the third sub-pixels (G) along a horizontal axis is narrower than a width of each of the first and second sub-pixels (R, B) along a horizontal axis, and a number of the third sub-pixels (G) is twice a number of each of the first and second sub-pixels (R, B).

4. The organic light emitting display device according to one of the preceding claims, wherein:

the repeating pattern is divided into sub-pixel groups (110) each comprising two first sub-pixels (R), two second sub-pixels (B) and four third sub-pixels (G) arranged in two adjacent rows and four adjacent columns; and
each of the sub-pixel groups (110) comprises:

one first sub-pixel (R) and one second sub-pixel (B) sequentially arranged in the first column;
two third sub-pixels (G) arranged in the second column;
one second sub-pixel (B) and one first sub-pixel (R) sequentially arranged in a third column adjacent to the second column; and
two third sub-pixels (G) arranged in a fourth column adjacent to the third column.

5. The organic light emitting display device according to claim 4, wherein the repeating pattern is repeated at least once in a row direction and at least once in a column direction.

6. The organic light emitting display device according to one of the preceding claims, wherein the third sub-pixels (G) have a width that is half of a width of each of the first and second sub-pixels (R, B) along the horizontal axis.

7. The organic light emitting display device according to one of the preceding claims, wherein the first sub-pixels (R) are red sub-pixels, the second sub-pixels (B) are blue sub-pixels, and the third sub-pixels (G) are green sub-pixels.

8. The organic light emitting display device according to one of the preceding claims, wherein the timing controller (500) is adapted to sequentially supply the first and second clock signals (CLA, CLB) during a

period between when a scan signal of the scan signals is supplied to an (i-1)-th scan line of the scan lines (S1, S2, Sn-1, Sn) and when a scan signal of the scan signals is supplied to an i-th scan line of the scan lines (S1, S2, Sn-1, Sn), and to sequentially supply the first and third clock signals (CLA, CLC) during a period between when a scan signal is supplied to the i-th scan line of the scan lines (S1, S2, Sn-1, Sn) and when a scan signal of the scan signals is supplied to an (i+1)-th scan line of the scan lines (S1, S2, Sn-1, Sn).

9. The organic light emitting display device according to one of the preceding claims, wherein the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) comprise a plurality of first data lines (D1, D5, D3m-5, D3m-1) for respectively connecting the first sub-pixels (R) in corresponding columns to the data distributor (400); a plurality of second data lines (D2, D4, D3m-4, D3m-2) for respectively connecting the second sub-pixels (B) in corresponding columns to the data distributor (400); and a plurality of third data lines (D3, D6, D3m-3, D3m) for respectively connecting the third sub-pixels (G) in corresponding columns to the data distributor (400).

10. The organic light emitting display device according to claim 9, wherein the number of first data lines (D1, D5, D3m-5, D3m-1), the number of second data lines (D4, D4, D3m-4, D3m-2), and the number of third data lines (D3, D6, D3m-3, D3m) are the same.

11. The organic light emitting display device according to one of the preceding claims, wherein the number of third sub-pixels (G) corresponds to a resolution of the display region, and the number of first sub-pixels (R) and the number of second sub-pixels (B) corresponds to half of the resolution of the display region.

12. A method of driving the organic light emitting display according to one of claims 1 through 11,
wherein the scan signals are sequentially supplied to the scan lines (S1, S2, Sn-1, Sn), and wherein
the data lines (D3, D6, D3m-3, D3m) connected to the third sub-pixels (G) from among the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) are coupled to corresponding ones of the output lines (O1, 02, Om-1, Om) of the data driver (300) when the first clock signal (CLA) is supplied;
the data lines (D1, D4, D3m-5, D3m-2) connected to the first and second sub-pixels (R, B) in odd-numbered rows from among the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) are coupled to the corresponding ones of the output lines (O1, 02, Om-1, Om) of the data driver (300) when the second clock signal (CLB) is supplied; and
the data lines (D2, D5, D3m-4, D3m-1) connected to the first and second sub-pixels (R, B) in even-numbered rows from among the data lines (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) are coupled to the corresponding ones of the output lines (O1, O2, Om-1, Om) of the data driver (300) when the third clock signal (CLC) is supplied,
wherein the first and second clock signals (CLA, CLB) are sequentially supplied during a period between when a scan signal of the scan signals is supplied to an (i-1)-th scan line of the scan lines (S1, S2, Sn-1, Sn) and when a scan signal of the scan signals is supplied to an i-th scan line of the scan lines (S1, S2, Sn-1, Sn), and
wherein the first and third clock signals (CLA, CLC) are sequentially supplied during a period between when a scan signal is supplied to the i-th scan line of the scan lines (S1, S2, Sn-1, Sn) and when a scan signal of the scan signals is supplied to an (i+1)-th scan line of the scan lines (S1, S2, Sn-1, Sn).

Patentansprüche

1. Organische lichtemittierende Anzeigevorrichtung, aufweisend:

eine Anzeigeregion (100), die erste Subpixel (R), zweite Subpixel (B) und dritte Subpixel (G) in Kreuzungsregionen von Ansteuerleitungen (S1, S2, Sn-1, Sn) und Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) aufweist, die in einem sich wiederholenden Muster angeordnet sind, wobei die ersten, zweiten und dritten Subpixel (R, B, G) Licht verschiedener Farben emittieren;
einen Ansteuertreiber (200) zum sequenziellen Anlegen von Ansteuersignalen an die Ansteuerleitungen (S1, S2, Sn-1, Sn);
einen Datentreiber (300) zum Anlegen von Datensignalen an die Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m);
einen Datenverteiler (400) zwischen dem Datentreiber (300) und den Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) zum Verteilen der Datensignale von Ausgangsleitungen (O1, 02, Om-1, Om) des Datentreibers (300) zu den Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) ; und
eine Zeitsteuerung (500), die zum Anlegen eines ersten, zweiten und dritten Taktsignals (CLA, CLB, CLC), die sich nicht überlappen, ausgebildet ist,
wobei erste und zweite Subpixel (R, B) alternie-

rend in einer ersten Spalte angeordnet sind und dritte Subpixel (G) in einer zweiten Spalte benachbart zur ersten Spalte angeordnet sind,
wobei eine erste Datenleitung (D1) der Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3 m-1, D3m) die ersten Subpixel (R) in der ersten Spalte mit dem Datenverteiler (400) verbindet und eine zweite Datenleitung (D2) der Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) die zweiten Subpixel (B) in der ersten Spalte mit dem Datenverteiler (400) verbindet,
wobei der Datenverteiler (400) aufweist:

eine Vielzahl erster Transistoren (MA1, MA2, MAm-1, MAm), die zwischen Datenleitungen (D3, D6, D3m-3, D3m), die aus den Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) mit den dritten Subpixeln (G) verbunden sind, und entsprechende der Ausgangsleitungen (O1, 02, Om-1, Om) des Datentreibers (300) geschaltet sind, wobei die Gate-Elektroden der ersten Transistoren (MA1, MA2, MAm-1, MAm) mit dem ersten Taktsignal (CLA) gekoppelt sind;
eine Vielzahl zweiter Transistoren (MB1, MB2, MBm-1, MBm), die zwischen Datenleitungen (D1, D4, D3m-5, D3m-2), die aus den Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) mit den ersten und zweiten Subpixeln (R, B) in ungeradzahligen Zeilen verbunden sind, und die entsprechenden der Ausgangsleitungen (O1, 02, Om-1, Om) des Datentreibers (300) geschaltet sind, wobei die Gate-Elektroden der zweiten Transistoren (MB1, MB2, MBm-1, MBm) mit dem zweiten Taktsignal (CLB) gekoppelt sind; und
eine Vielzahl dritter Transistoren (MC1, MC2, MCm-1, MCM), die zwischen Datenleitungen (D2, D5, D3m-4, D3m-1), die aus den Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) mit den ersten und zweiten Subpixeln (R, B) in geradzahligen Zeilen verbunden sind, und die entsprechenden der Ausgangsleitungen (O1, 02, Om-1, Om) des Datentreibers (300) geschaltet sind, wobei die Gate-Elektroden der dritten Transistoren (MC1, MC2, MCm-1, MCm) mit dem dritten Taktsignal (CLC) gekoppelt sind; und wobei
die Zeitsteuerung (500) weiterhin ausgebildet ist, während jeder Periode zwischen zwei anschließenden Ansteuersignalen das erste Taktsignal (CLA) an den Datenverteiler (400) anzulegen, und während der Perioden zwischen zwei anschließenden Ansteuersignalen alternierend das zweite oder dritte Taktsignal (CLB, CLC) an den Datenverteiler (400) anzulegen.

2. Organische lichtemittierende Anzeigevorrichtung nach Anspruch 1, weiterhin aufweisend eine dritte Spalte benachbart zur zweiten Spalte, in der erste und zweite Subpixel (R, B) alternierend angeordnet sind, und eine vierte Spalte benachbart zur dritten Spalte, in der dritte Subpixel (G) angeordnet sind, wobei die ersten und zweiten Subpixel (R, B) in der ersten und dritten Spalte jeweils diagonal um die zweite Spalte in einer Schachbrettanordnung angeordnet sind.

3. Organische lichtemittierende Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei eine Breite der dritten Subpixel (G) entlang einer horizontalen Achse kleiner als eine Breite jedes der ersten und zweiten Subpixel (R, B) entlang einer horizontalen Achse ist, und eine Anzahl der dritten Subpixel (G) doppelt so groß wie eine Anzahl jedes der ersten und zweiten Subpixel (R, B) ist.

4. Organische lichtemittierende Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei:

das sich wiederholende Muster in Subpixelgruppen (110) unterteilt ist, von denen jede zwei erste Subpixel (R), zwei zweite Subpixel (B) und vier dritte Subpixel (G) aufweist, die in zwei benachbarten Zeilen und vier benachbarten Spalten angeordnet sind; und
jede der Subpixelgruppen (110) aufweist:

einen ersten Subpixel (R) und einen zweiten Subpixel (B), die sequenziell in der ersten Spalte angeordnet sind;
zwei dritte Subpixel (G), die in der zweiten Spalte angeordnet sind;
einen zweiten Subpixel (B) und einen ersten Subpixel (R), die sequenziell in einer dritten Spalte benachbart zur zweiten Spalte angeordnet sind; und
zwei dritte Subpixel (G), die in einer vierten Spalte benachbart zur dritten Spalte angeordnet sind.

5. Organische lichtemittierende Anzeigevorrichtung nach Anspruch 4, wobei sich das sich wiederholende Muster zumindest einmal in einer Zeilenrichtung und zumindest einmal in einer Spaltenrichtung wiederholt.

6. Organische lichtemittierende Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei

die dritten Subpixel (G) eine Breite aufweisen, die halb so groß wie eine Breite von jedem der ersten und zweiten Subpixel (R, B) entlang der horizontalen Achse ist.

7. Organische lichtemittierende Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei die ersten Subpixel (R) rote Subpixel sind, die zweiten Subpixel (B) blaue Subpixel sind und die dritten Subpixel (G) grüne Subpixel sind.

8. Organische lichtemittierende Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei die Zeitsteuerung (500) ausgebildet ist, während einer Periode zwischen dem Anlegen eines Ansteuersignals der Ansteuersignale an eine (i-1)te Ansteuerleitung der Ansteuerleitungen (S1, S2, Sn-1, Sn) und dem Anlegen eines Ansteuersignals der Ansteuersignale an eine ite Ansteuerleitung der Ansteuerleitungen (S1, S2, Sn-1, Sn) sequenziell das erste und zweite Taktsignal (CLA, CLB) anzulegen und während einer Periode zwischen dem Anlegen eines Ansteuersignals an die ite Ansteuerleitung der Ansteuerleitungen (S1, S2, Sn-1, Sn) und dem Anlegen eines Ansteuersignals der Ansteuersignale an eine (i+1)te Ansteuerleitung der Ansteuerleitungen (S1, S2, Sn-1, Sn) sequenziell das erste und dritte Taktsignal (CLA, CLC) anzulegen.

9. Organische lichtemittierende Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei die Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) Folgendes aufweisen: eine Vielzahl erster Datenleitungen (D1, D5, D3m-5, D3m-1) zum jeweiligen Verbinden der ersten Subpixel (R) in entsprechenden Spalten mit dem Datenverteiler (400); eine Vielzahl zweiter Datenleitungen (D2, D4, D3m-4, D3m-2) zum jeweiligen Verbinden der zweiten Subpixel (B) in entsprechenden Spalten mit dem Datenverteiler (400); und eine Vielzahl dritter Datenleitungen (D3, D6, D3m-3, D3m) zum jeweiligen Verbinden der dritten Subpixel (G) in entsprechenden Spalten mit dem Datenverteiler (400).

10. Organische lichtemittierende Anzeigevorrichtung nach Anspruch 9, wobei die Anzahl erster Datenleitungen (D1, D5, D3m-5, D3m-1), die Anzahl zweiter Datenleitungen (D4, D4, D3m-4, D3m-2) und die Anzahl dritter Datenleitungen (D3, D6, D3m-3, D3m) gleich sind.

11. Organische lichtemittierende Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei die Anzahl dritter Subpixel (G) einer Auflösung der Anzeigeregion entspricht, und die Anzahl erster Subpixel (R) und die Anzahl zweiter Subpixel (B) der Hälfte der Auflösung der Anzeigeregion entspricht.

12. Verfahren zur Ansteuerung der organischen lichtemittierenden Anzeigevorrichtung nach einem der Ansprüche 1 bis 11,
wobei die Ansteuersignale sequenziell an die Ansteuerleitungen (S1, S2, Sn-1, Sn) angelegt werden, und wobei
die Datenleitungen (D3, D6, D3m-3, D3m), die aus den Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) mit den dritten Subpixeln (G) verbunden sind, mit entsprechenden der Ausgangsleitungen (O1, 02, Om-1, Om) des Datentreibers (300) gekoppelt werden, wenn das erste Taktsignal (CLA) angelegt wird;
die Datenleitungen (D1, D4, D3m-5, D3m-2), die aus den Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) mit den ersten und zweiten Subpixeln (R, B) in ungeradzahligen Zeilen verbunden sind, mit den entsprechenden der Ausgangsleitungen (O1, 02, Om-1, Om) des Datentreibers (300) gekoppelt werden, wenn das zweite Taktsignal (CLB) angelegt wird; und
die Datenleitungen (D2, D5, D3m-4, D3m-1), die aus den Datenleitungen (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) mit den ersten und zweiten Subpixeln (R, B) in geradzahligen Zeilen verbunden sind, mit den entsprechenden der Ausgangsleitungen (O1, 02, Om-1, Om) des Datentreibers (300) gekoppelt werden, wenn das dritte Taktsignal (CLC) angelegt wird,
wobei das erste und zweite Taktsignal (CLA, CLB) während einer Periode zwischen dem Anlegen eines Ansteuersignals der Ansteuersignale an eine (i-1)te Ansteuerleitung der Ansteuerleitungen (S1, S2, Sn-1, Sn) und dem Anlegen eines Ansteuersignals der Ansteuersignale an eine ite Ansteuerleitung der Ansteuerleitungen (S1, S2, Sn-1, Sn) sequenziell angelegt werden, und
wobei das erste und dritte Taktsignal (CLA, CLC) während einer Periode zwischen dem Anlegen eines Ansteuersignals an die ite Ansteuerleitung der Ansteuerleitungen (S1, S2, Sn-1, Sn) und dem Anlegen eines Ansteuersignals der Ansteuersignale an eine (i+1)te Ansteuerleitung der Ansteuerleitungen (S1, S2, Sn-1, Sn) sequenziell angelegt werden.

Revendications

1. Dispositif d'affichage électroluminescent organique, comprenant :

une zone d'affichage (100) comprenant des premiers sous-pixels (R), des deuxièmes sous-pixels (B) et des troisièmes sous-pixels (G) au niveau de zones de croisement de lignes de balayage (S1, S2, Sn-1, Sn) et de lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) et agencées se-

lon une configuration à répétition, les premiers, les deuxièmes et les troisièmes sous-pixels (R, B, G) émettant de la lumière de différentes couleurs ;

un circuit d'attaque de balayage (200) destiné à fournir de manière séquentielle des signaux de balayage aux lignes de balayage (S1, S2, Sn-1, Sn) ;

un circuit d'attaque de données (300) destiné à fournir des signaux de données aux lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m);

un distributeur de données (400) entre le circuit d'attaque de données (300) et les lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) destiné à distribuer les signaux de données depuis des lignes de sortie (O1, O2, Om-1, Om) du circuit d'attaque de données (300) aux lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m -4, D3m-3, D3m-2, D3m-1, D3m) ; et

une unité de commande de synchronisation (500) adaptée pour fournir des premier, deuxième et troisième signaux d'horloge (CLA, CLB, CLC) qui ne se chevauchent pas entre eux,

où des premiers et des deuxièmes sous-pixels (R, B) sont agencés en alternance dans une première colonne, et des troisièmes sous-pixels (G) sont agencés dans une deuxième colonne adjacente à la première colonne,

où une première ligne de données (D1) parmi les lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) relie les premiers sous-pixels (R) dans la première colonne au distributeur de données (400) et une deuxième ligne de données (D2) parmi les lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) relie les deuxièmes sous-pixels (B) dans la première colonne au distributeur de données (400), où le distributeur de données (400) comprend :

une pluralité de premiers transistors (MA1, MA2, MAm-1, MAm) couplés entre des lignes de données (D3, D6, D3m-3, D3m) reliées aux troisièmes sous-pixels (G) parmi les lignes de données (D1, D2 , D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) et des lignes de sortie correspondantes parmi les lignes de sortie (O1, O2, Om-1, Om) du circuit d'attaque de données (300), où les électrodes grille des premiers transistors (MA1, MA2, MAm-1, MAm) sont couplées au premier signal d'horloge (CLA);

une pluralité de deuxièmes transistors (MB1, MB2, MBm-1, MBm) couplés entre des lignes de données (D1, D4, D3m-5, D3m-2) reliées aux premiers et aux deuxièmes sous-pixels (R, B) dans des rangées numérotées impaires parmi les lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) et des lignes de sortie correspondantes parmi les lignes de sortie (O1, O2, Om-1, OM) du circuit d'attaque de données (300), où les électrodes grille des deuxièmes transistors (MB1, MB2, MBm-1, MBm) sont couplées au deuxième signal d'horloge (CLB) ; et

une pluralité de troisièmes transistors (MC1, MC2, MCm-1, MCm) couplés entre des lignes de données (D2, D5, D3m-4, D3m-1) reliées aux premiers et aux deuxièmes sous-pixels (R, B) dans des rangées numérotées paires parmi les lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) et des lignes de sortie correspondantes parmi les lignes de sortie (O1, O2, Om-1, Om) du circuit d'attaque de données (300), où les électrodes grille des troisièmes transistors (MC1, MC2, MCm-1, MCm) sont couplées au troisième signal d'horloge (CLC) ; et où l'unité de commande de synchronisation (500) est en outre adaptée pour fournir le premier signal d'horloge (CLA) au distributeur de données (400) pendant chaque période entre deux signaux de balayage subséquents, et pour fournir en alternance l'un du deuxième et du troisième signal d'horloge (CLB, CLC) au distributeur de données (400) pendant les périodes entre deux signaux de balayage subséquents.

2. Dispositif d'affichage électroluminescent organique selon la revendication 1, comprenant en outre une troisième colonne adjacente à la deuxième colonne dans laquelle des premiers et des deuxièmes sous-pixels (R, B) sont agencés en alternance, et une quatrième colonne adjacente à la troisième colonne dans laquelle des troisièmes sous-pixels (G) sont agencés, où les premiers et les deuxièmes sous-pixels (R ; B) dans les première et troisième colonnes sont respectivement agencés en diagonale sur la deuxième colonne dans un agencement en damier.

3. Dispositif d'affichage électroluminescent organique selon l'une des revendications précédentes, dans lequel la largeur des troisièmes sous-pixels (G) le long d'un axe horizontal est plus petite que la largeur de chacun des premiers et des deuxièmes sous-pixels (R, B) le long d'un axe horizontal, et le nombre des troisièmes sous-pixels (G) est le double du nombre de chacun des premiers et des deuxièmes sous-pixels (R, B).

4. Dispositif d'affichage électroluminescent organique selon l'une des revendications précédentes, dans lequel :

le motif de répétition est divisé en groupes (110) de sous-pixels comprenant chacun deux premiers sous-pixels (R), deux deuxièmes sous-pixels (B) et quatre troisièmes sous-pixels (G) agencés en deux rangées adjacentes et quatre colonnes adjacentes ; et
chacun des groupes (110) de sous-pixels comprend :

un premier sous-pixel (R) et un deuxième sous-pixel (B) agencés de manière séquentielle dans la première colonne ;
deux troisièmes sous-pixels (G) agencés dans la deuxième colonne ;
un deuxième sous-pixel (B) et un premier sous-pixel (R) agencés de manière séquentielle dans une troisième colonne adjacente à la deuxième colonne ; et
deux troisièmes sous-pixels (G) agencés dans une quatrième colonne adjacente à la troisième colonne.

5. Dispositif d'affichage électroluminescent organique selon la revendication 4, dans lequel le motif de répétition est répété au moins une fois dans la direction d'une rangée et au moins une fois dans la direction d'une colonne.

6. Dispositif d'affichage électroluminescent organique selon l'une des revendications précédentes, dans lequel les troisièmes sous-pixels (G) ont une largeur qui est la moitié d'une largeur de chacun des premiers et des deuxièmes sous-pixels (R, B) le long de l'axe horizontal.

7. Dispositif d'affichage électroluminescent organique selon l'une des revendications précédentes, dans lequel les premiers sous-pixels (R) sont des sous-pixels rouges, les deuxièmes sous-pixels (B) sont des sous-pixels bleus, et les troisièmes sous-pixels (G) sont des sous-pixels verts.

8. Dispositif d'affichage électroluminescent organique selon l'une des revendications précédentes, dans lequel l'unité de commande de synchronisation (500) est adaptée pour fournir de manière séquentielle les premier et deuxième signaux d'horloge (CLA, CLB) pendant une période entre le moment où un signal de balayage parmi les signaux de balayage est fourni à une (i-1)-ème ligne de balayage parmi les lignes de balayage (S1, S2, Sn-1, Sn) et le moment où un signal de balayage parmi les signaux de balayage est fourni à une i-ème ligne de balayage parmi les lignes de balayage (S1, S2, Sn-1, Sn), et pour fournir de manière séquentielle les premier et troisième signaux d'horloge (CLA, CLC) pendant une période entre le moment où un signal de balayage est fourni à l'i-ème ligne de balayage parmi les lignes de balayage (S1, S2, Sn-1, Sn) et le moment où un signal de balayage parmi les signaux de balayage est fourni à une (i+1)-ème ligne de balayage parmi les lignes de balayage (S1, S2, Sn-1, Sn).

9. Dispositif d'affichage électroluminescent organique selon l'une des revendications précédentes, dans lequel les lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1 , D3m) comprennent une pluralité de premières lignes de données (D1, D5, D3m-5, D3m-1) permettant de relier respectivement les premiers sous-pixels (R) dans des colonnes correspondantes au distributeur de données (400) ; une pluralité de deuxièmes lignes de données (D2, D4, D3m-4, D3m-2) permettant de relier respectivement les deuxièmes sous-pixels (B) dans des colonnes correspondantes au distributeur de données (400) ; et une pluralité de troisièmes lignes de données (D3, D6, D3m-3, D3m) permettant de relier respectivement les troisièmes sous-pixels (G) dans des colonnes correspondantes au distributeur de données (400).

10. Dispositif d'affichage électroluminescent organique selon la revendication 9, dans lequel le nombre de premières lignes de données (D1, D5, D3m-5, D3m-1), le nombre de deuxièmes lignes de données (D4, D4, D3m-4, D3m-2), et le nombre de troisièmes lignes de données (D3, D6, D3m-3, D3m) sont identiques.

11. Dispositif d'affichage électroluminescent organique selon l'une des revendications précédentes, dans lequel le nombre de troisièmes sous-pixels (G) correspond à une résolution de la zone d'affichage, et le nombre de premiers sous-pixels (R) et le nombre de deuxièmes sous-pixels (B) correspond à la moitié de la résolution de la zone d'affichage.

12. Procédé de commande du dispositif d'affichage électroluminescent organique selon l'une des revendications 1 à 11,
dans lequel les signaux de balayage sont fournis de manière séquentielle aux lignes de balayage (S1, S2, Sn-1, Sn), et où
les lignes de données (D3, D6, D3m-3, D3m) reliées aux troisièmes sous-pixels (G) parmi les lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) sont couplées à des lignes de sortie correspondantes parmi les lignes de sortie (O1, O2, Om-1, Om) du circuit d'attaque de données (300) lorsque le premier signal d'horloge (CLA) est fourni ;

les lignes de données (D1, D4, D3m-5, D3m-2) reliées aux premiers et aux deuxièmes sous-pixels (R, B) dans des rangées numérotées impaires parmi les lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) sont couplées aux lignes de sortie correspondantes parmi les lignes de sortie (O1, O2, Om-1, Om) du circuit d'attaque de données (300) lorsque le deuxième signal d'horloge (CLB) est fourni ; et

les lignes de données (D2, D5, D3m-4, D3m-1) reliées aux premiers et aux deuxièmes sous-pixels (R, B) dans des rangées numérotées paires parmi les lignes de données (D1, D2, D3, D4, D5, D6, D3m-5, D3m-4, D3m-3, D3m-2, D3m-1, D3m) sont couplées aux lignes de sortie correspondantes parmi les lignes de sortie (O1, O2, Om-1, Om) du circuit d'attaque de données (300) lorsque le troisième signal d'horloge (CLC) est fourni,

où les premier et deuxième signaux d'horloge (CLA, CLB) sont fournis de manière séquentielle pendant une période entre le moment où un signal de balayage parmi les signaux de balayage est fourni à une (i-1)-ème ligne de balayage parmi les lignes de balayage (S1, S2, Sn-1, Sn) et le moment où un signal de balayage parmi les signaux de balayage est fourni à une i-ème ligne de balayage parmi les lignes de balayage (S1, S2, Sn-1, Sn), et

où les premier et troisième signaux d'horloge (CLA, CLC) sont fournis de manière séquentielle pendant une période entre le moment où un signal de balayage est fourni à l'i-ème ligne de balayage parmi les lignes de balayage (S1, S2, Sn-1, Sn) et le moment où un signal de balayage parmi les signaux de balayage est fourni à une (i+1)-ème ligne de balayage parmi les lignes de balayage (S1, S2, Sn-1, Sn).

FIG. 1

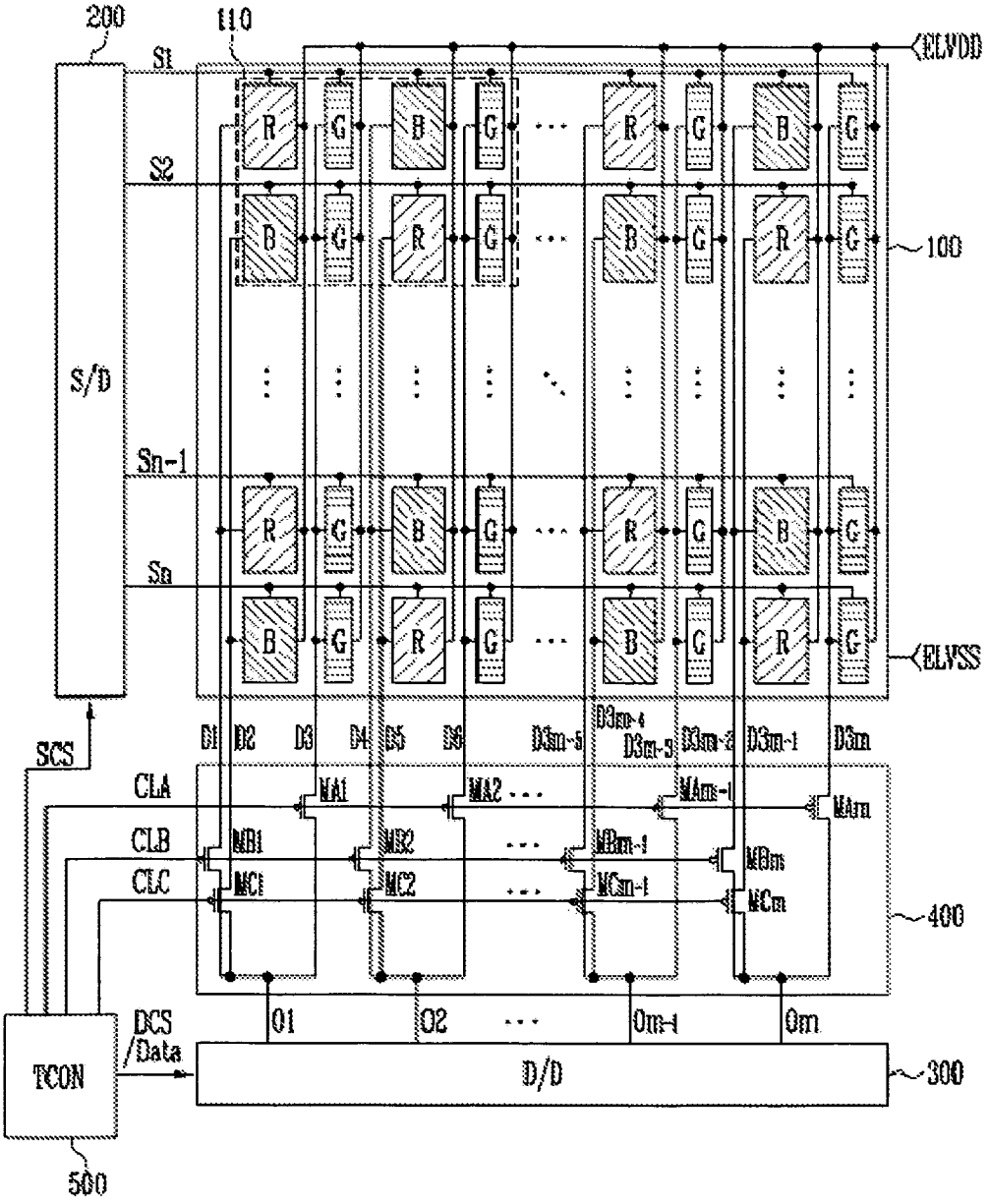

200
110
S1
S2
Sn-1
Sn
S/D
ELVDD
ELVSS
100
R
G
B
SCS
CLA
CLB
CLC
MA1
MA2
MAm-1
MAm
MB1
MB2
MBm-1
MBm
MC1
MC2
MCm-1
MCm
400
O1
O2
Om-1
Om
DCS
/Data
TCON
D/D
300
500

FIG. 2

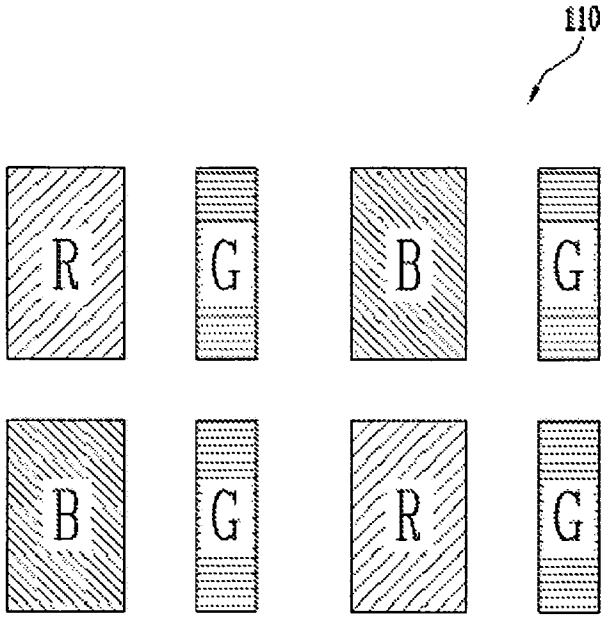
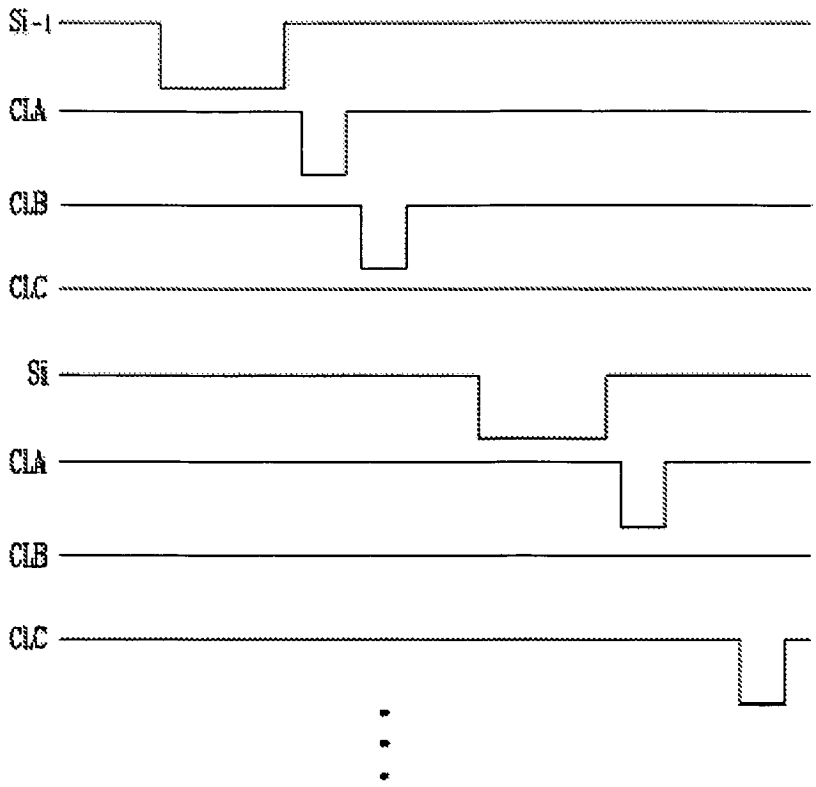


FIG. 3



REFERENCES CITED IN THE DESCRIPTION

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- US 20090167648 A1 **[0009]**
- EP 1764771 A2 **[0009]**
- EP 1635324 A1 **[0009]**

专利名称(译)	有机发光显示装置		
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其他公开文献	EP2280391A1		
外部链接	Espacenet		

摘要(译)

有机发光显示装置包括显示区域（100），该显示区域包括在扫描线（S1，S2，Sn-）的交叉区域处的第一子像素（R），第二子像素（B）和第三子像素（G）。 1，Sn）和数据线（D1，D2，D3，D4，D5，D6，D3m-5，D3m-4，D3m-3，D3m-2，D3m-1，D3m）以重复图案排列，发射不同颜色光的第一，第二和第三子像素（R，B，G），扫描驱动器（200），用于向扫描线（S1，S2，Sn-1，Sn）提供扫描信号;数据驱动器（300），用于向数据线（D1，D2，D3，D4，D5，D6，D3m-5，D3m-4，D3m-3，D3m-2，D3m-1，D3m）提供数据信号;数据驱动器（300）与数据线（D1，D2，D3，D4，D5，D6，D3m-5，D3m-4，D3m-3，D3m-2，D3m-1）之间的数据分配器（400），D3m）用于将数据信号从数据驱动器（300）的输出线（01,02，Om-1，Om）分配到数据线（D1，D2，D3，D4，D5，D6，D3m-5），D3m-4，D3m-3，D3m-2，D3m-1，D3m）。第一和第二子像素（R，B）交替排列在第一列中，第三子像素（G）排列在与第一列相邻的第二列中。

FIG. 1