(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 1 965 370 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
22.01.2014 Bulletin 2014/04

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(21) Application number: **08101553.9**

(22) Date of filing: **13.02.2008**

(54) Organic light emitting display and driving circuit thereof

Organische lichtemittierende Anzeige und Schaltkreis zu ihrer Ansteuerung

Affichage électroluminescent organique et circuit de commande correspondant

(84) Designated Contracting States:
DE FR GB HU

(30) Priority: **02.03.2007 KR 20070020737**

(43) Date of publication of application:
03.09.2008 Bulletin 2008/36

(73) Proprietor: **Samsung Display Co., Ltd.**
Yongin-City, Gyeonggi-Do, 446-711 (KR)

(72) Inventors:
- **Lee, Hyunjung**
  Gyeonggi-do (KR)
- **Chung, Kyunghoon**
  Gyeonggi-do (KR)

(74) Representative: **Hengelhaupt, Jürgen et al**
Gulde Hengelhaupt Ziebig & Schneider
Patentanwälte - Rechtsanwälte
Wallstrasse 58/59
10179 Berlin (DE)

(56) References cited:
EP-A1- 1 653 434
WO-A-2005/122178
US-A- 5 568 163

EP 1 965 370 B1

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] Embodiments of the present invention relate to a light emitting display, e.g., an organic light emitting display, and a driving circuit thereof More particularly, embodiments of the invention relate to light emitting displays and driving circuits thereof in which a single light emitting control driving line is electrically coupled to multiple, e.g., two, rows of pixels of a display and is capable of simultaneously supplying a light emitting control signal to the multiple, e.g., two, rows of pixels simultaneously and/or substantially simultaneously, i.e., is capable of respectively supplying a light emitting control signal to the multiple, e.g., two, rows of pixels during a same driving period in order to reduce a number of driving circuits, reduce manufacturing cost, and improve yield.

2. Description of the Related Art

[0002] In general, an organic light emitting display is a display device that is capable of electrically exciting a light emitting material, e.g., a fluorescent or phosphorescent organic compound, to emit light and display an image by driving N x M organic light emitting diodes (OLEDs). An OLED may include an anode, e.g., indium tin oxide (ITO), an organic thin film, and a cathode, e.g., metal. The organic thin film may include multi-layers, e.g., an emitting layer (EML) in which light is emitted when electrons are combined with holes, an electron transport layer (ETL) in which the electrons are transported, and a hole transport layer (HTL) in which the holes are transported. The organic thin film may further include an electron injecting layer (EIL) in which additional electrons are injected and a hole injecting layer (HIL) in which holes are injected.

[0003] Such OLEDs may be driven using a passive matrix method and/or an active matrix method in which an MOS (metal oxide silicon) thin film transistor (TFT) may be used. In the passive matrix method, an anode and a cathode, which extend perpendicular to each other, may be used to select and drive a line. In the active matrix method, each of the TFTs and a capacitor is connected to an ITO pixel electrode to store a voltage using the capacitance of the capacitor.

[0004] Such organic light emitting displays may be used as a display device for a variety of devices, e.g., a personal computer, a mobile phone, a portable information terminal, such as a PDA, or a display device for a plurality of information equipment.

[0005] A plurality of light emitting display devices that have a relatively lighter-weight and smaller size than cathode ray tube displays have been developed. For example, organic light emitting displays have been developed. The organic light emitting displays also have relatively excellent luminous efficiency, brightness, wide-viewing angle, and fast response speed.

[0006] However, as the resolution of the organic light emitting displays increases, the size of a driving unit used to drive the pixels thereof becomes large. To help reduce the size of the organic light emitting display, a dead space is used for the driving unit thereof. However, the amount of dead space of a real product, e.g., an organic light emitting display, is limited. If the size of the driving unit for driving the relatively higher-resolution organic light emitting display becomes larger than the size of the limited dead space, the size of the organic light emitting display increases. Accordingly, there is a problem in that the size of the organic light emitting display may be increased as a result of, e.g., the relatively large size of the driving unit.

[0007] Further, many light emitting control driving circuits include both PMOS transistors and NMOS transistors. Such light emitting control drivers thus require additional processing steps and/or substrate. Accordingly, there is a problem in that the organic light emitting display may become relatively large and heavy, and the processing thereof may become complicated.

[0008] EP 1 653 434 A1 (SAMSUNG SDI CO LTD [KR]) 3 May 2006 (2006-05-03) Scan driving for an (O)LED display. The technical problem to be solved is of how to increase the aperture ratio of a pixel circuitry including an illumination control transistor, and of how to design the scan driver thereof. The proposed technical solution is: To share the illumination control line between a plurality of pixel lines and to include a (N)OR gate-network for generating the signal delivered to illumination control lines (summation of scan periods of rows sharing the same illumination control line).

SUMMARY OF THE INVENTION

[0009] The present invention as defined in the attached set of claims 1 to 7 is therefore directed to providing a light emitting display and a driving circuit thereof that substantially overcome one or more of the problems due to the limitations and disadvantages of the related art.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The above and other features and advantages of the present invention will become more apparent to those of ordinary skill in the art by describing in detail exemplary embodiments thereof with reference to the attached drawings, in which:

FIG. 1 illustrates a block diagram of an organic light emitting display according to an exemplary embodiment of the invention;

FIG. 2 illustrates a block diagram of an exemplary embodiment of a light emitting control driver employable by the organic light emitting display shown in FIG. 1;

FIG. 3 illustrates a circuit diagram of a light emitting control driving circuit employable by the light emitting control driver shown in FIG. 2;

FIG. 4 illustrates a timing diagram of exemplary signals employable for driving the light emitting control driving circuit shown in FIG. 3;

FIG. 5 illustrates a circuit diagram of an operating state of the light emitting control driving circuit shown in FIG. 3 during a first driving period;

FIG. 6 illustrates a circuit diagram of an operating state of the light emitting control driving circuit shown in FIG. 3 during a second driving period;

FIG. 7 illustrates a circuit diagram of an operating state of the light emitting control driving circuit shown in FIG. 3 during a third driving period;

FIG. 8 illustrates a circuit diagram of another exemplary embodiment of a light emitting control driving circuit employable by the light emitting control driver shown in FIG. 2;

FIG. 9 illustrates a timing diagram of exemplary signals employable for driving the light emitting control driving circuit shown in FIG. 8; and illustrates a timing diagram of exemplary signals employable for driving the light emitting control driving circuit shown in FIG. 8; and

FIG. 10 illustrates a timing diagram of exemplary signals employable for driving the light emitting control driver shown in FIG. 2.

DETAILED DESCRIPTION OF THE INVENTION

[0011] Korean Patent Application No. 10-2007-0020737, filed on March 2, 2007, in the Korean Intellectual Property Office, and entitled: "Organic Light Emitting Display and Driving Circuit Thereof," is incorporated by reference herein in its entirety.

[0012] Aspects of the present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are illustrated. Aspects of the invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0013] Throughout the specification, like reference numerals refer to like elements having similar structures or operations throughout the specification. Further, it will be understood that when one part is described as being electrically coupled to another part, the two parts may be directly connected to each other or may be indirectly connected via other elements positioned or connected therebetween.

[0014] FIG. 1 illustrates a block diagram of an organic light emitting display 100 according to an exemplary embodiment of the invention.

[0015] As shown in FIG. 1, the organic light emitting display 100 may include a scan driver 110, a data driver 120, a light emitting control driver 130, and an organic light emitting display panel (hereinafter, referred to as panel 140).

[0016] The panel 140 may include a plurality of scan lines (Scan[1], Scan[2], ..., Scan[n]) and a plurality of light emitting control lines (Em[1], Em[2], ···, Em[n/2]) arranged in a row direction, a plurality of data lines (Data [1], Data[2], ···, Data[m]) arranged in a column direction, and a plurality of pixels 141 defined by the plurality of scan lines (Scan[1], Scan[2], ···, Scan[n]), the plurality of data lines (Data[1], Data[2], ···, Data[m]), and the plurality of light emitting control lines (Em[1], Em[2], ···, Em[n/2]).

[0017] The pixels 141 may be formed in pixel regions defined by respective ones of two adjacent scan lines (Scan[1], Scan[2], ..., Scan[n]) and two adjacent ones of the data lines (Data[1], Data[2], •••, Data[m]).

[0018] The scan driver 110 may sequentially supply respective scan signals to the panel 140 through the plurality of scan lines (Scan[1], Scan[2], •••, Scan[n]).

[0019] The data driver 120 may sequentially supply respective data signals to the panel 140 through the plurality of data lines (Data[1]; Data[2], •••, Data[m]).

[0020] The light emitting control driver 130 may sequentially supply light emitting control signals to the panel 140 through the plurality of light emitting control lines (Em [1], Em[2], •••, Em[n/2]). The plurality of pixels 141 may be connected to the light emitting control lines (Em[1], Em[2], •••, Em[n/2]) and may receive the respective light emitting control signals to determine a point of time at which current generated in respective ones of the pixels 141 flows to respective light emitting diode thereof. The pixels 141 may be electrically coupled between the light emitting control lines (Em[1], Em[2], •••, Em[n/2]) and the scan lines (Scan[1], Scan[2], •••, Scan[n]). Each of the light emitting control lines (Em[1], Em[2], •••, Em[n/2]) may be electrically coupled to a plurality of, e.g., two, rows of pixels to simultaneously transfer the respective light emitting signal to the corresponding pixels 141 in the plurality of, e.g., two, rows of pixels associated therewith.

[0021] In the description of exemplary embodiments herein, each of the light emitting control lines (Em[1], Em [2], •••, Em[n/2]) will be described as being connected to two rows of the pixels. Further, in the following description of exemplary embodiments a predetermined group, e.g., a row, of the pixels 141 may be referred to as a pixel unit. However, embodiments of the invention are not limited thereto.

[0022] In some embodiments of the invention, e.g., a first light emitting control line (Em[1]) may be electrically coupled to the pixels 141 of first and second pixel units PS_1, PS_2 (see FIG. 2) that may be electrically coupled to the first and second scan lines (Scan[1], Scan[2]) to simultaneously transfer the first light emitting control signal to the pixels 141 of the first and second pixel units PS_1, PS_2. By electrically coupling each of the light emitting control lines (Em[1], Em[2], •••, Em[n/2]) to two

of the scan lines (Scan[1], Scan[2], •••, Scan[n]), the size of the light emitting control driver 130 according to embodiments of the invention may be reduced to, e.g., one-half of a light emitting control driver having, e.g., a separately driven light emitting control line electrically coupled to each of the scan lines, i.e., a separate light emitting control driving unit for each of the light emitting control lines and each of the scan lines.

[0023] Further, the light emitting control driver 130 according to embodiments of the invention may be implemented using transistors of only a same kind as transistors of the pixels 141 such that the light emitting control driver 130 may be formed on a same substrate without additional processing when forming the panel 140 of the light emitting display. Therefore, embodiments of the invention may enable the light emitting control driver 130 to be formed on the same substrate as the pixels 141 without requiring additional processing and/or an additional chip.

[0024] FIG. 2 illustrates a block diagram of an exemplary embodiment of the light emitting control driver 130 employable by the organic light emitting display shown in FIG. 1. As illustrated in FIG. 2, the light emitting control driver 130 may include first to n/2 light emitting control driving units (Emission_1 to Emission_n/2). The first to the n/2 light emitting control driving units (Emission_1 to Emission_n/2) may be electrically coupled to first to nth pixel units (PS_1 to PS_n) to apply a respective light emitting control signal to each of the pixel units (PS_1, PS_2, ...,PS_n). More particularly, in embodiments of the invention, each of the n pixel units (PS_1, PS_2, ... PS_n) may be electrically coupled to a respective one of the n/2 light emitting control driving units (Emission_1, Emission_2, ..., Emission_n/2), where n may be any positive integer, and multiple ones, e.g., two, of the n pixel units (PS_1, PS_2, ... PS_n) may be coupled to each of the light emitting control driving units (Emission_1 to Emission_n/2). Thus, embodiments of the invention may enable a size of a light emitting control driver to be reduced to, e.g., one half of a light emitting control driver in which only one pixel unit is electrically coupled to each light emitting control driving unit thereof.

[0025] The first light emitting control driving unit (Emission_1) may include a first clock terminal (clka) electrically coupled to a first clock line (CLK1), a second clock terminal (clkb) electrically coupled to a first negative clock line (CLKB1), an input terminal (In) electrically coupled to an initial driving line (Sp), an output terminal (Out) and a negative output terminal (OutB). The input terminal (In) may receive an initial driving signal. The first light emitting control driving unit (Emission_1) may output a first light emitting control signal to a first light emitting control line (Em[1]), which may be electrically coupled to the output terminal (Out) thereof. The first light emitting control driving unit (Emision_1) may also output a first light emitting negative control signal to a first light emitting negative control line (EmB[1]), which may be electrically coupled to the negative output terminal (OutB) thereof.

[0026] In some embodiments of the invention, the first light emitting control driving unit (Emission_1) may be electrically coupled to the first pixel unit (PS_1) and the second pixel unit (PS_2), and may apply the first light emitting control signal to the first pixel unit (PS_1) and the second pixel unit (PS_2) respectively. More particularly, the first light emitting control line (Em[1]) may be electrically coupled to the first pixel unit (PS_1) and the second pixel unit (PS_2), and the first light emitting control driving unit (Emission_1) may apply the first light emitting control signal to the first pixel unit (PS_1) and the second pixel unit (PS_2) simultaneously, e.g., respectively during a same driving period.

[0027] The second light emitting control driving unit (Emission_2) may include a first clock terminal (clka) electrically coupled to a second clock line (CLK2), a second clock terminal (clkb) electrically coupled to a second negative clock line (CLKB2), an input terminal (In), an output terminal (Out) and a negative output terminal (OutB). The input terminal (In) thereof may be electrically coupled to the first light emitting negative control line (EmB[1]), and may receive the first light emitting negative control signal. The second light emitting control driving unit (Emission_2) may output a second light emitting control signal to a second light emitting control line (Em[2]), which may be electrically coupled to the output terminal (Out) thereof and may output a second light emitting negative control signal to a second light emitting negative control line (EmB[2]), which may be electrically coupled to the negative output terminal (OutB) thereof.

[0028] In some embodiments of the invention, the second light emitting control driver (Emission_2) may be electrically coupled to a third pixel unit (PS_3) and a fourth pixel unit (PS_4) via the second light emitting control line (Em[2]), and may apply the second light emitting control signal to the third pixel unit (PS_3) and the fourth pixel unit (PS_4) respectively. More particularly, the second light emitting control driving unit (Emission_2) may apply the second light emitting control signal to the third pixel unit (PS_3) and the fourth pixel unit (PS_4) simultaneously, e.g., respectively during a same driving period.

[0029] The third light emitting control driver (Emission_3) may include a first clock terminal (clka) electrically coupled to the first negative clock line (CLKB1), a second clock terminal (clkb) electrically coupled to the first clock line (CLK1), an input terminal (In), an output terminal (Out) and a negative output terminal (OutB). The input terminal (In) thereof may be electrically coupled to the second light emitting negative control line (EmB[2]) and may receive the second light emitting negative control signal. The third light emitting control driving unit (Emission_3) may output a third light emitting control signal to a third light emitting control line (Em[3]), which may be electrically coupled to the output terminal (Out) thereof and may output a third light emitting negative control signal to a third light emitting negative control line (EmB[3]), which may be electrically coupled to the negative output

terminal (OutB) thereof.

[0030] In some embodiments of the invention, the third light emitting control driving unit (Emission_3) may be electrically coupled to the fifth pixel unit (PS_5) and the sixth pixel unit (PS_6) via the third light emitting control line (Em[3]). The third light emitting control driving unit (Emission_3) may apply the third light emitting control signal to the fifth pixel unit (PS_5) and the sixth pixel unit (PS_6) respectively. More particularly, the third light emitting control driving unit (Emission_3) may apply the third light emitting control signal to the fifth pixel unit (PS_5) and the sixth pixel unit (PS_6) simultaneously, e.g., respectively during a same driving period.

[0031] The fourth light emitting control driving unit (Emission_4) may include a first clock terminal (clka) electrically coupled to the second negative clock line (CLKB2), a second clock terminal (clkb) electrically coupled to the second clock line (CLK2), and input terminal (In), an output terminal (Out) and a negative output terminal (OutB). The input terminal (In) may be electrically coupled to the third light emitting negative control line (EmB[3]) and may receive the third light emitting negative control signal. The fourth light emitting control driving unit (Emission_4) may output a fourth light emitting control signal to a fourth light emitting control line (Em[4]), which may be electrically coupled to the output terminal (Out) thereof. The fourth light emitting control driving unit (Emission_4) may output a fourth light emitting negative control signal to the fourth light emitting negative control line (EmB[4]), which may be electrically coupled to the negative output terminal (OutB) thereof.

[0032] In some embodiments of the invention, the fourth light emitting control driving unit (Emission_4) may be electrically coupled to a seventh pixel unit (PS_7) and an eighth pixel unit (PS_8), and may apply the fourth light emitting control signal to the seventh pixel unit (PS_7) and the eighth pixel unit (PS_8) respectively. More particularly, the fourth light emitting control driving unit (Emission_4) may apply the fourth light emitting control signal to the seventh pixel unit (PS_7) and the eight pixel unit (PS_8) simultaneously, e.g., respectively during a same driving period.

[0033] In some embodiments of the invention, the light emitting control driving units (Emission_1 to Emission_n/2) may be coupled with the pixel units (PS_1 to PS_n) in a pattern following the coupling scheme described above with regard to the first, second, third and fourth light emitting control driving units (Emission_1, Emission_2, Emission_3 and Emission_4).

[0034] More particularly, e.g., in some embodiments of the invention, in the odd-numbered light emitting control driving units (Emission_1, Emission_3, Emission_5, etc.), first and second clock terminals (clka, clkb) thereof may be alternately coupled to the first clock line (CLK1) and the first negative clock line (CLKB1). That is, e.g., if the first and second clock terminals (clka, clkb) of the fifth light emitting control driving unit (Emission_5) are respectively electrically coupled to the first clock line (CLK1) and the first negative clock line (CLKB1) thereof, the first and second clock terminals (clka, clkb) of the seventh (e.g., subsequent odd-numbered) light emitting control driving unit (Emission_7) may be respectively electrically coupled to the first negative clock line (CLKB1) and the first clock line (CLK1) thereof.

[0035] More particularly, e.g., in some embodiments of the invention, in the even-numbered light emitting control driving units (Emission_2, Emission_4, Emission_6, etc.) first and second clock terminals (clka, clkb) thereof may be alternately coupled to the second clock line (CLK2) and the first negative clock line (CLKB2). That is, e.g., if the first and second clock terminals (clka, clkb) of the sixth light emitting control driving unit (Emission_6) are respectively electrically coupled to the second clock line (CLK2) and the second negative clock line (CLKB2) thereof, the first and second clock terminals (clka, clkb) of the eighth (e.g., subsequent even-numbered) light emitting control driving unit (Emission_8) may be respectively electrically coupled to the second negative clock line (CLKB2) and the second clock line (CLK2) thereof.

[0036] Further, with regard to other terminals of the light emitting control driving units, the input terminal (In) thereof may be electrically coupled to the light emitting negative control line of a previous light emitting control driver, a light emitting control signal may be output via the light emitting control line electrically coupled to the output terminal (Out) thereof, and a light emitting negative control signal may be output via the light emitting negative control line of the negative output terminal (OutB) thereof.

[0037] FIG. 3 illustrates a circuit diagram of a light emitting control driving circuit 300 employable by the light emitting control driver 130 shown in FIG. 2.

[0038] More particularly, the light emitting control driving circuit 300 may be employed by each of the light emitting control driving units (Emission_1, Emission_2, Emission_n/2). As illustrated in FIG. 3, the light emitting control driving circuit 300 may include a first switching element (S1), a second switching element (S2), a third switching element (S3), a fourth switching element (S4), a fifth switching element (S5), a sixth switching element (S6), a seventh switching element (S7), an eighth switching element (S8), a ninth switching element (S9), a first storage capacitor (C1) and a second storage capacitor (C2).

[0039] The first switching element (S1) may include a first electrode (a drain electrode or a source electrode) electrically coupled to a control electrode of the third switching element (S3), a second electrode (a source electrode or a drain electrode) electrically coupled to the input terminal (In) of the respective light emitting control driving unit (e.g., Emission_1), and a control electrode (gate electrode) electrically coupled to the first clock terminal (clka). When a clock signal of a low level is applied to the control electrode of the first switching element (S1), the first switching element (S1) is turned on and thus, a signal applied to the input terminal (In) is applied to the

control electrode of the third switching element (S3).

[0040] The second switching element (S2) may include a first electrode electrically coupled to the first power supply line (VDD), a second electrode electrically coupled between a first electrode of the third switching element (S3), a control electrode of the fourth switching element (S4) and a control electrode of the seventh switching element (S7), and a control electrode electrically coupled to the first clock terminal (clka). When a clock signal of a low level is applied to the control electrode of the first switching element (S2), the second switching element (S2) is turned on and thus, a first power voltage applied from the first power supply line (VDD) is applied to the control electrode of the fourth switching clement (S4) and the control electrode of the seventh switching element (S7).

[0041] The third switching element (S3) may include a first electrode electrically coupled between the control electrode of the fourth switching element (S4) and the control electrode of the seventh switching element (S7), a second electrode electrically coupled to the second clock terminal (clkb), and a control electrode electrically coupled to the first electrode of the first switching element (S1). When an input signal of a low level transmitted from the first switching element (S1) is applied to the control electrode of the third switching element (S3), the third switching element (S3) is turned on and thus, the clock signal applied from the second clock terminal (clkb) is applied to the control electrode of the fourth switching element (S4) and the control electrode of the seventh switching element (S7).

[0042] The fourth switching element (S4) may include a first electrode electrically coupled to the first power supply line (VDD), a second electrode electrically coupled between the first electrode of the fifth switching element (S5), a control electrode of the sixth switching element (S6) and a control electrode of the ninth switching element (S9), a control electrode electrically coupled between the second switching element (S2) and the third switching element (S3). When an input signal of a low level, e.g., clock signal of a low level, transmitted from the third switching element (S3) is applied to the control electrode of the fourth switching element (S4), the fourth switching element (S4) is turned on and thus, the first power voltage applied from the first power supply line (VDD) is applied to the control electrode of the sixth switching element (S6) and the control electrode of the ninth switching element (S9).

[0043] The fifth switching element (S5) may include a first electrode electrically coupled between the control electrode of the sixth switching element (S6) and the control electrode of the ninth switching element (S9), a second electrode electrically coupled to the second power supply line (VSS), and a control electrode electrically coupled to the first clock terminal (clka). When a clock signal of a low level is applied to the control electrode of the fifth switching element (S5), the fifth switching element (S5) is turned on and thus, the second power voltage applied from the second power supply line (VSS) is applied to the control electrode of the sixth switching element (S6) and the control electrode of the ninth switching element (S9).

[0044] The sixth switching element (S6) may include a first electrode electrically coupled to the first power supply line (VDD), a second electrode electrically coupled between the first electrode of the seventh switching element (S7), a control electrode of the eighth switching element (S8) and the negative output terminal (OutB) of the respective light emitting control driving unit, e.g., (Emission_1), and a control electrode electrically coupled between the fourth switching element (S4) and the fifth switching element (S5). When the second power voltage transmitted from the fifth switching element (S5) is applied to the control electrode of the sixth switching element (S6), the sixth switching element (S6) is turned on and thus, the first power voltage applied from the first power supply line (VDD) is output to the control electrode of the eighth switching element (S8) and the negative output terminal (OutB).

[0045] The seventh switching element (S7) may include a first electrode electrically coupled between the control electrode of the eighth switching element (S8) and the negative output terminal (OutB) of the respective light emitting control driving unit, e.g., (Emission_1), a second electrode electrically coupled to the second power supply line (VSS), and a control electrode electrically coupled between the second switching element (S2) and the third switching element (S3). When a clock signal of a low level transmitted from the third switching element (S3) is applied to the control electrode of the seventh switching element (S7), the seventh switching element (S7) is turned on and thus, the second power voltage applied from the second power supply line (VSS) is output to the control electrode of the eighth switching element (S8) and the negative output terminal (OutB).

[0046] The eighth switching element (S8) may include a first electrode electrically coupled to the first power supply line (VDD), a second electrode electrically coupled between the first electrode of the ninth switching element (S9), and the output terminal (Out) of the respective light emitting control driving unit, e.g., (Emission_1), and a control electrode electrically coupled between the sixth switching element (S6) and the seventh switching element (S7). When the second power voltage transmitted from the seventh switching element (S7) is applied to the control electrode of the eighth switching element (S8), the eighth switching element (S8) is turned on and thus, the first power voltage applied from the first power supply line VDD is output to the output terminal (Out).

[0047] The ninth switching element (S9) may include a first electrode electrically coupled to the output terminal (Out), a second electrode electrically coupled to the second power supply line (VSS), and a control electrode electrically coupled between the fourth switching element (S4) and the fifth switching element (S5). When the second power voltage transmitted from the fifth switching

element (S5) is applied to the control electrode of the ninth switching element (S9), the ninth switching element (S9) is turned on and thus, the second power voltage applied from the second power supply line (VSS) is applied to the output terminal (Out).

[0048] The first storage capacitor (C1) may include a first electrode electrically coupled between the first electrode of the first switching element (S1) and the control electrode of the third switching element (S3), and a second electrode electrically coupled between the second switching element (S2) and the third switching element (S3). The first storage capacitor (C1) may store a voltage difference between the first electrode and the control electrode of the third switching element (S3).

[0049] The second storage capacitor (C2) may include a first electrode electrically coupled to the control electrode of the ninth switching element (S9), and a second electrode electrically coupled among the eighth switching element (S8), the ninth switching element (S9), and the output terminal (Out) of the respective light emitting control driving unit, e.g., (Emission_1). The second storage capacitor (C2) may store a voltage difference between the first electrode and the control electrode of the ninth switching element (S9).

[0050] As shown in FIG. 3, all of the switching elements, e.g., S1, S2, S3, S4, S5, S6, S7, S8 and S9, of the light emitting control driving circuits 300 of the light emitting control driving units (Emission_1 to Emission_n/2) may be of a same type, e.g., p-type transistors such as PMOS transistors, but not limited thereto as, e.g., all of the switching elements, e.g., S1 to S9, may be, e.g., n-type transistors.

[0051] If the pixels 141 of the organic light emitting display include transistors of only a same type as transistors of the light emitting control driving circuits, it is possible to simplify the process of forming the organic light emitting display as the light emitting control driving circuits may be formed on a same substrate as the pixels 141 of the display without requiring additional processing. Further, if the light emitting control driving circuits 300 and the pixels 141 are formed on the same substrate, it is possible to reduce the size, weight, and cost of the organic light emitting display. Accordingly, the pixels 141 include, e.g., only p-type transistors, i.e., no n-type transistors, by structuring the light emitting control driving circuit 300 shown in FIG. 3 to include transistors of only p-type, e.g., PMOS transistors, as the first through ninth switching elements (S1 to S9), it is possible to simplify the process of forming the light emitting control driving circuits 300 and the pixels 141 and to form them on a same substrate without requiring additional processing.

[0052] FIG. 4 illustrates a timing diagram of exemplary signals employable for driving the light emitting control driving circuit 300 shown in FIG. 3.

[0053] As shown in FIG. 4, the timing diagram of the light emitting control driving circuit 300 shown in FIG. 3 may include a first driving period (T51), a second driving period (T52) and a third driving period (T53). Operation of the light emitting control driving circuit 300 will be described below with reference to FIGS. 5, 6 and 7 illustrating respective operating states of the light emitting control driving circuit 300.

[0054] More particularly, FIG. 5 illustrates a circuit diagram of an operating state of the light emitting control driving circuit 300 shown in FIG. 3 during the first driving period (T51).

[0055] During the first driving period (T51), when a clock signal of a low level is applied to the first clock terminal (clka), the first switching element (S1), the second switching element (S2) and the fifth switching element (S5) are turned on. More particularly, during the first driving period (T51), the first switching element (S1) may be turned on, and then, an input signal of a low level applied to the input terminal (In) may be applied to the control electrode of the third switching element (S3). When the third switching element (S3) receives the input signal at the low level, the third switching element (S3) is turned on and supplies a clock signal at a high level supplied from a second clock terminal (clkb) to the control electrode of the fourth switching element (S4) and the control electrode of the seventh switching element (S7).

[0056] During the first driving period (T51), the second switching element (S2) is also turned on and applies the first power voltage of the first power supply line (VDD) to the control electrode of the fourth switching element (S4) and the control electrode of the seventh switching element (S7). As a result, the fourth switching element (S4) and the seventh switching element (S7) receiving the clock signal at the high level and the first power voltage of a high level are turned off. Accordingly, the first storage capacitor (C1) coupled between the first electrode and the control electrode of the third switching element (S3) may store a voltage corresponding to a voltage difference between the first power voltage received from the second switching element (S2) and the input signal received from the first switching element (S1).

[0057] Further, during the first driving period (T51), the fifth switching element (S5) is turned on and applies the second power voltage of the second power supply line (VSS) to the control electrode of the sixth switching element (S6) and the control electrode of the ninth switching element (S9) such that the sixth switching element (S6) and the ninth switching element (S9) are turned on. When the sixth switching element (S6) is turned on, the sixth switching element (S6) applies the first power voltage of the first power supply line (VDD) to the control electrode of the eighth switching element (S8) and the negative output terminal (OutB) such that the eighth switching element (S8) is turned off and the first power voltage is output through the negative output terminal (OutB). Further, the ninth switching element (S9) is turned on and outputs the second power voltage of the second power supply line (VSS) to the output terminal (Out). As a result, the second storage capacitor (C2) may store a voltage corresponding to the voltage difference between the second power voltage received from the fifth switching ele-

ment (S5) and the second power voltage received from the ninth switching element (S9). The voltage stored in the second storage capacitor (C2) may be used to compensate for voltage lost in the driving circuit 300 when the second power voltage is output.

[0058] FIG. 6 illustrates a circuit diagram of an operating state of the light emitting control driving circuit 300 shown in FIG. 3 during the second driving period (T52).

[0059] During the second driving period (T52), when a clock signal at a high level is supplied to the first clock terminal (clka), the first switching element (S1), the second switching element (S2), and the fifth switching element (S5) are turned off. At this time, the third switching element (S3) is turned on by the voltage stored in the first storage capacitor (C1) during the first driving period (T51) and supplies the clock signal at a low level supplied from the second clock terminal (clkb) to the control electrode of the fourth switching element (S4) and the control electrode of the seventh switching element (S7). The fourth switching element (S4) and the seventh switching element (S7) are turned on by receiving the clock signal at the low level. The fourth switching element (S4) is turned on and applies the first power voltage of the first power supply line (VDD) to the control electrode of the sixth switching element (S6) and the control electrode of the ninth switching element (S9) such that the sixth switching element (S6) and the ninth switching element (S9) are turned off.

[0060] Further, during the second driving period (T52), the seventh switching element (S7) is turned on and applies the second power voltage of the second power supply line (VSS) to the control electrode of the eighth switching element (S8) and the negative output terminal (OutB) such that the eighth switching element (S8) is turned on and the second power voltage is output through the negative output terminal (OutB). Further, the eighth switching element (S8) is turned on and outputs the first power voltage of the first power supply line (VDD) to the output terminal (Out). At this time, the second storage capacitor (C2) may store the voltage corresponding to the voltage difference between the first power voltage received from the fourth switching element (S4) and the first power voltage received from the eighth switching element (S8). The voltage stored in the second storage capacitor (C2) may be used to compensate for voltage lost in the driving circuit when the first power voltage is output. Since the first switching element (S1) is turned off, the light emitting control driving circuit 300 operates without any change regardless of whether the input signal supplied to the input terminal (In) is at a high level or at a low level.

[0061] FIG. 7 illustrates a circuit diagram of an operating state of the light emitting control driving circuit 300 shown in FIG. 3 during the third driving period (T53).

[0062] During the third driving period (T53), when a clock signal at a low level is supplied to the first clock terminal (clka), the first switching element (S1), the second switching element (S2), and the fifth switching element (S5) are turned on. The first switching element (S1) is turned on and supplies an input signal at a high level transferred from the input terminal (In) to the control electrode of the third switching element (S3) such that the third switching element (S3) is turned off.

[0063] Further, during the third driving period (T53), the second switching element (S2) is turned on and applies the first power voltage of the first power supply line (VDD) to the control electrode of the fourth switching element (S4) and the control electrode of the seventh switching element (S7). The fourth switching element (S4) and the seventh switching element (S7) are turned off due to the first power voltage received from the second switching element (S2).

[0064] Further, during the third driving period (T53), the fifth switching element (S5) is turned on and applies the second power voltage of the second power supply line (VSS) to the control electrode of the sixth switching element (S6) and the control electrode of the ninth switching element (S9) such that the sixth switching element (S6) and the ninth switching element (S9) are turned on. When the sixth switching element (S6) is turned on, the sixth switching element (S6) applies the first power voltage of the first power supply line (VDD) to the control electrode of the eighth switching element (S8) and the negative output terminal (OutB) such that the eighth switching element (S8) is turned off and the first power voltage is output through the negative output terminal (OutB). Further, the ninth switching element (S9) is turned on and outputs the second power voltage of the second power supply line (VSS) to the output terminal (Out). At this time, the second storage capacitor (C2) stores the voltage corresponding to the voltage difference between the second power voltage received from the fifth switching element (S5) and the second power voltage received from the ninth switching element (S9). The voltage stored in the second storage capacitor (C2) may be used to compensate for voltage lost in the driving circuit 300 when the second power voltage is output.

[0065] FIG. 8 illustrates a circuit diagram of a light emitting control driving circuit 300' employable by the light emitting control driver shown in FIG. 2.

[0066] More particularly, in embodiments of the invention, the light emitting control driving circuit 300' may be employed by each of the light emitting control driving units (Emission_1, Emission_2, Emission_n/2). In general, only differences between the first exemplary light emitting control driving circuit 300 shown in Fig. 3 and the second exemplary light emitting control driving circuit 300' shown in FIG. 8 will be described below.

[0067] As shown in FIG. 8, the light emitting control driving circuit 300' may include a first switching element (S1'), the second through ninth switching elements (S2 through S9), the first storage capacitor (C1), and the second storage capacitor (C2).

[0068] The first switching element (S1') may include a first electrode (drain electrode or source electrode) electrically coupled to a control electrode of the third switching element (S3), a second electrode (source electrode or

drain electrode) electrically coupled to the input terminal (In), and a control electrode (gate electrode) electrically coupled to the input terminal (In). When a clock signal at a low level is supplied to the control electrode, the first switching element (S1') is turned on to supply an input signal supplied from the input terminal (In) to the control electrode of the third switching element (S3).

[0069] The coupling scheme of the second through ninth switching elements (S2 through S9), the first storage capacitor (C1) and the second storage capacitor (C2) corresponds to the coupling scheme described above with regard to the first exemplary light emitting control driving circuit 300 shown in Fig. 3.

[0070] FIG. 9 illustrates a timing diagram of exemplary signals employable for driving the light emitting control driving circuit 300' shown in FIG. 8.

[0071] As shown in FIG. 9, in embodiments of the invention, like the timing diagram of the light emitting control driving circuit 300 shown in FIG. 5, the timing diagram of the exemplary signals employable for driving light emitting control driving circuit 300' shown in FIG. 8 may include the first driving period (T51), the second driving period (T52), and the third driving period (T53).

[0072] During the first driving period (T51), when an input signal at a low level is supplied to the input terminal (In), the first switching element (S1') is turned on and a clock signal at a low level is supplied to the first clock terminal (clka) such that the second switching element (S2) and the fifth switching element (S5) are turned on. First, the first switching element (S1') is turned on to supply an input signal at the low level supplied from the input terminal (In) to the control electrode of the third switching element (S3). When the third switching element (S3) receives the input signal at the low level, the third switching element (S3) is turned on and supplies a clock signal at a high level supplied from a second clock terminal (clkb) to the control electrode of the fourth switching element (S4) and the control electrode of the seventh switching element (S7). The fourth switching element (S4) and the seventh switching element (S7), which receive the clock signal at the high level and the first power voltage, are turned off. The first storage capacitor (C1) coupled between the first electrode and the control electrode of the third switching element (S3) may store a voltage corresponding to the voltage difference of the first power voltage received from the second switching element (S2) and the input signal received from the first switching element (S1').

[0073] Next, the fifth switching element (S5) is turned on and applies the second power voltage of the second power supply line (VSS) to the control electrode of the sixth switching element (S6) and the control electrode of the ninth switching element (S9) such that the sixth switching element (S6) and the ninth switching element (S9) are turned on. When the sixth switching element (S6) is turned on, the sixth switching element (S6) applies the first power voltage of the first power supply line (VDD) to the control electrode of the eighth switching element (S8) and the negative output terminal (OutB) such that the eighth switching element (S8) is turned off and the first power voltage is output through the negative output terminal (OutB). Further, the ninth switching element (S9) is turned on and outputs the second power voltage of the second power supply line (VSS) to the output terminal (Out). At this time, the second storage capacitor (C2) may store the voltage corresponding to the voltage difference between the second power voltage received from the fifth switching element (S5) and the second power voltage received from the ninth switching element (S9). The voltage stored in the second storage capacitor (C2) may be used to compensate for voltage lost in the driving circuit 300' when the second power voltage is output.

[0074] During the second driving period (T52), when an input signal at a high level is supplied to the input terminal (In), the first switching element (S1') is turned off. Further, when the clock signal at a high level is supplied to the first clock terminal (clka), the second switching element (S2) and the fifth switching element (S5) are turned off. At this time, the third switching element (S3) is turned on with the voltage stored in the first storage capacitor (C1) during the first driving period (T51), and supplies the clock signal at a low level supplied from the second clock terminal (clkb) to the control electrode of the fourth switching element (S4) and the control electrode of the seventh switching element (S7). The fourth switching element (S4) and the seventh switching element (S7) receive the clock signal at the low level and are turned on. First, the fourth switching element (S4) is turned on and applies the first power voltage of the first power supply line (VDD) to the control electrode of the sixth switching element (S6) and the control electrode of the ninth switching element (S9) such that the sixth switching element (S6) and the ninth switching element (S9) are turned off.

[0075] Next, the seventh switching element (S7) is turned on and applies the second power voltage of the second power supply line (VSS) to the control electrode of the eighth switching element (S8) and the negative output terminal (OutB) such that the eighth switching element (S8) is turned on and the second power voltage is output through the negative output terminal (OutB). Further, the eighth switching element (S8) is turned on and outputs the first power voltage of the first power supply line (VDD) to the output terminal (Out). At this time, the second storage capacitor (C2) stores the voltage corresponding to the voltage difference between the first power voltage received from the fourth switching element (S4) and the first power voltage received from the eighth switching element (S8). The voltage stored in the second storage capacitor (C2) may be used to compensate for the voltage lost in the driving circuit 300' when the first power voltage is output. Further, since the first switching element (S1') is turned off, the light emitting control driving circuit 300' operates without any change regardless of whether the input signal to be supplied to the input terminal (In) is at a high level or at a low level.

[0076] During the third driving period (T53), when the input signal at a high level is supplied to the input terminal (In), the first switching element (S1') is turned off. Further, when the clock signal at a low level is supplied to the first clock terminal (clka), the second switching element (S2) and the fifth switching element (S5) are turned on. When the second switching element (S2) is turned on, the first power voltage of the first power supply line (VDD) is applied to the control electrode of the fourth switching element (S4) and the control electrode of the seventh switching element (S7). The fourth switching element (S4) and the seventh switching element (S7) are turned off due to the first power voltage received from the second switching element (S2). When the fifth switching element (S5) is turned on, the second power voltage of the second power supply line (VSS) is applied to the control electrode of the sixth switching element (S6) and the control electrode of the ninth switching element (S9) such that the sixth switching element (S6) and the ninth switching element (S9) are turned on. When the sixth switching element (S6) is turned on, the sixth switching element (S6) applies the first power voltage of the first power supply line (VDD) to the control electrode of the eighth switching element (S8) and the negative output terminal (OutB) such that the eighth switching element (S8) is turned off and the first power voltage is output through the negative output terminal (OutB). Further, the ninth switching element (S9) is turned on and outputs the second power voltage of the second power supply line (VSS) to the output terminal (Out). At this time, the second storage capacitor (C2) stores the voltage corresponding to the voltage difference between the second power voltage received from the fifth switching element (S5) and the second power voltage received from the ninth switching element (S9). The voltage stored in the second storage capacitor (C2) may be used to compensate for voltage lost in the driving circuit 300' when the second power voltage is output.

[0077] FIG. 10 illustrates a timing diagram of exemplary signals employable for driving the light emitting control driver 130 shown in FIG. 2.

[0078] As described above, the light emitting control driver 130 described below may include, e.g., the light emitting control driving circuit 300 and/or 300' described in FIGS. 3 and 8. That is, operation of the first light emitting control driving unit (Emission_1) to the n/2-th light emitting control driving unit (Emission_n/2) may be the same as described with regard to the timing diagrams illustrated in FIGS. 4 and 9.

[0079] As illustrated in FIG. 10, the timing chart of the light emitting control driver 130 may include the first driving period (T1), the second driving period (T2), the third driving period (T3), the fourth driving period (T4) and the fifth driving period (T5).

[0080] As described above, the first light emitting control driving unit (Emission_1) may include a first clock terminal (clka) electrically coupled to the first clock line (CLK1), a second clock terminal (clkb) electrically coupled to the first negative clock line (CLKB1), and an input terminal (In) electrically coupled to the initial driving line (Sp).

[0081] During the first driving period (T1), the first light emitting control driving unit (Emission_1) may receive a first clock signal at a low level, a first negative clock signal of a high level, and an initial driving signal at a low level, and may output a first light emitting control signal at a low level to the first light emitting control line (Em[1]) of an output terminal (Out) thereof, and may output the first light emitting negative control signal at a high level to the first light emitting negative control line (EmB[1]) of a negative output terminal (OutB) thereof. Thus, in embodiments of the invention, during the first driving period (T1), the operation of the first light emitting control driving unit (Emission_1) may be same as the operation of the light emitting control driving circuit 300 and/or 300' during the first driving period (T51), as described with reference to FIGS. 4 and 9.

[0082] During the second driving period (T2), the first light emitting control driving unit (Emission_1) may receive a first clock signal at a high level, a first negative clock signal at a low level, and an initial driving signal at a high level, may output the first light emitting control signal of a high level to the first light emitting control line (Em[1]) via the output terminal (Out) thereof, and may output the first light emitting negative control signal at a low level to the first light emitting negative control line (EmB[1]) via the negative output terminal (OutB) thereof. Thus, in embodiments of the invention, during the second driving period (T2), the operation of the first light emitting control driving unit (Emission_1) may be same as the operation of the light emitting control driving circuit 300 and/or 300' during the second driving period (T52), as described with reference to FIGS. 4 and 9.

[0083] Further, during the second driving period (T2), when the first light emitting control signal at a high level may be output by the first light emitting control driving unit (Emission_1) to the first light emitting control line (Em[1]), the first pixel unit (PS_1) and the second pixel unit (PS_2) may operate when they respectively receive a scan signal at a low level from the first scan line (Scan [1]) and the second scan line (Scan[2]).

[0084] As described above, the second light emitting control driving unit (Emission_2) may include a first clock terminal (clka) electrically coupled to the second clock line (CLK2), a second clock terminal (CLKB) electrically coupled to the second negative clock line (CLKB2), and an input terminal (In) electrically coupled to the first light emitting negative control line (EmB[1]).

[0085] During the second driving period (T2), the second light emitting control driving unit (Emission_2) may receive the second clock signal at a low level, a second negative clock signal at a high level, and a first light emitting negative control signal at a low level, may output the second light emitting control signal at a low level to the second light emitting control line (Em[2]) of the output terminal (Out) thereof, and may output the second light

emitting negative control signal of a high level is output to the second light emitting negative control line (EmB [2]) of the negative output terminal (OutB) thereof. Thus, in embodiments of the invention, during the second driving period (T2), the operation of the second light emitting control driving unit (Emission_2) may be the same as the operation of the light emitting control driving circuit 300, 300' during the first driving unit (T51), as described with reference to FIGS. 4 and 9.

[0086] During the third driving period (T3), the first light emitting control driving unit (Emission_1) may operate in a same manner as it operated during the second driving period (T2).

[0087] During the third driving period (T3), a second clock signal at a high level, a second negative clock signal at a low level, and a first light emitting negative control signal at a low level may be applied to the second light emitting control driving unit (Emission_2), and the second light emitting control driving unit (Emission_2) may output the second light emitting control signal at a high level to the second light emitting control line (Em[2]) via the output terminal (Out) thereof, and the second light emitting negative control signal at a low level to the second light emitting negative control line (EmB[2]) via the negative output terminal (OutB) thereof. Thus, in embodiments of the invention, during the third driving period (T3), the operation of the second light emitting control driving unit (Emission_2) may be the same as the operation of the light emitting control driving circuit 300, 300' during the second driving period (T52) described with reference to FIGS. 4 and 9.

[0088] Further, during the third driving period (T3), when the second light emitting control signal at a high level may be output by the second light emitting control driving unit (Emission_2) to the second light emitting control line (Em[2]), the third pixel unit (PS_3) and the fourth pixel unit (PS_4) may operate when they respectively receive a scan signal at a low level from the third scan line (Scan[3]) and the fourth scan line (Scan[4]).

[0089] As described above, the third light emitting control driving unit (Emission_3) may include a first clock terminal (clka) electrically coupled to the first negative clock line (CLKB1), a second clock terminal (clkb) electrically coupled to the first clock line (CLK1), and an input terminal (In) electrically coupled to the second light emitting negative control line (EmB[2]).

[0090] During the third driving period (T3), the third light emitting control driving unit (Emission_3) may receive a first clock signal at a high level, a first negative clock signal at a low level, and a second light emitting negative control signal at a low level, and the third light emitting control driving unit (Emission_3) may output the third light emitting control signal at a low level to the third light emitting control line (Em[3]) via the output terminal (Out) thereof, and the third light emitting negative control signal at a high level to the third light emitting negative control line (EmB[3]) via the negative output terminal (OutB) thereof. Thus, in embodiments of the invention, during the third driving period (T3), the operation of the third light emitting control driving unit (Emission_3) may be the same as the operation of the light emitting control driving circuit 300, 300' during the first driving period (T51), as described with regard to FIGS. 4 and 9.

[0091] During the fourth driving period (T4), a first clock signal at a low level, a first negative clock signal at a high level, and an initial driving signal of a high level may be applied to the first light emitting control driving unit (Emission_1), and the first light emitting control driving unit (Emission_1) may output the first light emitting control signal at a low level to the first light emitting control line (Em[1]) via the output terminal (Out) thereof, and may output the first light emitting negative control signal at a high level to the first light emitting negative control line (EmB[1]) via the negative output terminal (OutB) thereof. Thus, in embodiments of the invention, during the fourth driving period (T4), the operation of the first light emitting control driving unit (Emission _1) may be the same as the operation of the light emitting control driving circuit 300, 300' during the third driving period (T53), as described with reference to FIGS. 4 and 9.

[0092] During the fourth driving period (T4), the second light emitting control driving unit (Emission_2) may operate in a same manner as it operated during the third driving period (T3).

[0093] During the fourth driving period (T4), the third light emitting control driving unit (Emission_3) may receive a first clock signal at a low level, a first negative clock signal at a high level, and a second light emitting negative control signal at a high level, and the third light emitting control driving unit (Emission_3) may output the third light emitting control signal at a high level to the third light emitting control line (Em[3]) via the output terminal (Out) thereof, and the third light emitting negative control signal at a low level to the third light emitting negative control line (EmB[3]) via the negative output terminal (OutB) thereof. Thus, in embodiments of the invention, during the fourth driving period (T4), the operation of the third light emitting control driving unit (Emission_3) may be the same as the operation of the light emitting control driving circuit 300, 300' during the second driving period (T52), as described in FIGS. 4 and 9.

[0094] Further, during the fourth driving period (T4), when the third light emitting control signal at a high level is output to the third light emitting control line (Em[3]) by the third light emitting control driving unit (Emission_3), the fifth pixel unit (PS_5) and the sixth pixel unit (PS_6) may operate when they respectively receive a scan line at a low level from the fifth scan line (Scan[5]) and the sixth scan line (Scan[6]).

[0095] As described above, the fourth light emitting control driving unit (Emission_4) may include a first clock terminal (clka) electrically coupled to the second negative clock line (CLKB2), a second clock terminal (clkb) electrically coupled to the second clock line (CLK2), and an input terminal (In) electrically coupled to the third light emitting negative control line (EmB[3]).

[0096] During the fourth driving period (T4), the fourth light emitting control driving unit (Emission_4) may receive a second clock signal at a high level, a second negative clock signal of a low level, and a third light emitting negative control signal at a low level, and the fourth light emitting control driving unit (Emission_4) may output the fourth light emitting control signal at a low level to the fourth light emitting control line (Em[4]) via the output terminal (Out) thereof, and the fourth light emitting negative control signal at a high level to the fourth light emitting negative control line (EmB[4]) via the negative output terminal (OutB) thereof. Thus, in embodiments of the invention, during the fourth driving period (T4), the operation of the fourth light emitting control driving unit (Emission_4) may be the same as the operation of the light emitting control driving circuit 300, 300' during the first driving period (T51), as described with regard to FIGS. 4 and 9.

[0097] During the fifth driving period (T5), the first light emitting control driving unit (Emission_1) may operate in a same manner as it operated during the fourth driving period (T4).

[0098] During the fifth driving period (T5), the second light emitting control driving unit (Emission_2) may receive a second clock signal at a low level, a second negative clock signal at a high level, and a first light emitting negative control signal at a high level, and the second light emitting control driving unit (Emission_2) may output the second light emitting control signal at a low level to the second light emitting control line (Em[2]) via the output terminal (Out) thereof, and the second light emitting negative control signal at a high level to the second light emitting negative control line (EmB[2]) via the negative output terminal (OutB) thereof. Thus, in embodiments of the invention, during the fifth driving period (T5), the operation of the second light emitting control driving unit (Emission_2) may be the same as the operation of the light emitting control driving circuit 300, 300' during the third driving period (T53), as described with regard to FIGS. 4 and 9.

[0099] During the fifth driving period (T5), the third light emitting control driving unit (Emission_3) may operate in a same manner as it operated during the fourth driving period (T4).

[0100] During the fifth driving period (T5), the fourth light emitting control driving unit (Emission_4) may receive a second clock signal at a low level, a second negative clock signal at a high level, and a third light emitting negative control signal at a low level, and the fourth light emitting control driving unit (Emission_4) may output the fourth light emitting control signal at a high level to the fourth light emitting control line (Em[4]) via the output terminal (Out) thereof, and the fourth light emitting negative control signal at a low level to the fourth light emitting negative control line (EmB[4]) via the negative output terminal (OutB) thereof. Thus, in embodiments of the invention, during the fifth driving period (T5), the operation of the fourth light emitting control driving unit (Emission_4) may be the same as the operation of the light emitting control driving circuit 300, 300' during the second driving period (T52), as described with reference to FIGS. 4 and 9.

[0101] Further, during the fifth driving period (T5), when the fourth light emitting control signal at a high level may be output by the fourth light emitting control driving unit (Emission_4) to the fourth light emitting control line (Em[4]), the seventh pixel unit (PS_7) and the eighth pixel unit (PS_8) may operation when they respectively receive a scan line at a low level from the seventh scan line (Scan[7]) and the eighth scan line (Scan[8]).

[0102] During subsequent driving period(s), e.g., (T6), (T7), etc., operations of the respective light emitting control driving units may substantially correspond to the operations of the first light emitting control driving unit to the fourth light emitting control driving unit (Emission_1 to Emission_4) during the first driving period (T1) to the fifth driving period (T5).

[0103] As illustrated above, an organic light emitting display and a driving circuit thereof according to embodiments of the present invention may be advantageous over conventional displays by enabling a size of the driving circuit and a manufacturing cost to be reduced, and a manufacturing yield thereof to be improved as one light emitting control driving line may be electrically coupled to pixels of multiple, e.g., two, rows, and thus a light emitting control signal may be provided to the pixels of multiple, e.g., two, rows simultaneously.

[0104] Further, as illustrated above, an organic light emitting display and a driving circuit thereof according to embodiments of the present invention may be advantageous by enabling a manufacturing cost and time to be reduced and for the yield to be improved as the light emitting control driving circuit may be implemented using transistors of only a same type as that of transistor(s) employed for implementing a pixel.

Claims

1. An organic light emitting display, comprising:

a first light emitting control driver electrically coupled to an initial driving line, a first clock line, and a first negative clock line, and adapted to output a first light emitting control signal via a first light emitting control line and a first light emitting negative control signal via a first light emitting negative control line,

a first pixel unit electrically coupled to the first light emitting control line;

a second pixel unit electrically coupled to the first light emitting control line;

a second light emitting control driver electrically coupled to the first light emitting negative control line, a second clock line, and a second negative clock line, and adapted to output a second light

emitting control signal via a second light emitting control line and a second light emitting negative control signal via a second light emitting negative control line;
a third pixel unit electrically coupled to the second light emitting control line; and
a fourth pixel unit electrically coupled to the second light emitting control line,
wherein

- the first light emitting control driver includes a first clock terminal electrically coupled to the first clock line, a second clock terminal electrically coupled to the first negative clock line, an input terminal electrically coupled to the initial driving line, an output terminal electrically coupled to the first light emitting control line for outputting the first light emitting control signal; and a negative output terminal electrically coupled to the first light emitting negative control line for outputting the first light emitting negative control signal and wherein the second light emitting control driver includes a first clock terminal electrically coupled to the second clock line, a second clock terminal electrically coupled, to the second negative clock line, an input terminal electrically coupled to the first light emitting negative control line, an output terminal electrically coupled to the second light emitting control line for outputting the second light emitting control signal; and a negative output terminal electrically coupled to the second light emitting negative control line for outputting the second light emitting negative control signal and
- a third light emitting control driver that includes a first clock terminal electrically coupled to the first negative clock line, a second clock terminal electrically coupled to the first clock line, an input terminal, an output terminal and a negative output terminal, wherein the input terminal is electrically coupled to the second light emitting negative control line and wherein the output terminal is electrically coupled to a third light emitting control line and wherein the negative ouput terminal is electrically coupled to a third light emitting negative control line and
- a fourth light emitting control driving unit that includes a first clock terminal electrically coupled to the second negative clock line, a second clock terminal electrically coupled to the second clock line, an input terminal, an output terminal and a negative output terminal, wherein the input terminal is electrically coupled to the third light emitting negative control line and wherein the output terminal is electrically coupled to a fourth light emitting control line and wherein the negative output terminal is electrically coupled to a fourth light emitting negative control line and

wherein each of the light emitting control drivers is implemented using transistors of only a same kind as transistors of the pixels.

2. The organic light emitting display as claimed in claim 1,
wherein the first pixel unit includes pixels of a first row of a panel that are electrically coupled between a first scanning driving line and first to m-th data lines.

3. The organic light emitting display as claimed in claim 1,
wherein the second pixel unit includes pixels of a second row of a panel that are electrically coupled between a second scanning driving line and first to m-th data lines.

4. The organic light emitting display as claimed in claim 1,
wherein the first pixel unit and the second circuit unit emit light based on the first light emitting control signal.

5. The organic light emitting display as claimed in claim 1,
wherein the third pixel unit includes pixels of a third row of a panel that are electrically coupled between a third scanning driving line and first data line to m-th data lines.

6. The organic light emitting display as claimed in claim 1,
wherein the fourth pixel unit includes pixels of a fourth row of a panel that are electrically coupled between a fourth scanning driving line and first data line to m-th data lines.

7. The organic light emitting display as claimed in claim 1,
wherein the third pixel unit and the fourth circuit unit emit light based on the second light emitting control signal.

Patentansprüche

1. Organische lichtemittierende Anzeige, aufweisend:

einen ersten Lichtemissionssteuertreiber, der mit einer Anfangsansteuerleitung, einer ersten Taktleitung und einer ersten negativen Taktlei-

tung elektrisch gekoppelt ist und angepasst ist, um ein erstes Lichtemissionssteuersignal über eine erste Lichtemissionssteuerleitung und ein erstes negatives Lichtemissionssteuersignal über eine erste negative Lichtemissionssteuerleitung auszugeben;
eine erste Pixeleinheit, die mit der ersten Lichtemissionssteuerleitung elektrisch gekoppelt ist;
eine zweite Pixeleinheit, die mit der ersten Lichtemissionssteuerleitung elektrisch gekoppelt ist;
einen zweiten Lichtemissionssteuertreiber, der mit der ersten negativen Lichtemissionssteuerleitung, einer zweiten Taktleitung und einer zweiten negativen Taktleitung elektrisch gekoppelt ist und angepasst ist, um ein zweites Lichtemissionssteuersignal über eine zweite Lichtemissionssteuerleitung und ein zweites negatives Lichtemissionssteuersignal über eine zweite negative Lichtemissionssteuerleitung auszugeben;
eine dritte Pixeleinheit, die mit der zweiten Lichtemissionssteuerleitung elektrisch gekoppelt ist; und
eine vierte Pixeleinheit, die mit der zweiten Lichtemissionssteuerleitung elektrisch gekoppelt ist, wobei

- der erste Lichtemissionssteuertreiber einen ersten Taktanschluss, der mit der ersten Taktleitung elektrisch gekoppelt ist, einen zweiten Taktanschluss, der mit der ersten negativen Taktleitung elektrisch gekoppelt ist, einen Eingangsanschluss, der mit der Anfangsansteuerleitung elektrisch gekoppelt ist, einen Ausgangsanschluss, der mit der ersten Lichtemissionssteuerleitung elektrisch gekoppelt ist, zum Ausgeben des ersten Lichtemissionssteuersignals, und einen negativen Ausgangsanschluss, der mit der ersten negativen Lichtemissionssteuerleitung elektrisch gekoppelt ist, zum Ausgeben des ersten negativen Lichtemissionssteuersignals aufweist, und wobei der zweite Lichtemissionssteuertreiber einen ersten Taktanschluss, der mit der zweiten Taktleitung elektrisch gekoppelt ist, einen zweiten Taktanschluss, der mit der zweiten negativen Taktleitung elektrisch gekoppelt ist, einen Eingangsanschluss, der mit der ersten negativen Lichtemissionssteuerleitung elektrisch gekoppelt ist, einen Ausgangsanschluss, der mit der zweiten Lichtemissionssteuerleitung elektrisch gekoppelt ist, zum Ausgeben des zweiten Lichtemissionssteuersignals, und einen negativen Ausgangsanschluss, der mit der zweiten negativen Lichtemissionssteuerleitung elektrisch gekoppelt ist, zum Ausgeben des zweiten negativen Lichtemissionssteuersignals aufweist; und
- einen dritten Lichtemissionssteuertreiber, der einen ersten Taktanschluss, der mit der ersten negativen Taktleitung elektrisch gekoppelt ist, einen zweiten Taktanschluss, der mit der ersten Taktleitung elektrisch gekoppelt ist, einen Eingangsanschluss, einen Ausgangsanschluss und einen negativen Ausgangsanschluss aufweist, wobei der Eingangsanschluss mit der zweiten negativen Lichtemissionssteuerleitung elektrisch gekoppelt ist und wobei der Ausgangsanschluss mit einer dritten Lichtemissionssteuerleitung elektrisch gekoppelt ist und wobei der negative Ausgangsanschluss mit einer dritten negativen Lichtemissionssteuerleitung elektrisch gekoppelt ist, und
- eine vierte Lichtemissionssteuer-Ansteuereinheit, die einen ersten Taktanschluss, der mit der zweiten negativen Taktleitung elektrisch gekoppelt ist, einen zweiten Taktanschluss, der mit der zweiten Taktleitung elektrisch gekoppelt ist, einen Eingangsanschluss, einen Ausgangsanschluss und einen negativen Ausgangsanschluss aufweist, wobei der Eingangsanschluss mit der dritten negativen Lichtemissionssteuerleitung elektrisch gekoppelt ist und wobei der Ausgangsanschluss mit einer vierten Lichtemissionssteuerleitung elektrisch gekoppelt ist und wobei der negative Ausgangsanschluss mit einer vierten negativen Lichtemissionssteuerleitung elektrisch gekoppelt ist, und

wobei jeder der Lichtemissionssteuertreiber unter Verwendung von Transistoren ausschließlich eines gleichen Typs als Transistoren der Pixel implementiert ist.

2. Organische lichtemittierende Anzeige nach Anspruch 1,
wobei die erste Pixeleinheit Pixel einer ersten Zeile einer Tafel aufweist, die elektrisch zwischen eine erste Abtast-Ansteuerleitung und eine erste bis mte Datenleitung gekoppelt sind.

3. Organische lichtemittierende Anzeige nach Anspruch 1,
wobei die zweite Pixeleinheit Pixel einer zweiten Zeile einer Tafel aufweist, die elektrisch zwischen eine zweite Abtast-Ansteuerleitung und eine erste bis mte Datenleitung gekoppelt sind.

4. Organische lichtemittierende Anzeige nach Anspruch 1,
wobei die erste Pixeleinheit und die zweite Schaltkreiseinheit Licht basierend auf dem ersten Lichtemissionssteuersignal emittieren.

5. Organische lichtemittierende Anzeige nach Anspruch 1,
wobei die dritte Pixeleinheit Pixel einer dritten Zeile einer Tafel aufweist, die elektrisch zwischen eine dritte Abtast-Ansteuerleitung und eine erste Datenleitung bis mte Datenleitung gekoppelt sind.

6. Organische lichtemittierende Anzeige nach Anspruch 1,
wobei die vierte Pixeleinheit Pixel einer vierten Zeile einer Tafel aufweist, die elektrisch zwischen eine vierte Abtast-Ansteuerleitung und eine erste Datenleitung bis mte Datenleitung gekoppelt sind.

7. Organische lichtemittierende Anzeige nach Anspruch 1,
wobei die dritte Pixeleinheit und die vierte Pixeleinheit Licht basierend auf dem zweiten Lichtemissionssteuersignal emittieren.

Revendications

1. Afficheur électroluminescent organique, comprenant :

un premier dispositif de commande de contrôle d'émission de lumière couplé électriquement à une ligne de commande initiale, à une première ligne d'horloge et à une première ligne d'horloge négative, et conçu pour délivrer un premier signal de contrôle d'émission de lumière par l'intermédiaire d'une première ligne de contrôle d'émission de lumière et un premier signal de contrôle négatif d'émission de lumière par l'intermédiaire d'une première ligne de contrôle négative d'émission de lumière ;
une première unité de pixels couplée électriquement à la première ligne de contrôle d'émission de lumière ;
une deuxième unité de pixels couplée électriquement à la première ligne de contrôle d'émission de lumière ;
un deuxième dispositif de commande de contrôle d'émission de lumière couplé électriquement à la première ligne de contrôle négative d'émission de lumière, à une deuxième ligne d'horloge et à une deuxième ligne d'horloge négative, et conçu pour délivrer un deuxième signal de contrôle d'émission de lumière par l'intermédiaire d'une deuxième ligne de contrôle d'émission de lumière et un deuxième signal de contrôle négatif d'émission de lumière par l'intermédiaire d'une deuxième ligne de contrôle négative d'émission de lumière ;
une troisième unité de pixels couplée électriquement à la deuxième ligne de contrôle d'émission de lumière ; et
une quatrième unité de pixels couplée électriquement à la deuxième ligne de contrôle d'émission de lumière, dans lequel

- le premier dispositif de commande de contrôle d'émission de lumière comprend une première borne d'horloge couplée électriquement à la première ligne d'horloge, une deuxième borne d'horloge couplée électriquement à la première ligne d'horloge négative, une borne d'entrée couplée électriquement à la ligne de commande initiale, une borne de sortie couplée électriquement à la première ligne de contrôle d'émission de lumière pour délivrer le premier signal de contrôle d'émission de lumière, et une borne de sortie négative couplée électriquement à la première ligne de contrôle négative d'émission de lumière pour délivrer le premier signal de contrôle négatif d'émission de lumière, et dans lequel le deuxième dispositif de commande de contrôle d'émission de lumière comprend une première borne d'horloge couplée électriquement à la deuxième ligne d'horloge, une deuxième borne d'horloge couplée électriquement à la deuxième ligne d'horloge négative, une borne d'entrée couplée électriquement à la première ligne de contrôle négative d'émission de lumière, une borne de sortie couplée électriquement à la deuxième ligne de contrôle d'émission de lumière pour délivrer le deuxième signal de contrôle d'émission de lumière, et une borne de sortie négative couplée électriquement à la deuxième ligne de contrôle négative d'émission de lumière pour délivrer le deuxième signal de contrôle négatif d'émission de lumière, et
- un troisième dispositif de commande de contrôle d'émission de lumière qui comprend une première borne d'horloge couplée électriquement à la première ligne d'horloge négative, une deuxième borne d'horloge couplée électriquement à la première ligne d'horloge, une borne d'entrée, une borne de sortie et une borne de sortie négative, dans lequel la borne d'entrée est couplée électriquement à la deuxième ligne de contrôle négative d'émission de lumière, et dans lequel la borne de sortie est couplée électriquement à une troisième ligne de contrôle d'émission de lumière, et dans le-

quel la borne de sortie négative est couplée électriquement à une troisième ligne de contrôle négative d'émission de lumière, et
- une quatrième unité de commande de contrôle d'émission de lumière qui comprend une première borne d'horloge couplée électriquement à la deuxième ligne d'horloge négative, une deuxième borne d'horloge couplée électriquement à la deuxième ligne d'horloge, une borne d'entrée, une borne de sortie et une borne de sortie négative, dans lequel la borne d'entrée est couplée électriquement à la troisième ligne de contrôle négative d'émission de lumière, et dans lequel la borne de sortie est couplée électriquement à une quatrième ligne de contrôle d'émission de lumière, et dans lequel la borne de sortie négative est couplée électriquement à une quatrième ligne de contrôle négative d'émission de lumière, et

dans lequel chacun des dispositifs de commande de contrôle d'émission de lumière est mis en oeuvre en utilisant des transistors uniquement d'un même type que les transistors des pixels.

2. Afficheur électroluminescent organique selon la revendication 1,
dans lequel la première unité de pixels comprend les pixels d'une première rangée d'un panneau qui sont couplés électriquement entre une première ligne de commande de balayage et des première à m^{ième} lignes de données.

3. Afficheur électroluminescent organique selon la revendication 1,
dans lequel la deuxième unité de pixels comprend les pixels d'une deuxième rangée d'un panneau qui sont couplés électriquement entre une deuxième ligne de commande de balayage et des première à m^{ième} lignes de données.

4. Afficheur électroluminescent organique selon la revendication 1,
dans lequel la première unité de pixels et la deuxième unité de circuit émettent une lumière sur la base du premier signal de contrôle d'émission de lumière.

5. Afficheur électroluminescent organique selon la revendication 1,
dans lequel la troisième unité de pixels comprend les pixels d'une troisième rangée d'un panneau qui sont couplés électriquement entre une troisième ligne de commande de balayage et des première à m^{ième} lignes de données.

6. Afficheur électroluminescent organique selon la revendication 1,
dans lequel la quatrième unité de pixels comprend les pixels d'une quatrième rangée d'un panneau qui sont couplés électriquement entre une quatrième ligne de commande de balayage et des première à m^{ième} lignes de données.

7. Afficheur électroluminescent organique selon la revendication 1,
dans lequel la troisième unité de pixels et la quatrième unité de circuit émettent une lumière sur la base du deuxième signal de contrôle d'émission de lumière.

Fig.1

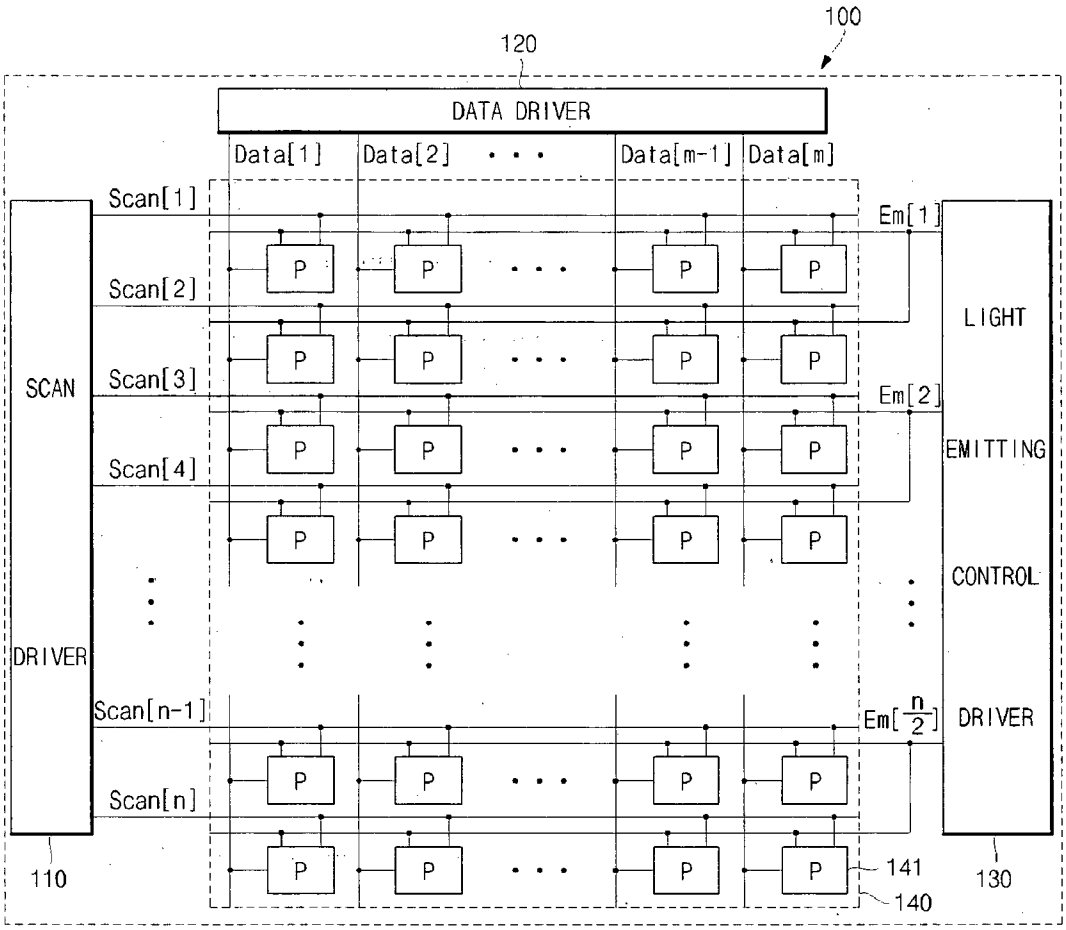

100
120
DATA DRIVER
Data[1]
Data[2]
Data[m-1]
Data[m]
Scan[1]
Scan[2]
Scan[3]
Scan[4]
Scan[n-1]
Scan[n]
SCAN
DRIVER
110
P
Em[1]
Em[2]
Em[n/2]
LIGHT
EMITTING
CONTROL
DRIVER
130
141
140

Fig.2

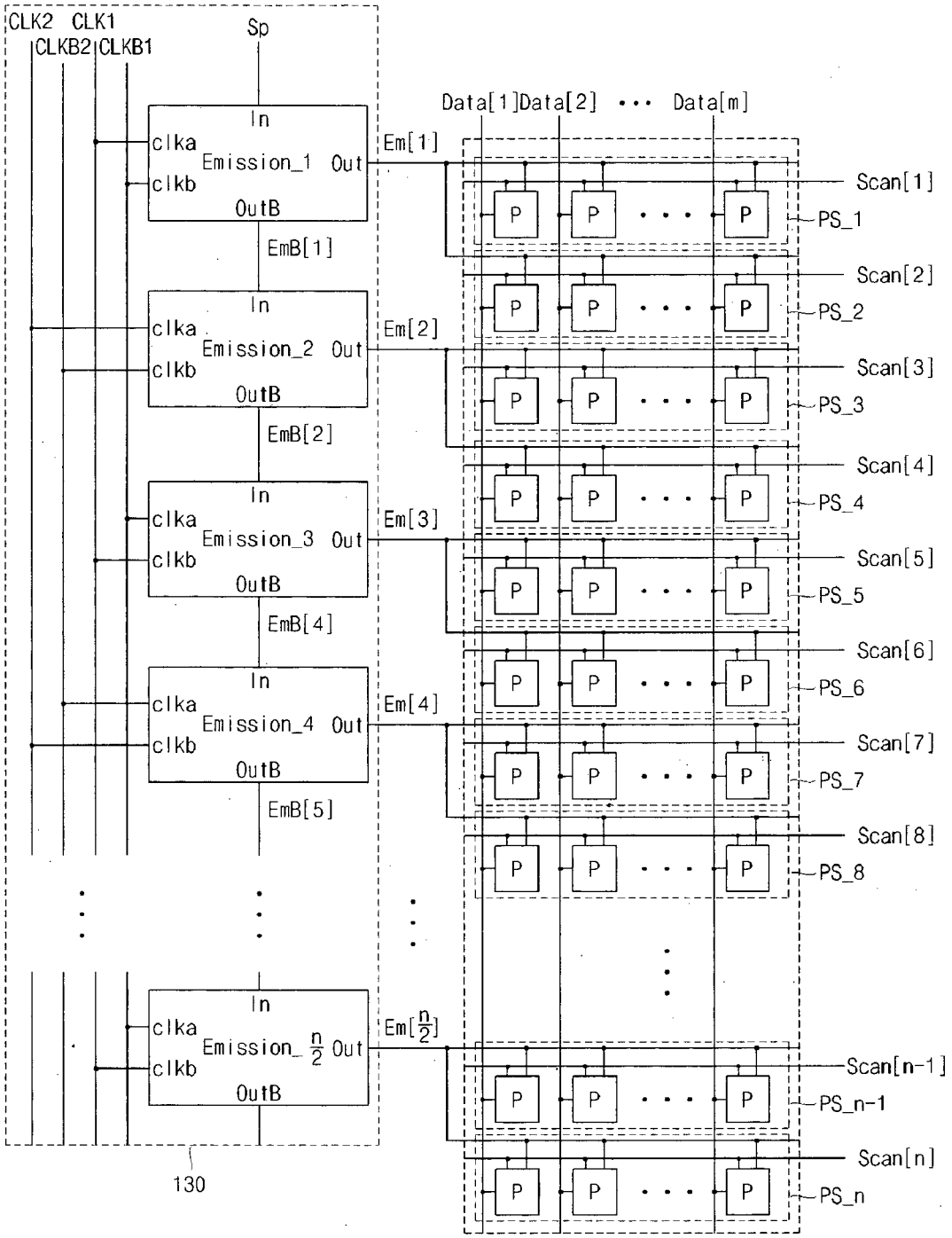

CLK2
CLK1
CLKB2
CLKB1
Sp
In
clka
clkb
Emission_1
Emission_2
Emission_3
Emission_4
Emission_n/2
Out
OutB
EmB[1]
EmB[2]
EmB[4]
EmB[5]
Em[1]
Em[2]
Em[3]
Em[4]
Em[n/2]
130
Data[1]
Data[2]
Data[m]
P
Scan[1]
Scan[2]
Scan[3]
Scan[4]
Scan[5]
Scan[6]
Scan[7]
Scan[8]
Scan[n-1]
Scan[n]
PS_1
PS_2
PS_3
PS_4
PS_5
PS_6
PS_7
PS_8
PS_n-1
PS_n

Fig.3

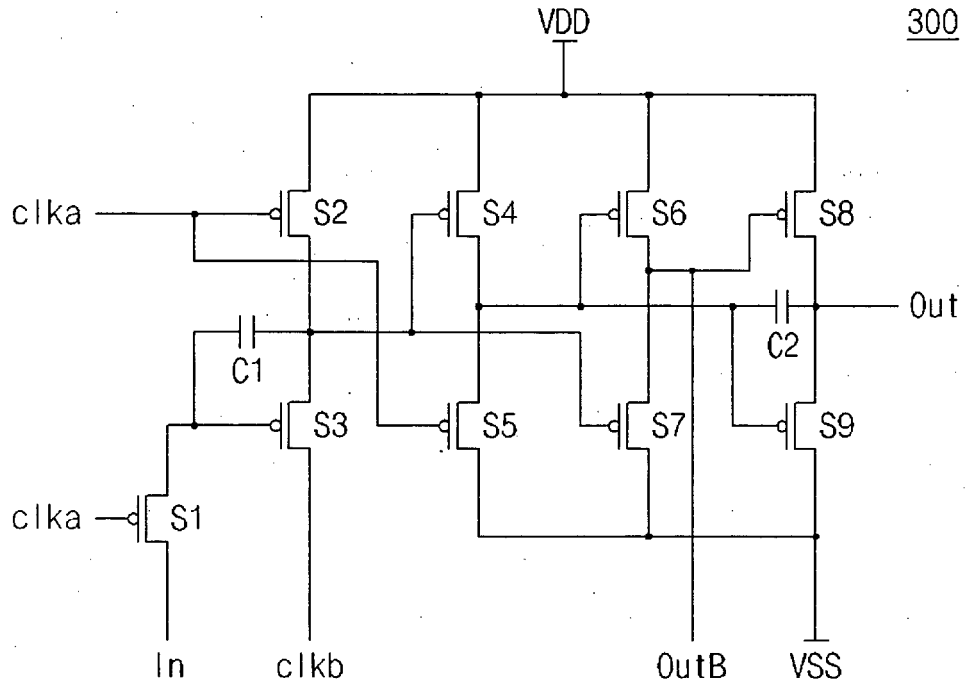

VDD
300
clka
S2
S4
S6
S8
Out
C1
C2
S3
S5
S7
S9
clka
S1
In
clkb
OutB
VSS

Fig.4

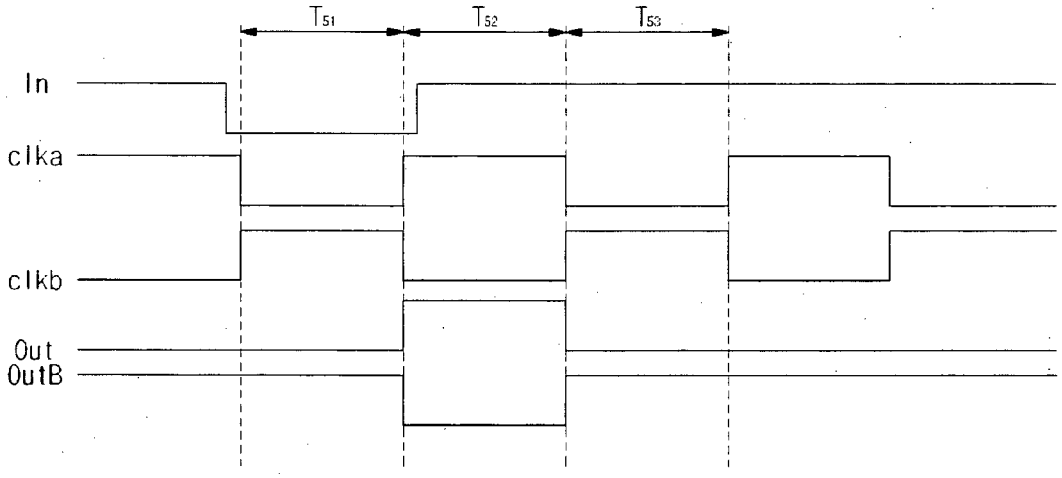

T51
T52
T53
In
clka
clkb
Out
OutB

Fig.5

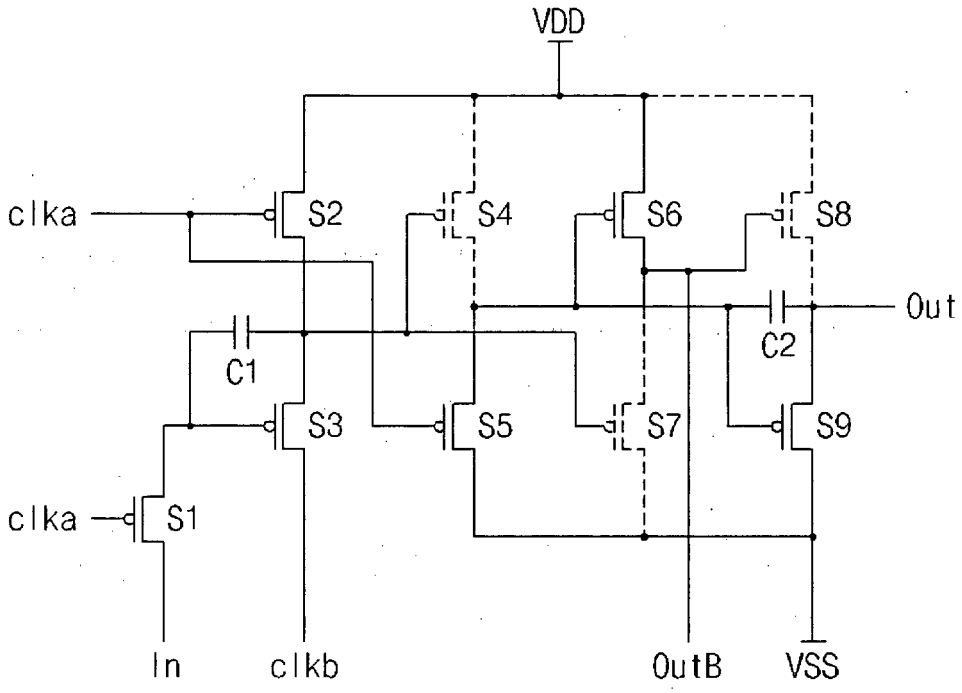

VDD
clka
S2
S4
S6
S8
Out
C1
C2
S3
S5
S7
S9
clka
S1
In
clkb
OutB
VSS

Fig.6

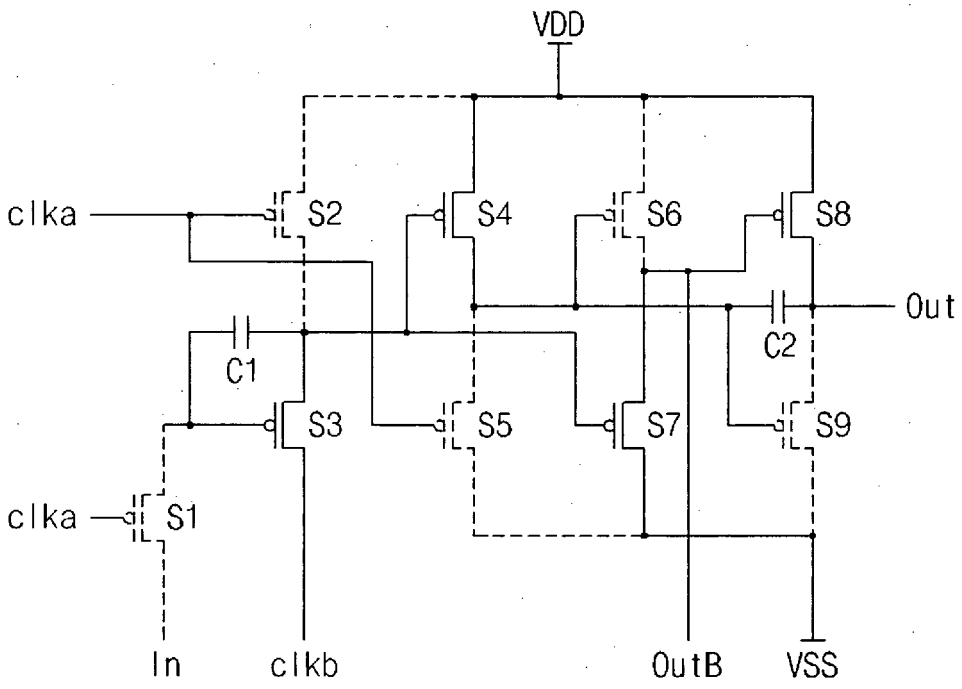

VDD
clka
S2
S4
S6
S8
Out
C1
C2
S3
S5
S7
S9
clka
S1
In
clkb
OutB
VSS

Fig.7

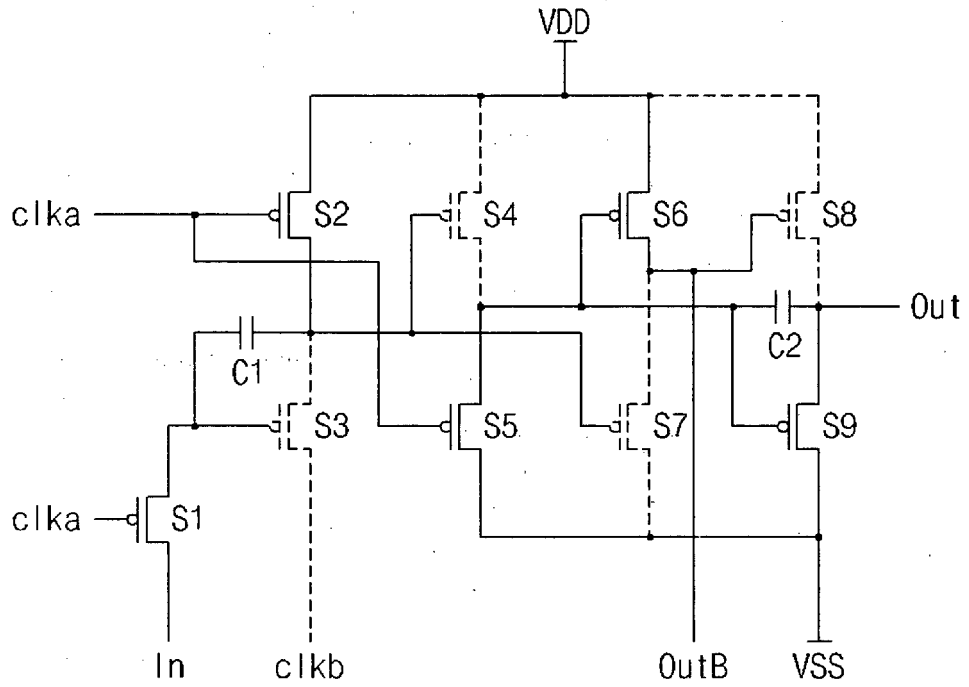

VDD
clka
S2
S4
S6
S8
Out
C1
C2
S3
S5
S7
S9
clka
S1
In
clkb
OutB
VSS

Fig.8

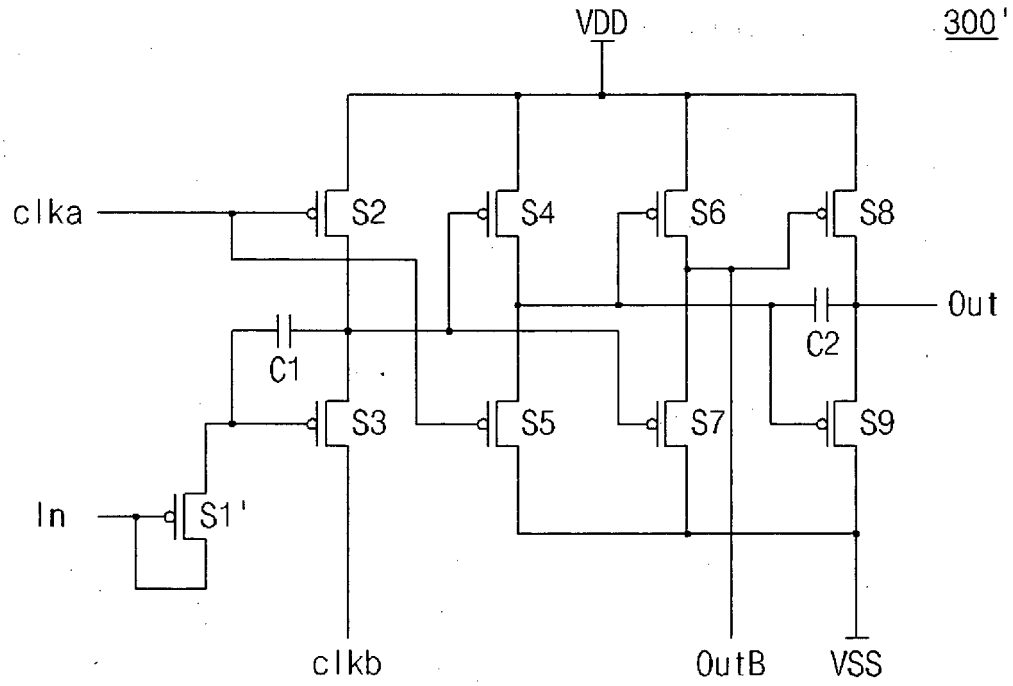

VDD
300'
clka
S2
S4
S6
S8
Out
C1
C2
S3
S5
S7
S9
In
S1'
clkb
OutB
VSS

Fig.9

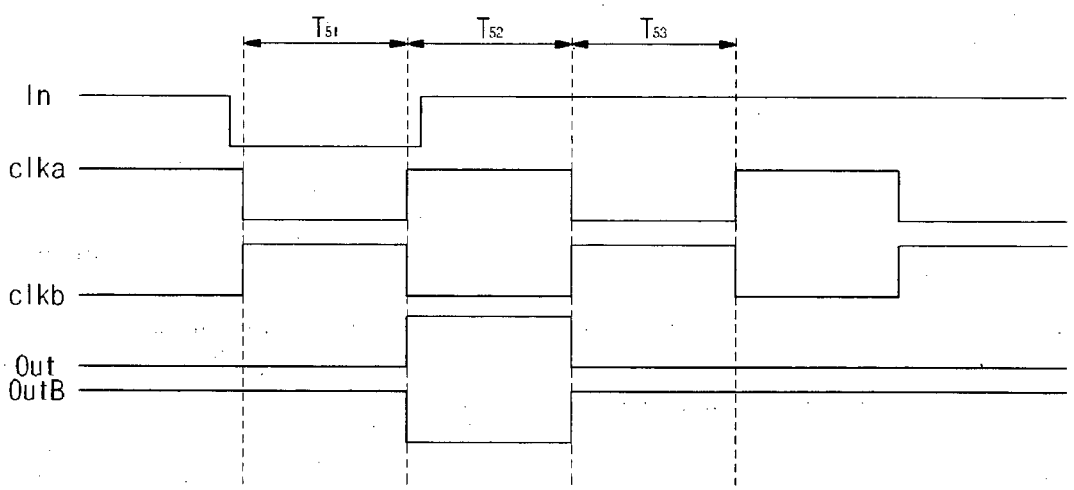
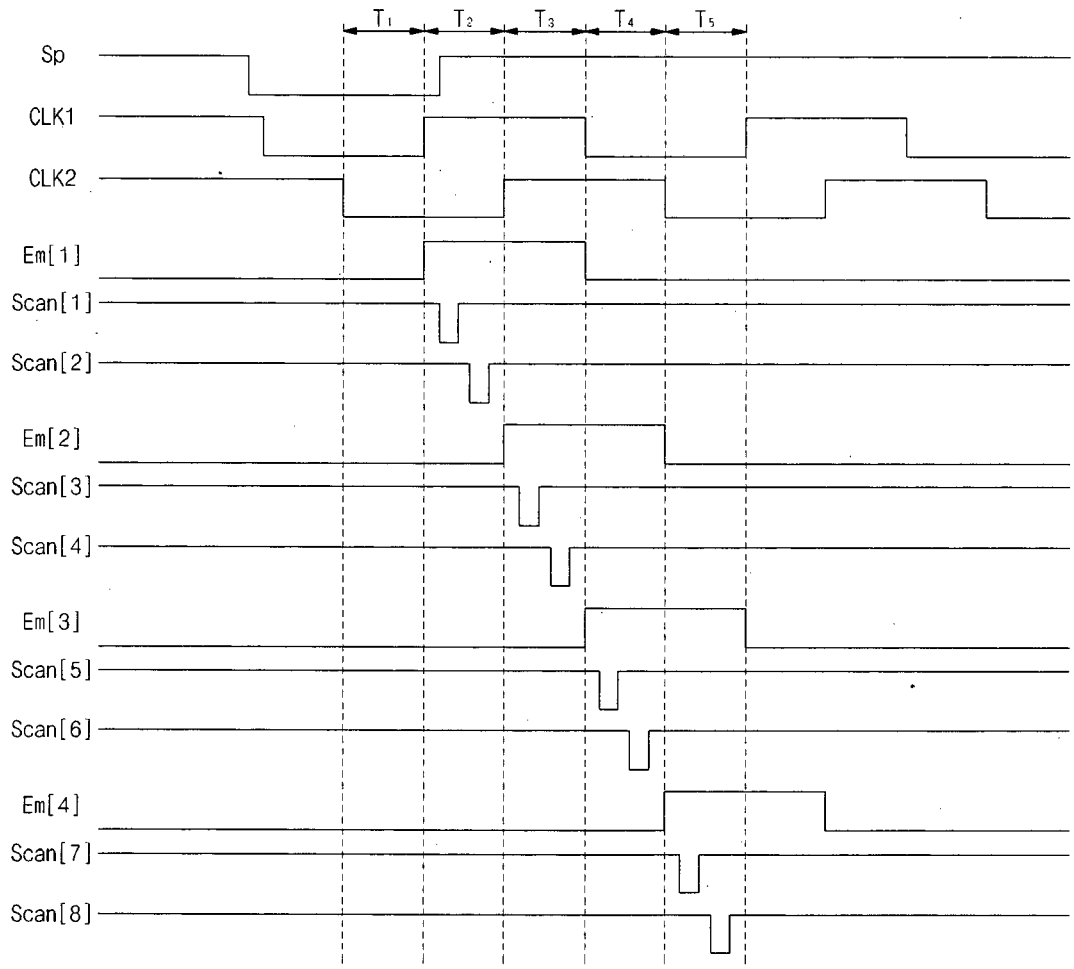

T51
T52
T53
In
clka
clkb
Out
OutB

Fig.10


T1
T2
T3
T4
T5
Sp
CLK1
CLK2
Em[1]
Scan[1]
Scan[2]
Em[2]
Scan[3]
Scan[4]
Em[3]
Scan[5]
Scan[6]
Em[4]
Scan[7]
Scan[8]

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- EP 1653434 A1 **[0008]**
- KR 1020070020737 **[0011]**

专利名称(译)	有机发光显示器及其驱动电路		
公开(公告)号	EP1965370B1	公开(公告)日	2014-01-22
申请号	EP2008101553	申请日	2008-02-13
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	LEE HYUNJUNG CHUNG KYUNGHOON		
发明人	LEE, HYUNJUNG CHUNG, KYUNGHOON		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3208 G09G3/3225 G09G3/3266 G09G2310/021 G09G2310/0286 G09G2330/021		
代理机构(译)	hengelhaupt，Jürgen		
优先权	1020070020737 2007-03-02 KR		
其他公开文献	EP1965370A3 EP1965370A2		
外部链接	Espacenet		

摘要(译)

包括多个发光控制驱动器的驱动电路，包括耦合到先前发光控制驱动器的初始驱动线或发光负控制线的输入端子，电耦合到第一时钟端子和第二时钟端子的第一时钟端子和第二时钟端子。分别反相的第一时钟线和第一负时钟线，或者第二时钟线和第二负时钟线，以及适于产生输出信号和负输出信号的输出端和负输出端当分别通过输入端，第一时钟端和第二时钟端接收输入信号，时钟信号和负时钟信号时。

Fig.1