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(54) **Shift register and organic light emitting display using the same**

Schieberegister und organische lichtemittierende Anzeigevorrichtung damit

Registre de déphasage et affichage électroluminescent organique l'utilisant

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Description

BACKGROUND

1. Field of the Invention

[0001] Aspects of the present invention relate to a shift register and an organic light emitting display using the same. More particularly, aspects of the present invention relate to a shift register and an organic light emitting display using the same, which has a simplified design and a reduced dead space.

2. Description of the Related Art

[0002] Generally, a flat panel display device, such an organic light emitting display, includes a pixel array in a matrix pattern arranged at intersections of data lines and scan lines.
The scan lines constitute horizontal lines (row lines) of a matrix pixel portion, and are selected by a shift register to receive a predetermined scan signal.
[0003] FIG. 1 is a block diagram showing a related art shift register.
With reference to FIG. 1, the related art shift register includes a plurality of stages (ST1 to STn), which are dependently connected to an input line of a start pulse SP.
[0004] The plurality of stages (ST1 to STn) sequentially shift a start pulse SP or an output signal of a previous stage to generate respective output signals (SS1 to SSn) corresponding to clock signals supplied from input lines of the clock signals (not shown).
[0005] The respective output signals (SS1 to SSn) generated by the respective stages (ST1 to STn) are provided to a pixel array.
[0006] There is a need for a design of a shift register having high reliance, simplicity of design of the shift register, and a reduction of the dead space by way of a reduced number of wires, such as power supply lines.
US2004/0227718 discloses a shift register including stages shifting an input signal with phase-delayed control signals and first and second supply voltages, and for applying shifted input signals as output signals and as input signals of succeeding stages.
US2006/0146978 discloses a shift register having a plurality of stages which output an output signal through an output signal line by using any three of a first voltage supply source, a previous stage's output signal, a next stage's output signal, and first to fourth clock signals.
EP0731441 discloses a shift register for scanning a liquid crystal display includes cascaded stages. A given stage is formed with an input transistor switch that is responsive to an output pulse of a stage upstream in the chain of the cascaded stages.

SUMMARY OF THE INTENTION

[0007] Accordingly, aspects of the present invention provide a shift register and an organic light emitting display using the same, with a shift register having a simple design, a high reliability, and a reduced dead space.
[0008] According to a first aspect of the invention there is provided a shift register as set out in Claim 1. Preferred features of this aspect are set out in Claims 2 to 9. According to a second aspect of the invention there is provided an organic light emitting display device as set out in Claim10. Preferred features of this aspect are set out in Claims 11 and 12.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Embodiments of the invention will now be described, by way of example, and with reference to the accompanying drawings in which:
[0010] FIG. 1 is a block diagram showing a related art shift register;
[0011] FIG 2 is a block diagram showing an organic light emitting display according to an embodiment of the present invention;
[0012] FIG. 3 is a block diagram showing a shift register according to an embodiment of the present invention included in the scan driver shown in FIG. 2;
[0013] FIG. 4 is a detailed circuitry diagram showing an arrangement of a shift register;
[0014] FIG 5 is an input/output signal waveform diagram of the arrangement shown in FIG. 4;
[0015] FIG. 6 is a detailed circuitry diagram showing an embodiment of a representative stage of the shift register shown in FIG. 3;
[0016] FIG 7A is a circuitry diagram implementing the representative stage STi' shown in FIG. 6 of the shift register shown in FIG 3; and
[0017] FIG. 7B is a view showing a simulation result of the circuit shown in FIG. 7A.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0018] Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiment are described below in order to explain the present invention by referring to the figures.
[0019] Hereinafter, embodiment of the present invention will be described with reference to the accompanying drawings, namely, FIG 2 and 3 and FIG. 6 to FIG. 7B. In the following discussion, when one element is connected to another element, one element may not only be directly connected to another element but also be indirectly connected to another element via another element(s). Further, prior discussed elements are not repeated for clarity. Also, like reference numerals refer to like elements throughout
[0020] FIG. 2 is a block diagram showing an organic light emitting display according to an embodiment of the present invention. The organic light emitting display in-

cludes a pixel portion 130 including pixels 140 formed in areas divided (or defined) by scan lines S1 through Sn and data lines D1 through Dm, a scan driver 110 to drive the scan lines S1 through Sn, a data driver 120 to drive the data lines D1 through Dm, and a timing control unit 150 to control the scan driver 110 and the data driver 120.

[0021] As shown, the scan driver 110 receives scan control signals SCSs including a start pulse SP and a clock signal CLK from the timing control unit 150 to generate (or output) scan signals, and provides the scan signals to the scan lines S 1 to Sn.

[0022] In order to do this, the scan driver 110 includes a shift register, which sequentially generates the scan signals in accordance with the start pulse SP and the clock signal CLK and provides the scan signals to the scan lines S 1 to Sn.

[0023] As shown, the data driver 120 receives the data control signal DCS and data (Data) from the timing control unit 150, and generates a data signal. The data signal is provided to the data lines D1 to Dm in synchronization with the scan signal.

[0024] The timing control unit 150 generates (or outputs) scan control signals SCSs and a data control signal DCS according to externally supplied signals, which may be synchronous thereto. The scan control signals SCSs generated by the timing control unit 150 are provided (or applied) to the scan driver 110, and the data control signal DCS generated (or output) by the timing controller 150 is provided (or applied) to the data driver 120. Furthermore, the timing control unit 150 provides (or outputs) externally supplied data (Data) to the data driver 120.

[0025] The pixel portion 130 includes a plurality of pixels 140, which respectively are electrically connected to the scan lines S1 to Sn and the data lines D1 to Dm. Each of the pixels 140 receives a voltage of a first pixel power supply ELVDD and a voltage of a second pixel power supply ELVSS from an exterior thereof, and receives a scan signal and a data signal from the scan driver 110 and the data driver 120, respectively. When one or more of the pixels 140 receive the voltage of a first pixel power supply ELVDD, the voltage of a second pixel power supply ELVSS, the scan signal, and/or the data signal, one or more of the pixels are selected by the scan signal and light corresponding to the data signal is generated (or output) therefrom, in the shown embodiment.

[0026] FIG. 3 is a block diagram showing a shift register according to an embodiment of the present invention included in the scan driver shown in FIG. 2.

[0027] With reference to FIG. 3, the shift register includes a plurality of stages ST11 to ST1n, which are dependently connected to an input line of a start pulse SP and three clock signal supply lines CLK1 to CLK3. Here, three clock signals CLK1, CLK2, and CLK3 are supplied in such a manner that phases (or pulses) of the three clock signals CLK1, CLK2, and CLK3 are sequentially delayed. In other embodiments, the three clocks signals CLK1, CLK2, and CLK3 are applied sequentially and/or periodically. In other embodiments, the clock signal supply lines may be connected differently to each of the stages ST11 to ST1n, and the clock signals CLK1 to CLK3 may be supplied in a different order or with different phases.

[0028] In the embodiment shown, the first stage ST11 delays a phase of the start pulse SP supplied thereto by one clock and outputs the phase-delayed start pulse in response to first to third clock signals CLK1 to CLK3.

[0029] Each of the second to n-th stages ST12 to ST1n delays a phase of an output signal SSi-1 of a previous stage supplied thereto by one clock and outputs the phase-delayed output signal in response to the first to third clock signals CLK1 to CLK3.

[0030] Accordingly, by the aforementioned operations thereof, the stages ST11 to ST1n sequentially generate (or output) respective phase-delayed output signals SS1 to SSn, and sequentially provide the generated output signals SS1 to SSn to the respective scan lines (S1 to Sn shown in FIG 2).

[0031] In the embodiment shown in FIG. 3, a shift register is driven by the sequentially phase-delayed three clock signals CLK1 to CLK3. However, in other embodiments, the shift register can be driven by sequentially phase-delayed four or more clock signals.

[0032] In such a case, each stage STi may receive only three of the four clock signals and generate an output signal SSi corresponding thereto.

[0033] For example, a first stage ST11 may receive first, third, and fourth clock signals, while a second stage ST12 may receive the second, fourth, and first clock signals, which are obtained by sequentially delaying phases of the first, third, and fourth clock signals, respectively by one clock. In the same manner, each of the third to n-th stages ST13 to ST1n respectively may sequentially receive three phase-delayed clock signals that are delayed by one clock from those of the previous stage.

[0034] FIG. 4 is a detailed circuitry diagram showing an arrangement of a shift register.

[0035] With reference to FIG 4, the representative stage STi includes a voltage level controller 410, first, second, and sixth transistors M1, M2, and M6, and first, second, and third capacitors C1, C2, and C3.

[0036] In the arrangement shown, the voltage level controller 410 controls a voltage level of a first node (first output node) N1 and a voltage level of a second node (second output node) N2 to be output as a high level or a low level.

[0037] More particularly, the voltage level controller 410 controls a voltage level of the second node (second output node) N2 according to the start pulse SP or an output signal SSi-1 of a previous stage. The voltage level controller 410 also controls a voltage level of the first node (first output node) N1 according to the start pulse SP or an output signal SSi-1 of a previous stage and the voltage level of the second node N2.

[0038] Accordingly, in the arrangement shown, the voltage level controller 410 includes third, fourth, and fifth

transistors M3, M4, and M5. In some arrangements, the third, fourth, and fifth transistors M3, M4, and/or M5 are formed of P-type transistors.

[0039] As shown, the third transistor M3 is coupled between an input line of the start pulse SP or an output signal SSi-1 of a previous stage, and the second node N2. A gate electrode of the third transistor M3 is coupled to an input line of the second clock signal CLK2. When the second clock signal CLK2 of a low level is supplied to the gate electrode of the third transistor M3, the third transistor M3 is turned-on and supplies the start pulse SP or the output signal SSi-1 of a previous stage to the second node N2.

[0040] As shown, the fourth transistor M4 is coupled between a first power supply VDD and the first node N1. A gate electrode of the fourth transistor M4 is coupled to the input line of the start pulse SP or the output signal SSi-1 of a previous stage. When the start pulse SP or the output signal SSi-1 of a previous stage having a low level is inputted to the gate electrode of the fourth transistor M4, the fourth transistor M4 is turned-on and electrically connects the first node N1 to the first power supply VDD.

[0041] As shown the fifth transistor M5 is coupled between the first power supply VDD and the first node N1. A gate electrode of the fifth transistor M5 is coupled to the second node N2. When a voltage level of the second node N2 drops to be equal to or less than a predetermined value, the fifth transistor M5 electrically connects the first node N1 to the first power supply VDD.

[0042] That is, the voltage level controller 410 controls a voltage level of the first node N1 and the voltage level of the second node N2 according to the start pulse SP or the output signal SSi-1 of a previous stage and the second clock signal CLK2.

[0043] As shown, the first transistor M1 is coupled between the first power supply VDD, which is a high level voltage source, and a third node (third output node) N3, which is an output node of the stage STi. A gate electrode of the first transistor M1 is coupled to the first node N1. When a voltage level of the first node N1 is low (namely, when a voltage of the first node N1 is less than that of a source electrode of the first transistor M1), the first transistor M1 is turned-on and electrically connects an output line of the stage STi to the first power supply VDD.

[0044] As shown, the second transistor M2 is coupled between the third node N3 and an input line of the third clock signal CLK3. A gate electrode of the second transistor M2 is coupled with the second node N2. When a voltage level of the second node N2 is low, the second transistor M2 is turned-on and electrically connects an output line of the stage STi to an input line of the third clock signal CLK3. That is, when the second transistor M2 is turned-on, a voltage level of the output signal SSi of the stage STi becomes identical with that of the third clock signal CLK3.

[0045] In the arrangement shown, the first and second transistors M1 and/or M2 are formed of P-type transistor. In other arrangements, N-type transistors or combinations of P-type or N-type transistors could be used.

[0046] As shown, the sixth transistor M6 is coupled between the first node N1 and a second power supply VSS, which is a low level voltage source that is less than that of the first power supply VDD. A gate electrode of the sixth transistor M6 is coupled to an input line of the first clock signal CLK1. When the first clock signal CLK1 of a low level is inputted to the input line of the first clock signal CLK1, the sixth transistor M6 is turned-on and electrically connects the first node N1 to the second power supply VSS. In this embodiment, the sixth transistor M6 comprises a P-type transistor. The combination of the sixth transistor M6 and the second power supply VSS functions as voltage changing means for changing a voltage of the first node N1 by a predetermined value in accordance with a level of a first clock signal CLK1.

[0047] As shown, the first capacitor C1 is coupled between the second node N2 and the third node N3. The first capacitor C1 is charged with a predetermined voltage corresponding to a potential difference between both terminals thereof in order to stabilize an operation of the second transistor M2.

[0048] As shown, the second capacitor C2 is coupled between the first power supply VDD and the first node N1.

[0049] As shown, the third capacitor C3 is coupled between the first power supply VDD and the second node N2.

[0050] The second and third capacitor C2 and C3 reduce a variation of (or to stabilize) a voltage, which is applied to the first power supply VDD, the first node N1, and/or the second node N2.

[0051] As is seen from the forgoing descriptions thereof, when a circuit of the stages STi is designed, a shift register is constructed using a relatively small number of elements, namely, a relatively small number of transistors M and capacitors C, to thereby easily design the shift register and to reduce dead space (in other words to make the shift register more compact).

[0052] Further, a manufacturing process thereof is simplified by designing the transistors M1 to M6 included in a representative stage STi with the same conductive type.

[0053] In particular, in a flat panel display such as an active matrix type organic light emitting display, a pixel array includes P-type transistors. When stages included in a shift register of a scan driver are constructed by transistors having the same conductive type as that of transistors included in the pixel array, the shift register can be formed simultaneously with the pixel array formed on a substrate. Accordingly, a manufacturing process of the flat panel display is simplified and eased in order to enhance the efficiency thereof.

[0054] That is, in the arrangement shown, the shift register is formed on the substrate together with the pixel array. However, arrangements are not limited thereto. For example, in some arrangements the shift register may be mounted on a chip and be mounted on a substrate

on which the pixel array is formed.

[0055] Additionally, in the stage STi shown in FIG. 4, the first, second, and third clock signals CLK1, CLK2, and CLK3 are supplied to one electrode of the sixth, third, and second transistor M6, M3, and M2, respectively. However, in other arrangements, the first, second, and third clock signals CLK1, CLK2, and CLK3 may be supplied and shifted by one clock for respective stages.

[0056] For example, in an immediate next stage of the stage STi shown in FIG. 4, the second, third, and first clock signals CLK2, CLK3, and CLK1 (which are clock signals respectively shifted by one clock from that of first, second, and third signals) may be supplied to respective one electrode of the sixth, third, and second transistor M6, M3, and M2, respectively. To enable supply of such shifted clock signals, the respective clock signal supply lines may be arranged accordingly to supply the second, third, and first clock signals CLK2, CLK3, and CLK1.

[0057] The following is a description of an operation of the stage STi shown in FIG. 4 with reference to the input/output signal waveform shown in FIG. 5. For the sake of convenience and brevity, discussion below will not consider factors such as a threshold voltage of transistors.

[0058] Referring to FIG. 5, first, during a t1 period, an output signal SSi-1 of a previous stage (or start pulse SP) of a high level is supplied to a source electrode of the third transistor M3 and a gate electrode of the fourth transistor M4.

[0059] Moreover, the first clock signal CLK1 of a low level is supplied to a gate electrode of the sixth transistor M6, and the second clock signal CLK2 and the third clock signal CLK3 of the high level are supplied to a gate electrode of the third transistor M3 and a drain electrode of the second transistor M2, respectively. In this embodiment, the first, second, and third clock signals CLK1, CLK2, and CLK3 have a waveform with a sequentially delayed phase.

[0060] Accordingly, the third and fourth transistor M3 and M4 maintain an off state, and the sixth transistor M6 is turned-on.

[0061] When the sixth transistor M6 is turned-on, a voltage of the second power supply VSS is transferred to the first node N1. Therefore, during the t1 period, the first node N1 is charged (supplied or applied) with a low level voltage.

[0062] At this time, as the voltage of the first node N1 drops to a low level, the first transistor M1 is turned-on to supply the voltage of the first power supply VDD to an output line of the stage STi. Accordingly, the output signal SSi of the stage STi maintains a high level during the t1 period. Additionally, the voltage charged (supplied or applied) in the second node N2 maintains a high level without variation (or distortions).

[0063] Next, during t2 period, an output signal SSi-1 of a previous stage (or start pulse SP) of a low level is supplied to a source electrode of the third transistor M3 and a gate electrode of the fourth transistor M4.

[0064] Moreover, the first clock signal CLK1 of a high level is supplied to a gate electrode of the sixth transistor M6, and the second clock signal CLK2 of a low level and the third clock signal CLK3 of the high level are supplied to the gate electrode of the third transistor M3 and the drain electrode of the second transistor M2, respectively.

[0065] Accordingly, the third transistor M3 is turned-on according to the second clock signal CLK2 of a low level, and transfers a low level (voltage or phase) of the output signal SSi-1 of a previous stage (or start pulse SP) to the second node N2 so that the second node N2 is charged with the low level thereof.

[0066] Further, as the fourth transistor M4 is turned-on according to the low level of the output signal SSi-1 of a previous stage (or start pulse SP) and the second node N2 is charged with the low level thereof, the fourth transistor M4 is turned-on, and charges (supplies or applies) the first node N1 with a high level voltage of the first power supply VDD.

[0067] As the first node N1 is charged with the high level voltage, the first transistor M1 is turned-off. As the second node N2 is charged with the low level voltage, the second transistor M2 is turned-on, so that the third clock signal CLK3 of a high level is supplied to an output line of the stage STi. At this time, a voltage capable of turning-on the second transistor M2 is stored (or charged) in the first capacitor C1.

[0068] Next, during the period t3, an output signal SSi-1 of a previous stage (or start pulse SP) of a high level is supplied to the source electrode of the third transistor M3 and the gate electrode of the fourth transistor M4.

[0069] Furthermore, the first and second clock signals CLK1 and CLK2 of a high level are respectively supplied to a gate electrode of the sixth transistor M6 and a gate electrode of the third transistor M3, and the third clock signal CLK3 of the low level is provided to the drain electrode of the second transistor M2.

[0070] Accordingly, the third, fourth, and sixth transistors M3, M4, and M6 are turned-off according to the output signal SSi-1 of a previous stage (or start pulse SP) of a high level, and the high level of the first and second clock signals CLK1 and CLK2.

[0071] In addition, because the voltage capable of turning-on the second transistor M2 was stored (or charged) in the first capacitor C1 during the previous time period of t2, the second transistor M2 maintains an on state. Accordingly, a waveform in the output signal SSi of the stage STi depends on that of the third clock signal CLK3. Therefore, the output signal SSi of the stage STi has a low level during the t3 period.

[0072] At this time, as the third clock signal CLK3 changes from a high level to a low level, through a coupling of a capacitor connected to the gate-source of the second transistor M2 (for example a parasitic capacitance coupled between the gate of the second transistor M2 and the input line of the third clock signal CLK3), the second node N2 is charged with a level (or voltage level) less than the low level thereof during the t2 period.

[0073] Accordingly, the fifth transistor M5 that is con-

nected to the second node N2 is turned-on, to thereby charge (or apply) a high level voltage VDD to the first node N1.

[0074] Thereafter, during the t4 period, an output signal SSi-1 of the previous stage (or start pulse SP) of a high level is supplied to the source electrode of the third transistor M3 and the gate electrode of the fourth transistor M4.

[0075] Furthermore the first, second, and third clock signals CLK1, CLK2, and CLK3 of a high level are respectively supplied to a gate electrode of the sixth transistor M6, a gate electrode of the third transistor M3, and a drain electrode of the second transistor M2.

[0076] Accordingly, the third, fourth, and sixth transistors M3, M4, and M6 maintain a turned-off state according to the output signal SSi-1 (or start pulse SP) of a previous stage of a high level, and the first and second clock signals CLK1 and CLK2.

[0077] In addition, the second transistor M2 maintains an on state by way of the first capacitor C1. Accordingly, the output signal SSi of the stage STi has a high level according to a waveform of the third clock signal CLK3.

[0078] At this time, by way of a coupling of a capacitor of gate-source of the second transistor M2, the second node N2 is charged with a level that is a predetermined value higher than that of the low level occurring during the t2 period and charged with an intermediate level voltage, which is similar or identical with a value thereof occurring during the t2 period. Accordingly, the fifth transistor M5 maintains a turned-on state, so that the first node N1 maintains a high level.

[0079] During the next time periods, since the output signal SSi-1 of the previous stage (start pulse SP) maintains a high level, the output signal SSi of the stage STi also maintains the high level.

[0080] For example, during the t5 period, although the second clock signal CLK2 of a low level is supplied, because the output signal SSi-1 of the previous stage (start pulse SP) supplied through the third transistor M3 continues to maintain a high level, the second node N2 is charged with a high level, with the result that a voltage capable of turning-off the second transistor M2 is applied to the second node N2 (or stored in the first capacitor C1). Next, during t6 period, although the third clock signal CLK3 of a low level is supplied, the second transistor M2 maintains a turned-off state, so that the output signal SSi of the representative stage STi maintains a high level regardless of a level of the third clock signal CLK3 due to the high level of the second node N2 (or the first capacitor C1).

[0081] In the aforementioned operations thereof, the various stages ST11 to ST1n of the shift register each delay a phase of the output signal SSi-1 of the previous stage (start pulse SP) that is supplied thereto by one clock in response to first, second, and/or third clock signals CLK1, CLK2, and/or CLK3, and outputs the phase-delayed signal to a respective output line SS1 to SSn.

[0082] FIG. 6 is a detailed circuitry diagram showing an embodiment of a representative stage of the shift register of the present invention shown in FIG. 3.

[0083] With reference to FIG. 6, a representative stage STi' comprises a voltage level controller 410 to control the voltage levels of first and second nodes (first and second output nodes) N1 and N2 according to a start pulse SP or an output signal SSi-1 of a previous stage and a second clock signal CLK2; a control capacitor Cc coupled between the first node N1 and an input line of a first clock signal CLK1; a first transistor M1 coupled between a first power supply VDD and a third node (third output node) N3 that is an output node of the stage STi and includes a gate electrode coupled to the first output node N1; and a second transistor M2 coupled between the third output node N3 and an input line of the third clock signal CLK3 and includes a gate electrode coupled to the second output node N3.

[0084] In the embodiment shown, the first and/or second transistors M1, M2 are formed of P-type transistors. The first, second, and third clock signals CLK1, CLK2, and CLK3 have a waveform of a sequentially delayed phase.

[0085] As shown, the voltage level controller 410 includes: a third transistor M3 coupled between an input line of the start pulse SP or an output signal SSi-1 of a previous stage and the second node N2 and includes a gate electrode coupled to an input line of the second clock signal CLK2; a fourth transistor M4 coupled between the first power supply VDD and the first node N1 and includes a gate electrode coupled to the input line of the start pulse SP or an output signal SSi-1 of a previous stage; and a fifth transistor M5 coupled between the first power supply VDD and the first node N1 and includes a gate electrode coupled to the second node N2. Here, the respective third, fourth, and fifth transistors M3, M4, and/or M5 are formed of P-type transistors.

[0086] As shown, the voltage level controller 410 controls a voltage level of the second node N2 according to the start pulse SP or the output signal SSi-1 of a previous stage and the second clock signal CLK2, and controls a voltage level of the first node N1 according to the start pulse SP or the output signal SSi-1 of a previous stage and a voltage level of the second node N2.

[0087] Moreover, the representative stage STi' further comprises a first capacitor C1 coupled between the second node N2 and the third node N3, a second capacitor C2 coupled between the first power supply VDD and the first node N1, and a third capacitor C3 coupled between the first power supply VDD and the second node N2.

[0088] In the representative stage STi' according to the embodiment of FIG. 6, the structures and the operations of the voltage level controller 410, the first and second transistors M1 and M2, and the first to third capacitors C1 to C3 are identical to those shown in the arrangement of FIG. 4. Accordingly, like or the same elements are designated by like or the same numerals. Description of those similar elements or components well not be repeated.

[0089] However, unlike the stage Ski of the embodiment of FIG. 4, the representative stage STi' of the embodiment of FIG. 6 is not connected to a second power supply VSS that is a low level voltage source.

[0090] In the embodiment of FIG. 4, the first node N1 is connected to the second power supply VSS, by way of the sixth transistor M6. When the first clock signal CLK1 has a low level, the sixth transistor M6 charges the first node N1 with a low level voltage of the second power supply VSS. In contrast, in the embodiment of FIG. 6 without the sixth transistor M6, a control capacitor Cc is coupled between the first node N1 and the first clock signal CLK input line that is provided thereto.

[0091] As shown in FIG. 6, when the first clock signal CLK1 of a low level is inputted to the control capacitor Cc, particularly, while the phase of the first clock signal CLK1 drops from a high level to a low level, the control capacitor Cc is charged with a low value of voltage obtained by reducing a voltage of the first node N1 by a predetermined value by way of the coupling.. The control capacitor Cc functions as voltage changing means for changing a voltage of the first node N1 by a predetermined value in accordance with a level of a first clock signal CLK1.

[0092] In detail, when the start pulse SP or an output signal SSi-1 of a previous stage and the first to third clock signals CLK1 to CLK3 in the manner shown in FIG. 5 are supplied to the representative stage STi', the control capacitor Cc functions to reduce a voltage level of the first node N1 to a low value by way of the coupling during the t1 period, which is a period when the first clock signal CLK1 supplies a low level voltage.

[0093] That is, the control capacitor Cc performs the same function as that of the sixth transistor M6 of the arrangement of FIG. 4, yet does not need the second power supply VSS of the arrangement of FIG. 4. In the arrangement of FIG 4, once the first clock signal CLK1 of a low level is supplied, the sixth transistor M6 electrically connects the first node N1 1 to the second power supply VSS that is a low level voltage source to reduce a voltage level of the first node N1 to a low value.

[0094] In this arrangement since an input/output signal waveform of the representative stage STi' is identical with that shown in FIG. 5, a detailed description of an operation of the stage Ski' during respective time periods is not repeated.

[0095] In the representative stage Ski' according to the aforementioned embodiment of FIG. 6, the number of power supply lines is reduced by removing the second power supply VSS. This causes a circuit to be easily designed and a dead space to be reduced.

[0096] FIG. 7A is a circuitry diagram implementing the representative stage STi' shown in FIG. 6 of the shift register shown in PIG. 3. PIG. 7B is a view showing a simulation result of the circuit shown in FIG. 7A.

[0097] With reference to FIG. 7A a shift register is arranged using the representative stage STi' of the embodiment shown in FIG. 6. As shown, three representative stages STi' are connected. With reference to FIG. 7B, the shift register of FIG. 7A sequentially shifts a phase of the start pulse SP supplied thereto according to the first, second, and/or third clock signals CLK1, CLK2, and/or CLK3, which are sequentially phase-delayed. Accordingly, the shift register implemented with the representative stage STi' obtains similar results as those of the shift register implemented with the representative stage STi.

[0098] It will be appreciated that in the above discussion of a signal includes embodiments having one or more signals and vice versa.

[0099] Although discussed in terms of an organic light emitting display, embodiments of the present invention also include other displays, such as liquid crystal displays and/or similar devices.

[0100] In some embodiments, the p-type transistor may be a field effect transistor, or equivalent.

[0101] In various embodiments, the stages have first, second, and third clock signal input lines an input line and an output line, wherein the input line of each stage is connected to the output line of the previous stage or the start pulse input line, and the input line corresponds to one of the first, second, and third clock signal input lines, and a voltage level controller to control voltage levels of the each stage according to an input line signal and a clock signal of the corresponding clock signal input line to output a pulse signal that corresponds to a clock signal of another one of the first, second, and third clock signal input line, as shown in FIG. 6, for example.

[0102] As is clear from the foregoing description, a shift register according to an embodiment of the present invention may ease designing of a shift register, reduce a dead space, and obtain reliable operation characteristics by reducing wires of a power supply line.

[0103] Further, by forming most, if not all transistors included in the shift register as P-type transistors, an active matrix type organic light emitting display including P-type transistors in a pixel array can be more easily manufactured.

[0104] Although a few embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes might be made in the embodiment without departing from the principles of the invention, the scope of which is defined in the claims and their equivalents.

Claims

1. A shift register including a plurality of stages (ST11, ..., ST1N) that are sequentially connected to each other, the plurality of stages (ST11, ..., STIN) including a first stage ST11 connected to a start pulse input line (SP), each of the plurality of stages (ST11, ..., ST1N) comprising:

   first, second and third nodes (N1,N2,N3), the

third node N3 being an output node of the stage;
a voltage level controller (410) for controlling voltage levels of the first and second nodes (N1,N2) according to a said start pulse or an output signal of a previous stage and a second clock signal (CLK2);
voltage changing means for changing a voltage of the first node (N 1) by a predetermined value in accordance with a level of a first clock signal (CLK1);
a first transistor (M1) coupled between a first power supply (VDD) and the third node (N3), and including a gate electrode coupled to the first node (N1); and
a second transistor (M2) coupled between the third node (N3) and an input line of the third clock signal (CLK3), and including a gate electrode coupled to the second node (N2);
wherein the voltage changing means comprises a control capacitor (Cc) coupled between the first node (N1) and an input line of the first clock signal (CLK1), **characterized in that** control capacitor (Cc) is configure to reduce a voltage of the first node (N1) according to the first clock signal (CLK1) applied to the control capacitor (Cc) prior to application of the start pulse or the output signal of the previous stage.

2. A shift register according to claim 1, wherein the voltage level controller includes:

a third transistor (M3) coupled between the start pulse input line or an output signal line of a previous stage and the second node, and including a gate electrode coupled to an input line of the second clock signal;
a fourth transistor (M4) coupled between the first power supply and the first node, and including a gate electrode coupled to the start pulse input line or an output signal of a previous stage; and
a fifth transistor (M5) coupled between the first power supply and the first node, and including a gate electrode coupled to the second node.

3. A shift register according to claim 2, wherein the third, fourth, and fifth transistors each comprise a P-type transistor.

4. A shift register according to any one of claims 1 to 3, wherein the voltage level controller is arranged to control a voltage level of the second node according to the start pulse or the output signal of a previous stage and the second clock signal, and
to control a voltage level of the first node according to the start pulse or the output signal of a previous stage and a voltage level of the second output node.

5. A shift register according to any preceding claim, wherein the control capacitor is arranged to reduce a voltage of the first node by a predetermined value when the first clock signal of low level is inputted to the control capacitor.

6. A shift register according to any preceding claim, wherein the first and second transistors each comprise a P-type transistor.

7. A shift register according to any preceding claim, wherein the first, second, and third clock signals have a waveform a phase of which is sequentially delayed.

8. A shift register according to any preceding claim, further comprising a first capacitor coupled between the second node and the third node.

9. A shift register according to any preceding claim, further comprising a second capacitor coupled between the first power supply and the first node, and a third capacitor coupled between the first power supply and the second node.

10. An organic light emitting display including the shift register according to any one of claims 1 to 9, the organic light emitting display comprising:

scan lines and data lines;
a pixel portion including a plurality of pixels electrically connected to the scan lines and the data lines;
a scan driver including the shift register arranged to sequentially apply scan signals to the scan lines; and
a data driver arranged to apply a data signal to the data lines.

11. An organic light emitting display according to claim 10, further comprising a substrate, wherein the shift register and the pixels comprise transistors of the same conduction type so that the shift register and the pixels are simultaneously formable on the substrate.

12. An organic light emitting display according to claim 10, wherein the transistors are p-type.

Patentansprüche

1. Schieberegister einschließlich einer Vielzahl von Stufen (ST11,...,ST1N), die sequenziell miteinander verbunden sind, wobei die Vielzahl von Stufen (ST11,...,ST1N) eine erste Stufe ST11 enthält, die an eine Startimpuls-Eingangsleitung (SP) angeschlossen ist, wobei jede der Vielzahl von Stufen (ST11,...,ST1N) Folgendes umfasst:

ein erster, zweiter und dritter Knoten (N1,N2,N3), wobei der dritte Knoten N3 ein Ausgangsknoten der Stufe ist;
eine Spannungspegelsteuerung (410) zum Steuern von Spannungspegeln des ersten und zweiten Knotens (N1,N2) gemäß einem solchen Startimpuls oder einem Ausgangssignal einer vorhergehenden Stufe und einem zweiten Taktsignal (CLK2);
Spannungsänderungsmittel zum Ändern einer Spannung des ersten Knotens (N1) durch einen vorgegebenen Wert gemäß einem Pegel eines ersten Taktsignals (CLK1);
einen ersten Transistor (M1), der zwischen einer ersten Leistungsversorgung (VDD) und dem dritten Knoten (N3) angekoppelt ist, und eine an den ersten Knoten (N1) gekoppelte Elektrode enthaltend; und
einen zweiten Transistor (M2), der zwischen dem dritten Knoten (N3) und einer Eingangsleitung des dritten Taktsignals (CLK3) angekoppelt ist, und eine Gate-Elektrode enthaltend, die an den zweiten Knoten (N2) gekoppelt ist;
worin das Spannungsänderungsmittel einen Steuerkondensator (Cc) umfasst, der zwischen dem ersten Knoten (N1) und einer Eingangsleitung des ersten Taktsignals (CLK1) angekoppelt ist, **dadurch gekennzeichnet, dass** der Steuerkondensator (Cc) dazu konfiguriert ist, eine Spannung des ersten Knotens (N1) gemäß einem ersten Taktsignal (CLK1) zu reduzieren, das vor Anlegen des Startimpulses oder des Ausgangssignals der vorhergehenden Stufe an den Steuerkondensator (Cc) angelegt wird.

2. Schieberegister nach Anspruch 1, worin die Spannungspegelstauerung Folgendes enthält:

einen dritten Transistor (M3), der zwischen der Startimpuls-Eingangsleitung oder einer Ausgangssignalleitung einer vorhergehenden Stufe und dem zweiten Knoten angekoppelt ist, und eine Gate-Elektrode enthaltend, die an eine Eingangsleitung des zweiten Taktsignals gekoppelt ist,
einen vierten Transistor (M4), der zwischen der ersten Leistungsversorgung und dem ersten Knoten angekoppelt ist, und eine Gate-Elektrode enthaltend, die an die Startimpuls-Eingangsleitung oder ein Ausgangssignal einer vorhergehenden Stufe gekoppelt ist; und
einen fünften Transistor (M5), der zwischen der ersten Leistungsversorgung und dem ersten Knoten angekoppelt ist, und eine Gate-Elektrode enthaltend, die an den zweiten Knoten gekoppelt ist.

3. Schieberegister nach Anspruch 2, worin der dritte, vierte und fünfte Transistor jeweils einen P-Typ-Transistor umfasst.

4. Schieberegister nach einem der Absprüche 1 bis 3, worin die Spannungspegelsteuerung dazu angeordnet ist, einen Spannungspegel des zweiten Knotens gemäß dem Startimpuls oder dem Ausgangssignal einer vorhergehenden Stufe und dem zweiten Taktsignal zu steuern, und
einen Spannungspegel des ersten Knotens gemäß dem Startimpuls oder dem Ausgangssignal einer vorhergehenden Stufe und einen Spannungspegel des zweiten Ausgangsknotens zu steuern.

5. Schieberegister nach einem der vorhergehenden Ansprüche, worin der Steuerkondensator dazu angeordnet ist, eine Spannung des ersten Knotens um einen vorgegebenen Wert zu reduzieren, wenn das erste Taktsignal mit niedrigem Pegel in den Steuerkondensator eingegeben wird.

6. Schieberegister nach einem der vorhergehenden Ansprüche, worin der erste und zweite Transistor jeweils einen P-Typ-Transistor umfassen.

7. Schieberegister nach einem der vorhergehenden Ansprüche, worin das erste, zweite und dritte Taktsignal jeweils eine Wellenform mit einer Phase haben, die sequenziell verzögert ist.

8. Schieberegister nach einem der vorhergehenden Absprüche, außerdem einen ersten Kondensator umfassend, der zwischen dem zweiten Knoten und dem dritten Knoten angekoppelt ist.

9. Schieberegister nach einem der vorhergehenden Ansprüche, außerdem einen zweiten Kondensator umfassend, der zwischen der ersten Leistungsversorgung und dem ersten Knoten angekoppelt ist, und einen dritten Kondensator, der zwischen der ersten Leistungsversorgung und dem zweiten Knoten angekoppelt ist.

10. Organische lichtemittierende Anzeigevorrichtung, das Schieberegister nach einem der Ansprüche 1 bis 9 enthaltend, wobei die lichtemittierende Anzeigevorrichtung Folgendes umfasst:

Scanleitungen und Datenleitungen;
einen Pixelabschnitt, eine Vielzahl von Pixeln enthaltend, die an die Scanleitungen und die Datenleitungen elektrisch angeschlossen sind;
einen Scantreiber einschließlich des Schieberegisters, der zum sequenziellen Anlegen von Scansignalen an die Scanleitungen angeordnet ist; und
einen Datentreiber, der zum Anlegen eines Datensignals an die Datenleitungen angeordnet

ist.

11. Organische lichtemittierende Anzeigevorrichtung nach Anspruch 10, außerdem ein Substrat umfassend, worin das Schieberegister und die Pixel Transistoren desselben Leitungstyps umfassen, sodass das Schieberegister und die Pixel auf dem Substrat gleichzeitig formbar sind.

12. Organische lichtemittierende Anzeigevorrichtung nach Anspruch 10, worin die Transistoren vom P-Typ sind.

Revendications

1. Registre de déphasage comprenant une pluralité d'étages (ST11, ST1N) lesquels sont séquentiellement connectés les uns aux autres, la pluralité d'étages (ST11, .. ., ST1N) comprenant un premier étage ST11 connecté à une ligne d'entrée d'impulsion de départ (SP), chaque étage de la pluralité d'étages (ST11, ..., ST1N) comprenant :

des premier, deuxième et troisième noeuds (N1, N2, N3), le troisième noeud N3 étant un noeud de sortie de l'étage ;
un contrôleur de niveaux de tension (410) pour commander des niveaux de tension des premier et deuxième noeuds (N1, N2) selon une dite impulsion de départ, ou un signal de sortie d'un étage précédent et un deuxième signal d'horloge (CLK2) ;
un moyen de modification de tension pour modifier une tension du premier noeud (N1) par une valeur prédéterminée selon un niveau d'un premier signal d'horloge (CLK1);
un premier transistor (M1) couplé entre un premier bloc d'alimentation (VDD) et le troisième noeud (N3), et comprenant une électrode de grille couplée au premier noeud (N1) ; et
un deuxième transistor (M2) couplé entre le troisième noeud (N3) et une ligne d'entrée du troisième signal d'horloge (CLK3), et comprenant une électrode de grille couplée au deuxième noeud (N2) ;
dans lequel le moyen de modification de tension comprend un condensateur de commande (Cc) couplé entre le premier noeud (N1) et une ligne d'entrée du premier signal d'horloge (CLK1), **caractérisé en ce que** le condensateur de commande (Cc) est configuré de manière à réduire une tension du premier noeud (N1) selon le premier signal d'horloge (CLK1) appliqué au condensateur de commande (Cc) préalablement à l'application de l'impulsion de départ ou du signal de sortie de l'étage précédent.

2. Registre de déphasage selon la revendication 1, dans lequel le contrôleur de niveau de tension comprend :

un troisième transistor (M3) couplé entre la ligne d'entrée d'impulsion de départ ou une ligne de signal de sortie d'un étage précédent et le deuxième noeud, et comprenant une électrode de grille couplée à une ligne d'entrée du deuxième signal d'horloge ;
un quatrième transistor (M4) couplé entre le premier bloc d'alimentation et le premier noeud, et comprenant une électrode de grille couplée à la ligne d'entrée d'impulsion de départ ou à un signal de sortie d'un étage précédent ; et
un cinquième transistor (M5) couplé entre le premier bloc d'alimentation et le premier noeud, et comprenant une électrode de grille couplée au deuxième noeud.

3. Registre de déphasage selon la revendication 2, dans lequel les troisième, quatrième, et cinquième transistors comprennent chacun un transistor de type P.

4. Registre de déphasage selon l'une quelconque des revendications 1 à 3, dans lequel le contrôleur de niveau de tension est agencé de manière à commander un niveau de tension du deuxième noeud selon l'impulsion de départ ou le signal de sortie d'un étage précédent et le deuxième signal d'horloge ; et agencé de manière à commander un niveau de tension du premier noeud selon l'impulsion de départ ou le signal de sortie d'un étage précédent et un niveau de tension du deuxième noeud de sortie.

5. Registre de déphasage selon l'une quelconque des revendications précédentes, dans lequel le condensateur de commande est agencé de manière à réduire une tension du premier noeud, d'une valeur prédéterminé, lorsque le premier signal d'horloge de niveau faible est appliqué au condensateur de commande.

6. Registre de déphasage selon l'une quelconque des revendications précédentes, dans lequel les premier et deuxième transistors comprennent chacun un transistor de type P.

7. Registre de déphasage selon l'une quelconque des revendications précédentes, dans lequel les premier, deuxième et troisième signaux d'horloge présentent une forme d'onde dont une phase est retardée de façon séquentielle.

8. Registre de déphasage selon l'une quelconque des revendications précédentes, comprenant en outre un premier condensateur couplé entre le deuxième

noeud et le troisième noeud.

9. Registre de déphasage selon l'une quelconque des revendications précédentes, comprenant en outre un second condensateur couplé entre le premier bloc d'alimentation et le premier noeud, et un troisième condensateur couplé entre le premier bloc d'alimentation et le deuxième noeud.

10. Affichage électroluminescent organique comprenant le registre de déphasage selon l'une quelconque des revendications 1 à 9, l'affichage luminescent organique comprenant :

des lignes de balayage et des lignes de données ;
une partie de pixels comprenant une pluralité de pixels connectés électriquement aux lignes de balayage et aux lignes de données ;
un pilote de balayage comportant le registre de déphasage agencé de manière à appliquer séquentiellement les signaux de balayage aux lignes de balayage ; et
un pilote de données agencé de manière à appliquer un signal de données aux lignes de données.

11. Affichage luminescent organique selon la revendication 10, comprenant en outre un substrat, dans lequel le registre de déphasage et les pixels comprennent des transistors du même type de conduction, de sorte que le registre de déphasage et les pixels peuvent être simultanément formés sur le substrat.

12. Affichage luminescent organique selon la revendication 10, dans lequel les transistors sont de type p.

FIG. 1
(RELATED ART)

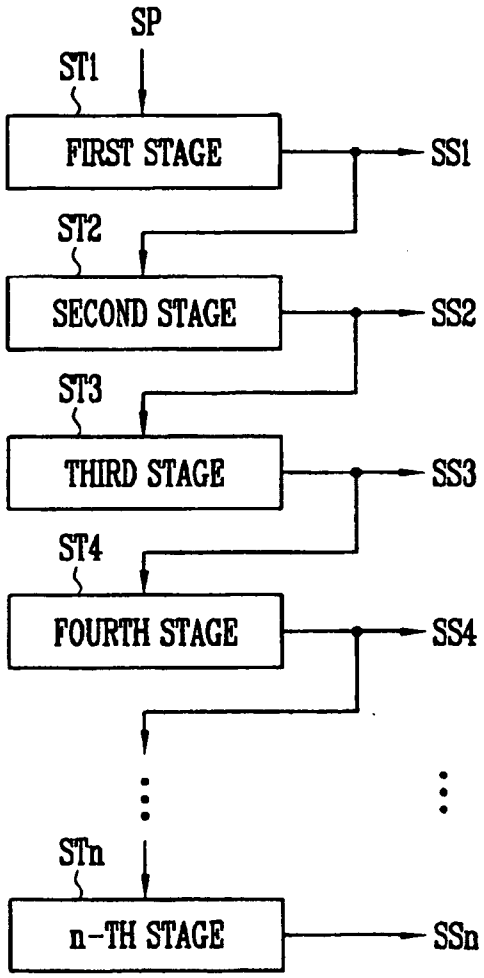


FIG. 2

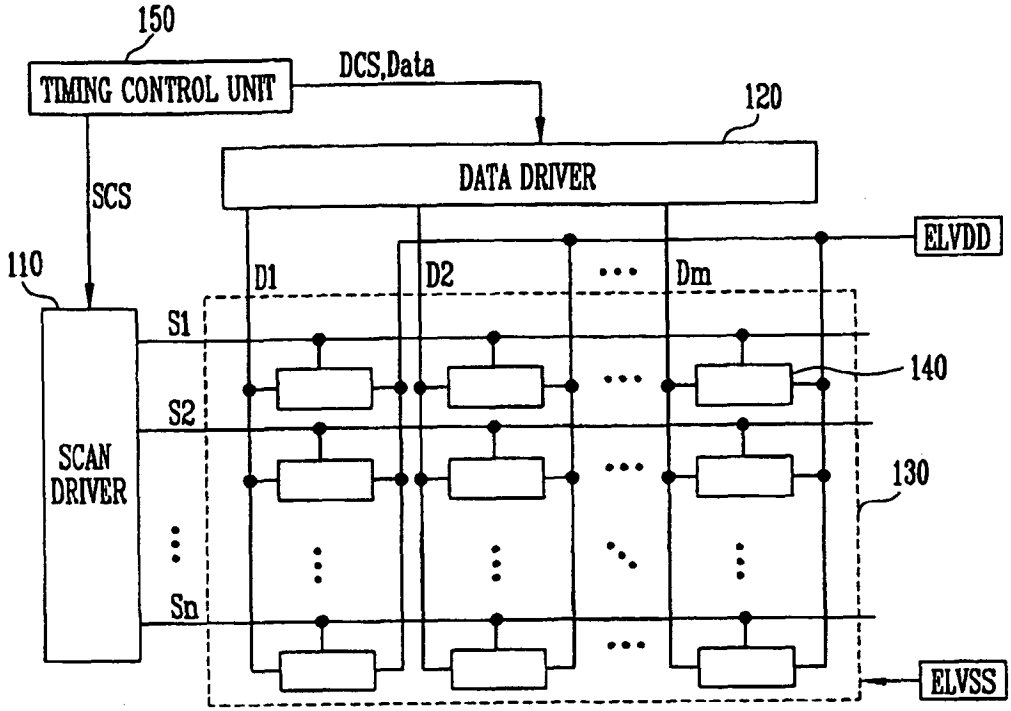

150
TIMING CONTROL UNIT
DCS,Data
120
DATA DRIVER
SCS
110
ELVDD
D1
D2
Dm
S1
S2
Sn
SCAN DRIVER
140
130
ELVSS

FIG. 3

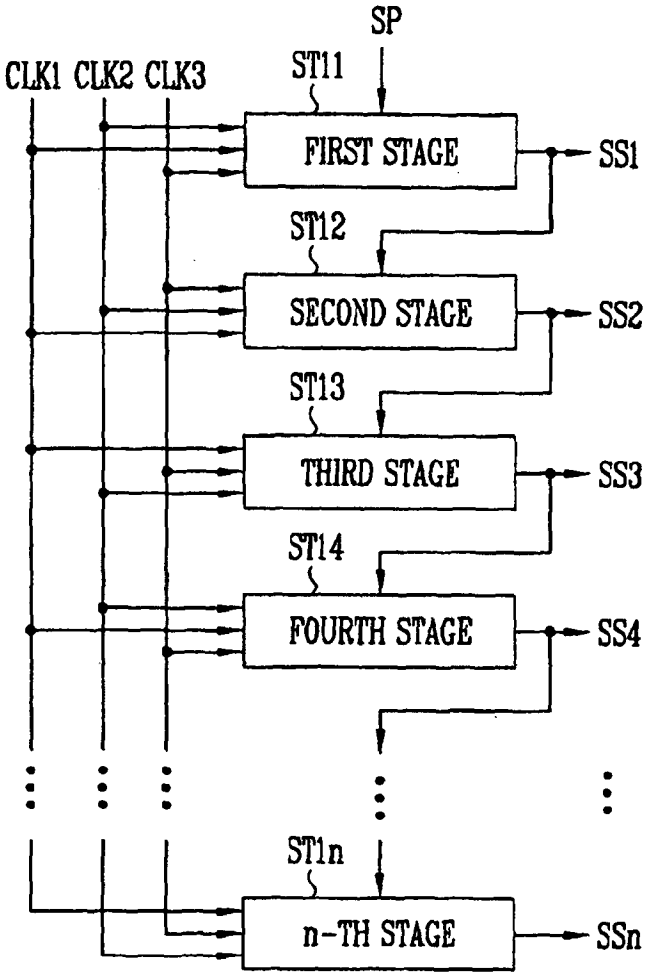

SP
CLK1 CLK2 CLK3
ST11
FIRST STAGE
SS1
ST12
SECOND STAGE
SS2
ST13
THIRD STAGE
SS3
ST14
FOURTH STAGE
SS4
ST1n
n-TH STAGE
SSn

FIG. 4

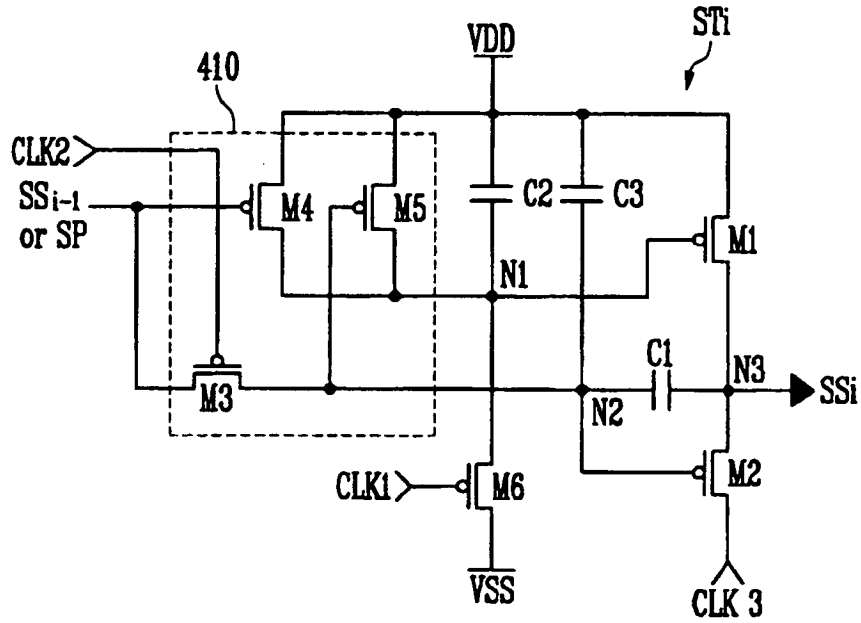

410
VDD
STi
CLK2
SSi-1
or SP
M4
M5
C2
C3
M1
N1
C1
N3
SSi
M3
N2
CLK1
M6
M2
VSS
CLK 3

FIG. 5

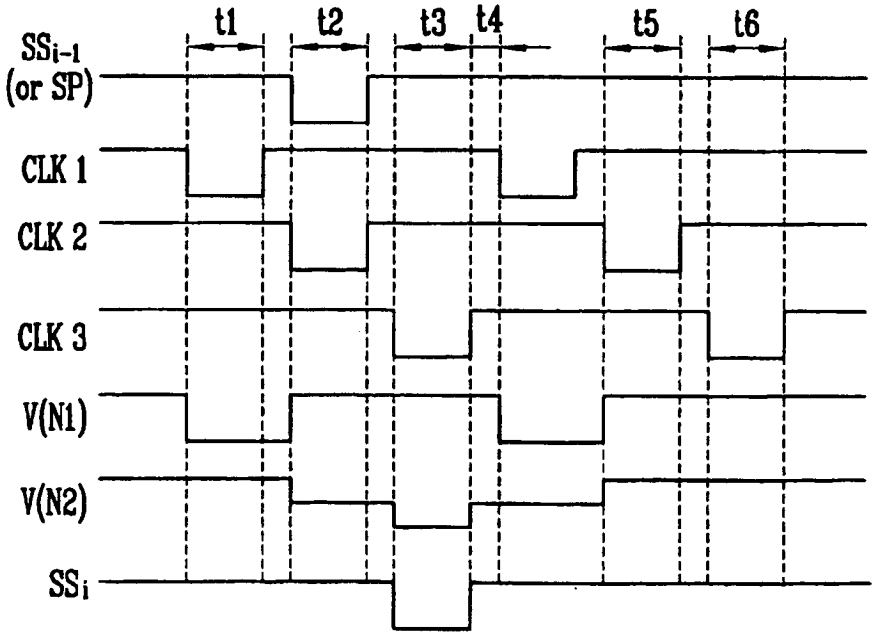

t1
t2
t3
t4
t5
t6
SSi-1
(or SP)
CLK 1
CLK 2
CLK 3
V(N1)
V(N2)
SSi

FIG. 6

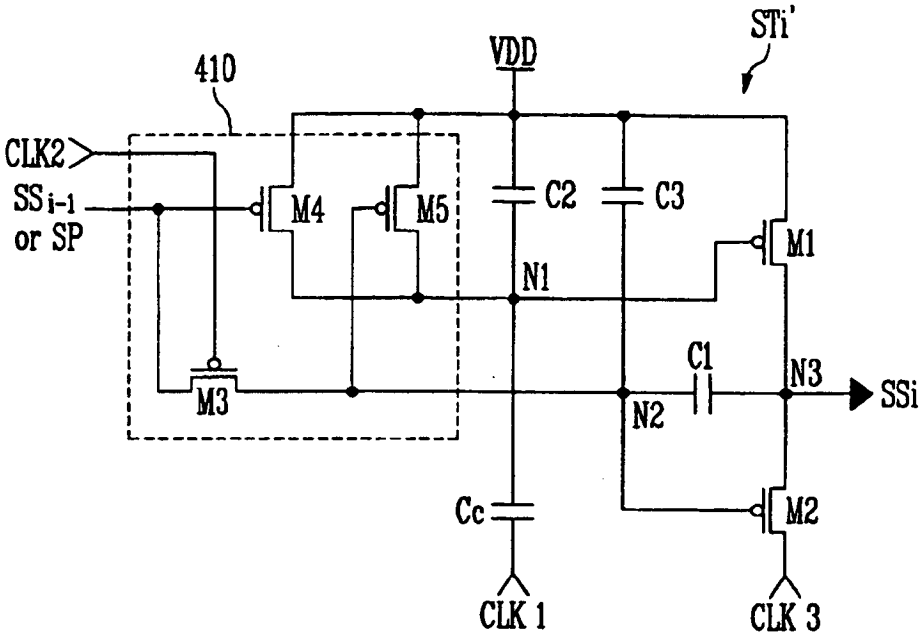

STi'
VDD
410
CLK2
SSi-1
or SP
M4
M5
C2
C3
M1
N1
C1
N3
SSi
M3
N2
Cc
M2
CLK 1
CLK 3

FIG. 7A

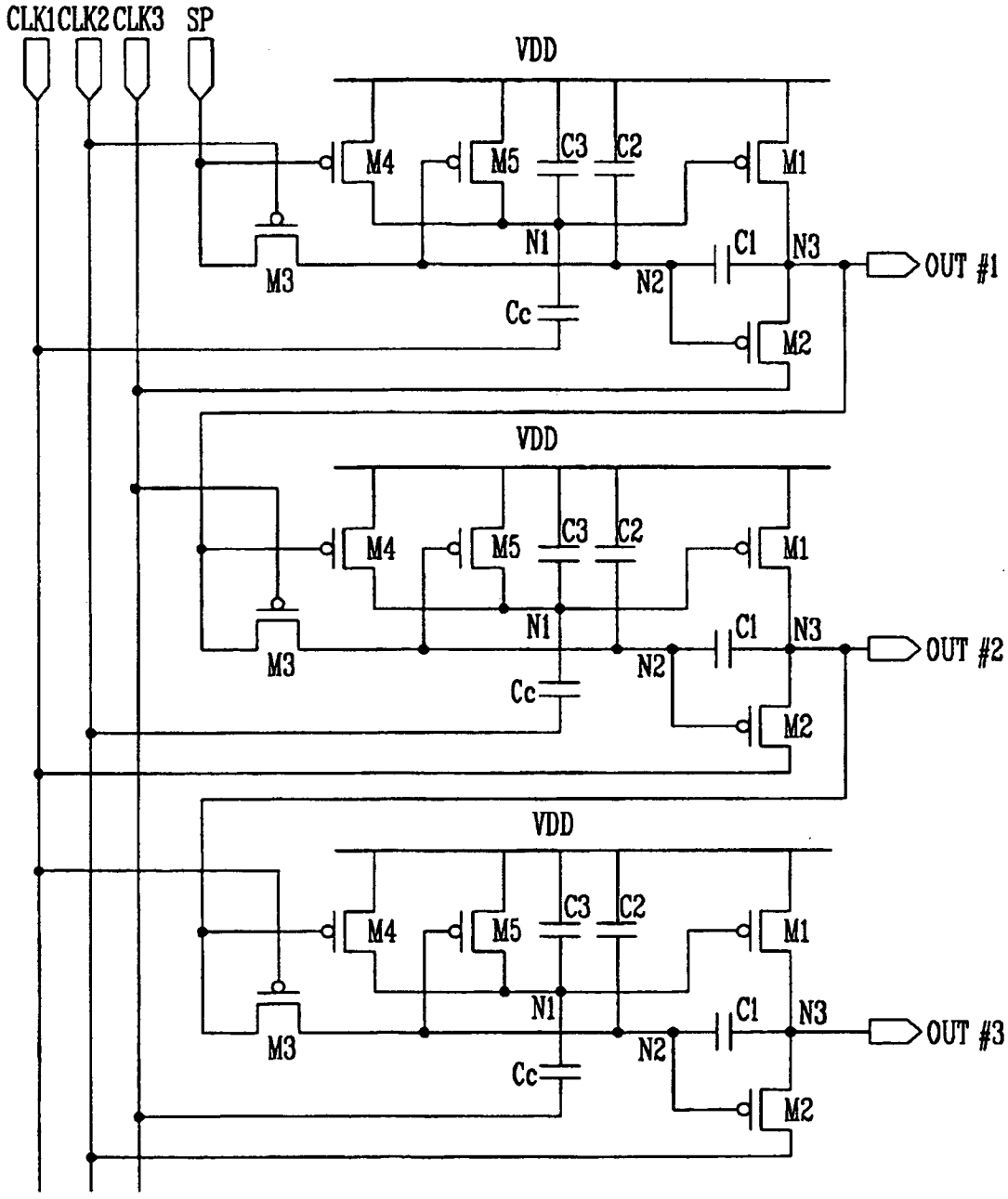
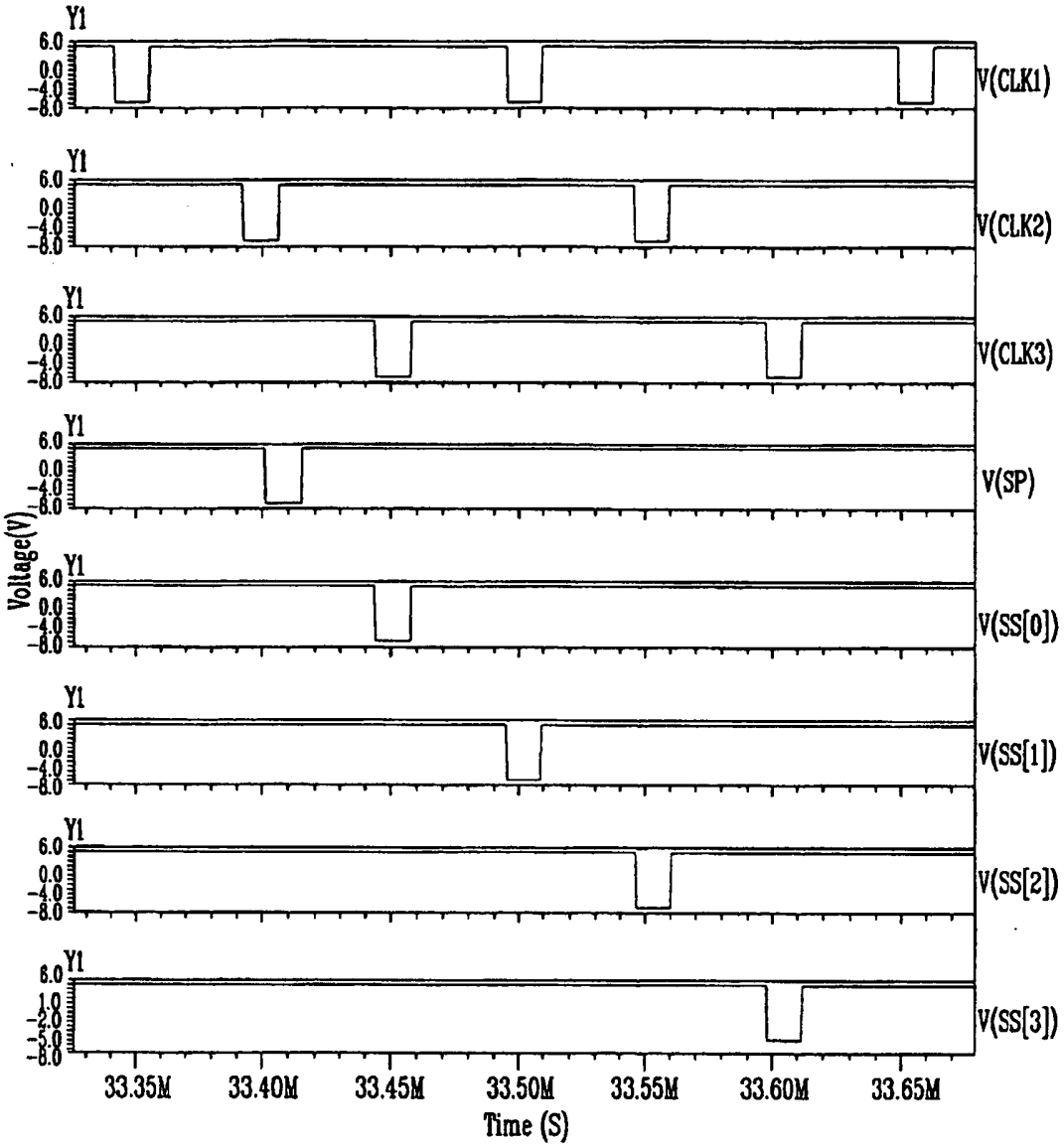

CLK1
CLK2
CLK3
SP
VDD
M4
M5
C3
C2
M1
N1
C1
N3
OUT #1
M3
N2
Cc
M2
VDD
M4
M5
C3
C2
M1
N1
C1
N3
OUT #2
M3
N2
Cc
M2
VDD
M4
M5
C3
C2
M1
N1
C1
N3
OUT #3
M3
N2
Cc
M2

FIG. 7B


Y1
6.0
0.0
-4.0
-8.0
V(CLK1)
V(CLK2)
V(CLK3)
V(SP)
V(SS[0])
V(SS[1])
V(SS[2])
1.0
-2.0
-5.0
V(SS[3])
Voltage(V)
33.35M
33.40M
33.45M
33.50M
33.55M
33.60M
33.65M
Time (S)

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 20040227718 A **[0006]**
- US 20060146978 A **[0006]**
- EP 0731441 A **[0006]**

专利名称(译)	移位寄存器和使用其的有机发光显示器		
公开(公告)号	EP1901274B1	公开(公告)日	2012-09-19
申请号	EP2007253314	申请日	2007-08-21
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星移动显示器有限公司.		
发明人	JEONG, JIN TAE LEGAL & IP TEAM		
IPC分类号	G09G3/32 G11C19/18		
CPC分类号	G11C19/184 G09G3/3266 G09G2300/0426 G09G2310/0286		
优先权	1020060088093 2006-09-12 KR		
其他公开文献	EP1901274A2 EP1901274A3		
外部链接	Espacenet		

摘要(译)

移位寄存器和使用该移位寄存器的有机发光显示器具有移位寄存器的简化设计，该移位寄存器具有高可靠性和减少的死区，包括依赖于连接到起始脉冲输入线的多个级，每个级包括：电压电平控制器，用于根据前一级的起始脉冲或输出信号和第二时钟信号控制第一和第二输出节点的电压电平;控制电容器，耦合在第一输出节点和第一时钟信号的输入线之间;第一晶体管，耦合在第一电源和第三输出节点之间，并包括耦合到第一输出节点的栅电极;第二晶体管，耦合在第三输出节点和第三时钟信号的输入线之间，并包括耦合到第二输出节点的栅电极。

FIG. 1
(RELATED ART)