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(54) **Title**: ORGANIC LIGHT-EMITTING DIODE DISPLAY WITH BOTTOM SHIELDS

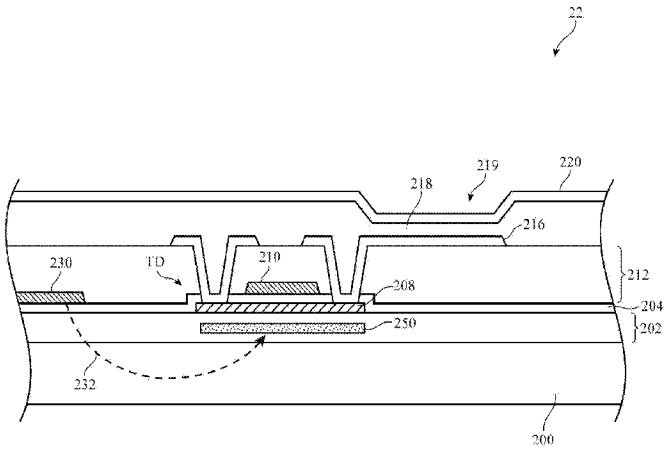


FIG. 5

(57) **Abstract**: A display may have an array of organic light-emitting diode display pixels. Each display pixel may have a light-emitting diode that emits light under control of a drive transistor. Each display pixel may also have control transistors for compensating and programming operations. The array of display pixels may have rows and columns. Row lines may be used to apply row control signals to rows of the display pixels. Column lines (data lines) may be used to apply display data and other signals to respective columns of display pixels. A bottom conductive shielding structure may be formed below each drive transistor. The bottom conductive shielding structure may serve to shield the drive transistor from any electric field generated from the adjacent row and column lines. The bottom conductive shielding structure may be electrically floating or coupled to a power supply line.

WO 2015/112203 A1

Organic Light-Emitting Diode Display with Bottom Shields

This application claims priority to United States Patent Application 14/488,725, filed September 17, 2014, and United States Provisional Patent Application No. 61/929,907, filed January 21, 2013, which are hereby incorporated by reference herein in their entireties.

Background

[0001] This relates generally to electronic devices with displays and, more particularly, to display driver circuitry for displays such as organic-light-emitting diode displays.

[0002] Electronic devices often include displays. For example, cellular telephones and portable computers include displays for presenting information to users.

[0003] Displays such as organic light-emitting diode displays have an array of display pixels based on light-emitting diodes. In this type of display, each display pixel includes a light-emitting diode and thin-film transistors for controlling application of a signal to the light-emitting diode to produce light.

[0004] An organic light-emitting diode display pixel includes a drive thin-film transistor connected to a data line via an access thin-film transistor. The access transistor may have a gate terminal that receives a scan signal via a corresponding scan line. Image data on the date line can be loaded into the display pixel by asserting the scan signal to turn on the access transistor.

[0005] In conventional organic light-emitting diode display pixels, the scan line is formed relatively close to the drive transistor. In certain operating scenarios, the scan line may be biased in a way that a horizontal electric field may be created between the scan line and the channel region of the drive transistor. An electric field generated in this way can interfere

with the operation of the drive thin-film transistor and therefore result in undesired color artifacts.

[0006] It would therefore be desirable to be able to provide improved displays such as improved organic light-emitting diode displays.

Summary

[0007] An electronic device may include a display having an array of display pixels. The display pixels may be organic light-emitting diode display pixels. Each display pixel may have an organic light-emitting diode that emits light. A drive transistor in each display pixel may apply current to the organic light-emitting diode in that display pixel. The drive transistor may be characterized by a threshold voltage.

[0008] Each display pixel may have control transistors that are used in compensating the display pixels for variations in the threshold voltages. During compensation operations, a reference voltage may be provided to the display pixels. The control transistors may also be used in loading display data into the display pixels during programming operations and in controlling display pixel emission operations.

[0009] Each display pixel may be provided with conductive shielding structures formed directly below the drive transistors to prevent any horizontal electric field generated from biasing the control transistors from interfering with the operation of the drive transistors. The conductive shielding structures may only be formed below the drive transistors and not the control transistors.

[0010] The conductive shielding structures may be formed from transparent conductive material or opaque conductive material. The conductive shielding structures may be electrically floating or may be shorted to a common power supply line such as a common cathode electrode. In particular, the conductive shielding structures may be formed in at least one buffer layer interposed between the drive transistor and a transparent substrate over which the drive transistor is formed. Conductive shields formed in this way are therefore sometimes referred to as bottom shields.

Brief Description of the Drawings

[0011] FIG. 1 is a diagram of an illustrative electronic device having a display in accordance with an embodiment.

[0012] FIG. 2 is a diagram of an illustrative display such as an organic light-emitting diode display having an array of organic light-emitting diode display pixels in accordance with an embodiment.

[0013] FIG. 3 is a diagram of an illustrative organic light-emitting diode display pixel of the type that may be used in a display in accordance with an embodiment.

[0014] FIG. 4 is a cross-sectional side view of conventional organic light-emitting diode display pixel structures.

[0015] FIG. 5 is a cross-sectional side view of an illustrative organic light-emitting diode display pixel having a drive transistor and a conductive shielding structure formed directly below the drive transistor in accordance with an embodiment.

[0016] FIG. 6 is a top view of multiple display pixels of the type shown in FIG. 5 having conductive shielding structures that are electrically floating in accordance with an embodiment.

[0017] FIG. 7 is a top view of multiple display pixels of the type shown in FIG. 5 having conductive shielding structures that are shorted to one another in accordance with an embodiment.

[0018] FIG. 8 is a diagram showing how at least some conductive shielding structures in a display pixel array may be shorted to a common cathode electrode in accordance with an embodiment.

[0019] FIG. 9 is a cross-sectional side view of a peripheral portion of the display pixel array of FIG. 9 showing how the conductive shielding structures can be connected to the cathode electrode using vias in accordance with an embodiment.

Detailed Description

[0020] An illustrative electronic device of the type that may be provided with an organic light-emitting diode (OLED) display is shown in FIG. 1. As shown in FIG. 1, electronic device 10 may have control circuitry 16. Control circuitry 16 may include storage and processing circuitry for supporting the operation of device 10. The storage and processing circuitry may include storage such as hard disk drive storage, nonvolatile memory (e.g., flash memory or other electrically-programmable-read-only memory configured to form a solid state drive), volatile memory (e.g., static or dynamic random-access-memory), etc. Processing circuitry in control circuitry 16 may be used to control the operation of device 10. The processing circuitry may be based on one or more microprocessors, microcontrollers, digital signal processors, baseband processors, power management units, audio codec chips, application specific integrated circuits, programmable integrated circuits, etc.

[0021] Input-output circuitry in device 10 such as input-output devices 12 may be used to allow data to be supplied to device 10 and to allow data to be provided from device 10 to external devices. Input-output devices 12 may include buttons, joysticks, click wheels, scrolling wheels, touch pads, key pads, keyboards, microphones, speakers, tone generators, vibrators, cameras, sensors, light-emitting diodes and other status indicators, data ports, etc. A user can control the operation of device 10 by supplying commands through input-output devices 12 and may receive status information and other output from device 10 using the output resources of input-output devices 12.

[0022] Input-output devices 12 may include one or more displays such as display 14. Display 14 may be a touch screen display that includes a touch sensor for gathering touch input from a user or display 14 may be insensitive to touch. A touch sensor for display 14 may be based on an array of capacitive touch sensor electrodes, acoustic touch sensor structures, resistive touch components, force-based touch sensor structures, a light-based touch sensor, or other suitable touch sensor arrangements.

[0023] Control circuitry 16 may be used to run software on device 10 such as operating system code and applications. During operation of device 10, the software running on control circuitry 16 may display images on display 14 in input-output devices.

[0024] FIG. 2 shows display 14 that includes structures formed on one or more layers such as substrate 24. Layers such as substrate 24 may be formed from planar rectangular layers of material such as planar glass layers. Display 14 may have an array of display pixels 22 for displaying images for a user. The array of display pixels 22 may be formed from rows and columns of display pixel structures on substrate 24. These structures may include thin-film transistors such as polysilicon thin-film transistors, semiconducting oxide thin-film transistors, etc. There may be any suitable number of rows and columns in the array of display pixels 22 (e.g., ten or more, one hundred or more, or one thousand or more).

[0025] Display driver circuitry such as display driver integrated circuit 15 may be coupled to conductive paths such as metal traces on substrate 24 using solder or conductive adhesive. Display driver integrated circuit 15 (sometimes referred to as a timing controller chip) may contain communications circuitry for communicating with system control circuitry 16 over path 25. Path 25 may be formed from traces on a flexible printed circuit or other cable. The control circuitry may be located on a main logic board in an electronic device such as a cellular telephone, computer, television, set-top box, media player, portable electronic device, or other electronic equipment in which display 14 is being used. During operation, the control circuitry may supply display driver integrated circuit 15 with information on images to be displayed on display 14. To display the images on display pixels 22, display driver integrated circuit 15 may supply clock signals and other control signals to display driver circuitry such as row driver circuitry 18 and column driver circuitry 20. Row driver circuitry 18 and/or column driver circuitry 20 may be formed from one or more integrated circuits and/or one or more thin-film transistor circuits.

[0026] Row driver circuitry 18 may be located on the left and right edges of display 14, on only a single edge of display 14, or elsewhere in display 14. During operation, row driver circuitry 18 may provide row control signals on horizontal lines 28 (sometimes referred to as row lines or "scan" lines). Row driver circuitry may sometimes be referred to as scan line driver circuitry.

[0027] Column driver circuitry 20 may be used to provide data signals D from display driver integrated circuit 15 onto a plurality of corresponding vertical lines 26. Column driver circuitry 20 may sometimes be referred to as data line driver circuitry or source driver

circuitry. Vertical lines 26 are sometimes referred to as data lines. During compensation operations, column driver circuitry 20 may use vertical lines 26 to supply a reference voltage. During programming operations, display data is loaded into display pixels 22 using lines 26.

[0028] Each data line 26 is associated with a respective column of display pixels 22. Sets of horizontal signal lines 28 run horizontally through display 14. Each set of horizontal signal lines 28 is associated with a respective row of display pixels 22. The number of horizontal signal lines in each row is determined by the number of transistors in the display pixels 22 that are being controlled independently by the horizontal signal lines. Display pixels of different configurations may be operated by different numbers of scan lines.

[0029] Row driver circuitry 18 may assert control signals such as scan signals on the row lines 28 in display 14. For example, driver circuitry 18 may receive clock signals and other control signals from display driver integrated circuit 15 and may, in response to the received signals, assert scan signals and an emission signal in each row of display pixels 22. Rows of display pixels 22 may be processed in sequence, with processing for each frame of image data starting at the top of the array of display pixels and ending at the bottom of the array (as an example). While the scan lines in a row are being asserted, control signals and data signals that are provided to column driver circuitry 20 by circuitry 16 direct circuitry 20 to demultiplex and drive associated data signals D onto data lines 26 so that the display pixels in the row will be programmed with the display data appearing on the data lines D. The display pixels can then display the loaded display data.

[0030] In an organic light-emitting diode display, each display pixel contains a respective organic light-emitting diode. A schematic diagram of an illustrative organic light-emitting diode display pixel 22 is shown in FIG. 3. As shown in FIG. 3, display pixel 22 may include a light-emitting diode 30 coupled to a drive transistor TD. A positive power supply voltage V_{DDEL} may be supplied to positive power supply terminal 34, whereas a ground power supply voltage V_{SSEL} may be supplied to ground power supply terminal 36. The state of drive transistor TD controls the amount of current flowing through diode 30 and therefore the amount of emitted light 40 from display pixel 22.

[0031] Display pixel 22 may have storage capacitors Cst1 and Cst2 and one or more transistors that are used as switches such as transistors SW1, SW2, and SW3. Signal EM and

scan signals SCAN1 and SCAN2 are provided to a row of display pixels 22 using row lines 28. Data D is provided to a column of display pixels 22 via data lines 26.

[0032] Signal EM is used to control the operation of emission transistor SW3. Transistor SW1 is used to apply the voltage of data line 26 to node A, which is connected to the gate of drive transistor TD. Transistor SW2 is used to apply a direct current (DC) bias voltage Vini to node B for circuit initialization during compensation operations.

[0033] During compensation operation, display pixels 22 are compensated for pixel-to-pixel variations such as transistor threshold voltage variations. The compensation period includes an initialization phase and a threshold voltage generation phase. Following compensation (i.e., after the compensation operations of the compensation period have been completed), data is loaded into the display pixels. The data loading process, which is sometimes referred to as data programming, takes place during a programming period. In a color display, programming may involve demultiplexing data and loading demultiplexed data into red, green, and blue pixels.

[0034] Following compensation and programming (i.e., after expiration of a compensation and programming period), the display pixels of the row may be used to emit light. The period of time during which the display pixels are being used to emit light (i.e., the time during which light-emitting diodes 30 emit light 40) is sometimes referred to as an emission period.

[0035] During the initialization phase, circuitry 18 asserts SCAN1 and SCAN2 (i.e., SCAN1 and SCAN2 are taken high). This turns on transistors SW1 and SW2 so that a reference voltage signal Vref and initialization voltage signal Vini are applied to nodes A and B, respectively. During the threshold voltage generation phase of the compensation period, signal EM is asserted and switch SW3 is turned on so that current flows through drive transistor TD to charge up the capacitance at node B. As the voltage at node B increases, the current through drive transistor TD will be reduced because the gate-source voltage Vgs of drive transistor TD will approach the threshold voltage Vt of drive transistor TD. The voltage at node B will therefore go to Vref-Vt.

[0036] After compensation (i.e., after initialization and threshold voltage generation), data is programmed into the compensated display pixels. During programming, emission

transistor SW3 is turned off by deasserting signal EM and a desired data voltage D is applied to node A using data line 26. The voltage at node A after programming is display data voltage Vdata. The voltage at node B rises because of coupling with node A. In particular, the voltage at node B is taken to Vref-Vt + (Vdata-Vref) *K, where K is equal to Cst1/(Cst1+Cst2+Coled), where Coled is the capacitance associated with diode 30.

[0037] After compensation and programming operations have been completed, the display driver circuitry of display 14 places the compensated and programmed display pixels into the emission mode (i.e., the emission period is commenced). During emission, signal EM is asserted for each compensated and programmed display pixel to turn on transistor SW3. The voltage at node B goes to Voled, the voltage associated with diode 30. The voltage at node A goes to Vdata + Voled – (Vref-Vt) – (Vdata-Vref)*K. The value of Vgs-Vt for the drive transistor is equal to the difference between the voltage Va of node A and the voltage Vb of node B. The value of Va-Vb is (Vdata-Vref)*(1-K), which is independent of Vt. Accordingly, each display pixel 22 has been compensated for threshold voltage variations so that the amount of light 40 that is emitted by each of the display pixels 22 in the row is proportional only to the magnitude of the data signal D for each of those display pixels.

[0038] FIG. 4 is a cross-sectional side view of conventional OLED display pixel structures. As shown in FIG. 4, the pixel structures are formed on a clear polyimide (PI) substrate 100. Multiple buffer layers 102 are formed on the PI substrate 100. Polysilicon 108 is patterned on buffer layers 102 to form an active region for drive transistor 106. Gate insulating layer 104 is formed on buffer layers 102 over polysilicon 108. A metal gate conductor 110 is formed on gate insulating layer 104 and serves as the gate terminal for drive transistor 106. A metal path 130 that is formed adjacent to transistor 106 may serve as one of the scan lines for the display pixel. A silicon nitride passivation layer (not shown in FIG. 4) may be formed on gate insulating layer 104 over metal structures 110 and 130.

[0039] Thin-film drive transistor 106 formed in this way passes current between cathode 58 (i.e., an indium tin oxide electrode) and anode 116 (i.e., a metal layer) of light-emitting diode 119. As this current passes through organic light-emitting diode emissive electroluminescent layer (emissive layer) 118, light 122 is generated. Display pixels generating light 122 in this way is typically referred to as top emission display pixels.

[0040] During normal display operations, scan line 130 is sometimes biased to a negative voltage (i.e., scan line 130 can be biased to -5V). Assuming buffer layers 102 includes two buffer layers, a negative charge is induced at the top of the PI substrate 100. Negative charge induced in this way can undesirably decrease the amount of current flowing through drive transistor 106 (i.e., the electric field generated between scan line 130 and the channel of transistor 106, as indicated by line 132, can negatively impact the performance of transistor 106). It may therefore be desirable to form display pixels that are immune to this horizontal field effect.

[0041] In accordance with an embodiment, a display pixel 22 having a bottom conductive shield is provided (see, e.g., FIG. 5). As shown in FIG. 5, thin-film transistor structures such as thin-film drive transistor TD may be formed on a transparent substrate 200 made from as glass, polyimide, or other transparent dielectric material. Thin-film transistor TD may serve as the display pixel drive transistor TD that is described in connection with FIG. 3.

[0042] One or more buffer layers such as buffer layers 306 may be formed on substrate 200. Buffer layers 306 may include layers sometimes referred to as a multi-buffer (MB) layer, an active oxide layer, and other layers formed from any suitable transparent dielectric material.

[0043] Active material 208 for transistor TD may be formed on buffer layers 202. Active material 208 may be a layer of polysilicon, indium gallium zinc oxide, amorphous silicon, or other semiconducting material. A gate insulating layer such as gate insulating layer 204 may be formed on buffer layers 202 and over the active material. Gate insulator 204 may be formed form a dielectric such as silicon oxide. A conductive gate structure such as gate conductor 210 may be disposed over gating insulator 204. Gate conductor 210 may serve as the gate terminal for thin-film transistor TD. The portion of active material 208 directly beneath gate 210 may serve as the channel region for transistor TD.

[0044] A conductive path such as path 230 may be formed in close proximity to transistor TD. Path 230 may, for example, be part of a control line for conveying one of the control/data signals to display pixel 22. In one arrangement, path 230 may be part of a scan line for carrying signal SCAN1 to corresponding switch SW1 in pixel 22 (FIG. 3). In another arrangement, path 230 may be part of a scan line for carrying signal SCAN2 to corresponding switch SW2 in pixel 22. In yet another arrangement, path 230 may be part of a control line

for carrying signal EM to corresponding switch SW3 in pixel 22.

[0045] A passivation layer such as a silicon nitride layer (not shown in FIG. 5) may optionally be formed on gate insulating layer 204 and over gate 210. After deposition of the passivation layer, a hydrogenation annealing process may be applied to passivate the thin-film transistor structures.

[0046] One or more dielectric layers 212 (sometimes referred to as interlayer dielectric or "ILD" layers) may be formed over the thin-film transistor structures. The material with which gate 210 and path 230 is formed is sometimes referred to as "M1" metal. The dielectric layer in which the M1 metal is formed may therefore be referred to as an M1 metal routing layer.

[0047] Thin-film transistor structures such as thin-film transistor TD may pass current between cathode 220 (e.g., a transparent conductive layer such as indium tin oxide or indium zinc oxide) and anode 216 (e.g., a light reflecting metal layer) of light-emitting diode 219. As this current passes through organic light-emitting diode emissive electroluminescent layer (emissive layer) 218, light may be generated. Light generated in this way may pass through a corresponding color filter element (not shown), which imparts a desired color to the emitted light. In general, either top or bottom emission display pixel configurations can be implemented for display 14.

[0048] As described above, electric field can sometimes be generated between transistor TD and an adjacent control path such as path 230, as indicated by dotted field line 232. In accordance with an embodiment of the present invention, a conductive shielding structure such as shield 250 may be formed directly beneath drive transistor TD within buffer layers 202. Shield 250 should not be in direct contact with active material 208 and gate insulating layer 204. Shielding structure 250 may be formed from transparent conductive materials such as indium tin oxide, molybdenum, and molybdenum tungsten or opaque conductive materials such as titanium, copper, aluminum, or other metals. Formed in this way, conductive bottom shield 250 may serve to block any horizontal field generated from metal path 230 or any other adjacent control lines for transistor TD (e.g., shield 250 may prevent any undesired horizontal electric fields from negatively impacting the operation of transistor TD). Shield 250 formed below transistor TD in this way is therefore sometimes referred to as

a "bottom" shield or an electric field shield.

[0049] In general, it may only be desirable to form bottom conductive shields directly below the drive transistors in each pixel. In other words, bottom conductive shields need not be formed for the peripheral switching transistors SW1, SW2, and SW3 (FIG. 3). Forming shield 250 only under drive thin-film transistor TD can help reduce any undesired parasitic capacitance within pixel 22, thereby minimizing dynamic power consumption.

[0050] The structures of FIG. 5 form a single subpixel of a particular color. There may be three or four subpixels per display pixel 22 or other suitable number of subpixels per display pixel 22 in display 14. FIG. 6 is a diagram of an exemplary display pixel 22 having three subpixels 22-R, 22-G, and 22-B. Subpixel 22-R may include circuitry for displaying red light (e.g., subpixel 22-R may include a light-emitting diode that emits light through a red color filter element). Subpixel 22-G may include circuitry for displaying green light (e.g., subpixel 22-G may include a light-emitting diode that emits light through a green color filter element). Subpixel 22-B may include circuitry for displaying blue light (e.g., subpixel 22-B may include a light-emitting diode that emits light through a blue color filter element). This is merely illustrative. In general, display pixel 22 may include any number of subpixels configured to transmit red light, green light, blue light, cyan light, magenta light, yellow light, white light, and/or other types of light in the visible spectrum.

[0051] As shown in FIG. 6, each of the subpixels includes a drive transistor TD and a respective conductive light shield 250 that directly overlaps with the footprint of drive transistor TD. Configured in this way, light shield structures 250 serve to prevent any electric field generated as a result of bias voltages applied on control path 230 from interfering with the operation of the drive transistors. The example of FIG. 6 in which bottom shields 250 are electrically floating (i.e., shields 250 are not actively driven by any pull-up or pull-down circuits and are not connected to one another) is merely illustrative. In other suitable arrangements, bottom shields 250 may be shorted using conductive shorting path 252 (see, e.g., FIG. 7).

[0052] As shown in FIG. 7, conductive shorting path 252 may be formed in the same layer as conductive shields 250 (e.g., conductive shorting path 252 may be formed in buffer layers 202 of FIG. 5). Conductive shorting path 252 may also be formed from the same material as

that of shields 250 (e.g., shorting path 252 may be formed from transparent conductive materials such as indium tin oxide, molybdenum, and molybdenum tungsten or opaque conductive materials such as titanium, copper, aluminum, or other metals). Shorting the bottom shields together via conductive path 252 can provide improved shielding capabilities, especially when paths 252 are shorted to some power supply line.

[0053] FIG. 8 is a diagram showing an array of pixels 22 in display 14. As shown in FIG. 8, at least a portion of bottom shields 250 (e.g., conductive shields 250-R, 250-G, and 250-B) can be shorted to a power supply line 254 (e.g., a power supply line on which ground power supply voltage V_{SSEL} is provided) via path 252. Bottom shield shorting paths 252 may be coupled to ground line 254 only at the periphery of display 14. Connected in this way, the bottom shield in each display subpixel is driven to a constant voltage V_{SSEL}, which enables the drive transistor to operate in a more consistent manner across the entire display pixel array.

[0054] Still referring to FIG. 8, the bottom shields in at least some display pixels 22 are floating and are not connected to power supply line 254. This is merely illustrative. As another example, the conductive shields 250 of each subpixel in the entire pixel array may be electrically floating. As yet another example, the conductive shields 250 of each subpixel in the entire pixel array may all be shorted to a ground power supply line, a positive power supply line, or other power supply lines.

[0055] As described above in connection with FIG. 5, bottom shielding structure 250 may be formed in buffer layers 202. In the arrangement in which bottom shielding structure 250 is shorted to a ground line (e.g., a common cathode electrode), the bottom shielding structure can be coupled to the cathode through conductive through-hole or "via" structures formed through the thin-film transistor layers.

[0056] A cross-sectional side view of a peripheral portion 260 of display 14 showing how the bottom shielding structure can be shorted to the cathode electrode is illustrated in FIG. 9. As shown in FIG. 9, conductive shorting path 252 is formed in buffer layers 202 and may extend into the periphery of display 14. One or more M1 metal routing paths such as metal structure 231 may be formed on gate insulating layer 204. A first via structure 290 may be formed through layers 212 and 204 to form a contact with bottom conductive path 252. In

particular, via 290 may establish an electrical connection between path 252 and anode 216. A second via structure 292 may be formed through layer 218 to form a contact with anode 216. In particular, via 282 may serve to establish an electrical connection between anode 216 and cathode 220. Configured in this way, bottom shielding structures 250 of the type shown in FIGS. 5, 7, and 8 may be shorted to the grounding cathode electrode through conductive path(s) 252 and vias 290 and 292.

[0057] In accordance with an embodiment, a display is provided that includes a substrate, a thin-film transistor formed over the substrate, at least one buffer layer interposed between the thin-film transistor and the substrate, and a conductive shielding structure formed in the buffer layer directly below the thin-film transistor.

[0058] In accordance with another embodiment, the conductive shielding structure is formed from transparent conductive material.

[0059] In accordance with another embodiment, the conductive shielding structure is formed from opaque conductive material.

[0060] In accordance with another embodiment, the conductive shielding structure is electrically floating.

[0061] In accordance with another embodiment, the display includes a power supply line, the conductive shielding structure is shorted to the power supply line.

[0062] In accordance with another embodiment, the display includes a cathode electrode shorted to the conductive shielding structure through vias.

[0063] In accordance with another embodiment, the thin-film transistor has a gate formed on a gate insulating layer, and the conductive shielding structure is not in direct contact with the gate insulating layer.

[0064] In accordance with another embodiment, the display includes additional thin-film transistor, the conductive shielding structure is only formed below the thin-film transistor but not below the additional thin-film transistors.

[0065] In accordance with an embodiment, a method of manufacturing a display pixel is provided that includes forming a thin-film transistor over a substrate, forming buffer layers

interposed between the thin-film transistor and the substrate, and forming an electric field shield in the buffer layers for the thin-film transistor.

[0066] In accordance with another embodiment, forming the electric field shield includes forming a conductive shielding structure directly below the thin-film transistor.

[0067] In accordance with another embodiment, the method includes forming a light-emitting diode that is coupled to the thin-film transistor.

[0068] In accordance with another embodiment, the light-emitting diode has a cathode electrode, the method includes shorting the electric field shield to the cathode electrode through conductive via structures.

[0069] In accordance with another embodiment, the electric field shield is not actively driven.

[0070] In accordance with another embodiment, the method includes forming an additional thin-film transistor over the substrate, and forming an additional electric field shield in the buffer layers for the additional thin-film transistor.

[0071] In accordance with another embodiment, the method includes forming a conductive path in the buffer layers that shorts the electric field shield and the additional electric field shield.

[0072] In accordance with an embodiment, an electronic device display is provided that includes display pixels arranged in an array, each display pixel in the array includes a drive transistor, and a conductive shield formed below the drive transistor.

[0073] In accordance with another embodiment, each display pixel in the array further includes a light-emitting diode coupled to the drive transistor.

[0074] In accordance with another embodiment, the conductive shield in each display pixel in the array is electrically floating.

[0075] In accordance with another embodiment, the conductive shield in each display pixel in the array is shorted to a common electrode.

[0076] In accordance with another embodiment, the conductive shield in each display pixel in a first portion of the array is electrically floating, and the conductive shield in each display

pixel in a second portion of the array is shorted to a common electrode.

[0077] The foregoing is merely illustrative and various modifications can be made by those skilled in the art without departing from the scope and spirit of the described embodiments. The foregoing embodiments may be implemented individually or in any combination.

Claims

What is Claimed is:

1. A display, comprising:

a substrate;

a thin-film transistor formed over the substrate;

at least one buffer layer interposed between the thin-film transistor and the substrate; and

a conductive shielding structure formed in the buffer layer directly below the thin-film transistor.

2. The display defined in claim 1, where the conductive shielding structure is formed from transparent conductive material.

3. The display defined in claim 1, where the conductive shielding structure is formed from opaque conductive material.

4. The display defined in claim 1, wherein the conductive shielding structure is electrically floating.

5. The display defined in claim 1, further comprising:

a power supply line, wherein the conductive shielding structure is shorted to the power supply line.

6. The display defined in claim 1, further comprising:

a cathode electrode shorted to the conductive shielding structure through vias.

7. The display defined in claim 1, wherein the thin-film transistor has a gate formed on a gate insulating layer, and wherein the conductive shielding structure is not in direct contact with the gate insulating layer.

8. The display defined in claim 1, further comprising:

additional thin-film transistor, wherein the conductive shielding structure is only formed below the thin-film transistor but not below the additional thin-film transistors.

9. A method of manufacturing a display pixel, comprising:

forming a thin-film transistor over a substrate;

forming buffer layers interposed between the thin-film transistor and the substrate; and

forming an electric field shield in the buffer layers for the thin-film transistor.

10. The method defined in claim 9, wherein forming the electric field shield comprises forming a conductive shielding structure directly below the thin-film transistor.

11. The method defined in claim 9, further comprising:

forming a light-emitting diode that is coupled to the thin-film transistor.

12. The method defined in claim 11, wherein the light-emitting diode has a

cathode electrode, the method further comprising:

shorting the electric field shield to the cathode electrode through conductive via structures.

13. The method defined in claim 9, wherein the electric field shield is not actively driven.

14. The method defined in claim 9, further comprising:

forming an additional thin-film transistor over the substrate; and

forming an additional electric field shield in the buffer layers for the additional thin-film transistor.

15. The method defined in claim 14, further comprising:

forming a conductive path in the buffer layers that shorts the electric field shield and the additional electric field shield.

16. An electronic device display, comprising:

display pixels arranged in an array, wherein each display pixel in the array comprises:

a drive transistor; and

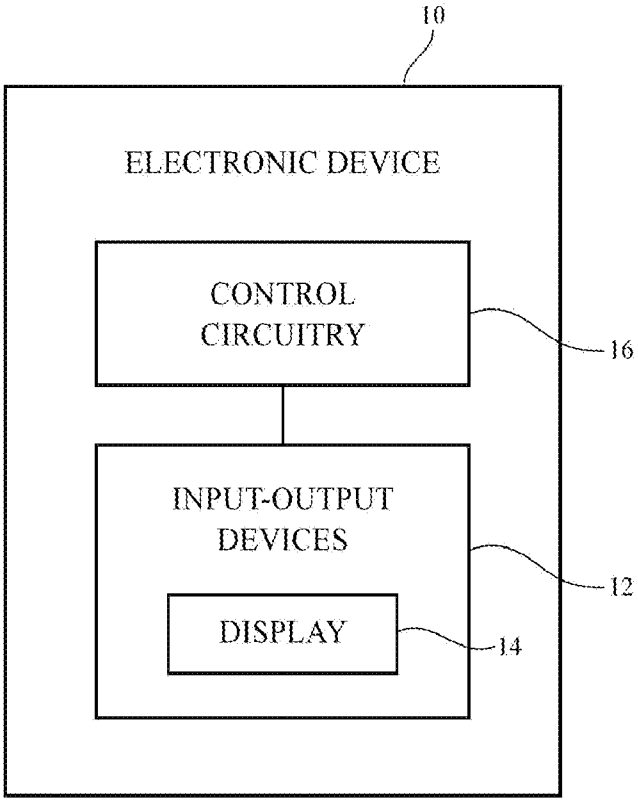
a conductive shield formed below the drive transistor.

17. The electronic device display defined in claim 16, where each display pixel in the array further comprises a light-emitting diode coupled to the drive transistor.

18. The electronic device display defined in claim 17, wherein the conductive shield in each display pixel in the array is electrically floating.

19. The electronic device display defined in claim 17, wherein the conductive shield in each display pixel in the array is shorted to a common electrode.

20. The electronic device display defined in claim 17, wherein the conductive shield in each display pixel in a first portion of the array is electrically floating, and wherein the conductive shield in each display pixel in a second portion of the array is shorted to a common electrode.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ELECTRONIC DEVICE
CONTROL CIRCUITRY
16
INPUT-OUTPUT DEVICES
12
DISPLAY
14

FIG. 1

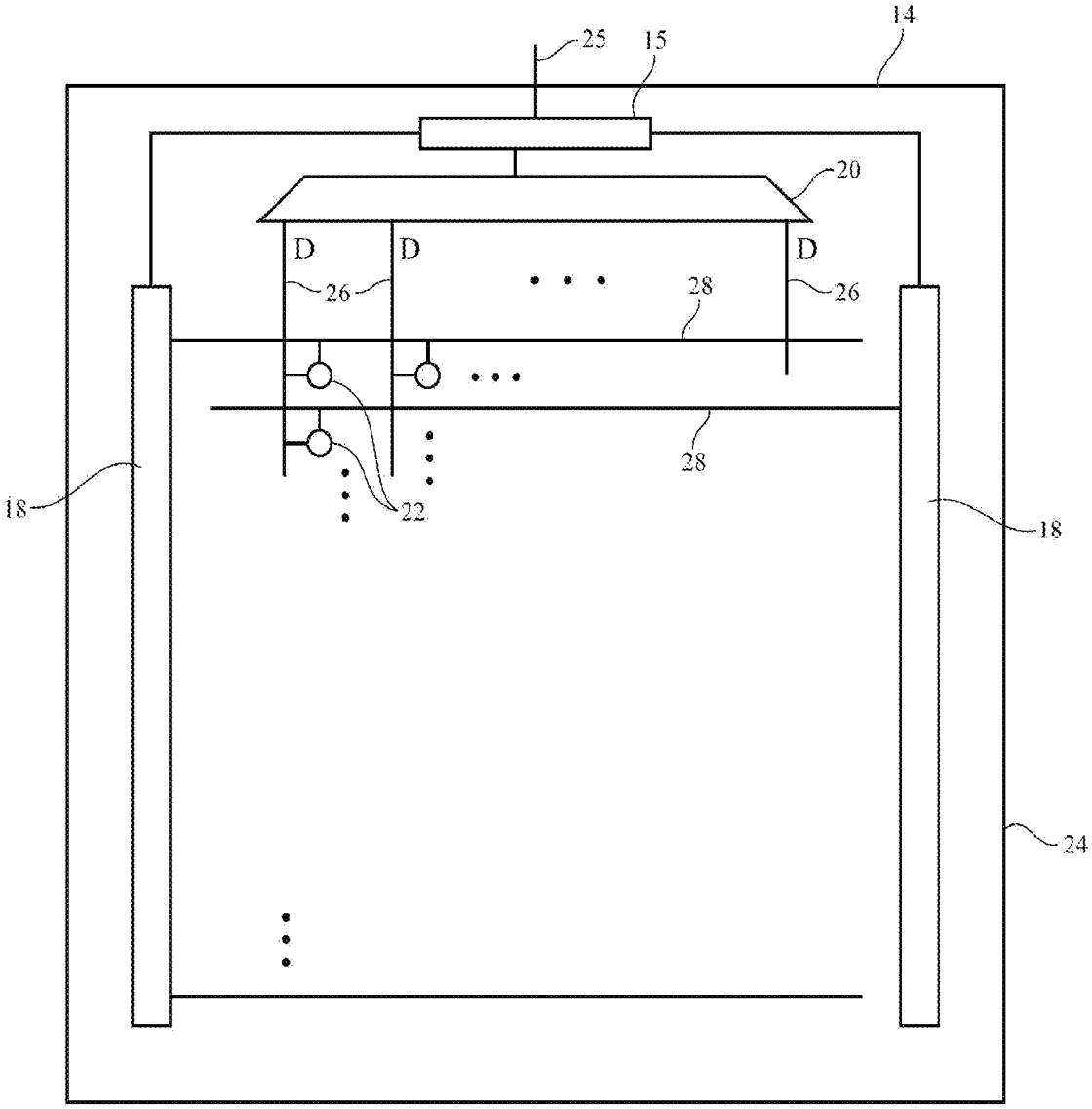
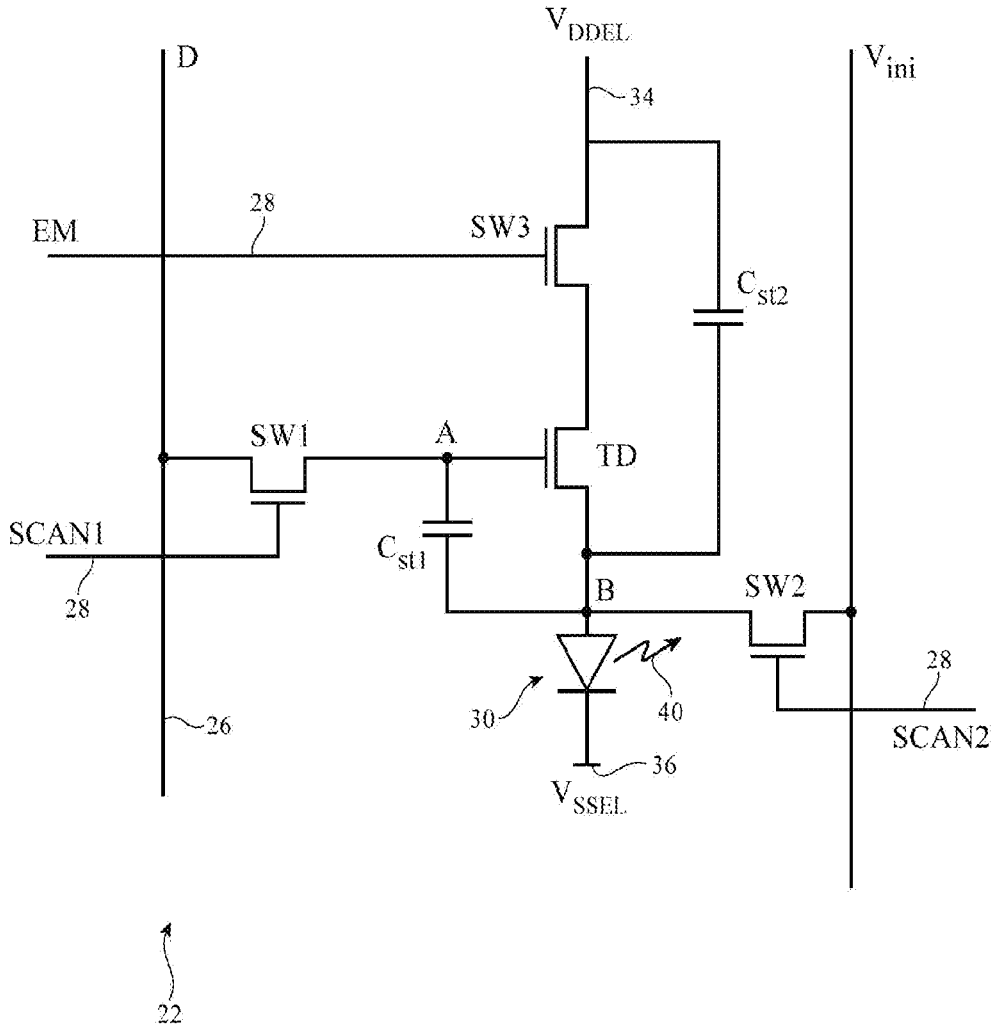


FIG. 2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SW1
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B
SW2
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28
30
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SCAN2
26
36
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22

FIG. 3

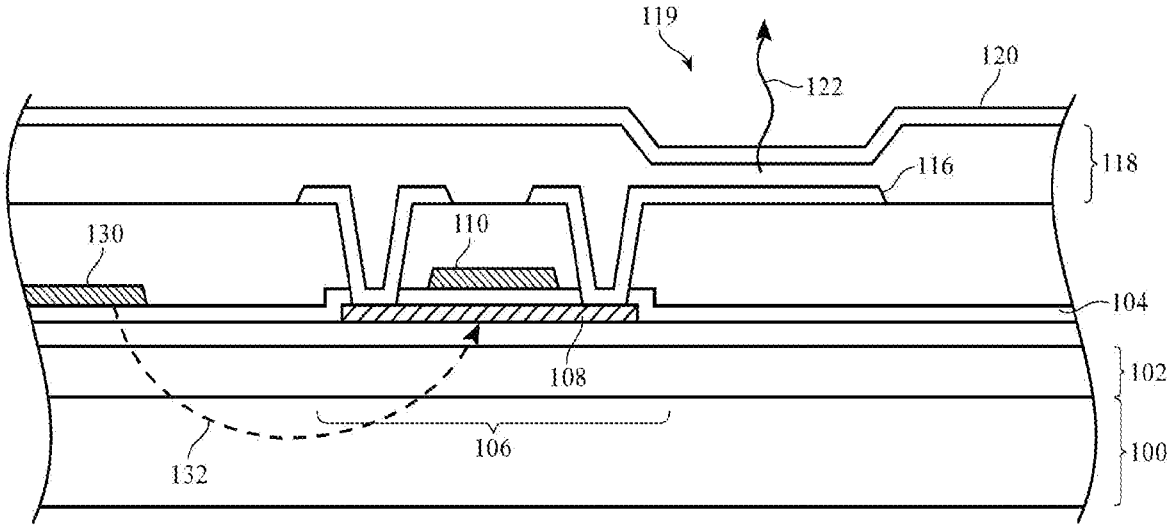

FIG. 4
(PRIOR ART)

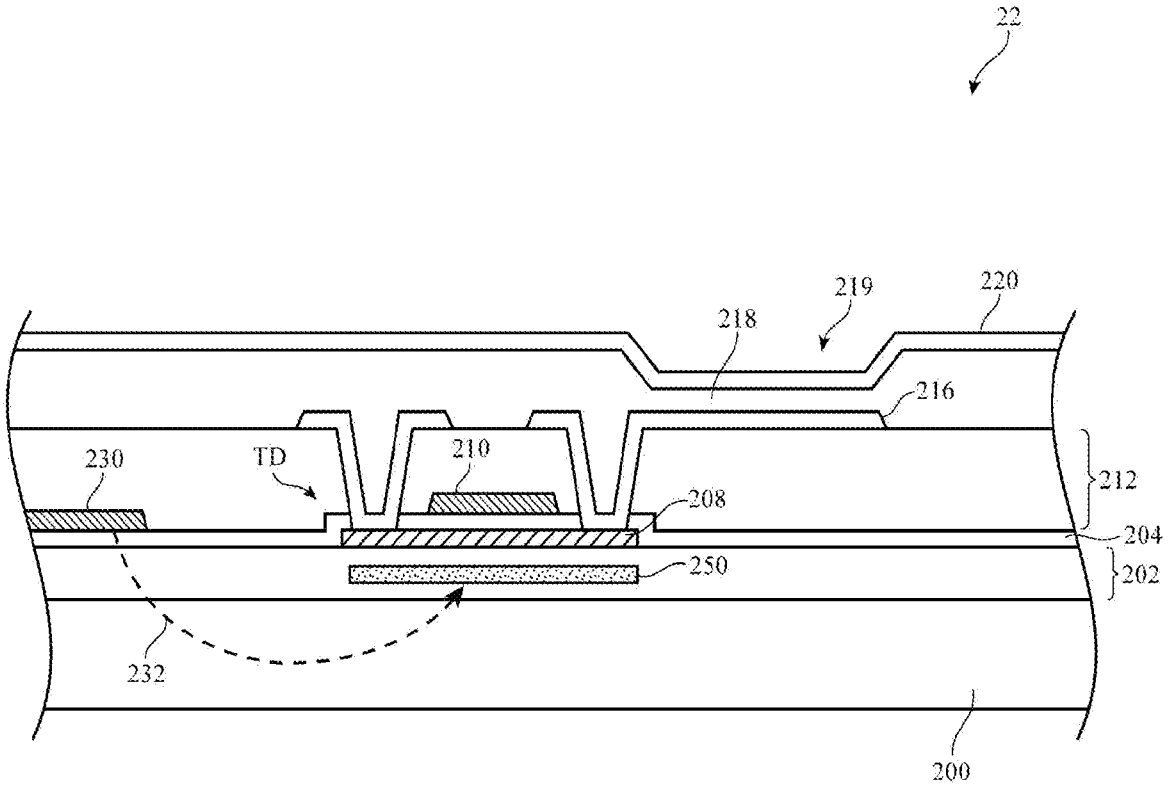

FIG. 5

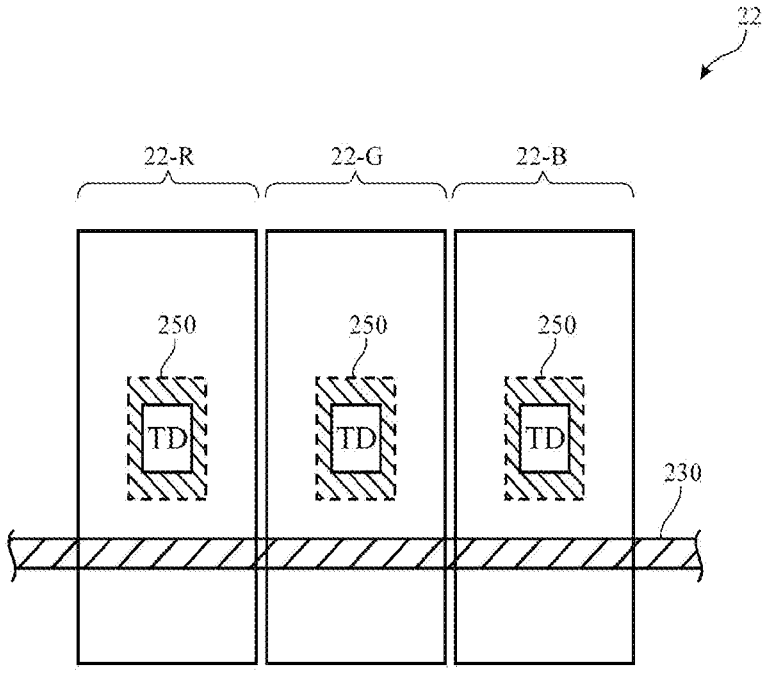
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FIG. 6

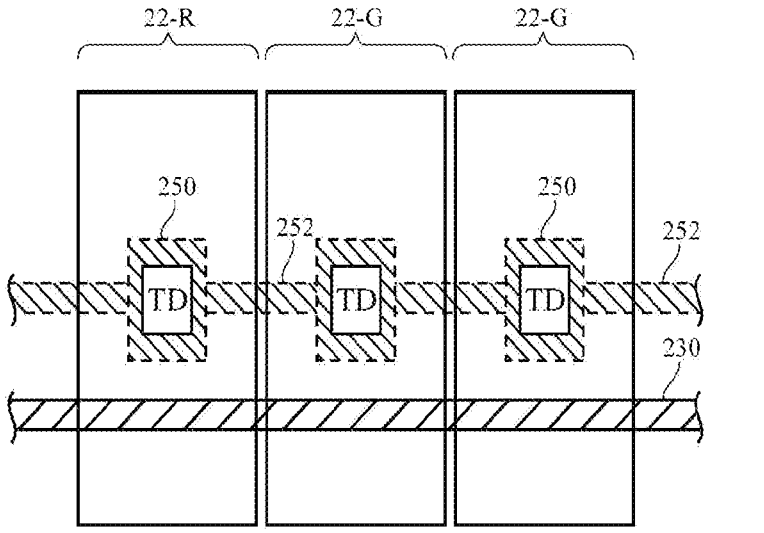
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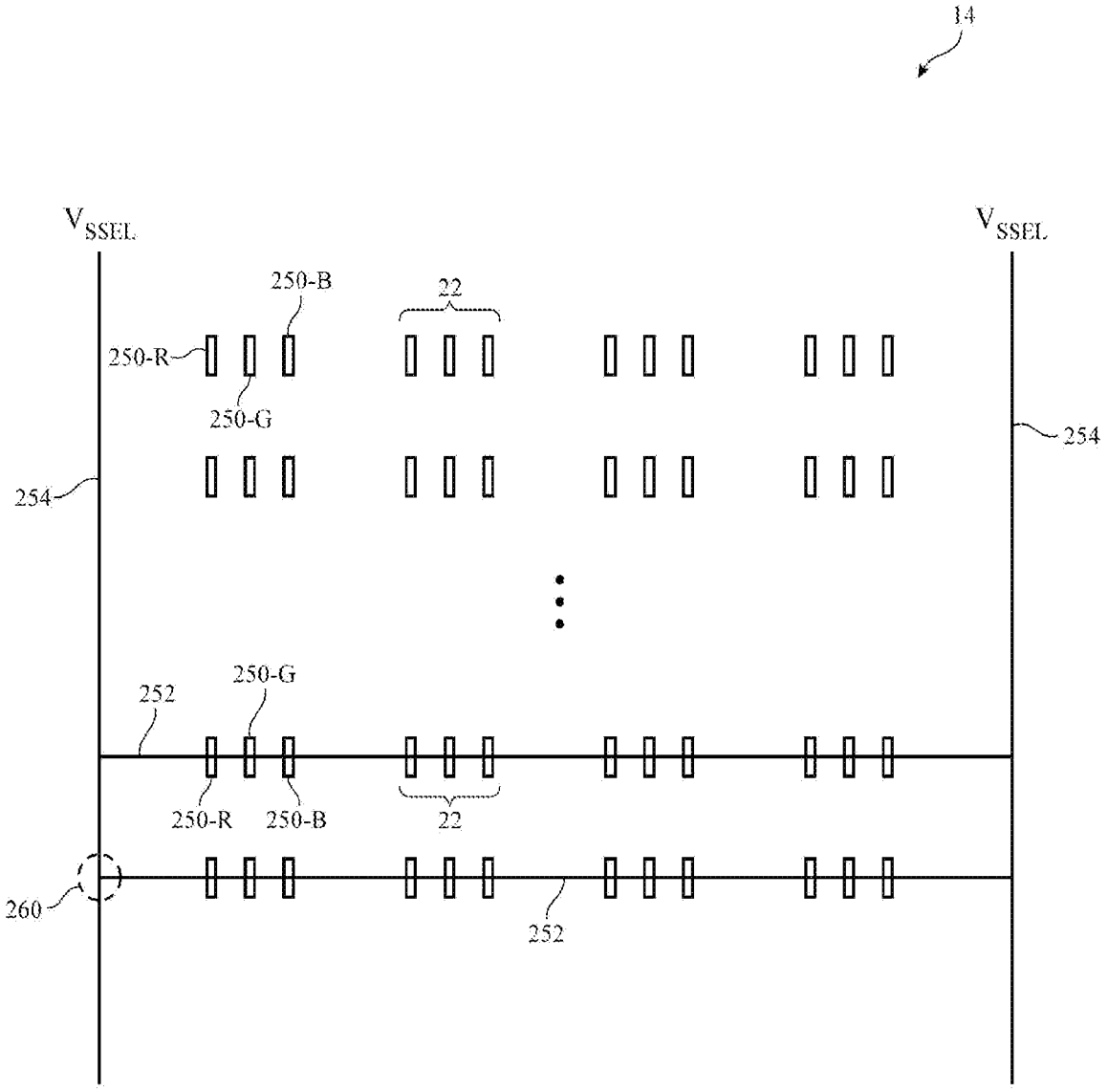
FIG. 7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V_{SSEL}
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250-B
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252

FIG. 8

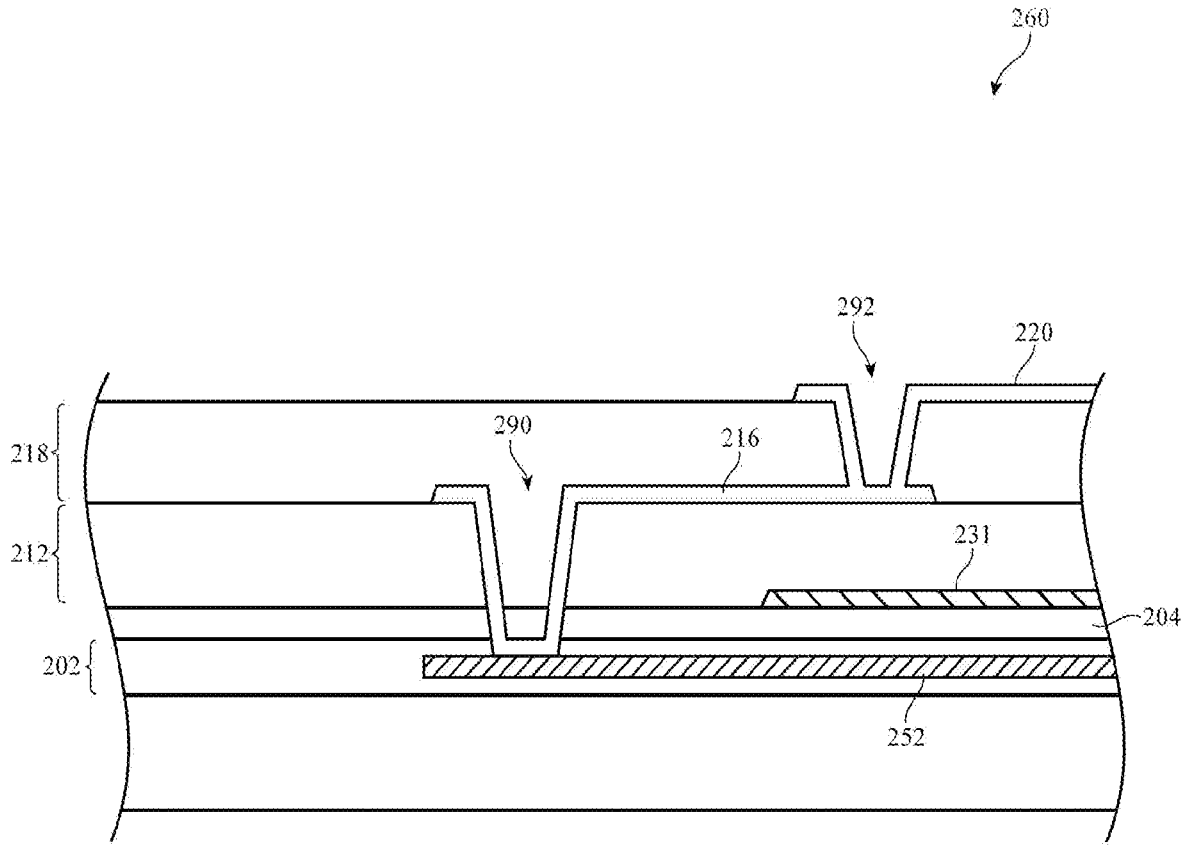

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/057061

A. CLASSIFICATION OF SUBJECT MATTER

H01L 51/52(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 51/52; H01L 31/18; G02F 1/1343; H01L 33/08; H01L 31/105; G02F 1/1333; G06F 3/041; H05B 33/10; G02F 1/1362

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: display, thin film transistor, buffer layer, conductive shielding, substrate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009-0101915 A1 (CHIEN-SEN WENG et al.) 23 April 2009 See paragraphs [0025], [0028], [0031], [0033], [0037]; figures 8, 10, 12; and claims 1, 6, 13.	1-4,7-11,13,14,16-18
A		5,6,12,15,19,20
A	US 2012-0126235 A1 (CHING-CHIEH SHIH et al.) 24 May 2012 See paragraphs [0033]-[0051].	1-20
A	KR 10-2014-0004887 A (LG DISPLAY CO., LTD.) 14 January 2014 See paragraphs [0067]-[0081]; and figures 6, 7.	1-20
A	KR 10-2013-0130552 A (SAMSUNG DISPLAY CO., LTD.) 02 December 2013 See paragraphs [0054]-[0067]; and figure 3.	1-20
A	WO 2013-134072 A1 (APPLE INC.) 12 September 2013 See paragraphs [0061]-[0062]; figure 13; and claim 1.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 December 2014 (31.12.2014)	**31 December 2014 (31.12.2014)**

Name and mailing address of the ISA/KR
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2014/057061

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009-0101915 A1	23/04/2009	TW 200919757 A	01/05/2009
		TW I324832 B	11/05/2010
		US 2011-0165727 A1	07/07/2011
		US 7952159 B2	31/05/2011
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		CN 101339923 B	27/06/2012
		JP 2009-099977 A	07/05/2009
		TW 200919735 A	01/05/2009
		TW I383504 B	21/01/2013
		US 2009-101913 A1	23/04/2009
		US 8133773 B2	13/03/2012
KR 10-2014-0004887 A	14/01/2014	None	
KR 10-2013-0130552 A	02/12/2013	US 2013-0313528 A1	28/11/2013
		US 8847213 B2	30/09/2014
WO 2013-134072 A1	12/09/2013	CN 104145213 A	12/11/2014
		KR 10-2014-0112092 A	22/09/2014
		US 2013-0235020 A1	12/09/2013

专利名称(译)	有机发光二极管显示屏，带底部屏蔽		
公开(公告)号	EP3097594A4	公开(公告)日	2017-06-07
申请号	EP2014879712	申请日	2014-09-23
[标]申请(专利权)人(译)	苹果公司		
申请(专利权)人(译)	苹果公司.		
当前申请(专利权)人(译)	苹果公司.		
[标]发明人	CHOI JAE WON GUILLOU JEAN PIERRE CHANG SHIH CHANG TSAI TSUNG TING GUPTA VASUDHA PARK YOUNG BAE		
发明人	CHOI, JAE WON GUILLOU, JEAN-PIERRE CHANG, SHIH CHANG TSAI, TSUNG-TING GUPTA, VASUDHA PARK, YOUNG BAE		
IPC分类号	H01L51/52		
CPC分类号	H01L27/3262 H01L27/3272 H01L29/78603 H01L29/78606 H01L29/78666 H01L29/78675 H01L29/7869 H01L2924/0002 H01L2924/00 H01L27/3248 H01L27/3276		
优先权	61/929907 2014-01-21 US 14/488725 2014-09-17 US		
其他公开文献	EP3097594A1		
外部链接	Espacenet		

摘要(译)

显示器可以具有有机发光二极管显示像素阵列。每个显示像素可以具有在驱动晶体管的控制下发光的发光二极管。每个显示像素还可以具有用于补偿和编程操作的控制晶体管。显示像素阵列可以具有行和列。行线可用于将行控制信号应用于显示像素的行。列线（数据线）可用于将显示数据和其他信号施加到各列显示像素。底部导电屏蔽结构可以形成在每个驱动晶体管下方。底部导电屏蔽结构可以用于屏蔽驱动晶体管免受从相邻行和列线产生的任何电场的影响。底部导电屏蔽结构可以是电浮动的或耦合到电源线。