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(54) **ORGANIC LIGHT EMITTING DISPLAY AND CIRCUIT THEREOF**

ORGANISCHE LICHTEMITTIERENDE ANZEIGE UND SCHALTUNG DAFÜR

AFFICHAGE ÉLECTROLUMINESCENT ORGANIQUE ET CIRCUIT CORRESPONDANT

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Description

BACKGROUND

Field

[0001] The present disclosure relates to an active-matrix organic light emitting display and a circuit thereof.

Discussion of the Related Art

[0002] An active-matrix organic light emitting display comprises self-luminous organic light emitting diodes OLED, and has the advantages of fast response time, high luminous efficiency, high luminance, and wide viewing angle. An organic light emitting diode, which is a self-luminous device, has the structure shown in FIG. 1. The organic light emitting diode comprises an anode and a cathode, and organic compound layers formed between the anode and the cathode. The organic compound layers comprise a hole transport layer HTL, an emission layer EML, and an electron transport layer ETL. When an operating voltage is applied to the anode and the cathode, a hole (indicated by "+" in FIG. 1) passing through the hole transport layer HTL and an electron (indicated by "-" in FIG. 1) passing through the electron transport layer ETL move to the emission layer EML, and form an exciton. As a result, the emission layer EML generates visible light.

[0003] In an organic light emitting display, pixels each comprising an organic light emitting diode are arranged in a matrix, and the luminance of the pixels is adjusted based on the grayscale of video data. Each individual pixel comprises a driving transistor that controls the driving current flowing through the organic light emitting diode based on a gate-source voltage, a capacitor that keeps the gate-source voltage of the driving transistor constant for one frame, and at least one switching transistor that programs the gate-source voltage of the driving transistor in response to a gate signal. A driving current is determined by the driving transistor's gate-source voltage corresponding to a data voltage, and the luminance of the pixel is proportional to the amount of driving current flowing through the organic light emitting diode.

[0004] Such an organic light emitting display has variations in driving current even with the same data voltage because the threshold voltage of the driving transistor varies between the pixels due to process deviation, variation of gatebias stress with time, etc. To solve this problem, the organic light emitting display uses a pixel structure that allows for sampling a change in the threshold voltage of the driving transistor and eliminating the effects of the change in threshold voltage on the driving current.

[0005] US 2003/0132931 A1 is entitled *"Semiconductor device and driving method thereof".* A circuit shown in Figure 39A and described in paragraphs 0682...0688 of the prior art document comprises seven transistors (3911, 3907, 3909, 3912, 3908, 3910, 3913) and supports several pixel driving phases. A first phase (Figure 39B) is designed to input an image signal (paragraph 0684). A second phase (Figures 39C/D) serves to acquire the threshold voltage of the driving transistor 3911 (paragraph 0685). A third phase (Figure 39E) serves to drive the EL device 3916 (paragraph 0686). During an "*initialization stage*" (paragraph 0399, Figure 2A), light is emitted at maximum brightness.

[0006] US 2015/0317931 A1 (assumed to correspond to its pre-published counterpart CN 104 123 910 A) discloses a *"Pixel compensation circuit"* that can automatically compensate a threshold voltage of a pixel transistor. Each of the two circuits disclosed (Figures 1 and 3) operates in a pre-charge period (I), a threshold voltage compensation period (II), and an emission period (III) (Figures 2 and 4 of the prior art document).

[0007] US 2012/0287025 A1 is entitled *"Active matrix display device and driving method thereof"* and operates a pixel circuit such as to render a potential difference between two nodes independent of the threshold voltage of a transistor so that an intended current can flow in a display element. A timing diagram (Figure 3) depicts one frame as including four periods (paragraph 0068 of the prior art document).

SUMMARY

[0008] In an exemplary embodiment of this disclosure, an organic light emitting display comprises a display panel having a plurality of pixels, a gate drive circuit that drives n scan lines (n being a natural number) and n emission lines on the display panel, and a data drive circuit that drives data lines on the display panel. Each of the pixels arranged in a jth row ($1<j\leq n$) includes a driving transistor having a gate electrode connected to a node A, a source electrode connected to a node B, and a drain electrode connected to a node C, and the driving transistor controlling a driving current applied to an organic light emitting diode, a first transistor that is connected between the data lines and the node B, a second transistor that is connected between the node A and a high-level driving voltage input terminal, a third transistor that is connected to the node B and the organic light emitting diode, a fourth transistor that is connected to the node C and the high-level driving voltage input terminal, a fifth transistor that is connected to the node A and the node C, a sixth transistor that is connected between a node D and an initial voltage input terminal, the node D located between the third transistor and the organic light emitting diode, and a capacitor that is connected to the node A and the node D. The gate of the

second transistor is connected to a scan line of a (j-1)th row of pixels. The gates of the third and fourth transistors are connected to the emission line of the jth row of pixels. The gates of the first and fifth transistors are connected to the scan line of the jth row of pixels. The gate of the sixth transistor is connected either to the scan line of the jth row of pixels or to the scan line of the (j-1)th row of pixels. A cathode of the organic light emitting diode is connected to a low-level driving voltage input terminal.

[0009] In one or more embodiments, a (j-1)th scan signal in which a data voltage is provided to the pixels arranged in a (j-1)th row has a turn-on voltage during a (j-1)th horizontal period, a jth scan signal has the turn-on voltage in which the data voltage is provided to the pixels arranged in a jth row during a jth horizontal period, and an emission signal provided to the jth row has the turn-on voltage after the jth scan signal is inverted to a turn-off voltage.

[0010] In one or more embodiments, during the (j-1)th horizontal period, the second transistor applies the high-level driving voltage received from the high-level driving voltage input terminal to the node A, in response to the (j-1)th scan signal.

[0011] In one or more embodiments, during the jth horizontal period, the first transistor applies the data voltage received from the data line to the node B, in response to the jth scan signal, and the fifth transistor connects the node A and the node C to operate the driving transistor, in response to the jth scan signal.

[0012] In one or more embodiments, during a (j+1)th horizontal period, the fourth transistor connects the high-level driving voltage input terminal and the node C, in response to the emission signal, and the third transistor connects the node B and the node D, in response to the emission signal, and the node D corresponds to an operating voltage of the organic light emitting diode from the initial voltage level by the driving current, and a difference between the initial voltage level and the operating voltage of the organic light emitting diode is applied to the node A so as to emit light of the organic light emitting diode while compensating the threshold voltage of the driving transistor.

[0013] In one or more embodiments, a gate electrode of the sixth transistor is connected to a (j-1)th scan line, and during a (j-1)th horizontal period, the sixth transistor applies the initial voltage received from the initial voltage input terminal to the node D, in response to a (j-1)th scan signal.

[0014] In one or more embodiments, a gate electrode of the sixth transistor is connected to a jth scan line, and during a jth horizontal period, the sixth transistor applies the initial voltage received from the initial voltage input terminal to the node D, in response to a jth scan signal.

[0015] In one or more embodiments, each of the pixels arranged in the jth row further comprises a seventh transistor that is connected between the node D and the initial voltage input terminal and that is switched on in response to a (j-1)th scan signal.

[0016] In one or more embodiments, during a (j-1)th horizontal period, the seventh transistor provides the initial voltage to the node D, in response to the (j-1)th scan signal.

[0017] In one or more embodiments, the initial voltage is lower than the driving voltage of the organic light emitting diode.

[0018] In one or more embodiments, a jth horizontal period includes a high-voltage holding period, and a high-level driving voltage is applied to the node A in response to the (j-1)th scan signal during the high-voltage holding period.

[0019] In one or more embodiments, at least one among the second transistor and the fifth transistor has a double-gate structure.

[0020] In one or more embodiments, the organic light emitting display further comprises a metal layer under a semiconductor layer of the driving transistor.

[0021] In one or more embodiments, a first electrode of the capacitor that receives an initial voltage from the initial voltage input terminal corresponds to the gate electrode of the driving transistor.

[0022] In one or more embodiments, the first electrode of the capacitor that receives an initial voltage from the initial voltage input terminal is disposed in an area corresponding to a semiconductor layer of the fifth transistor that operates during a sampling period.

[0023] In one or more embodiments, the capacitor having a first electrode and a second electrode is connected between an initial voltage input terminal and the at least one transistor, wherein the area of the first electrode that receives the initial voltage is larger than the area of the second electrode.

[0024] In one or more embodiments, the first electrode of the capacitor is not connected to a high level driving voltage input terminal, and is connected to the initial voltage input terminal, thereby reducing the number of contact holes.

[0025] In one or more embodiments, the organic light emitting diode having an anode connected to the first electrode of the capacitor and a cathode opposite to the anode, wherein the driving transistor is compensated by the capacitor that receives the initial voltage.

[0026] In one or more embodiments, a single frame includes an initial period in which a gate voltage of the driving transistor is initialized, a sampling period for compensating the threshold voltage of the driving transistor, and a light emission period in which the organic light emitting diode emits light. A value corresponding to an image signal to be displayed the organic light emitting diode is applied to the data line during the sampling period. And the initial voltage is applied to at least one electrode of the capacitor during the initial period.

[0027] In one or more embodiments, the sampling period comprises a period in which the initial period is held.

[0028] In one or more embodiments, the organic light emitting display comprises a high voltage holding period at an initial stage of the sampling period. And the high level driving voltage is applied to other electrodes of the capacitor in response to the gate voltage during the high voltage holding period.

[0029] In one or more embodiments, the initial period for the pixel of the jth row overlaps a period in which the data voltage is provided to the pixel of the (j-1)th row.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The accompanying drawings, which are included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this specification, illustrate embodiments of the disclosure and together with the description serve to explain the principles of the disclosure. In the drawings:

FIG. 1 is a view showing an organic light emitting diode and the principle of light emission by the organic light emitting diode;
FIG. 2 is a view showing an organic light emitting display according to an exemplary embodiment of the present disclosure;
FIG. 3 is a view showing a pixel structure according to a first exemplary embodiment;
FIG. 4 is a timing diagram showing gate signals according to the first exemplary embodiment;
FIG. 5A is an equivalent circuit diagram for explaining operation of pixels during an initial period according to the first exemplary embodiment;
FIG. 5B is an equivalent circuit diagram for explaining operation of pixels during a sampling period according to the first exemplary embodiment;
FIG. 5C is an equivalent circuit diagram for explaining operation of pixels during a light emission period according to the first exemplary embodiment;
FIG. 6 is a view showing a pixel structure according to a second exemplary embodiment;
FIG. 7A is an equivalent circuit diagram for explaining operation of pixels during an initial period according to the second exemplary embodiment;
FIG. 7B is an equivalent circuit diagram for explaining operation of pixels during a sampling period according to the second exemplary embodiment;
FIG. 7C is an equivalent circuit diagram for explaining operation of pixels during a light emission period according to the second exemplary embodiment;
FIG. 8 is a view showing an organic light emitting display according to a third exemplary embodiment;
FIG. 9A is an equivalent circuit diagram for explaining operation pixels during an initial period according to the third exemplary embodiment;
FIG. 9B is an equivalent circuit diagram for explaining operation pixels during a sampling period according to the third exemplary embodiment;
FIG. 9C is an equivalent circuit diagram for explaining operation pixels during a light emission period according to the third exemplary embodiment.
FIG. 10 is a timing diagram of gate signals according to the second exemplary embodiment;
FIG. 11 is a view showing a modification embodiment of the first exemplary embodiment;
FIG. 12 is a view showing an array of a region for forming a capacitor in a pixel according to an exemplary embodiment of the present disclosure; and
FIG. 13 is a cross-sectional view taken along line I-I' of FIG. 12 according to an exemplary embodiment of the present disclosure.

DETAILED DESCRIPTION

[0031] The various aspects and features of the present disclosure and methods of accomplishing the same may be understood more readily by reference to the following detailed descriptions of exemplary embodiments and the accompanying drawings. The present disclosure may, however, be embodied in many different forms and should not be construed as being limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concept of the present disclosure to those skilled in the art, and the present disclosure is defined by the appended claims.

[0032] The shapes, sizes, proportions, angles, numbers, etc. shown in the figures to describe the exemplary embodiments of the present disclosure are merely examples and not limited to those shown in the figures. Like reference numerals denote like elements throughout the specification. In describing the present disclosure, detailed descriptions of related well-known technologies will be omitted to avoid unnecessary obscuring the present disclosure. When the terms 'comprise', 'have', 'include' and the like are used, other parts may be added as long as the term 'only' is not used.

The singular forms may be interpreted as the plural forms unless explicitly stated.

[0033] The elements may be interpreted to include an error margin even if not explicitly stated.

[0034] When the position relation between two parts is described using the terms 'on', 'over', 'under', 'next to' and the like, one or more parts may be positioned between the two parts as long as the term 'immediately' or 'directly' is not used.

[0035] When the temporal relationship between two events is described using the terms 'after', 'following', 'next', 'before' and the like, the two events may not occur in succession as long as the term 'immediately' or 'directly' is not used.

[0036] It will be understood that, although the terms first, second, etc., may be used to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, a first element discussed below could be termed a second element without departing from the technical disclosure.

[0037] The features of various exemplary embodiments of the present disclosure may be combined with one another either partly or wholly, and may technically interact or work together in various ways. The exemplary embodiments may be carried out independently or in combination with one another.

[0038] An organic light emitting display for threshold voltage compensation requires a sampling period for sampling the threshold voltage of a driving transistor before pixels are charged with a data voltage. As display panels have higher resolution, the length of 1 horizontal period (H) is shortened and thus the sampling period also is shortened. The shortened sampling period leads to lower threshold voltage compensating capability, thus resulting in an adverse effect on the display quality of the display panels.

[0039] Moreover, if an organic light emitting display uses a reference voltage to sample the threshold voltage of a driving transistor, a data driver needs to swing between the reference voltage and the data voltage. Here, the data voltage is a data value for an image to be displayed. Accordingly, the data driver's output voltage undergoes many transitions because the data driver outputs the reference voltage and the data voltage alternately, resulting in higher power consumption.

[0040] In addition, if a substrate where transistors are disposed is formed of a polyimide material, mobile charges can be easily trapped. The trapped mobile charges may affect a semiconductor layer of the transistors and reduce driving current, thus deteriorating the performance of the transistors.

[0041] One aspect of this disclosure is to provide an organic light emitting display that can reduce power consumption by allowing for efficient compensation of the threshold voltage of a driving transistor.

[0042] Another aspect of this disclosure is to provide a compensation circuit for minimizing the effect of a mobile charge trapped in a substrate on a semiconductor layer of transistor.

[0043] The aspects of the present disclosure are not limited to the above-mentioned aspects, and other aspects will be clearly apparent to those skilled in the art from the following description.

[0044] Hereinafter, exemplary embodiments of the present disclosure will be described in detail with reference to the accompanying drawings.

[0045] FIG. 2 is a view showing an organic light emitting display according to an exemplary embodiment of the present disclosure.

[0046] Referring to FIG. 2, an organic light emitting display according to an exemplary embodiment of the present disclosure comprises a display panel 10 with pixels PXL arranged in a matrix, a data driver 12 for driving data lines DL, a gate driver 13 for driving scan lines SL and emission lines EL, and a timing controller 11 for controlling the operation timings of the data driver 12 and gate driver 13.

[0047] A plurality of pixels PXL are disposed on the display panel 10, and the pixels PXL are connected to the data lines DL, scan lines SL, and emission lines EL. The data lines DL are arranged in a column direction, and transmit a data voltage Vdata received from the data driver 12 to the pixels PXL. The first to nth scan lines SL are arranged in pixel rows R#1 to R#(n) (n is a natural number) in the row direction, respectively, and transmit a scan voltage received from the gate driver 13 to the pixels PXL. The first to nth emission lines EL are arranged in the pixel rows R#1 to R#(n) in row direction, respectively, and transmit an emission voltage received from the gate driver 13 to the pixels PXL.

[0048] The pixels PXL may commonly receive a high-level driving voltage ELVDD, low-level driving voltage ELVSS and an initial voltage Vini from a power generator. The initial voltage Vini may be chosen from a range of voltages lower than the low-level driving voltage ELVSS to prevent unnecessary light emission by the organic light emitting diodes OLED.

[0049] The transistors comprising each pixel PXL may be implemented as oxide transistors having an oxide semiconductor layer. The oxide transistors are advantageous for the display panel 10 to have a large area, when electron mobility, process deviation, etc. are all taken into consideration. The oxide semiconductor layer may be formed of, but is not limited to, ITO (indium tin oxide), IZO (indium zinc oxide), IGZO (indium gallium zinc oxide), or ITZO (indium tin zinc oxide). The present disclosure is not limited to the oxide transistors, but the semiconductor layer of the transistors may be formed of amorphous silicon (a-Si), polycrystalline silicon (poly-Si), organic semiconductor, etc.

[0050] Each individual pixel PXL comprises a plurality of transistors and capacitors to compensate for changes in the threshold voltage of the driving transistor. A pixel structure according to the exemplary embodiment of the present disclosure will be described later.

[0051] The timing controller 11 re-aligns digital video data RGB input from an external source to match the resolution of the display panel 10 and supplies it to the data driver 12. Also, the timing controller 11 generates a data control signal DDC for controlling the operation timing of the data driver 12 and a gate control signal GDC for controlling the operation timing of the gate driver 13, based on timing signals such as a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a dot clock signal DCLK, and a data enable signal DE.

[0052] The data driver 12 converts the digital video data RGB input from the timing controller 11 to an analog data voltage based on the data control signal DDC. The data driver 12 supplies the data voltage to the data lines DL. The data voltage may have a value corresponding to an image signal to be displayed by an organic light emitting diode OLED.

[0053] The gate driver 13 generates a scan signal and an emission signal based on the gate control signal GDC. The gate driver 13 sequentially provides a scan signal SCAN to the scan lines SL and sequentially provides an emission signal EM(j) to the emission lines EL. That is, the gate driver 13 sequentially provides the scan signal SCAN to the first to nth scan lines SL and the emission signal EM(j) to the first to nth emission lines EL. The gate driver 13 may be formed directly in a non-display area of the display panel 10 according to the GIP (gate-driver-in-panel) technology.

[0054] FIG. 3 is a view showing a pixel structure according to a first exemplary embodiment. FIG. 4 is a view showing gate signals provided to the pixel shown in FIG. 3.

[0055] Referring to FIG. 3, pixels PXL(j) arranged in a jth row will be described below.

[0056] The pixels PXL(j) arranged in the jth row R#j (j is a natural number less than n) are connected to a (j-1)th scan line SL(j-1), a jth scan line SL(j), and a jth emission line EL(j).

[0057] Each of the pixels PXL(j) comprises an organic light emitting diode OLED, a driving transistor DT, first transistor to sixth transistor T1 to T6, and a capacitor Cst. The exemplary embodiment discloses N-type transistors, the semiconductor type of the transistors is not limited thereto. If the first transistor to the sixth transistor T1 to T6 are implemented as P-type, the gate signals SCAN(j), SCAN(j-1), and EM(j) shown in FIG. 4 should be inverted. Compared to P-type transistors, N-type transistors allow for faster current flow, thus offering a higher switching speed. Also, the first transistor to the sixth transistors T1 to T6 may be PMOS transistors, CMOS transistors, etc.

[0058] The organic light emitting diode OLED emits light by a driving current supplied from the driving transistor DT. The organic light emitting diode OLED comprises multiple layers of organic layers between an anode and a cathode. The organic layers may comprise at least one among a hole transfer layer, an electron transfer layer, and an emission layer EML. The hole transfer layer includes a layer that injects or transfers holes into the emission layer, for example, it may be a hole injection layer HIL, a hole transport layer HTL, an electron blocking layer EBL, etc. The electron transfer layer includes a layer that injects or transfers electrons into the emission layer, for example, it may be an electron transport layer ETL, an electron injection layer EIL, a hole blocking layer HBL, etc.

[0059] The anode of the organic light emitting diode OLED is connected to a node D, and the cathode of the organic light emitting diode OLED is connected to an input terminal of the low-level driving voltage ELVSS.

[0060] The driving transistor DT controls the driving current applied to the organic light emitting diode OLED based on its gate-source voltage Vgs. A gate electrode of the driving transistor DT is connected to a node A, its source electrode is connected to a node B, and its drain electrode is connected to a node C.

[0061] First and second electrodes of the first transistor T1 are connected to the node B and a data line DL, respectively, and its gate electrode is connected to the jth scan line SL(j). That is, the first transistor T1 is switched on in response to the jth scan signal SCAN(j) and transmits a data voltage from the data line DL to the node B.

[0062] First and second electrodes of the second transistor T2 are connected to the node A and an input terminal of the high-level driving voltage ELVDD, respectively, and its gate electrode is connected to the (j-1)th scan line SL(j-1). That is, the second transistor T2 transmits the high-level driving voltage ELVDD to the node A in response to the (j-1)th scan signal SCAN(j-1).

[0063] First and second electrodes of the third transistor T3 are connected to the node B and the organic light emitting diode OLED, respectively, and its gate electrode is connected to the jth emission line EL(j). That is, the third transistor T3 switches the current path between the driving transistor DT and the organic light emitting diode OLED, in response to the jth emission signal EM(j).

[0064] First and second electrodes of the fourth transistor T4 are connected to the node C and the input terminal of the high-level driving voltage ELVDD, respectively, and its gate electrode is connected to the jth emission line EL(j). That is, the fourth transistor T4 transmits the high-level driving voltage ELVDD to the node C in response to the jth emission signal EM(j).

[0065] First and second electrodes of the fifth transistor T5 are connected to the node A and the node C, respectively, and its gate electrode is connected to the jth scan line SL(j).

[0066] First and second electrodes of the sixth transistor T6 are connected to the node D and the initial voltage Vini, respectively, and its gate electrode is connected to the jth scan line SL(j).

[0067] The capacitor Cst is connected between the node A and the node D. The capacitor Cst may be used to sample the threshold voltage of the driving transistor according to the source follower configuration.

[0068] In the first exemplary embodiment, the operation of the pixels arranged in the jth row R#j will be described

below with reference to FIGS. 4 and FIGS. 5A through 5C and [Table 1]. FIGS. 5A to 5C are equivalent circuit diagrams for explaining operation of the pixels in response to driving signals. [Table 1] is a table showing the voltages for each node corresponding to t operation periods of the pixels.

[0069] The first to sixth transistors T1 to T6 according to the first exemplary embodiment are implemented as N-type transistors. Thus, the high-level driving voltage of each driving signal represents a turn-on voltage for the transistors, and the low-level driving voltage of each driving signal represents a turn-off voltage for the transistors.

[0070] The operation of each pixel comprises an initial period Tj, a sampling period Ts, and a light emission period Te shown in FIG. 4. The initial period Tj, sampling period Ts, and light emission period Te each process for 1 horizontal period 1H. A jth horizontal period jH may be defined as a period in which the jth scan signal SCAN(j) is provided to the pixel of the jth row R#j.

[0071] For each pixel, a single frame may comprise an initial period Tj in which the gate voltage of the driving transistor is initialized, a sampling period Ts for compensating the threshold voltage of the driving transistor, and a light emission period Te in which the organic light emitting diode OLED emits light. During the sampling period Ts, a value corresponding to an image signal to be displayed by the organic light emitting diode OLED may be applied to the data line DL. Also, an initial voltage may be applied to at least one electrode of the capacitor during the initial period Tj.. The sampling period Ts may comprise a period in which the initial period Tj is held.

[Table 1]

	Initial period	Sampling period	Light emission period
Node A	ELVDD	Vdata+Vth	Vdata+Vth+(Voled-Vini)
Node B	Voled	Vdata	Voled
Node D	Voled	Vini	Voled

[0072] In FIG. 5A, the transistors that operate during the initial period Tj are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. Referring to FIGS. 4 and 5A, the initial period Tj processes for a (j-1)th horizontal period (j-1)H allocated to drive a (j-1)th pixel row.

[0073] During the initial period Tj, the (j-1)th scan signal SCAN(j-1) is input at the high-voltage level, and the jth scan signal SCAN(j) and the emission signal EM(j) are input at the low-voltage level. The second transistor T2 turns on in response to the (j-1)th scan signal SCAN(j-1), and provides the high-level driving voltage ELVDD to the node A. That is, the node A is reset to the high-level driving voltage ELVDD during the initial period Tj. The jth emission signal EM(j) is inverted to a turn-off voltage level, and the third transistor T3 turns off. As a result, the current path between the driving transistor DT and the organic light emitting diode OLED is interrupted during the initial period Tj. In this case, the node B and the node D may have the driving voltage Voled of the organic light emitting diode OLED that was applied to it during the light emission period of the previous frame, but the organic light emitting diode OLED does not emit light since the operating voltage Voled of the organic light emitting diode is not actually held. Thus, the voltages of the node B and node D will be denoted by "Voled" in [Table 1], for convenience.

[0074] In FIG. 5B, the transistors that operate during the sampling period Ts are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. Referring to FIGS. 4 and 5B, the sampling period Ts processes for the jth horizontal period jH in which a data voltage is applied to the pixels arranged in the jth pixel row.

[0075] During the sampling period Ts, the (j-1)th scan signal SCAN(j-1) is inverted to the low-voltage level, and the jth scan signal SCAN(j) is inverted to the high-voltage level. The emission signal EM(j) is held at the low-voltage level. As the (j-1)th scan signal SCAN(j-1) is inverted to the low level, the second transistor T2 turns off, and the current path between the input terminal of the high-level driving voltage ELVDD and the node A may be blocked.

[0076] During the sampling period Ts, the fifth transistor T5 turns on in response to the jth scan signal SCAN(j), and the node A and the node C are connected. Accordingly, the node C has the high-level driving voltage ELVDD, which is the voltage at the node A, and as the voltage at the node C rises, the driving transistor DT turns on. With the driving transistor DT turning on, the voltage at the node B rises by a drain-source current Ids to a voltage for turning off the driving transistor DT. At the same time, the first transistor T1 turns on in response to the jth scan signal SCAN(j), and provides a data voltage Vdata to the node B. That is, the voltage at the node B increases until Vdata is reached. Also, as the fifth transistor T5 turns on during the sampling period Ts, the node A and the node C are connected. So, the driving transistor DT becomes diode-connected transistor (that is, the gate electrode and drain electrode of the driving transistor are shorted so that the driving transistor acts as a diode). Thus, the node A having the same voltage as the gate of the driving transistor DT corresponds to a voltage of the sum of the voltage Vdata at the node B and the threshold voltage Vth.

[0077] Next, during the sampling period Ts, the sixth transistor T6 turns on in response to the jth scan signal SCAN(j), and provides the initial voltage Vini to the node D. The initial voltage Vini is set to a voltage at which the organic light emitting diode OLED does not operate. That is, a low voltage is applied to the anode of the organic light emitting diode OLED during the sampling period Ts, thereby preventing the organic light emitting diode OLED from emitting light at times other than the light emission period Te.

[0078] In FIG. 5C, the transistors that operate during the light emission period Te are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. Referring to FIGS. 4 and 5C, the light emission period Te continues until the start of the initial period Tj of the next frame following the completion of the sampling period Ts.

[0079] During the light emission period Te, the (j-1)th scan signal SCAN(j-1) and jth scan signal SCAN(j) are input at the low-voltage level (turn-off voltage), and the emission signal EM(j) is inverted to the high-voltage level (turn-on voltage). The third transistor T3 turns on in response to the emission signal EM(j), and therefore, during the light emission period Te, provides a driving current Ioled to the organic light emitting diode OLED in phase with the data voltage at the node B.

[0080] In the light emission period Te, the node D, which is initialized to the initial voltage Vini during the sampling period Ts, is set to the same voltage Voled as the organic light emitting diode OLED. This creates a voltage difference of "Voled-Vini" at the node D, and this voltage difference is also applied to the node A. Accordingly, the node A, which is held at the voltage of "Vdata+Vth" during the sampling period Ts, corresponds to a voltage of "Vdata+Vth+(Voled-Vini)".

[0081] During the light emission period Te, the node B also corresponds to the voltage of "Voled". That is, during the light emission period Te, the gate voltage of the driving transistor DT becomes "Vdata+Vth+(Voled-Vini)" and its source voltage becomes "Voled". Therefore, "Vgs={Vdata+Vth+(Voled-Vini)}-Voled=Vdata+Vth-Vini".

[0082] Accordingly, the relationship for the driving current Ioled flowing through the OLED during the light emission period Te is expressed by the following Equation 1:

[Equation 1]

$$I_{oled} = (k/2)(Vgs-Vth)^2=(k/2)(Vdata-Vini)^2$$

wherein k indicates a proportional constant determined by the electron mobility, parasitic capacitance, and channel capacity of the driving transistor DT.

[0083] The organic light emitting diode OLED emits light by this driving current relationship, which enables a desired grayscale representation. In other words, the relationship for the driving current Ioled of the organic light emitting diode OLED is $k/2(Vgs-Vth)^2$, and the Vgs programmed in the sampling period Ts already includes the Vth component. Thus, the Vth component is ultimately eliminated from the relationship for the driving current Ioled. This minimizes the effect of a change in threshold voltage Vth on the driving current Ioled.

[0084] As can be seen from the value of a voltage that is input according to the operating sequence of the pixels, the organic light emitting display according to the first exemplary embodiment does not use a reference voltage during the sampling period Ts, and this reduces transitions of the voltage output from the data driver 12. Accordingly, the power consumption of the data driver 12 may be reduced.

[0085] Moreover, in the organic light emitting display according to the first exemplary embodiment, the sampling period (or initial period in the sampling period) for the pixel of the jth row overlaps the period in which the data voltage is provided to the pixel of (j-1)th row. Accordingly, the first exemplary embodiment ensures a sufficient sampling period for the driving transistor. This allows for efficient compensation of the threshold voltage of the driving transistor DT.

[0086] FIG. 6 is a view showing a pixel structure according to a second exemplary embodiment. Driving signals for the pixel structure according to the second exemplary embodiment are identical to those for the pixel structure of FIG. 4 according to the first exemplary embodiment. A detailed description of the components of the second exemplary embodiment substantially identical to those according to the foregoing exemplary embodiment will be omitted.

[0087] Referring to FIG. 6, the jth pixels PXL(j) arranged in the jth row will be described below.

[0088] Each of the jth pixels PXL(j) comprises an organic light emitting diode OLED, a driving transistor DT, first to sixth transistors T1 to T6, and a capacitor Cst. The exemplary embodiment discloses N-type transistors, the semiconductor type of the transistors is not limited thereto.

[0089] The organic light emitting diode OLED emits light by a current supplied from the driving transistor DT.

[0090] The driving transistor DT controls the driving current applied to the organic light emitting diode OLED based on its gate-source voltage Vgs. A gate electrode of the driving transistor DT is connected to a node A, its source electrode is connected to a node B, and its drain electrode is connected to a node C.

[0091] First and second electrodes of the first transistor T1 are connected to the node B and a data line DL, respectively, and its gate electrode is connected to the jth scan line SL(j). That is, the first transistor T1 is switched on in response to the jth scan signal SCAN(j) and transmits a data voltage from the data line DL to the node B.

[0092] First and second electrodes of the second transistor T2 are connected to the node A and an input terminal of the high-level driving voltage ELVDD, respectively, and its gate electrode is connected to the (j-1)th scan line SL(j-1). That is, the second transistor T2 transmits the high-level driving voltage ELVDD to the node A in response to the (j-1)th scan signal SCAN(j-1).

[0093] First and second electrodes of the third transistor T3 are connected to the node B and the anode of the organic light emitting diode OLED, respectively, and its gate electrode is connected to the jth emission line EL(j). That is, the third transistor T3 switches the current path between the driving transistor DT and the organic light emitting diode OLED, in response to the jth emission signal EM(j).

[0094] First and second electrodes of the fourth transistor T4 are connected to the node C and the input terminal of the high-level driving voltage ELVDD, respectively, and its gate electrode is connected to the jth emission line EL(j). That is, the fourth transistor T4 transmits the high-level driving voltage ELVDD to the node C in response to the jth emission signal EM(j).

[0095] First and second electrodes of the fifth transistor T5 are connected to the node A and the node C, respectively, and its gate electrode is connected to the jth scan line SL(j).

[0096] First and second electrodes of the sixth transistor T6 are connected to the node D and the initial voltage Vini, respectively, and its gate electrode is connected to the (j-1)th scan line SL(j-1).

[0097] The capacitor Cst is connected between the node A and the node D. The capacitor Cst is used to sample the threshold voltage of the driving transistor according to the source follower configuration.

[0098] In the second exemplary embodiment, the operation of the pixels arranged in the jth row R#j will be described below with reference to FIGS. 4 and FIGS. 7A through 7C and [Table 2]. FIGS. 7A to 7C are equivalent circuit diagrams for explaining operation of the pixels in response to driving signals. [Table 2] is a table showing the voltages for each node corresponding to operation periods of the pixels. Detailed description of redundancies between the operations of the first and second exemplary embodiments will be omitted.

[Table 2]

	Initial period	Sampling period	Light emission period
Node A	ELVDD	Vdata+Vth	Vdata+Vth+(Voled-Vini)
Node B	Voled	Vdata	Voled
Node D	Vini	Vini	Voled

[0099] In the second exemplary embodiment, gate signals for driving the pixels are identical to those of the first exemplary embodiment. The operation of the pixels according to the second exemplary embodiment comprises an initial period Tj, a sampling period Ts, and a light emission period Te.

[0100] Referring to FIG. 7A, the transistors that operate during the initial period Tj are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. During the initial period Tj, the (j-1)th scan signal SCAN(j-1) is input at the high-voltage level, and the jth scan signal SCAN(j) and the emission signal EM(j) are input at the low-voltage level. The second transistor T2 turns on in response to the (j-1)th scan signal SCAN(j-1), and provides the high-level driving voltage ELVDD to the node A. That is, the node A is initialized to the high-level driving voltage ELVDD during the initial period Tj.

[0101] The jth emission signal EM(j) is inverted to a turn-off voltage level, and the third transistor T3 turns off. As a result, the current path between the driving transistor DT and the organic light emitting diode OLED is blocked during the initial period Tj.

[0102] Next, during the initial period Tj, the sixth transistor T6 turns on in response to the (j-1)th scan signal SCAN(j-1), and provides an initial voltage Vini to the node D. That is, the initial voltage Vini, which is lower than the low-level driving voltage ELVSS, is applied, thereby preventing the organic light emitting diode OLED from emitting light at times other than the light emission period Te.

[0103] Referring to FIG. 7B, the transistors that operate during the sampling period Ts are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. The sampling period Ts processes for the jth horizontal period jH in which a data voltage is applied to the jth pixels PXL(j).

[0104] During the sampling period Ts, the (j-1)th scan signal SCAN(j-1) is inverted to the low-voltage level, and the jth scan signal SCAN(j) is inverted to the high-voltage level. The emission signal EM(j) is held at the low-voltage level. As the (j-1)th scan signal SCAN(j-1) is inverted to the low-voltage level, the second transistor T2 turns off, and the current path between the input terminal of the high-level driving voltage ELVDD and the node A is blocked.

[0105] During the sampling period Ts, the fifth transistor T5 turns on in response to the jth scan signal SCAN(j), and the node A and the node C are connected. Accordingly, the node C has the high-level driving voltage ELVDD, which is

the voltage at the node A, and as the voltage at the node C rises, the driving transistor DT turns on. With the driving transistor DT turning on, the voltage at the node B rises by a drain-source current Ids to a voltage for turning off the driving transistor DT. At the same time, the first transistor T1 turns on in response to the jth scan signal SCAN(j), and provides a data voltage Vdata to the node B. That is, the voltage at the node B increases until Vdata is reached. Also, as the driving transistor DT turns on during the sampling period Ts, the node A and the node C are connected. So, the fifth transistor T5 becomes a diode-connected transistor(that is, the gate electrode and drain electrode of the driving transistor are shorted so that the driving transistor acts as a diode). Thus, the node A having the same voltage as the gate of the driving transistor DT is set to a voltage equal to the sum of the voltage Vdata at the node B and the threshold voltage Vth.

[0106] Referring to FIG. 7C, the transistors that operate during the light emission period Te are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. The light emission period Te continues until the start of the initial period Tj of the next frame following the completion of the sampling period Ts.

[0107] During the light emission period Te, the (j-1)th scan signal SCAN(j-1) and jth scan signal SCAN(j) are input at the low-voltage level (turn-off voltage), and the emission signal EM(j) is inverted to the high-voltage level (turn-on voltage). The third transistor T3 turns on in response to the emission signal EM(j), and therefore, during the light emission period Te, provides a driving current Ioled to the organic light emitting diode OLED in phase with the data voltage at the node B.

[0108] In the light emission period Te, the node D, which is initialized to the initial voltage Vini during the initial period Tj, is set to the same voltage Voled as the organic light emitting diode OLED. This creates a voltage difference of "Voled-Vini" across the node D, and this voltage difference is also applied to the node A. Accordingly, the node A, which is held at the voltage of "Vdata+Vth" during the sampling period Ts, corresponds to a voltage of "Vdata+Vth+(Voled-Vini)".

[0109] During the light emission period Te, the node B also corresponds to the voltage of "Voled". That is, during the light emission period Te, the gate voltage of the driving transistor DT becomes "Vdata+Vth+(Voled-Vini)" and its source voltage becomes "Voled". Therefore, "Vgs={Vdata+Vth+(Voled-Vini)}-Voled=Vdata+Vth-Vini".

[0110] Accordingly, the relationship for the driving current Ioled flowing through the OLED during the light emission period Te is expressed by the above Equation 1.

[0111] That is, in the second exemplary embodiment, the Vth component is ultimately eliminated from the relationship for the driving current Ioled. This minimizes the effect of a change in threshold voltage Vth on the driving current Ioled.

[0112] FIG. 8 is a view showing an organic light emitting display according to a third exemplary embodiment. FIG. 8 shows a modification embodiment of the first exemplary embodiment shown in FIG. 3. In FIG. 8, the same components as FIG. 3 are denoted by the same reference numerals, and a detailed description of them will be omitted. Also, the gate signals of FIG. 4 according to the first exemplary embodiment may be used as driving signals for driving the organic light emitting display according to the third exemplary embodiment.

[0113] The organic light emitting display according to the third exemplary embodiment further comprises a seventh transistor T7. A first electrode of the seventh transistor T7 is connected to the node D, its second electrode is connected to an input terminal of the initial voltage Vini, and its gate electrode is connected to the (j-1)th scan line SL[j-1] and receives the (j-1)th scan signal SCAN[j-1].

[0114] In FIG. 9A, the transistors that operate during the initial period Tj are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. FIG. 9A is an equivalent circuit diagram for explaining operation of the pixels during the initial period Tj according to the third exemplary embodiment. Referring to FIGS. 4, 8, and 9A to 9C, the seventh transistor T7 according to the third exemplary embodiment initializes the node D to the initial voltage Vini in response to the (j-1)th scan signal SCAN(j-1). That is, the initial voltage Vini, which is lower than the low level driving voltage ELVSS, is applied, thereby preventing the organic light emitting diode OLED from emitting light at times other than the light emission period Te.

[0115] FIGS. 9B and 9C are views showing for explaining operation of the pixels during the sampling period Ts and the light emission period Te according to the third exemplary embodiment. The transistors that operate during the sampling period Ts and the light emission period Te are indicated by the solid lines, and the transistors that do not operate during these periods are indicated by the dotted lines. The transistors of the pixels operate the same as the above-described first exemplary embodiment during the sampling period Ts and the light emission period Te, so a detailed description thereof will be omitted.

[0116] In the organic light emitting display according to the third exemplary embodiment of the present disclosure, the node D is initialized during the (j-1)th horizontal period (j-1)H by using the seventh transistor T7, and the node D is initialized during the jth horizontal period jH by using the sixth transistor T6.

[0117] In the first exemplary embodiment of the present disclosure, the node D is initialized only during the jth horizontal period jH, which is the sampling period for the jth pixels P(j). In the first exemplary embodiment, the node D is in an electrically floating state during the (j-1)th horizontal period (j-1)H. Thus, the voltage at the node A rises instantly due to coupling of the capacitor Cst, in the initializing process of the node A to the high-level driving voltage ELVDD during the (j-1)th horizontal period (j-1)H. As a consequence, the organic light emitting diode OLED may emit light instantly. That is, in the first exemplary embodiment, pixels may emit light at an unwanted time during the initial period.

[0118] On the contrary, in the third exemplary embodiment shown in FIG. 8, the node D is initialized to the initial voltage Vini during the initial period Tj as well by using the seventh transistor T7. That is, the seventh transistor T7 holds the node D at the initial voltage Vini at which the organic light emitting diode OLED does not operate, thereby preventing a rise in the voltage at the node D. As a consequence, the third exemplary embodiment may prevent the organic light emitting diode OLED from emitting light at an unwanted time during the initial period Tj due to the rise in the voltage at the node D. Also, a low voltage may be applied to the anode of the organic light emitting diode OLED during the initial period Tj, thereby preventing the organic light emitting diode OLED from emitting light at times other than the light emission period Te due to coupling of the capacitor in the initializing process of the gate electrode of the driving transistor to the high-level driving voltage.

[0119] FIG. 10 is a timing diagram of gate signals according to the second exemplary embodiment, which is a modification of FIG. 4. The timing diagram of the gate signals of FIG. 10 according to the second exemplary embodiment may apply to the pixels of FIGS. 3 and 8 according to the first and third exemplary embodiments of the present disclosure.

[0120] In the first and third exemplary embodiments, the sixth transistor T6 initializes the node D to the initial voltage Vini, in response to a 2jth scan signal SCAN2(j) applied at a turn-on voltage, during the sampling period Ts. That is, the voltage at the node D works as the operating voltage Voled of the organic light emitting diode OLED until the start of the sampling period Ts, and is initialized to the initial voltage Vini during the sampling period Ts. Since the initial voltage Vini is set to a voltage lower than the operating voltage Voled of the organic light emitting diode OLED, the voltage at the node D decreases during the initial period Tj. The operation of the pixels during the sampling period Ts according to the first exemplary embodiment is as shown in FIG. 5B, and the operation of the pixels during the sampling period Ts according to the third exemplary embodiment is as shown in FIG. 9B. As shown in FIGS. 5B and 9B, in the first and third exemplary embodiments, the node A floats during the sampling period Ts. When the voltage at the node A is initialized to the initial voltage Vini while the node A is floating state, the voltage at the node A decreases due to coupling of the capacitor Cst. As a consequence, the voltage at the node A, which normally has to be sampled as a voltage value of "Vdata+Vth", decreases, thus leading to the problem of not sensing the threshold voltage Vth.

[0121] In comparison, according to the timing diagram of the gate signals of FIG. 10 according to the second exemplary embodiment of the present disclosure, the operation of the pixels comprises a high-voltage holding period Th at the initial stage of the sampling period Ts. During the high-voltage holding period Th, the second transistor T2 supplies the high-level driving voltage ELVDD to the node A in response to the 1(j)th scan signal SCAN1(j). Accordingly, the organic light emitting display according to the first and third exemplary embodiments may prevent a voltage drop at the node A due to coupling effect of the capacitor Cst since the node D is initialized. Also, by supplying the high-level driving voltage to the gate electrode of the driving transistor at the initial stage of the sampling period, the present disclosure prevents a voltage drop at the gate electrode of the driving transistor due to coupling of the capacitor Cst in the initializing process of the organic light emitting diode. Moreover, the high-level driving voltage may be applied to other electrodes of the capacitor in response to the gate voltage of the driving transistor during the high-voltage holding period, thereby preventing a voltage drop at the gate electrode of the driving transistor.

[0122] As for the gate signals according to the second exemplary embodiment, a first scan signal SCAN1(j) and second scan signal SCAN2(j) provided in the pixel of jth row R#j have different pulses widths, as shown in FIG. 10. Accordingly, the gate signals of FIG. 10 according to the second exemplary embodiment may be individually output by using individual shift registers. In order to use the gate signals according to the second exemplary embodiment, a first scan line to which the first scan signal SCAN1(j) is applied and a second scan line to which the second scan signal SCAN2(j) is applied may be arranged in each pixel of R#1 to R#(n) row.

[0123] FIG. 11 is a view showing a modification embodiment of the first exemplary embodiment shown in FIG. 3. In FIG. 11, the same components as the first exemplary embodiment are denoted by the same reference numerals, and a detailed description of them will be omitted.

[0124] The first and second electrodes of the fifth transistor T5 are connected to the node A and node C, respectively, and its gate electrode is connected to the jth scan line SL(j). The fifth transistor T5 has a double-gate structure, which can reduce leakage current. If a leakage current occurs while the fifth transistor T5 is in the off state, the voltage across the capacitor Cst is lowered. Once the voltage across the capacitor Cst is lowered, the gate-source voltage of the driving transistor DT changes. The gate-source voltage of the driving transistor DT determines the luminance of the organic light emitting diode OLED, and as a result, the leakage current of the fifth transistor T5 causes a change in luminescence intensity. Accordingly, the double-gate structure of the fifth transistor T5 connected to the capacitor Cst may reduce the leakage current of the fifth transistor T5 and prevent an unwanted change in luminescence intensity.

[0125] That is, if a leakage current occurs to a transistor connected to the capacitor Cst, this may cause distortion in luminescence intensity. This can be solved by applying a double-gate structure to the transistor connected to the capacitor Cst.

[0126] For instance, the second transistor T2 also may have a double-gate structure. Alternatively, at least one of the second and fifth transistors T2 and T5 may have a double-gate structure.

[0127] Accordingly, the gate structure of the second and fifth transistors T2 and T5 may be any one selected from

among those illustrated in the following [Table 3].

[Table 3]

Second transistor	Fifth transistor
Single gate	Single gate
Single gate	Double gate
Double gate	Single gate
Double gate	Double gate

[0128] Also, the second and fifth transistors T2 and T5 with the double-gate structure may be equally used in the pixel structure of FIG. 6 according to the second exemplary embodiment and the pixel structure of FIG. 8 according to the third exemplary embodiment.

[0129] The pixel structures of FIGS. 3, 6, and 8 according to the above-described exemplary embodiments comprise transistors and a capacitor which have their distinctive technical characteristics. These pixel structures may be seen in a pixel array for a display panel.

[0130] FIG. 12 is a view showing a planar array in a capacitor forming region in FIGS. 3, 6, and 8. In the description of FIG. 8, the seventh transistor T7 may be substituted for the sixth transistor T6.

[0131] Referring to FIG. 12 and FIG. 13, a cross-sectional view of the sixth transistor T6 and capacitor Cst of FIG. 12 taken along line I-I', the sixth transistor T6 comprises a semiconductor layer 210, a drain electrode connected to the semiconductor layer 210 through a contact hole 242, and a source electrode 231 connected to the semiconductor layer 210 through a contact hole 232, and the capacitor Cst comprises a first electrode 241 and a second electrode. The first electrode 241 of the capacitor Cst is connected to the drain electrode of the sixth transistor T6, and the second electrode is a gate electrode 250 of the driving transistor DT. The source electrode 231 of the sixth transistor T6 may be connected to an initial voltage input terminal. Also, a semiconductor layer 260 of the driving transistor DT is formed below the gate electrode 250, and a source contact hole 271 and a drain contact hole 273 may be connected to a source electrode and a drain electrode, each of a respective transistor.

[0132] The first electrode 241 of the capacitor Cst is not connected to a high-level driving voltage input terminal, but is connected to the initial voltage input terminal. Thus, the first electrode 241 of the capacitor can be designed with ease to share a single contact hole. For example, the first electrode of the capacitor of FIG. 8 shares a single contact hole with the sixth and seventh transistors, resulting in a reduction in the number of contact holes and ensuring sufficient design margin.

[0133] The transistors may be formed on a substrate 110, and the substrate 110 may be made of a polyimide insulating layer. In this case, a mobile charge is generated in the polyimide insulating layer. This may affect the semiconductor layers of the transistors and reduce the driving current. The transistors discussed herein may be a transistor array comprising at least one transistor. Accordingly, the first electrode 241 may be larger than the gate electrode 250 of the driving transistor DT. In this way, the initial voltage Vini is applied to the first electrode 241, thus suppressing the effect of a mobile charge in the substrate 110. This can improve the reduction in the driving current of the driving transistor DT caused by the mobile charge. The initial voltage Vini may be a negative voltage.

[0134] Alternatively, a metal layer 114 may be positioned under the semiconductor layer 260 of the driving transistor DT to decrease the effect of the mobile charge on the semiconductor layer 260 of the driving transistor DT. The metal layer 114 may be the same size as or larger than the semiconductor layer 260 of the driving transistor DT.

[0135] The first electrode 241 of the capacitor Cst may be extended to become a transistor that samples the threshold voltage of the driving transistor DT or a transistor that operates during the sampling period. Also, the first electrode 241 of the capacitor Cst may be disposed in an area corresponding to a semiconductor layer of the fifth transistor to decrease the effect of the mobile charge on the semiconductor layer of the fifth transistor. Referring to FIG. 13, a first buffer layer 120 is positioned on the substrate 110. The first buffer layer 120 may be formed of any one among silicon oxide (SiOx), silicon nitride (SiNx), and a multi-layer thereof.

[0136] The metal layer 114 is positioned on the first buffer layer 120, and the metal layer 114 may be made of a semiconductor, such as silicon (Si), or a conductive metal; for example, any one among molybdenum (Mo), aluminum (Al), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), copper (Cu), and an alloy of two or more thereof.

[0137] The substrate 110 may be a glass, plastic, or polyimide insulating layer, and may be composed of two or more layers. The substrate 110 may be a substrate with flexibility. Accordingly, a flexible organic light emitting display may be formed of a flexible material such as plastic. Also, when organic light emitting diodes that allow for easy fabrication of flexible displays are used in vehicle lighting or vehicle displays, the vehicle lighting or vehicle displays may have various designs and offer design freedom depending on their structure or appearance.

[0138] A second buffer layer 130 is positioned on the metal layer 114. The second buffer layer 130 may be formed of any one among silicon oxide (SiOx), silicon nitride (SiNx), and a multi-layer thereof.

[0139] The semiconductor layer 210 is positioned on the second buffer layer 130. The semiconductor layer 210 may comprise silicon semiconductor or oxide semiconductor. The semiconductor layer 210 of the sixth transistor T6 comprises a drain region 214, a source region 215, lightly-doped regions 212 and 213, and a channel region 211 positioned between the lightly-doped regions 212 and 213. The semiconductor layer 210 may be doped with an n-type impurity such as phosphorous (P), arsenic (As), or antimony (Sb). The semiconductor layer 260 of the driving transistor DT may be formed by the same process as the semiconductor layer 210 of the sixth transistor T6.

[0140] A first insulating layer 140 is positioned on the semiconductor layer 210. The first insulating layer 140 may be formed of any one among silicon oxide (SiOx), silicon nitride (SiNx), and a multi-layer thereof.

[0141] A gate electrode 220 of the sixth transistor T6 is positioned above the channel region 211 of the semiconductor layer 210. The gate electrode 220 may be formed of any one among molybdenum (Mo), aluminum (Al), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), copper (Cu), and an alloy of two or more thereof. The gate electrode 250 of the driving transistor DT may be formed by the same process as the gate electrode 220 of the sixth transistor T6.

[0142] A second insulating layer 150 is positioned on the gate electrodes 220 and 250. The second insulating layer 150 may be formed of any one among silicon oxide (SiOx), silicon nitride (SiNx), and a multi-layer thereof.

[0143] The first electrode 241 of the capacitor Cst and the drain electrode and source electrode of the sixth transistor T6, all of which are electrically connected to an initial voltage (Vini) supply line, are positioned on the second insulating layer 150. Although FIGS. 12 and 13 illustrate that part of the first electrode 241 of the capacitor Cst corresponds to the drain electrode of the sixth transistor T6, the first electrode 241 of the capacitor Cst may be used as a second gate electrode, as well as a drain electrode or a gate electrode. Like the gate electrode 220, the second gate electrode may be formed of any one among molybdenum (Mo), aluminum (Al), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), copper (Cu), and an alloy of two or more thereof. The area of the first electrode 241 that receives the initial voltage may be larger than the area of the second electrode of the capacitor Cst.

[0144] A third insulating layer 160 is positioned on the first electrode 241 of the capacitor Cst and the drain electrode of the sixth transistor T6. The third insulating layer 160 may be formed of any one among silicon oxide (SiOx), silicon nitride (SiNx), and a multi-layer thereof.

[0145] An organic light emitting diode comprises an anode connected to the first electrode 241 of the capacitor Cst and a cathode opposite to the anode. An organic light emitting display of this specification may be used in applications such as TV, mobile, tablet PCs, monitors, smartwatches, laptop computers, vehicle displays, etc. An organic light emitting display of this specification also may be used in displays of various shapes such as flat displays, bendable displays, foldable displays, and rollable displays.

[0146] The exemplary embodiments of this disclosure ensure a sufficiently long threshold voltage sampling period because the gate electrode of the driving transistor is initialized during the previous horizontal period. Accordingly, the threshold voltage of the driving transistor can be efficiently compensated.

[0147] Moreover, the exemplary embodiments of this disclosure can reduce transitions of the data voltage output from the data driver since they does not use a reference voltage. Accordingly, the power consumption of the data driver can be reduced.

[0148] In addition, by applying a low voltage to the anode of an organic light emitting diode connected to one electrode of the capacitor, the exemplary embodiments of this disclosure can prevent the organic light emitting diode from emitting light at other times than the light emission period due to coupling of the capacitor in the initializing process of the gate electrode of the driving transistor, connected to another electrode of the capacitor, to the high-level driving voltage.

[0149] Furthermore, the exemplary embodiments of this disclosure can prevent a voltage drop at the gate electrode of the driving transistor due to coupling of the storage capacitor in the initializing process of the organic light emitting diode, by initializing the organic light emitting diode during the sampling period and, if one electrode of the capacitor is connected to the anode of the organic light emitting diode and another electrode of the capacitor is connected to the gate electrode of the driving transistor, supplying the high-level driving voltage to the gate electrode of the driving transistor at the initial stage of the sampling period.

[0150] Furthermore, the exemplary embodiments of this disclosure can prevent distortion in luminescence caused by leakage current by having double-gate transistors connected to the capacitor.

[0151] Furthermore, the exemplary embodiments of this disclosure can reduce the effect of a mobile charge on the semiconductor layer of the driving transistor by placing a metal layer under the semiconductor layer of the driving transistor.

[0152] Furthermore, the exemplary embodiments of this disclosure can reduce the effect of a mobile charge on the semiconductor layer of the driving transistor because one electrode of the capacitor has a larger area than the gate electrode of the driving transistor.

[0153] Furthermore, the exemplary embodiments of this disclosure can reduce the effect of a mobile charge on the semiconductor layer of transistors by placing one electrode of the capacitor in an area corresponding to the semiconductor layer of the transistors that operate during the sampling period.

[0154] Furthermore, the exemplary embodiments of this disclosure can ensure design margin by reducing the number of contact holes within a pixel because one electrode of the capacitor is connected to the initial voltage input terminal, rather than the high-level driving voltage input terminal, thus allowing the one electrode of the capacitor to be connected to the initial voltage input terminal and the transistors via a single contact hole.

[0155] Throughout the description, it should be understood by those skilled in the art that various changes and modifications are possible without departing from the technical principles of the present disclosure. Therefore, the technical scope of the present disclosure is not limited to the detailed descriptions in this specification but should be defined by the scope of the appended claims.

Claims

1. An organic light emitting display comprising:

a display panel (10) having a plurality of pixels (PXL);
a gate drive circuit (13) that drives n scan lines (SL1, ... SL(n), n being a natural number) and n emission lines (EL1, ..., EL(n)) on the display panel (10); and
a data drive circuit (12) that drives data lines (DL) on the display panel (10),
each of the pixels (PXL) arranged in a jth row ($1<j\leq n$) comprising:

a driving transistor (DT) having a gate electrode connected to a node A, a source electrode connected to a node B, and a drain electrode connected to a node C, and the driving transistor (DT) controlling a driving current applied to an organic light emitting diode (OLED);
a first transistor (T1) that is connected between the data lines (DL) and the node B;
a second transistor (T2) that is connected between the node A and a high-level driving voltage input terminal (ELVDD);
a third transistor (T3) that is connected to the node B and the organic light emitting diode (OLED);
a fourth transistor (T4) that is connected to the node C and the high-level driving voltage input terminal;
a fifth transistor (T5) that is connected to the node A and the node C;
a sixth transistor (T6) that is connected between a node D and an initial voltage input terminal (Vini), the node D located between the third transistor (T3) and the organic light emitting diode (OLED); and
a capacitor (Cst) that is connected to the node A and the node D;

wherein
the gate of the second transistor (T2) is connected to a scan line (SL(j-1)) of a (j-1)th row of pixels;
the gates of the third and fourth transistors (T3, T4) are connected to the emission line (EM(j)) of the jth row of pixels;
the gates of the first and fifth transistors (T1, T5) are connected to the scan line (SL(j)) of the jth row of pixels;
the gate of the sixth transistor (T6) is connected either to the scan line (SL(j)) of the jth row of pixels or to the scan line (SL(j-1)) of the (j-1)th row of pixels; and
a cathode of the organic light emitting diode (OLED) is connected to a low-level driving voltage input terminal (ELVSS).

2. The organic light emitting display of claim 1, wherein a (j-1)th scan signal (SCAN(j-1)) in which a data voltage is provided to the pixels (PXL) arranged in a (j-1)th row has a turn-on voltage during a (j-1)th horizontal period, a jth scan signal (SCAN(j)) has the turn-on voltage in which the data voltage is provided to the pixels (PXL) arranged in a jth row during a jth horizontal period, and an emission signal (EM(j)) provided to the jth row has the turn-on voltage after the jth scan signal (SCAN(j)) is inverted to a turn-off voltage.

3. The organic light emitting display of claim 2, wherein, during the (j-1)th horizontal period, the second transistor (T2) applies the high-level driving voltage received from the high-level driving voltage input terminal to the node A, in response to the (j-1)th scan signal (SCAN(j-1)).

4. The organic light emitting display of claim 3, wherein, during the jth horizontal period, the first transistor (T1) applies the data voltage received from the data line (DL) to the node B, in response to the jth scan signal (SCAN(j)), and the fifth transistor (T5) connects the node A and the node C to operate the driving transistor (DT), in response to the jth scan signal (SCAN(j)).

5. The organic light emitting display of claim 4, wherein, during a (j+1)th horizontal period, the fourth transistor (T4) connects the high-level driving voltage input terminal and the node C, in response to the emission signal (EM(j)), and the third transistor (T3) connects the node B and the node D, in response to the emission signal (EM(j)), and the node D corresponds to an operating voltage of the organic light emitting diode (OLED) from the initial voltage level by the driving current, and a difference between the initial voltage level and the operating voltage of the organic light emitting diode (OLED) is applied to the node A so as to emit light of the organic light emitting diode (OLED) while compensating the threshold voltage of the driving transistor (DT).

6. The organic light emitting display of any one of claims 1 to 5, wherein a gate electrode of the sixth transistor (T6) is connected to a (j-1)th scan line (SL(j-1)), and during a (j-1)th horizontal period, the sixth transistor (T6) applies the initial voltage received from the initial voltage input terminal to the node D, in response to a (j-1)th scan signal (SCAN(j-1)).

7. The organic light emitting display of any one of claims 1 to 5, wherein a gate electrode of the sixth transistor (T6) is connected to a jth scan line (SL(j)), and during a jth horizontal period, the sixth transistor (T6) applies the initial voltage received from the initial voltage input terminal to the node D, in response to a jth scan signal (SCAN(j)).

8. The organic light emitting display of claim 7, wherein each of the pixels (PXL) arranged in the jth row further comprises a seventh transistor (T7) that is connected between the node D and the initial voltage input terminal and that is switched on in response to a (j-1)th scan signal (SCAN(j-1)).

9. The organic light emitting display of claim 8, wherein, during a (j-1)th horizontal period, the seventh transistor (T7) provides the initial voltage to the node D, in response to the (j-1)th scan signal (SCAN(j-1)).

10. The organic light emitting display of claim 9, wherein the initial voltage is lower than the driving voltage of the organic light emitting diode (OLED).

11. The organic light emitting display of any one of claims 1 to 10, wherein a jth horizontal period includes a high-voltage holding period, and a high-level driving voltage is applied to the node A in response to the (j-1)th scan signal (SCAN(j-1)) during the high-voltage holding period.

12. The organic light emitting display of any one of claims 1 to 11, wherein at least one among the second transistor (T2) and the fifth transistor (T5) has a double-gate structure.

13. The organic light emitting display of any one of claims 1 to 12, further comprising a metal layer (114) under a semiconductor layer (260) of the driving transistor (DT).

14. The organic light emitting display of any one of claims 1 to 13, wherein a first electrode (241) of the capacitor (Cst) that receives an initial voltage from the initial voltage input terminal corresponds to the gate electrode of the driving transistor (DT).

15. The organic light emitting display of any one of claims 1 to 13, wherein a first electrode (241) of the capacitor (Cst) that receives the initial voltage from the initial voltage input terminal is disposed in an area corresponding to a semiconductor layer of the fifth transistor (T5) that operates during a sampling period.

16. The organic light emitting display of any one of claims 1 to 15, wherein the capacitor (Cst) having a first electrode (241) and a second electrode is connected between the initial voltage input terminal and the at least one transistor, wherein the area of the first electrode (241) that receives the initial voltage is larger than the area of the second electrode.

17. The organic light emitting display of any one of claims 1 to 16, wherein a first electrode (241) of the capacitor (Cst) is not connected to the high level driving voltage input terminal, and is connected to the initial voltage input terminal, thereby reducing the number of contact holes.

18. The organic light emitting display of any one of claims 1 to 17, wherein the organic light emitting diode (OLED) having an anode connected to a first electrode (241) of the capacitor (Cst) and a cathode opposite to the anode, wherein the driving transistor (DT) is compensated by the capacitor (Cst) that receives the initial voltage.

19. The organic light emitting display of any one of claims 1 to 18, wherein a single frame includes:

an initial period in which a gate voltage of the driving transistor (DT) is initialized;
a sampling period for compensating the threshold voltage of the driving transistor (DT); and
a light emission period in which the organic light emitting diode (OLED) emits light,
wherein a value corresponding to an image signal to be displayed the organic light emitting diode (OLED) is applied to the data line (DL) during the sampling period, and
wherein the initial voltage is applied to at least one electrode of the capacitor (Cst) during the initial period.

20. The organic light emitting display of claim 19, wherein the sampling period comprises a period in which the initial period is held.

21. The organic light emitting display of any one of claims 19 to 20, further comprising a high voltage holding period at an initial stage of the sampling period, and the high level driving voltage is applied to other electrodes of the capacitor (Cst) in response to the gate voltage during the high voltage holding period.

22. The organic light emitting display of any one of claims 19 to 21, wherein the initial period for the pixel of the jth row overlaps a period in which the data voltage is provided to the pixel of the (j-1)th row.

Patentansprüche

1. Eine organische lichtemittierende Anzeige, aufweisend:

ein Anzeigefeld (10), das eine Vielzahl von Pixeln (PXL) hat;
eine Gate-Treiberschaltung (13), die n Scanleitungen (SL1, ... SL(n), wobei n eine natürliche Zahl ist) und n Emissionsleitungen (EL1,..., EL(n)) auf dem Anzeigefeld (10) ansteuert; und
eine Daten-Treiberschaltung (12), die Datenleitungen (DL) auf dem Anzeigefeld (10) ansteuert,
jedes der Pixel (PXL), die in einer j-ten Reihe ($1<j\leq n$) angeordnet sind, aufweisend:

einen Treibertransistor (DT), der eine Gate-Elektrode, die mit einem Knoten A verbunden ist, eine Source-Elektrode, die mit einem Knoten B verbunden ist, und eine Drain-Elektrode, die mit einem Knoten C verbunden ist, hat, und wobei der Treibertransistor (DT) einen Treiberstrom steuert, der an eine organische lichtemittierende Diode (OLED) angelegt ist;
einen ersten Transistor (T1), der zwischen die Datenleitungen (DL) und den Knoten B geschaltet ist;
einen zweiten Transistor (T2), der zwischen den Knoten A und einen Hochpegel-Treiberspannungseingangsanschluss (ELVDD) geschaltet ist;
einen dritten Transistor (T3), der mit dem Knoten B und der organischen lichtemittierenden Diode (OLED) verbunden ist;
einen vierten Transistor (T4), der mit dem Knoten C und dem Hochpegel-Treiberspannungseingangsanschluss verbunden ist;
einen fünften Transistor (T5), der mit dem Knoten A und dem Knoten C verbunden ist;
einen sechsten Transistor (T6), der zwischen einen Knoten D und einen Anfangsspannungseingangsanschluss (Vini) geschaltet ist, wobei der Knoten D zwischen dem dritten Transistor (T3) und der organischen lichtemittierenden Diode (OLED) angeordnet ist; und
einen Kondensator (Cst), der mit dem Knoten A und dem Knoten D verbunden ist;

wobei
das Gate des zweiten Transistors (T2) mit einer Scanleitung (SL(j-1)) einer (j-1)-ten Reihe von Pixeln verbunden ist;
die Gates des dritten und vierten Transistors (T3, T4) mit der Emissionsleitung (EM(j)) der j-ten Reihe von Pixeln verbunden sind;
die Gates des ersten und fünften Transistors (T1, T5) mit der Scanleitung (SL(j)) der j-ten Reihe von Pixeln verbunden sind;
das Gate des sechsten Transistors (T6) entweder mit der Scanleitung (SL(j)) der j-ten Reihe von Pixeln oder mit der Scanleitung (SL(j-1)) der (j-1)-ten Reihe von Pixeln verbunden ist; und
eine Kathode der organischen lichtemittierenden Diode (OLED) mit einem Niedrigpegel-Treiberspannungseingangsanschluss (ELVSS) verbunden ist.

2. Die organische lichtemittierende Anzeige gemäß Anspruch 1, wobei ein (j-1)-tes Scansignal (SCAN(j-1)), in welchem eine Datenspannung an die Pixel (PXL), die in einer (j-1)-ten Reihe angeordnet sind, bereitgestellt wird, eine Einschaltspannung während einer (j-1)-ten Horizontal-Periode hat, ein j-tes Scansignal (SCAN (j)) während einer j-ten Horizontal-Periode die Einschaltspannung hat, in welcher die Datenspannung an die Pixel (PXL), die in einer j-ten Reihe angeordnet sind, bereitgestellt wird, und ein Emissions-Signal (EM(j)), das für die j-te Reihe bereitgestellt wird, die Einschaltspannung hat, nachdem das j-te Scansignal (SCAN (j)) zu einer Ausschaltspannung invertiert worden ist.

3. Die organische lichtemittierende Anzeige gemäß Anspruch 2, wobei während der (j-1)-ten Horizontal-Periode der zweite Transistor (T2) die Hochpegel-Treiberspannung, die von dem Hochpegel-Treiberspannungseingangsanschluss empfangen wird, an den Knoten A als Antwort auf das (j-1)-te Scansignal (SCAN(j-1)) anlegt.

4. Die organische lichtemittierende Anzeige gemäß Anspruch 3, wobei während der j-ten Horizontal-Periode der erste Transistor (T1) die Datenspannung, die von der Datenleitung (DL) empfangen wird, als Antwort auf das j-te Scansignal (SCAN(j)) an den Knoten B anlegt, und der fünfte Transistor (T5) den Knoten A und den Knoten C verbindet, um den Treibertransistor (DT) als Antwort auf das j-te Scansignal (SCAN(j)) zu betreiben.

5. Die organische lichtemittierende Anzeige gemäß Anspruch 4, wobei während einer (j+1)-ten Horizontal-Periode der vierte Transistor (T4) den Hochpegel-Treiberspannungseingangsanschluss und den Knoten C als Antwort auf das Emissionssignal (EM(j)) verbindet, und der dritte Transistor (T3) den Knoten B und den Knoten D als Antwort auf das Emissionssignal (EM(j)) verbindet, und der Knoten D durch den Treiberstrom zu einer Betriebsspannung der organischen lichtemittierenden Diode (OLED) korrespondiert von dem Anfangsspannungspegel, und eine Differenz zwischen dem Anfangsspannungspegel und der Betriebsspannung der organischen lichtemittierenden Diode (OLED) an den Knoten A angelegt ist, sodass Licht der organischen lichtemittierenden Diode (OLED) emittiert wird, während die Schwellenspannung des Treibertransistors (DT) kompensiert wird.

6. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 1 bis 5, wobei eine Gate-Elektrode des sechsten Transistors (T6) mit einer (j-1)-ten Scanleitung (SL(j-1)) verbunden ist, und während einer (j-1)-ten Horizontal-Periode der sechste Transistor (T6) die Anfangsspannung, die von dem Anfangsspannungseingangsanschluss empfangen wird, an den Knoten D als Antwort auf ein (j-1)-tes Scansignal (SCAN(j-1)) anlegt.

7. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 1 bis 5, wobei eine Gate-Elektrode des sechsten Transistors (T6) mit einer j-ten Scanleitung (SL(j)) verbunden ist, und während einer j-ten Horizontal-Periode der sechste Transistor (T6) die Anfangsspannung, die von dem Anfangsspannungseingangsanschluss empfangen wird, an den Knoten D als Antwort auf ein j-tes Scansignal (SCAN(j)) anlegt.

8. Die organische lichtemittierende Anzeige gemäß Anspruch 7, wobei jedes der Pixel (PXL), die in der j-ten Reihe angeordnet sind, ferner einen siebten Transistor (T7) aufweist, der zwischen den Knoten D und den Anfangsspannungseingangsanschluss geschaltet ist und der als Antwort auf ein (j-1)-tes Scansignal (SCAN(j-1)) eingeschaltet wird.

9. Die organische lichtemittierende Anzeige gemäß Anspruch 8, wobei während einer (j-1)-ten Periode der siebte Transistor (T7) die Anfangsspannung an dem Knoten D als Antwort auf das (j-1)-te Scansignal (SCAN(j-1)) bereitstellt.

10. Die organische lichtemittierende Anzeige gemäß Anspruch 9, wobei die Anfangsspannung niedriger ist als die Treiberspannung der organischen lichtemittierenden Diode (OLED).

11. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 1 bis 10, wobei eine j-te Horizontal-Periode eine Hochspannungshalteperiode enthält, und eine Hochpegel-Treiberspannung an den Knoten A als Antwort auf das (j-1)-te Scansignal (SCAN(j-1)) während der Hohe-Spannung-Halteperiode angelegt ist.

12. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 1 bis 11, wobei mindestens einer von dem zweiten Transistor (T2) und dem fünften Transistor (T5) eine Doppel-Gate-Struktur hat.

13. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 1 bis 12, ferner aufweisend:
eine Metallschicht (114) unter einer Halbleiterschicht (260) des Treibertransistors (DT).

14. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 1 bis 13, wobei eine erste Elektrode (241) des Kondensators (Cst), die eine Anfangsspannung von dem Anfangsspannungseingangsanschluss empfängt, zu der Gate-Elektrode des Treibertransistors (DT) korrespondiert.

15. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 1 bis 13, wobei eine erste Elektrode (241) des Kondensators (Cst), die die Anfangsspannung von dem Anfangsspannungseingangsanschluss empfängt, in einem Gebiet angeordnet ist, das zu einer Halbleiterschicht des fünften Transistors (T5) korrespondiert, der während einer Abtastperiode arbeitet.

16. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 1 bis 15, wobei der Kondensator (Cst), der eine erste Elektrode (241) und eine zweite Elektrode hat, zwischen den Anfangsspannungseingangsanschluss und den mindestens einen Transistor geschaltet ist, wobei das Gebiet der ersten Elektrode (241), die die Anfangsspannung empfängt, größer ist als die Fläche der zweiten Elektrode.

17. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 1 bis 16, wobei eine erste Elektrode (241) des Kondensators (Cst) nicht mit dem Hochpegel-Treiberspannungseingangsanschluss verbunden ist und mit dem Anfangsspannungseingangsanschluss verbunden ist, wodurch die Anzahl an Kontaktlöchern reduziert wird.

18. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 1 bis 17, wobei die organische lichtemittierende Diode (OLED) eine Anode hat, die mit einer ersten Elektrode (241) des Kondensators (Cst) verbunden ist, und gegenüber der Anode eine Kathode, wobei der Treibertransistor (DT) durch den Kondensator (Cst) kompensiert wird, der die Anfangsspannung empfängt.

19. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 1 bis 18, wobei ein einzelner Frame enthält:

eine Anfangsperiode, in welcher eine Gate-Spannung des Treibertransistors (DT) initialisiert wird;
eine Abtastperiode zur Kompensation der Schwellenspannung des Treibertransistors (DT); und
eine Lichtemissionsperiode, in welcher die organische lichtemittierende Diode (OLED) Licht emittiert,
wobei ein Wert, der zu einem durch die organische lichtemittierende Diode (OLED) anzuzeigenden Bildsignal korrespondiert, an der Datenleitung (DL) während der Abtastperiode anliegt, und
wobei die Anfangsspannung an mindestens einer Elektrode des Kondensators (Cst) während einer Anfangsperiode angelegt ist.

20. Die organische lichtemittierende Anzeige gemäß Anspruch 19, wobei die Abtastperiode eine Periode aufweist, in der die Anfangsperiode gehalten wird.

21. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 19 bis 20, ferner aufweisend: eine Hohe-Spannung-Halteperiode in einer Anfangsphase der Abtastperiode, und wobei die Hochpegel-Treiberspannung an andere Elektroden des Kondensators (Cst) als Antwort auf die Gate-Spannung während der Hohe-Spannung-Halteperiode angelegt ist.

22. Die organische lichtemittierende Anzeige gemäß einem der Ansprüche 19 bis 21, wobei die Anfangsperiode für das Pixel der j-ten Reihe eine Periode überlappt, in der die Datenspannung an das Pixel der (j-1)-ten Reihe bereitgestellt wird.

Revendications

1. Affichage électroluminescent organique comprenant :

un panneau d'affichage (10) ayant une pluralité de pixels (PXL) ;
un circuit de commande de grille (13) qui commande « n » lignes de balayage (SL1, ..., SL(n), « n » étant un nombre naturel) et « n » lignes d'émission (EL1, ..., EL(n)) sur le panneau d'affichage (10) ; et
un circuit de commande de données (12) qui commande des lignes de données (DL) sur le panneau d'affichage (10) ;
dans lequel chacun des pixels (PXL) agencés dans une jième rangée ($1 < j \leq n$) comprend :

un transistor de commande (DT) présentant une électrode grille connectée à un noeud A, une électrode

source connectée à un noeud B, et une électrode drain connectée à un noeud C, et le transistor de commande (DT) commandant un courant de commande appliqué à une diode électroluminescente organique (OLED) ;
un premier transistor (T1) qui est connecté entre les lignes de données (DL) et le noeud B ;
un deuxième transistor (T2) qui est connecté entre le noeud A et une borne d'entrée de tension de commande de haut niveau (ELVDD) ;
un troisième transistor (T3) qui est connecté au noeud B et à la diode électroluminescente organique (OLED) ;
un quatrième transistor (T4) qui est connecté au noeud C et à la borne d'entrée de tension de commande de haut niveau ;
un cinquième transistor (T5) qui est connecté au noeud A et au noeud C ;
un sixième transistor (T6) qui est connecté entre un noeud D et une borne d'entrée de tension initiale (Vini), le noeud D étant situé entre le troisième transistor (T3) et la diode électroluminescente organique (OLED) ; et
un condensateur (Cst) qui est connecté au noeud A et au noeud D ;

dans lequel
la grille du deuxième transistor (T2) est connectée à une ligne de balayage (SL(j-1)) d'une (j-1)ième rangée de pixels ;
les grilles des troisième et quatrième transistors (T3, T4) sont connectées à la ligne d'émission (EM(j)) de la jième rangée de pixels ;
les grilles des premier et cinquième transistors (T1, T5) sont connectées à la ligne de balayage (SL(j)) de la jième rangée de pixels ;
la grille du sixième transistor (T6) est connectée soit à la ligne de balayage (SL(j)) de la jième rangée de pixels, soit à la ligne de balayage (SL(j-1)) de la (j-1)ième rangée de pixels ; et
une cathode de la diode électroluminescente organique (OLED) est connectée à une borne d'entrée de tension de commande de bas niveau (ELVSS).

2. Affichage électroluminescent organique selon la revendication 1, dans lequel un (j-1)ième signal de balayage (SCAN(j-1)), dans lequel une tension de données est fournie aux pixels (PXL) agencés dans une (j-1)ième rangée, présente une tension de mise sous tension au cours d'une (j-1)ième période horizontale, un jième signal de balayage (SCAN(j)) présente la tension de mise sous tension dans laquelle la tension de données est fournie aux pixels (PXL) agencés dans une jième rangée au cours d'une jième période horizontale, et un signal d'émission (EM(j)) fourni à la jième rangée présente la tension de mise sous tension après que le jième signal de balayage (SCAN(j)) a été inversé à une tension de mise hors tension.

3. Affichage électroluminescent organique selon la revendication 2, dans lequel, au cours de la (j-1)ième période horizontale, le deuxième transistor (T2) applique la tension de commande de haut niveau, reçue en provenance de la borne d'entrée de tension de commande de haut niveau, au noeud A, en réponse au (j-1)ième signal de balayage (SCAN(j-1)).

4. Affichage électroluminescent organique selon la revendication 3, dans lequel, au cours de la jième période horizontale, le premier transistor (T1) applique la tension de données, reçue en provenance de la ligne de données (DL), au noeud B, en réponse au jième signal de balayage (SCAN(j)), et le cinquième transistor (T5) connecte le noeud A et le noeud C en vue d'exploiter le transistor de commande (DT), en réponse au jième signal de balayage (SCAN(j)).

5. Affichage électroluminescent organique selon la revendication 4, dans lequel, au cours d'une (j+1)ième période horizontale, le quatrième transistor (T4) connecte la borne d'entrée de tension de commande de haut niveau et le noeud C, en réponse au signal d'émission (EM(j)), le troisième transistor (T3) connecte le noeud B et le noeud D, en réponse au signal d'émission (EM(j)), et le noeud D correspond à une tension de fonctionnement de la diode électroluminescente organique (OLED) à partir du niveau de tension initiale par le courant de commande, et une différence entre le niveau de tension initiale et la tension de fonctionnement de la diode électroluminescente organique (OLED) est appliquée au noeud A, de manière à émettre de la lumière de la diode électroluminescente organique (OLED) tout en compensant la tension de seuil du transistor de commande (DT).

6. Affichage électroluminescent organique selon l'une quelconque des revendications 1 à 5, dans lequel une électrode grille du sixième transistor (T6) est connectée à une (j-1)ième ligne de balayage (SL(j-1)), et au cours d'une (j-1)ième période horizontale, le sixième transistor (T6) applique la tension initiale, reçue en provenance de la borne d'entrée de tension initiale, au noeud D, en réponse à un (j-1)ième signal de balayage (SCAN(j-1)).

7. Affichage électroluminescent organique selon l'une quelconque des revendications 1 à 5, dans lequel une électrode grille du sixième transistor (T6) est connectée à une jième ligne de balayage (SL(j)), et au cours d'une jième période horizontale, le sixième transistor (T6) applique la tension initiale, reçue en provenance de la borne d'entrée de tension initiale, au noeud D, en réponse à un jième signal de balayage (SCAN(j)).

8. Affichage électroluminescent organique selon la revendication 7, dans lequel chacun des pixels (PXL) agencés dans la jième rangée comprend en outre un septième transistor (T7) qui est connecté entre le noeud D et la borne d'entrée de tension initiale et qui est mis sous tension en réponse à un (j-1)ième signal de balayage (SCAN(j-1)).

9. Affichage électroluminescent organique selon la revendication 8, dans lequel, au cours d'une (j-1)ième période horizontale, le septième transistor (T7) fournit la tension initiale au noeud D, en réponse au (j-1)ième signal de balayage (SCAN(j-1)).

10. Affichage électroluminescent organique selon la revendication 9, dans lequel la tension initiale est inférieure à la tension de commande de la diode électroluminescente organique (OLED).

11. Affichage électroluminescent organique selon l'une quelconque des revendications 1 à 10, dans lequel une jième période horizontale inclut une période de maintien de haute tension, et une tension de commande de haut niveau est appliquée au noeud A en réponse au (j-1)ième signal de balayage (SCAN(j-1)) au cours de la période de maintien de haute tension.

12. Affichage électroluminescent organique selon l'une quelconque des revendications 1 à 11, dans lequel au moins l'un parmi le deuxième transistor (T2) et le cinquième transistor (T5) présente une structure à double grille.

13. Affichage électroluminescent organique selon l'une quelconque des revendications 1 à 12, comprenant en outre une couche métallique (114) sous une couche semi-conductrice (260) du transistor de commande (DT).

14. Affichage électroluminescent organique selon l'une quelconque des revendications 1 à 13, dans lequel une première électrode (241) du condensateur (Cst) qui reçoit une tension initiale en provenance de la borne d'entrée de tension initiale correspond à l'électrode grille du transistor de commande (DT).

15. Affichage électroluminescent organique selon l'une quelconque des revendications 1 à 13, dans lequel une première électrode (241) du condensateur (Cst) qui reçoit la tension initiale en provenance de la borne d'entrée de tension initiale est disposée dans une zone correspondant à une couche semi-conductrice du cinquième transistor (T5) qui fonctionne au cours d'une période d'échantillonnage.

16. Affichage électroluminescent organique selon l'une quelconque des revendications 1 à 15, dans lequel le condensateur (Cst) présentant une première électrode (241) et une seconde électrode est connecté entre la borne d'entrée de tension initiale et ledit au moins un transistor, dans lequel la zone de la première électrode (241) qui reçoit la tension initiale est plus grande que la zone de la seconde électrode.

17. Affichage électroluminescent organique selon l'une quelconque des revendications 1 à 16, dans lequel une première électrode (241) du condensateur (Cst) n'est pas connectée à la borne d'entrée de tension de commande de haut niveau, et est connectée à la borne d'entrée de tension initiale, ce qui réduit par conséquent le nombre de trous de contact.

18. Affichage électroluminescent organique selon l'une quelconque des revendications 1 à 17, dans lequel la diode électroluminescente organique (OLED) présente une anode connectée à une première électrode (241) du condensateur (Cst), et une cathode opposée à l'anode, et dans lequel le transistor de commande (DT) est compensé par le condensateur (Cst) qui reçoit la tension initiale.

19. Affichage électroluminescent organique selon l'une quelconque des revendications 1 à 18, dans lequel une trame unique inclut :

une période initiale au cours de laquelle une tension de grille du transistor de commande (DT) est initialisée ;
une période d'échantillonnage pour compenser la tension de seuil du transistor de commande (DT) ; et
une période d'émission de lumière au cours de laquelle la diode électroluminescente organique (OLED) émet de la lumière ;

dans lequel une valeur correspondant à un signal d'image devant être affiché par la diode électroluminescente organique (OLED) est appliquée à la ligne de données (DL) au cours de la période d'échantillonnage ; et
dans lequel la tension initiale est appliquée à au moins une électrode du condensateur (Cst) au cours de la période initiale.

20. Affichage électroluminescent organique selon la revendication 19, dans lequel la période d'échantillonnage comprend une période au cours de laquelle la période initiale est maintenue.

21. Affichage électroluminescent organique selon l'une quelconque des revendications 19 à 20, comprenant en outre une période de maintien de haute tension à un stade initial de la période d'échantillonnage, et dans lequel la tension de commande de haut niveau est appliquée à d'autres électrodes du condensateur (Cst) en réponse à la tension de grille au cours de la période de maintien de haute tension.

22. Affichage électroluminescent organique selon l'une quelconque des revendications 19 à 21, dans lequel la période initiale pour le pixel de la jième rangée chevauche une période au cours de laquelle la tension de données est fournie au pixel de la (j-1)ième rangée.

FIG. 1

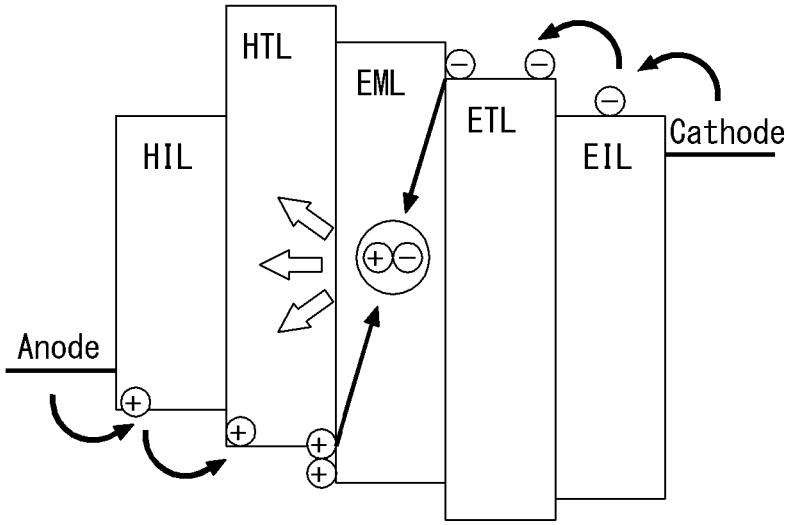


FIG. 2

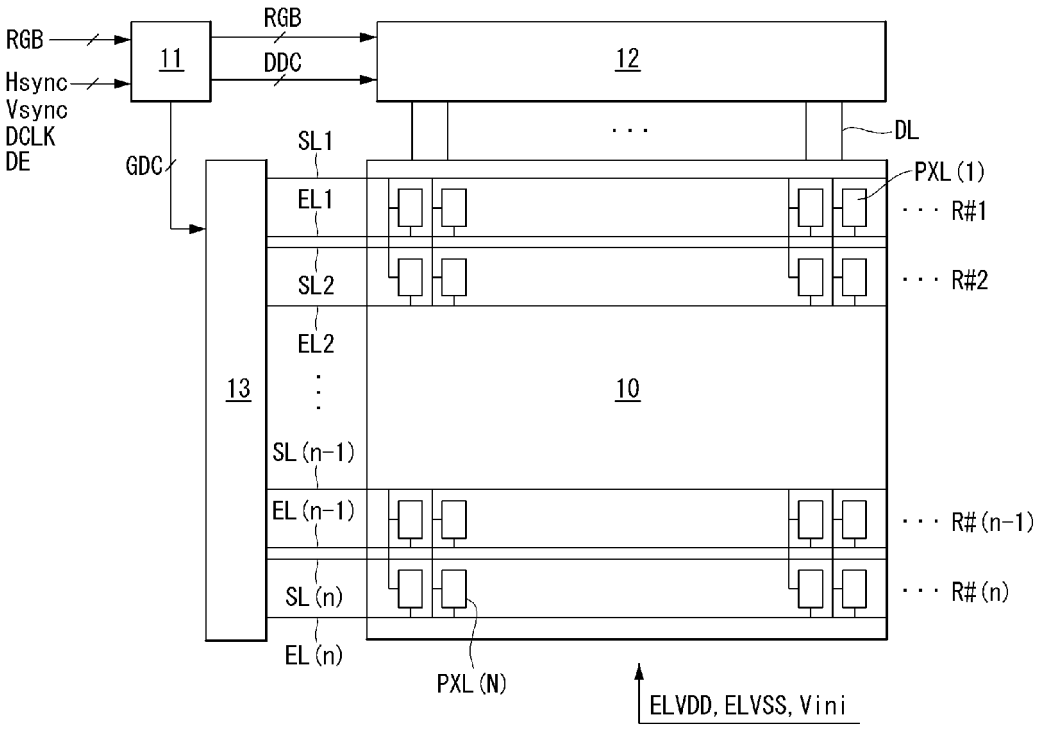

RGB
Hsync
Vsync
DCLK
DE
11
RGB
DDC
12
GDC
SL1
EL1
SL2
EL2
13
10
SL(n-1)
EL(n-1)
SL(n)
EL(n)
DL
PXL(1)
R#1
R#2
R#(n-1)
R#(n)
PXL(N)
ELVDD, ELVSS, Vini

FIG. 3

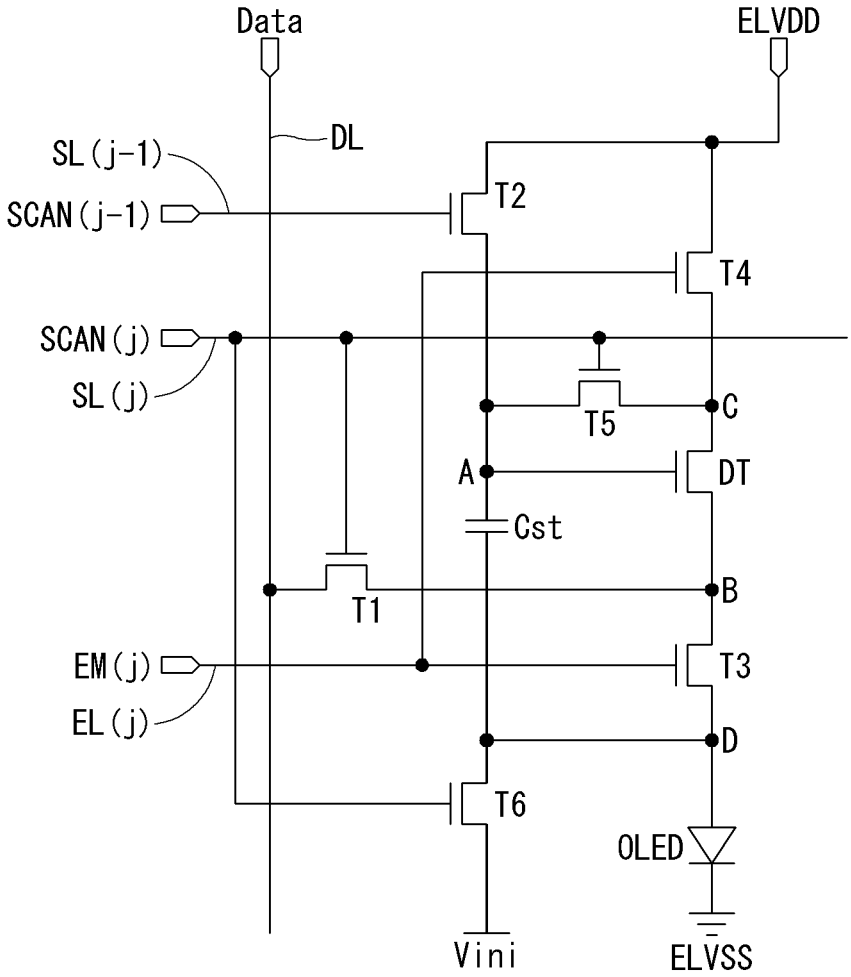

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
A
DT
Cst
T1
B
EM(j)
EL(j)
T3
D
T6
OLED
Vini
ELVSS

FIG. 4

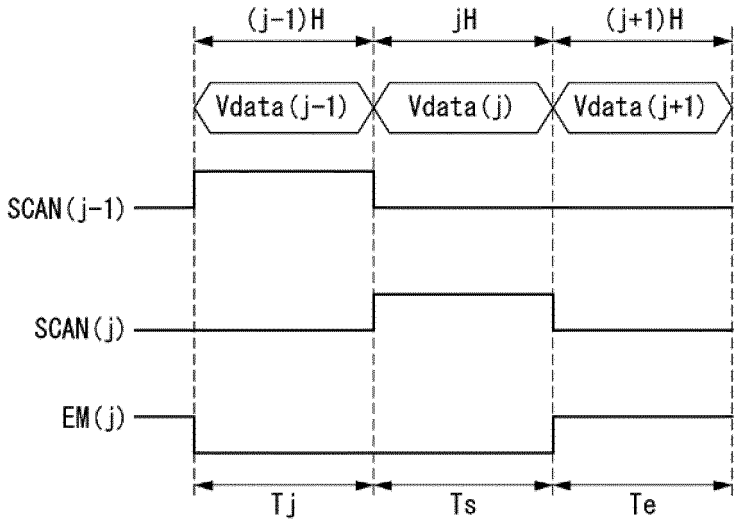


FIG. 5A

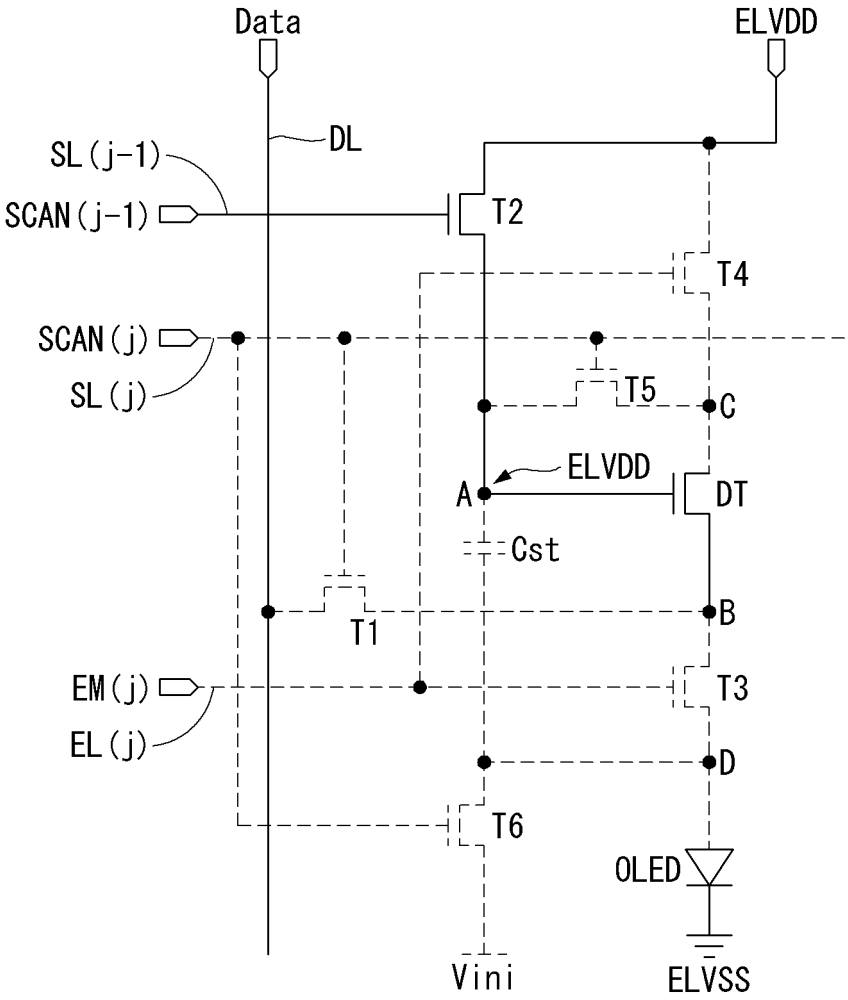

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
ELVDD
A
DT
Cst
T1
B
EM(j)
EL(j)
T3
D
T6
OLED
Vini
ELVSS

FIG. 5B

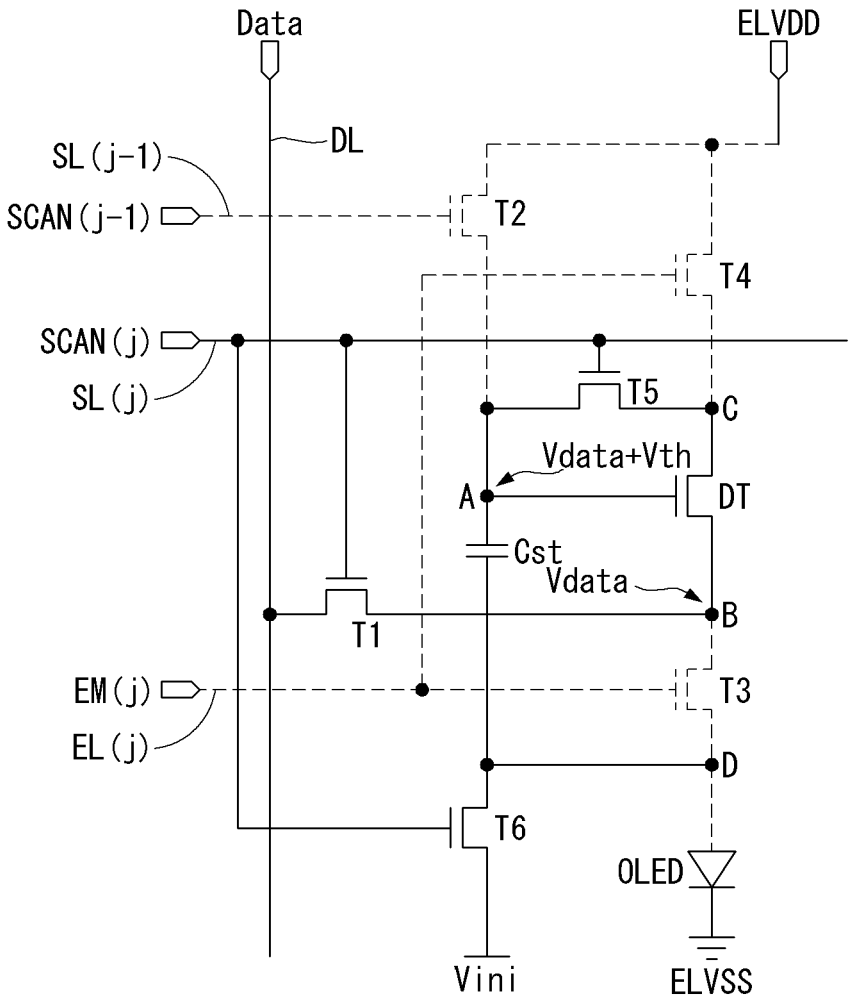

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
Vdata+Vth
A
DT
Cst
Vdata
B
T1
EM(j)
EL(j)
T3
D
T6
OLED
Vini
ELVSS

FIG. 5C

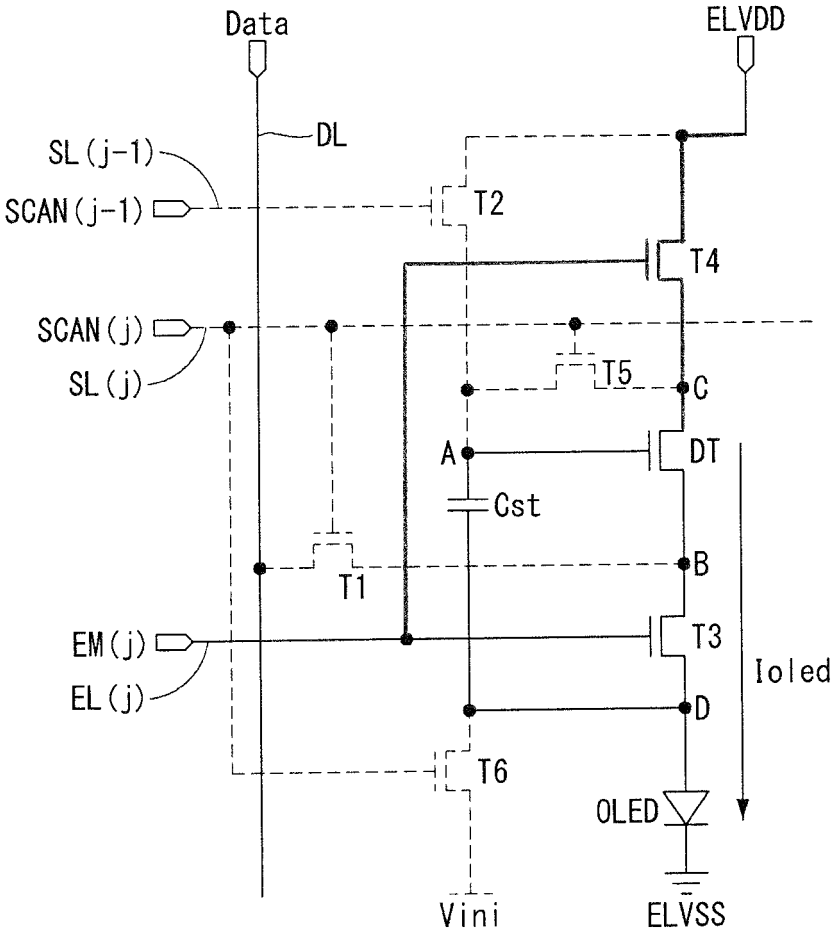

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
A
DT
Cst
B
T1
EM(j)
EL(j)
T3
Ioled
D
T6
OLED
Vini
ELVSS

FIG. 6

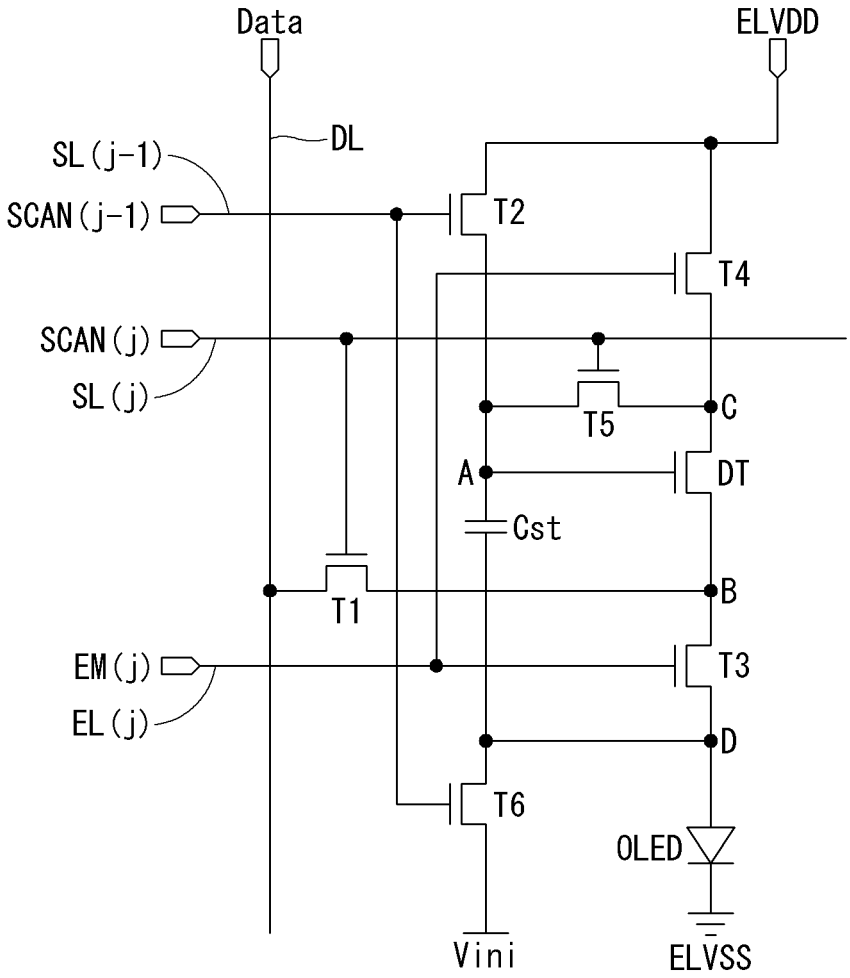

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
A
DT
Cst
T1
B
EM(j)
EL(j)
T3
D
T6
OLED
Vini
ELVSS

FIG. 7A

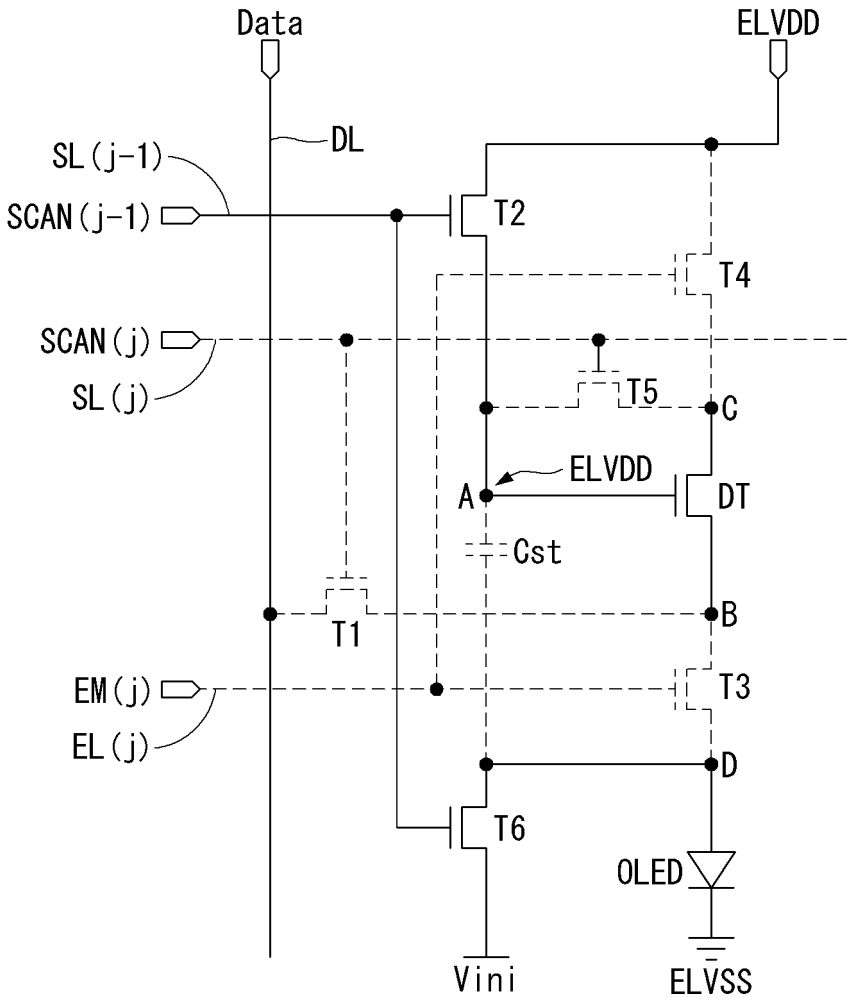

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
ELVDD
A
DT
Cst
T1
B
EM(j)
EL(j)
T3
D
T6
OLED
Vini
ELVSS

FIG. 7B

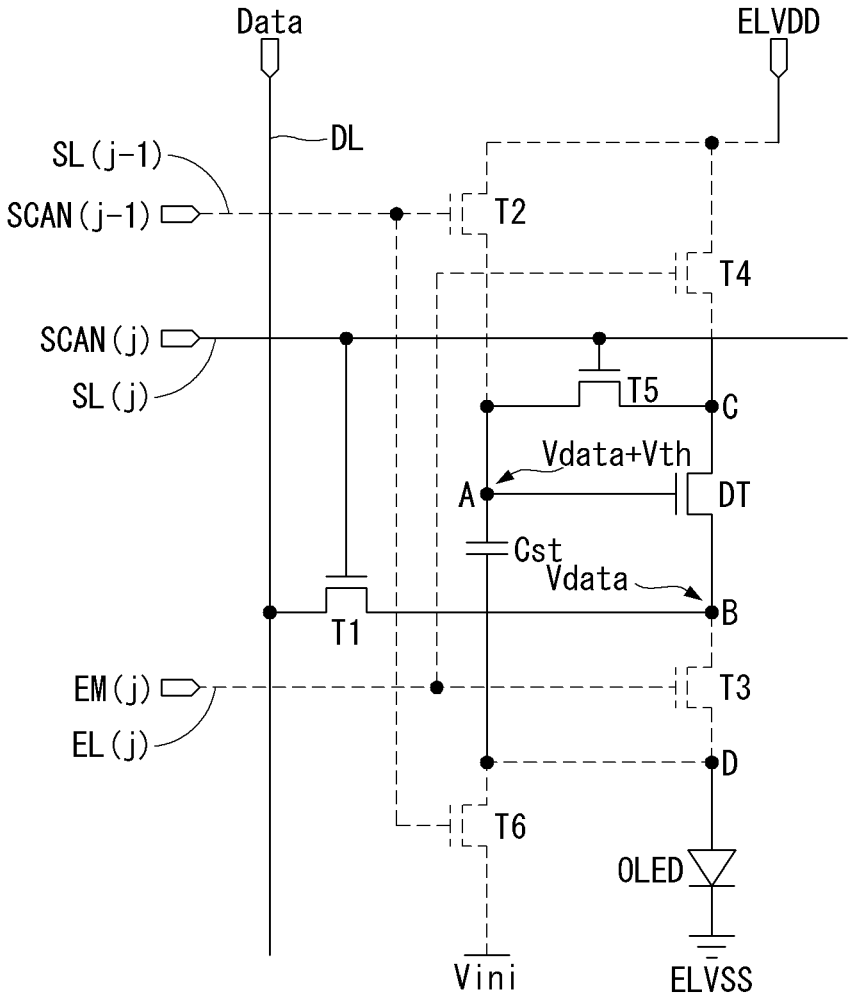

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
Vdata+Vth
A
DT
Cst
Vdata
B
T1
EM(j)
EL(j)
T3
D
T6
OLED
Vini
ELVSS

FIG. 7C

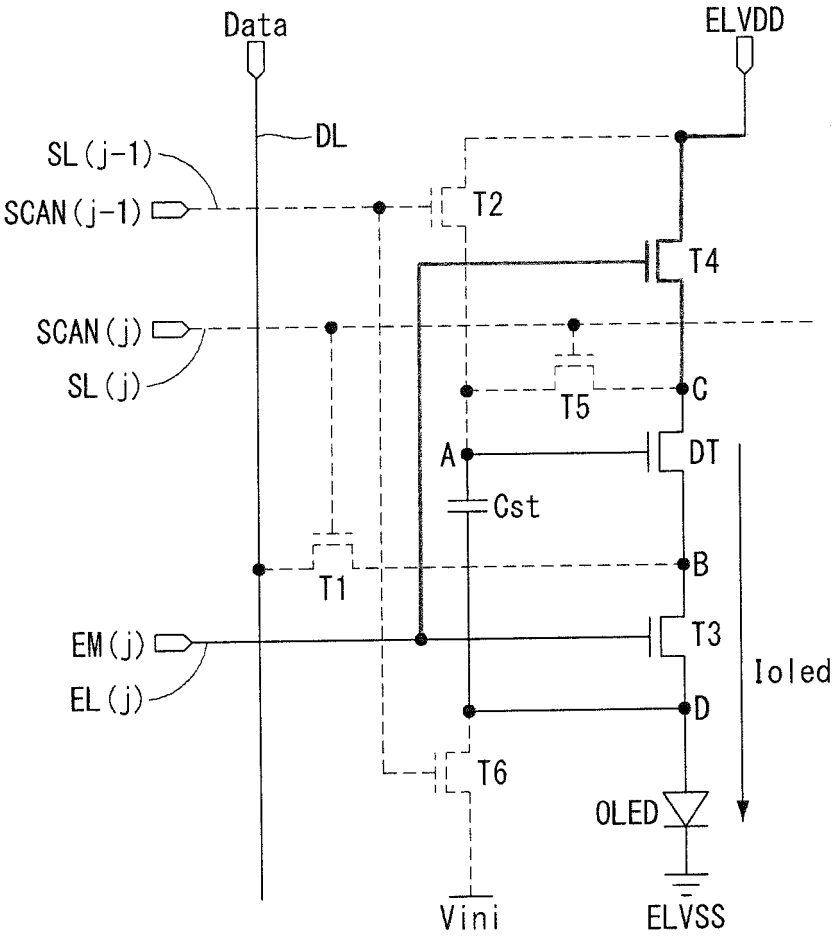

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
A
DT
Cst
B
T1
EM(j)
EL(j)
T3
Ioled
D
T6
OLED
Vini
ELVSS

FIG. 8

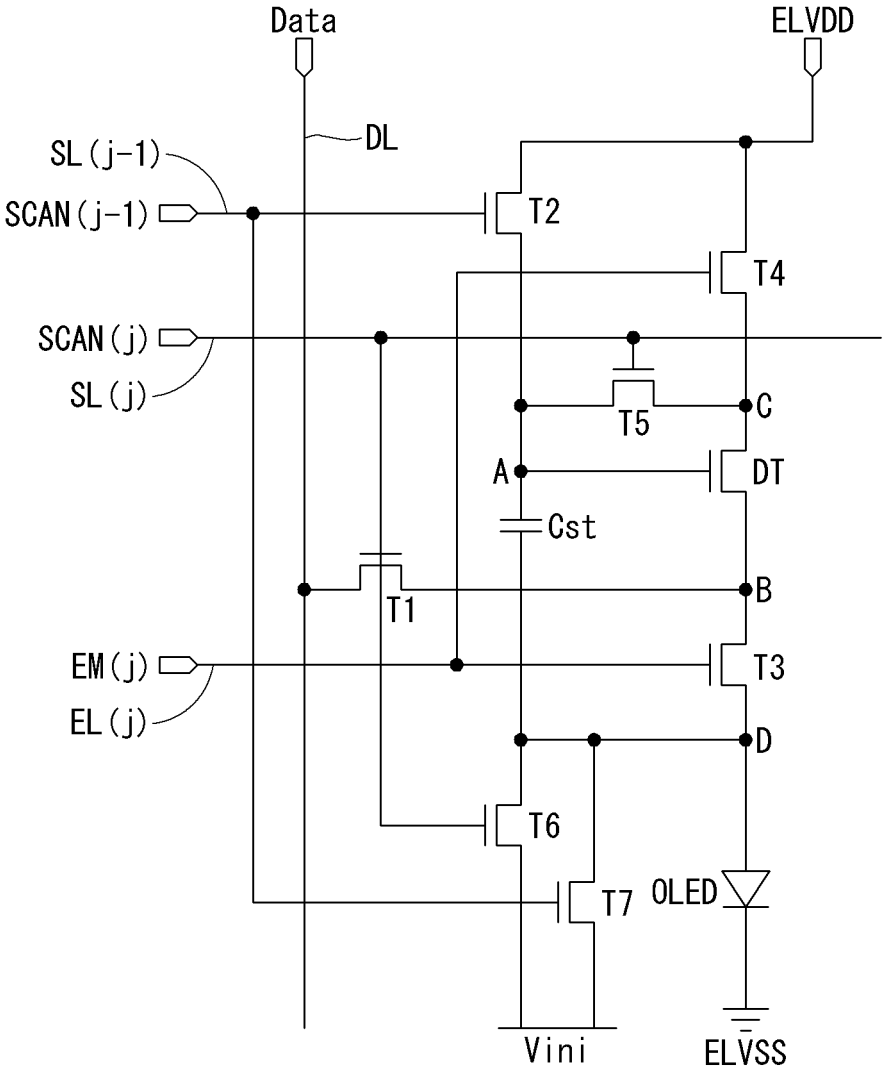

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
A
DT
Cst
T1
B
EM(j)
EL(j)
T3
D
T6
T7
OLED
Vini
ELVSS

FIG. 9A

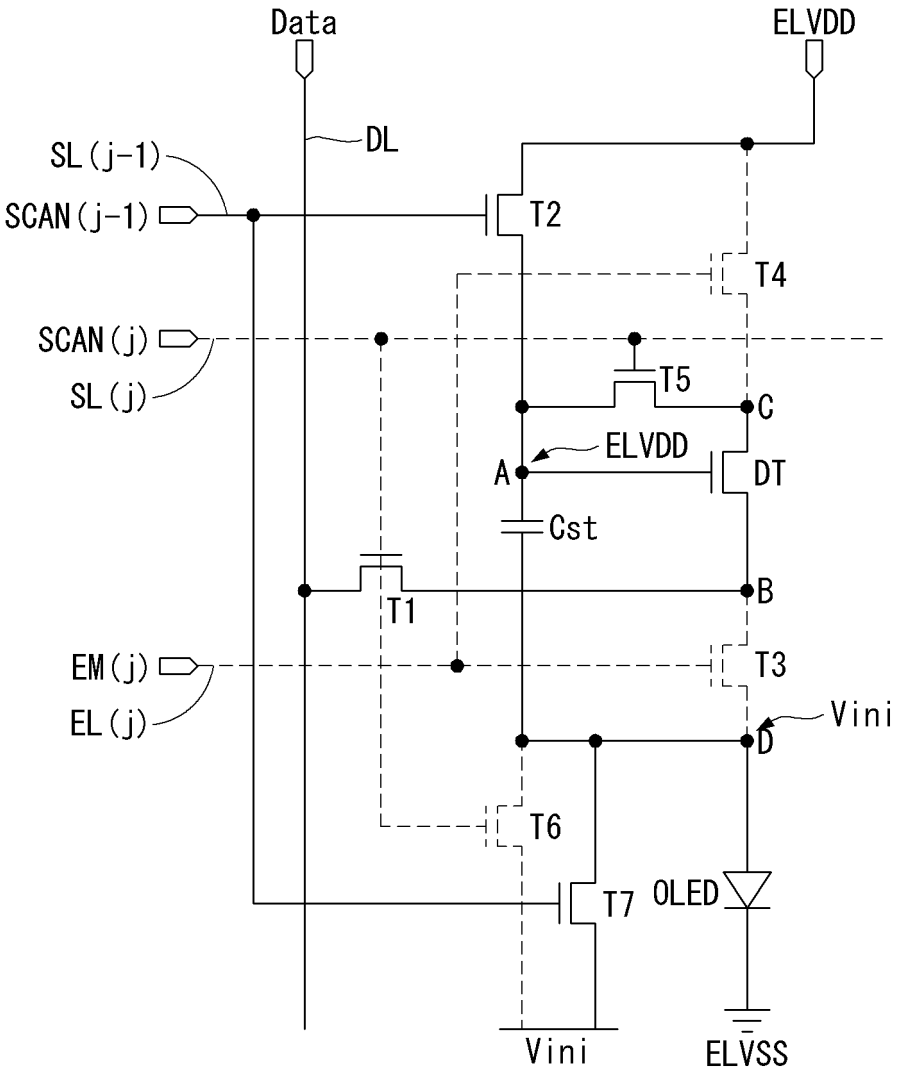

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
ELVDD
A
DT
Cst
B
T1
EM(j)
EL(j)
T3
Vini
D
T6
T7
OLED
Vini
ELVSS

FIG. 9B

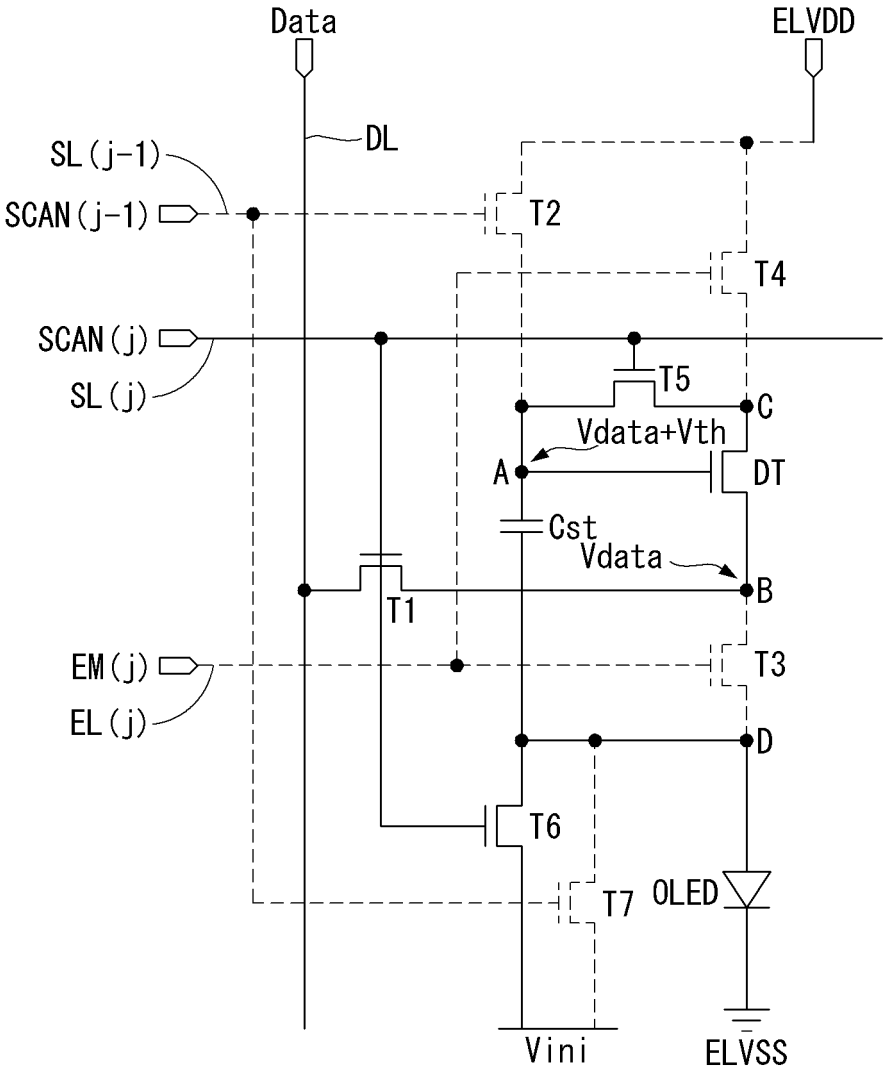

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
Vdata+Vth
A
DT
Cst
Vdata
B
T1
EM(j)
EL(j)
T3
D
T6
T7
OLED
Vini
ELVSS

FIG. 9C

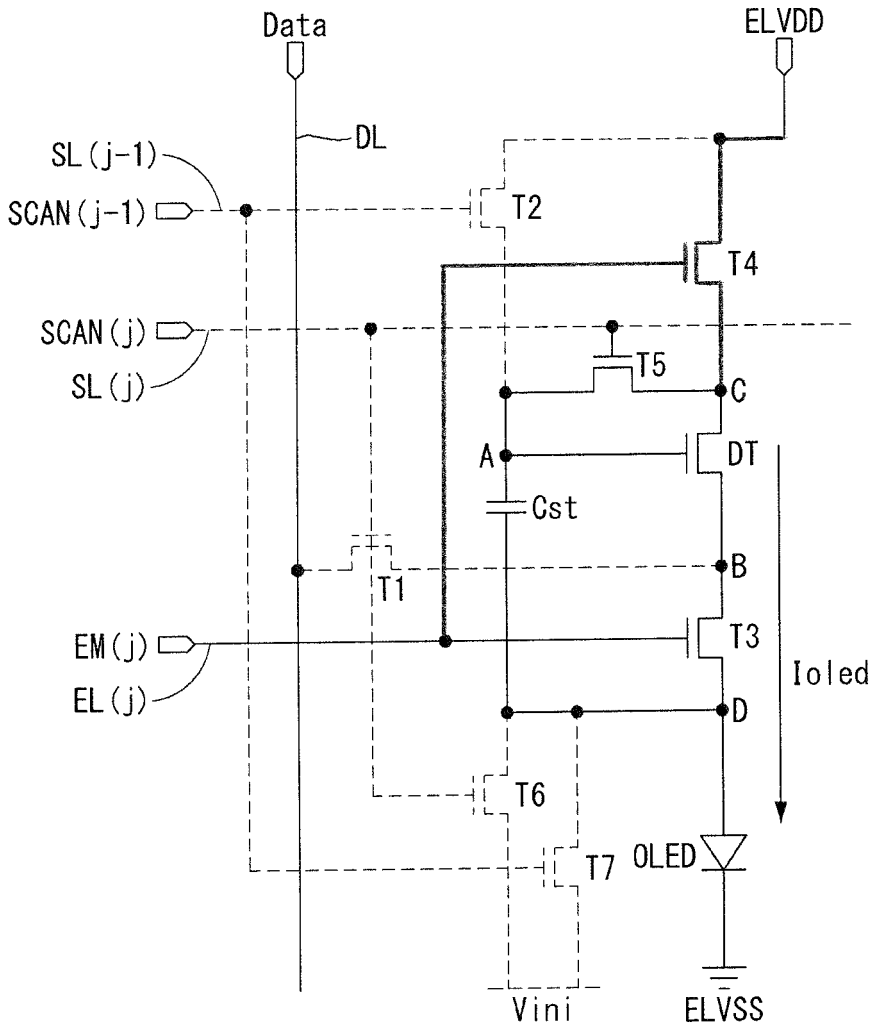

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
A
DT
Cst
B
T1
EM(j)
EL(j)
T3
Ioled
D
T6
T7
OLED
Vini
ELVSS

FIG. 10

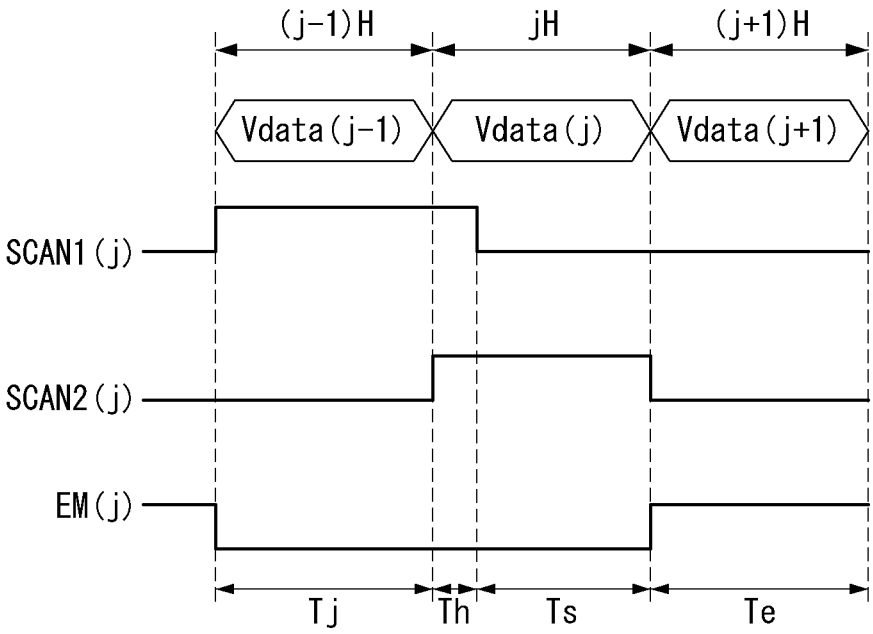

(j-1)H
jH
(j+1)H
Vdata(j-1)
Vdata(j)
Vdata(j+1)
SCAN1(j)
SCAN2(j)
EM(j)
Tj
Th
Ts
Te

FIG. 11

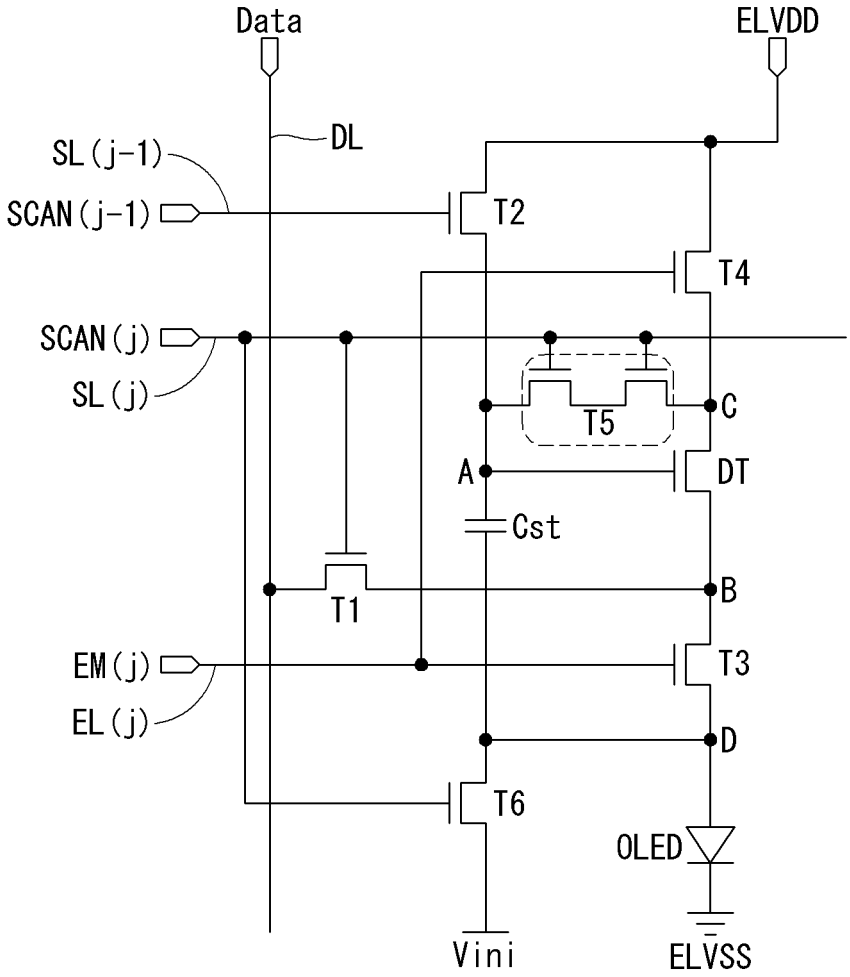

Data
ELVDD
DL
SL(j-1)
SCAN(j-1)
T2
T4
SCAN(j)
SL(j)
T5
C
A
DT
Cst
T1
B
EM(j)
EL(j)
T3
D
T6
OLED
Vini
ELVSS

FIG. 12

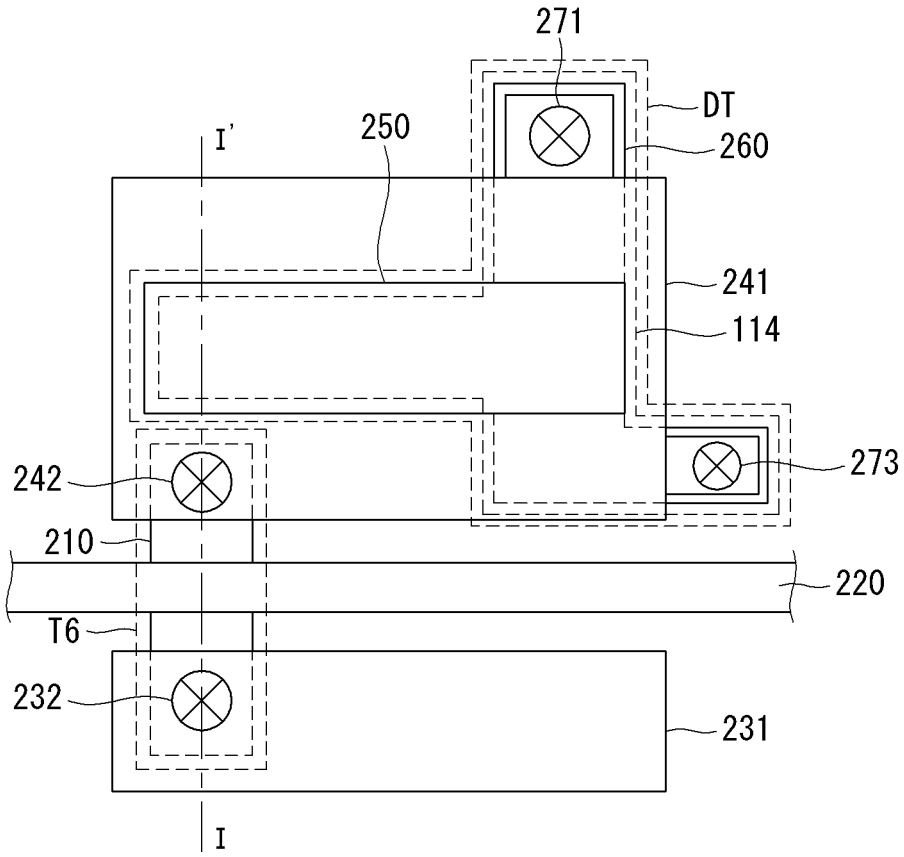
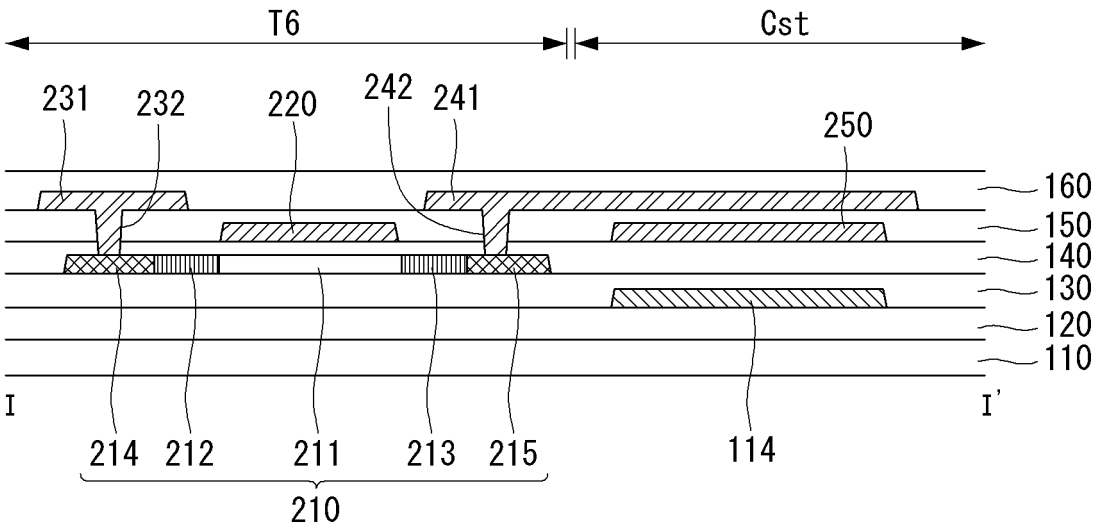


FIG. 13


T6
Cst
231
232
220
242
241
250
160
150
140
130
120
110
I
I'
214
212
211
213
215
114
210

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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- US 20150317931 A1 **[0006]**
- CN 104123910 A **[0006]**
- US 20120287025 A1 **[0007]**

专利名称(译)	有机发光显示器及其电路		
公开(公告)号	EP3098805B1	公开(公告)日	2018-07-25
申请号	EP2016171308	申请日	2016-05-25
[标]申请(专利权)人(译)	乐金显示有限公司		
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当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	JUNG SANGHOON KIM JUNGCHUL KWON JUNYOUNG SUK JUNGYOUP SUNG KIYOUNG		
发明人	JUNG, SANGHOON KIM, JUNGCHUL KWON, JUNYOUNG SUK, JUNGYOUP SUNG, KIYOUNG		
IPC分类号	G09G3/3233		
CPC分类号	G09G3/3233 G09G3/2085 G09G3/3266 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2310/0216 G09G2310/0264 G09G2320/045 G09G2330/021 G09G2330/028		
优先权	1020160053638 2016-04-30 KR 1020150152672 2015-10-30 KR 1020150075330 2015-05-28 KR		
其他公开文献	EP3098805A1		
外部链接	Espacenet		

摘要(译)

有机发光显示器包括：显示面板（10），具有多个像素（PXL）;栅极驱动电路（13），用于驱动显示面板（10）上的扫描线（SL1，..... SL（n））和发光线（EL1，...，EL（n））;以及驱动显示面板（10）上的数据线（DL）的数据驱动电路（12），布置在第n行（n为自然数）的每个像素（PXL）包括：驱动晶体管（DT）具有连接到节点A的栅电极，连接到节点B的源电极，以及连接到节点C的漏电极，以及控制施加到有机发光二极管（OLED）的驱动电流的驱动晶体管（DT）;第一个晶体管（T1）就是连接在数据线（DL）和节点B之间;第二晶体管（T2），连接在节点A和高电平驱动电压输入端之间;第三晶体管（T3），连接到节点B和有机发光二极管（OLED）;第四晶体管（T4），连接到节点C和高电平驱动电压输入端;第五晶体管（T5），连接到节点A和节点C;第六晶体管（T6），连接在节点D和初始电压输入端之间，节点D位于第三晶体管（T3）和有机发光二极管（OLED）之间;和一个连接到节点A和电容器的电容器（Cst）节点D.

[Equation 1]

$$I_{oled} = (k/2)(Vgs-Vth)^2=(k/2)(Vdata-Vini)^2$$