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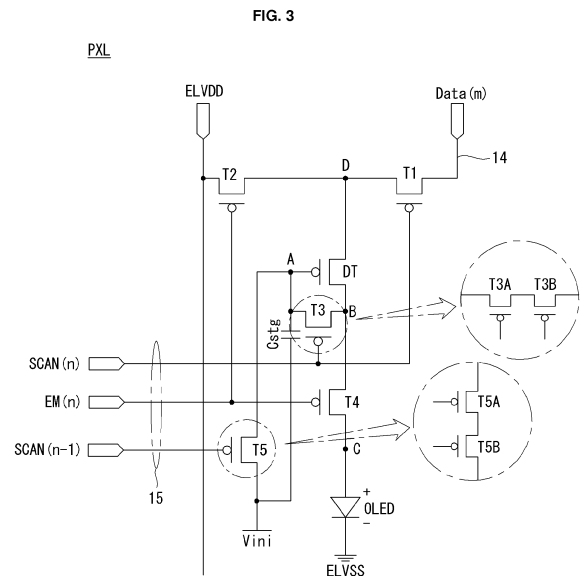
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(54) **ORGANIC LIGHT EMITTING DISPLAY**

(57) An organic light emitting display comprises a display panel (10) having a plurality of pixels (PXL); a gate drive circuit (13) that drives scan lines and emission lines on the display panel (10); and a data drive circuit (12) that drives data lines (14) on the display panel (10), each of the pixels (PXL) arranged in an nth row (n is a natural number) comprising: an organic light emitting diode (OLED) having an anode connected to a node C and a cathode connected to a low-level driving voltage input terminal; a driving transistor (DT) having a gate electrode connected to a node A, a source electrode connected to a node D, and a drain electrode connected to a node B, and the driving transistor (DT) controlling a driving current applied to the organic light emitting diode (OLED); a first transistor (T1) that is connected between a data line (14) and the node D; a second transistor (T2) that is connected between the node D and a high-level driving voltage input terminal; a third transistor (T3) that is connected to the node A and the node B; a fourth transistor (T4) that is connected to the node B and the node C; a fifth transistor (T5) that is connected between the node A and an initial voltage input terminal; and a capacitor (Cstg) that is connected between the node A and the initial voltage input terminal.



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DescriptionBACKGROUND5 Field

[0001] The present disclosure relates to an active-matrix organic light emitting display.

10 Discussion of the Related Art

[0002] An active-matrix organic light emitting display comprises self-luminous organic light emitting diodes OLED, and has the advantages of fast response time, high luminous efficiency, high luminance, and wide viewing angle.

15 **[0003]** An organic light emitting diode OLED, which is a self-luminous device, has the structure shown in FIG. 1. The organic light emitting diode OLED comprises an anode and a cathode, and organic compound layers formed between the anode and the cathode. The organic compound layers comprise a hole transport layer HTL, an emission layer EML, and an electron transport layer ETL. When an operating voltage is applied to the anode and the cathode, a hole (indicated by "+" in FIG. 1) passing through the hole transport layer HTL and an electron (indicated by "-" in FIG. 1) passing through the electron transport layer ETL move to the emission layer EML, and forming an exciton. As a result, the emission layer EML generates visible light.

20 **[0004]** Despite their high contrast ratio and color reproduction, organic light emitting displays may have a leakage current due to unexpected light emission from organic light emitting diodes during operation of a compensation circuit, resulting in a reduction in the efficiency of the organic light emitting diodes.

25 SUMMARY

[0005] In an exemplary embodiment of this disclosure, an organic light emitting display comprises a display panel having a plurality of pixels, a gate drive circuit that drives scan lines and emission lines on the display panel, and a data drive circuit that drives data lines on the display panel. Each of the pixels is arranged in an nth row (n is a natural number) includes an organic light emitting diode having an anode connected to a node C and a cathode connected to a low-level driving voltage input terminal, a driving transistor having a gate electrode connected to a node A, a source electrode connected to a node D, and a drain electrode connected to a node B, the driving transistor controlling a driving current applied to the organic light emitting diode, a first transistor that is connected between a data line and the node D, a second transistor that is connected between the node D and a high-level driving voltage input terminal, a third transistor that is connected to the node A and the node B, a fourth transistor that is connected to the node B and the node C, a fifth transistor that is connected between the node A and an initial voltage input terminal, and a capacitor that is connected between the node A and the initial voltage input terminal.

30 **[0006]** In one or more embodiments, one frame comprises an initial period in which the node A is initialized, a sampling period in which a threshold voltage of the driving transistor is sampled and stored at the node A, an emission period in which a source-gate voltage of the driving transistor is programmed to have the sampled threshold voltage, and the organic light emitting diode emits light by a driving current corresponding to the programmed source-gate voltage, wherein a gate electrode of the fifth transistor is connected to an (n-1)th scan line to which an (n-1)th scan signal is applied, a gate electrode of the first transistor and a gate electrode of the third transistor are connected to an nth scan line to which an nth scan signal is applied, and a gate electrode of the second transistor and a gate electrode of the fourth transistor are connected to an nth emission line to which an nth emission signal is applied, and in the initial period, the (n-1)th scan signal is applied at an ON level, and the nth scan signal and the nth emission signal are applied at an OFF level, in the sampling period, the nth scan signal is applied at the ON level, and the (n-1)th scan signal and the nth emission signal are applied at the OFF level, and in the emission period, the nth emission signal is applied at the ON level, and the (n-1)th scan signal and the nth scan signal are applied at the OFF level.

45 **[0007]** In one or more embodiments, the organic light emitting display further comprises a sixth transistor connected between the initial voltage input terminal and the node C.

50 **[0008]** In one or more embodiments, one frame comprises an initial period in which the node A and the node C are initialized, a sampling period in which a threshold voltage of the driving transistor is sampled and stored at the node A, an emission period in which a source-gate voltage of the driving transistor is programmed to have the sampled threshold voltage, and the organic light emitting diode emits light by a driving current corresponding to the programmed source-gate voltage, wherein a gate electrode of the fifth transistor and a gate electrode of the sixth transistor are connected to an (n-1)th scan line to which an (n-1)th scan signal SCAN(n-1) is applied, a gate electrode of the first transistor and a gate electrode of the third transistor are connected to an nth scan line to which an nth scan signal is applied, and a gate electrode of the second transistor and a gate electrode of the fourth transistor are connected to an nth emission

line to which an n th emission signal is applied, and in the initial period, the $(n-1)$ th scan signal is applied at an ON level, and the n th scan signal and the n th emission signal are applied at an OFF level, in the sampling period, the n th scan signal is applied at the ON level, and the $(n-1)$ th scan signal and the n th emission signal are applied at the OFF level, and in the emission period, the n th emission signal is applied at the ON level, and the $(n-1)$ th scan signal and the n th scan signal are applied at the OFF level.

[0009] In one or more embodiments, one frame comprises an initial period in which the node A and the node C are initialized, a sampling period in which a threshold voltage of the driving transistor is sampled and stored at the node A, an emission period in which a source-gate voltage of the driving transistor is programmed to have the sampled threshold voltage, and the organic light emitting diode emits light by a driving current corresponding to the programmed source-gate voltage, wherein a gate electrode of the fifth transistor is connected to an $(n-1)$ th scan line to which an $(n-1)$ th scan signal SCAN($n-1$) is applied, a gate electrode of the first transistor, a gate electrode of the third transistor, and a gate electrode of the sixth transistor are connected to an n th scan line to which an n th scan signal is applied, and a gate electrode of the second transistor and a gate electrode of the fourth transistor are connected to an n th emission line to which an n th emission signal is applied, and in the initial period, the $(n-1)$ th scan signal is applied at an ON level, and the n th scan signal and the n th emission signal are applied at an OFF level, in the sampling period, the n th scan signal is applied at the ON level, and the $(n-1)$ th scan signal and the n th emission signal are applied at the OFF level, and in the emission period, the n th emission signal is applied at the ON level, and the $(n-1)$ th scan signal and the n th scan signal are applied at the OFF level.

[0010] In one or more embodiments, the initial period is included in an $(n-1)$ th horizontal period, and the sampling period is included in an n th horizontal period.

[0011] In one or more embodiments, in each pixel, each transistor whose source electrode or drain electrode is connected to one electrode of the capacitor comprises at least two series-connected transistors, which are switched on by a same control signal.

[0012] In one or more embodiments, a first electrode of the capacitor is positioned between insulating layers that is disposed between a semiconductor layer and a source electrode of the fifth transistor, and the first electrode of the capacitor is connected via a contact hole to a drain electrode of the fifth transistor and to a drain electrode of the sixth transistor.

[0013] In one or more embodiments, the organic light emitting display further comprises a metal layer under a semiconductor layer of the driving transistor.

[0014] In one or more embodiments, a first electrode of the capacitor that receives an initial voltage from the initial voltage input terminal is disposed corresponding to the gate electrode of the driving transistor.

[0015] In one or more embodiments, a first electrode of the capacitor that receives an initial voltage from the initial voltage input terminal is disposed in an area corresponding to a semiconductor layer of the third transistor that operates during a sampling period.

[0016] In one or more embodiments, a first electrode of the capacitor is the gate electrode of the driving transistor connected to the node A, a second electrode of the capacitor corresponds to an electrode connected to the initial voltage input terminal, and the second electrode is not connected to a high-level driving voltage input terminal and is connected to the initial voltage input terminal.

[0017] In another exemplary embodiment of this disclosure an organic light emitting display comprises a display panel having a plurality of pixels, a gate drive circuit that drives scan lines and emission lines on the display panel, and a data drive circuit that drives data lines on the display panel. Each of the pixels is arranged in an n th row (n is a natural number) includes an organic light emitting diode having an anode connected to a node C and a cathode connected to a low-level driving voltage input terminal, a driving transistor having a gate electrode connected to a node A, a source electrode connected to a high-level driving voltage input terminal, and a drain electrode connected to a node B, the driving transistor controlling a driving current applied to the organic light emitting diode, a first transistor that is connected between a data line and a node D, a second transistor that is connected to the node A and the node B, a third transistor that is connected between the node D and an initial voltage input terminal, a fourth transistor that is connected to the node B and the node C, a fifth transistor that is connected between the node A and the initial voltage input terminal, a sixth transistor that is connected between the initial voltage input terminal and the node C, and a capacitor that is connected to the node A and the node D.

[0018] In one or more embodiments, one frame comprises an initial period in which the node A and the node C are initialized, a sampling period in which a threshold voltage of the driving transistor is sampled and stored at the node A, an emission period in which a source-gate voltage of the driving transistor is programmed to have the sampled threshold voltage, and the organic light emitting diode emits light by a driving current corresponding to the programmed source-gate voltage, wherein a gate electrode of the fifth transistor and a gate electrode of the sixth transistor are connected to an $(n-1)$ th scan line to which an $(n-1)$ th scan signal SCAN($n-1$) is applied, a gate electrode of the first transistor and a gate electrode of the second transistor are connected to an n th scan line to which an n th scan signal is applied, and a gate electrode of the third transistor and a gate electrode of the fourth transistor are connected to an n th emission line

to which an n th emission signal is applied, and in the initial period, the $(n-1)$ th scan signal is applied at an ON level, and the n th scan signal and the n th emission signal are applied at an OFF level, in the sampling period, the n th scan signal is applied at the ON level, and the $(n-1)$ th scan signal and the n th emission signal are applied at the OFF level, and in the emission period, the n th emission signal is applied at the ON level, and the $(n-1)$ th scan signal and the n th scan signal are applied at the OFF level.

[0019] In one or more embodiments, the initial period is included in an $(n-1)$ th horizontal period, and the sampling period is included in an n th horizontal period. and the second transistor comprises at least two series-connected transistors, which are switched on by a same control signal.

[0020] In one or more embodiments, the capacitor (Cstg) connected between an initial voltage input terminal and the third transistor, and a gate electrode of the fifth transistor for initializing the driving transistor of the n th pixel is connected to a scan line in a $(n-1)$ th pixel.

[0021] In one or more embodiments, the capacitor is connected to receive the initial voltage, rather than a high-level driving voltage, so that the number of contact holes is minimized.

[0022] In one or more embodiments, an electrode of the capacitor) connected to the initial voltage input terminal, and a contact hole for connecting a drain electrode or a source electrode of the fifth transistor and the initial voltage input terminal. A drain electrode or a source electrode of the sixth transistor for providing a negative voltage is connected to at least one electrode of the organic light emitting diode via the contact hole.

[0023] In one or more embodiments, the capacitor comprises a first electrode that receives an initial voltage, a second electrode connected to the driving transistor. The first electrode is larger in size than the second electrode.

[0024] In one or more embodiments, a first electrode of the capacitor is disposed in an area corresponding to a semiconductor layer of the third transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The accompanying drawings, which are included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this specification, illustrate embodiments of the disclosure and together with the description serve to explain the principles of the disclosure. In the drawings:

FIG. 1 is a view showing an organic light emitting diode and the principle of light emission by the organic light emitting diode;

FIG. 2 is a view showing an organic light emitting display according to an exemplary embodiment of the present disclosure;

FIG. 3 is an equivalent circuit diagram of a pixel structure according to an exemplary embodiment of the present disclosure;

FIG. 4 is a waveform diagram showing data signals and gate signals which are applied to the pixel of FIG. 3;

FIGS. 5A, 5B, and 5C are equivalent circuit diagrams of the pixel corresponding to the initial period, sampling period, and emission period of FIG. 4;

FIG. 6 is a view showing the voltages for nodes A, B, and C of the pixel during the initial period, sampling period, and emission period;

FIG. 7 is an equivalent circuit diagram showing a modification of the pixel structure of FIG. 3;

FIG. 8 is a waveform diagram showing data signals and gate signals which are applied to the pixel of FIG. 7;

FIGS. 9A, 9B, and 9C are equivalent circuit diagrams of the pixel corresponding to the initial period, sampling period, and emission period of FIG. 7;

FIG. 10 is a view showing the voltages for nodes A, B, and C of the pixel during the initial period, sampling period, and emission period;

FIG. 11 is an equivalent circuit diagram showing a modification of the pixel structure of FIG. 7;

FIG. 12 is an equivalent circuit diagram showing a modification of the pixel structure of FIG. 3;

FIG. 13 is a waveform diagram showing data signals and gate signals which are applied to the pixel of FIG. 12;

FIGS. 14A, 14B, and 14C are equivalent circuit diagrams of the pixel corresponding to the initial period, sampling period, and emission period of FIG. 12;

FIG. 15 is a waveform diagram showing data signals and gate signals which are applied to the pixel of FIG. 12;

FIGS. 16 to 18 are views showing various examples of implementing a scan driver's shift registers and inverters of an emission driver in a gate drive circuit;

FIG. 19 is a view showing an array of a region for forming a capacitor in a pixel according to an exemplary embodiment of the present disclosure;

FIG. 20 is a cross-sectional view taken along line I-I' of FIG. 19; and

FIG. 21 is a view showing an array of a region for forming a capacitor according to a comparative example.

DETAILED DESCRIPTION

5 [0026] The various aspects and features of the present disclosure and methods of accomplishing the same may be understood more readily by reference to the following detailed descriptions of exemplary embodiments and the accompanying drawings. The present disclosure may, however, be embodied in many different forms and should not be construed as being limited to the exemplary embodiments set forth herein. Rather, these exemplary embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concept of the present disclosure to those skilled in the art, and the present disclosure is defined by the appended claims.

10 [0027] The shapes, sizes, proportions, angles, numbers, etc. shown in the figures to describe the exemplary embodiments of the present disclosure are merely examples and not limited to those shown in the figures. Like reference numerals denote like elements throughout the specification. In describing the present disclosure, detailed descriptions of related well-known technologies will be omitted to avoid unnecessary obscuring of the present disclosure. When the terms 'comprise', 'have', 'include' and the like are used, other parts may be added as long as the term 'only' is not used. The singular forms may be interpreted as the plural forms unless explicitly stated.

15 [0028] The elements may be interpreted to include an error margin even if not explicitly stated.

[0029] When the position relation between two parts is described using the terms 'on', 'over', 'under', 'next to' and the like, one or more parts may be positioned between the two parts as long as the term 'immediately' or 'directly' is not used.

[0030] When the temporal relationship between two events is described using the terms 'after', 'following', 'next', 'before' and the like, the two events may not occur in succession as long as the term 'immediately' or 'directly' is not used.

20 [0031] It will be understood that, although the terms first, second, etc., may be used to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, a first element discussed below could be termed a second element without departing from the technical spirit of the present disclosure.

25 [0032] The features of various exemplary embodiments of the present disclosure may be combined with one another either partly or wholly, and may technically interact or work together in various ways. The exemplary embodiments may be carried out independently or in combination with one another.

[0033] Hereinafter, exemplary embodiments of the present disclosure will be described in detail with reference to the accompanying drawings. The same reference numerals refer to substantially the same elements throughout the specification. In the following description, when it is deemed that detailed description of well-known functions or configurations related to the present invention may unnecessarily obscure the subject matter of the present invention, the detailed description thereof will be omitted.

[0034] Although the exemplary embodiments disclose that all transistors constituting each pixel are P-type transistors, the technical idea of this disclosure is not limited thereto and the transistors may be N-type, or a combination of P-type transistors and N-type transistors.

35 [0035] A pixel structure for the aforementioned organic light emitting display may comprise a driving transistor, a capacitor, and a plurality of transistors. Initial, sampling, and emission steps are required to drive the organic light emitting diode.

[0036] Initializing may be done by applying an initial voltage to a gate terminal of the driving transistor and an anode terminal of the organic light emitting diode. The gate terminal of the driving transistor is initialized to an initial voltage Vini. Hereupon, an unwanted electric current may flow to the organic light emitting diode, thereby reducing the efficiency of the organic light emitting diode. Also, an excessive electric current may flow instantaneously to an input terminal of the initial voltage (Vini), causing a display quality defect and damage to circuit components due to an instantaneous drop in the initial voltage Vini.

40 [0037] Constant electric current flowing from the driving transistor to the organic light emitting diode can ensure reliability. However, the characteristics of a semiconductor layer of the driving transistor change over time. That is, the threshold voltage of the driving transistor can be changed to a negative or positive voltage. Accordingly, a plurality of transistors and a capacitor need to be arranged within the pixel in order to compensate for a change in the threshold voltage of the driving thin film transistor and allow the organic light emitting diode to emit light with a target luminance. To compensate for changes in the characteristics of the semiconductor layer of the driving transistor, more transistors are arranged in a limited pixel area and their arrangement becomes complex, thus it becomes difficult to simplify a pixel structure and a layout of the pixel for a given pixel area.

[0038] Moreover, more pixels are required for light emission, in order to make high-resolution displays. For this reason, the length of 1 horizontal period (H) is shortened and thus the sampling period also is shortened. The shortened sampling period may lower the accuracy of threshold voltage compensation of the driving transistor.

55 [0039] Therefore, one aspect of this disclosure is to provide an organic light emitting display that blocks an electric current flowing to the organic light emitting diode at times other than an emission period and ensures the accuracy of threshold voltage compensation of the driving transistor.

[0040] Another aspect of this disclosure is to provide an organic light emitting display which ensures design margin

within a pixel area by reducing the number of contact holes for connecting a plurality of transistors and a capacitor.

[0041] Another aspect of this disclosure is to provide an organic light emitting display which can improve the accuracy of threshold voltage compensation of the driving transistor by ensuring a sufficient sampling period.

[0042] Another aspect of this disclosure is to provide an organic light emitting display which prevents the effect of a mobile charge on a semiconductor layer of the driving transistor.

[0043] The aspects of the present disclosure are not limited to the above-mentioned aspects, and other aspects will be apparent to those skilled in the art in the following description

[0044] Hereinafter, exemplary embodiments of the present disclosure will be described in detail with reference to FIGS. 2 to 21.

[0045] FIG. 2 is a view showing an organic light emitting display according to an exemplary embodiment of the present disclosure.

[0046] Referring to FIG. 2, an organic light emitting display according to an exemplary embodiment of the present disclosure comprises a display panel 10 with pixels PXL, a data drive circuit 12 for driving data lines 14, a gate drive circuit 13 for driving gate lines 15, and a timing controller 11 for controlling the operation timings of the data drive circuit 12 and gate drive circuit 13.

[0047] A plurality of data lines 14 and a plurality of gate lines 15 intersect each other on the display panel 10, and the pixels PXL are arranged in a matrix at the intersections. Pixels PXL arranged on the same horizontal line constitute one pixel row. Pixels PXL arranged on one pixel row are connected to one gate line 15, and this gate line 15 may comprise at least one scan line and at least one emission line. That is, each pixel PXL may be connected to one data line 14, at least one scan line, and at least one emission line. The pixels PXL may commonly receive high-level driving voltage ELVDD and low-level driving voltage ELVSS and an initial voltage Vini from a power generator. The initial voltage Vini may be chosen from a range of voltages well lower than operating voltage of organic light emitting diodes OLED to prevent unnecessary light emission by the organic light emitting diodes OLED during an initial period and a sampling period. That is, the initial voltage Vini may be set equal to or lower than the low-level driving voltage ELVSS. Accordingly, by applying the initial voltage Vini, which is lower than the low-level driving voltage ELVSS, during the initial period, unnecessary light emission from the organic light emitting diodes OLED can be suppressed, resulting in an improvement in the lifetime of the organic light emitting diodes OLED.

[0048] The transistors comprising each pixel PXL may be implemented as oxide transistors having an oxide semiconductor layer. The oxide transistors are advantageous for the display panel 10 to have a large area, when electron mobility, process deviation, etc. are all taken into consideration. The oxide semiconductor layer may be formed of, but is not limited to, ITO (indium tin oxide), IZO (indium zinc oxide), IGZO (indium gallium zinc oxide), or ITZO (indium tin zinc oxide). The present disclosure is not limited to the oxide transistors, and the semiconductor layer of the transistors may be formed of amorphous silicon (a-Si), polycrystalline silicon (poly-Si), organic semiconductor, etc. Each individual pixel PXL comprises a plurality of transistors and capacitors to compensate for changes in the threshold voltage of a driving transistor. A pixel structure disclosed herein can compensate for changes in the threshold voltage of the driving transistor and ensure a sampling period for compensating the threshold voltage. This will be described later in detail with reference to FIGS. 3 to 21.

[0049] In each pixel PXL, each transistor whose source or drain electrode is connected to one electrode of the capacitor may comprise at least two series-connected transistors so as to suppress the effect of leakage current as much as possible. The at least two series-connected transistors are switched on by a same control signal. For example, the third transistor T3 may be designed as a double-gate transistor comprising T3A and T3B, as shown in FIG. 3, which are switched on by the same control signal and connected in series. Likewise, the fifth transistor T5 may be designed as a double-gate transistor comprising T5A and T5B which are switched on by the same control signal and connected in series. As used below, the term "a double-gate transistor" refers to a structure in which two transistors are connected in series with gate electrodes of the two transistors connected together.

[0050] As shown in FIG. 7, the sixth transistor T6, as well as the third transistor T3 and the fifth transistor T5, may be designed as a double-gate transistor comprising T6A and T6B. Also, as shown in FIG. 11, the second transistor T2, as well as the third transistor T3 and the fifth transistor T5, may be designed as a double-gate transistor comprising T2A and T2B. Also, as shown in FIG. 12, the second transistor T2 may be designed as a double-gate transistor comprising T2A and T2B.

[0051] That is, at least one of the transistors connected to the capacitor may comprise two series-connected transistors, so as to prevent distortion in luminescence intensity caused by leakage current.

[0052] Referring again to FIG. 2, the timing controller 11 re-aligns digital video data RGB input from an external source to match the resolution of the display panel 10 and supplies it to the data drive circuit 12. Also, the timing controller 11 generates a data control signal DDC for controlling the operation timing of the data drive circuit 12 and a gate control signal GDC for controlling the operation timing of the gate drive circuit 13, based on timing signals such as a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a dot clock signal DCLK, and a data enable signal DE.

[0053] The data drive circuit 12 converts the digital video data RGB input from the timing controller 11 to an analog data voltage based on the data control signal DDC.

[0054] The gate drive circuit 13 generates a scan signal and an emission signal based on the gate control signal GDC. The gate drive circuit 13 may comprise a scan driver and an emission driver. The scan driver may generate a scan signal and provide it to the scan lines on a line-sequential basis, in order to drive at least one scan line connected to each pixel row. The emission driver may generate an emission signal and provide it to the emission lines, in order to drive at least one emission line connected to each pixel row.

[0055] The gate drive circuit 13 may be formed directly in a non-display area of the display panel 10 according to the GIP (gate-driver In Panel) technology.

[0056] FIG. 3 is an equivalent circuit diagram of a pixel structure according to the present disclosure. FIG. 4 is a waveform diagram showing data signals and gate signals which are applied to the pixel of FIG. 3.

[0057] Referring to FIG. 3, each pixel PXL arranged in an n th row (n is a natural number) comprises an organic light emitting diode OLED, a driving transistor DT, a first transistor T1, a second transistor T2, a third transistor T3, a fourth transistor T4, a fifth transistor T5, and a capacitor Cstg.

[0058] The organic light emitting diode OLED emits light by a driving current supplied from the driving transistor DT. The organic light emitting diode OLED comprises multiple layers of organic compounds between an anode and a cathode. The organic compound layers may comprise at least one among a hole transfer layer, an electron transfer layer, and an emission layer EML. The hole transfer layer includes a layer that injects or transfers holes into the emission layer, for example, a hole injection layer HIL, a hole transport layer HTL, an electron blocking layer EBL, etc. The electron transfer layer includes a layer that injects or transfers electrons into the emission layer, for example, an electron transport layer ETL, an electron injection layer EIL, a hole blocking layer HBL, etc. The anode of the organic light emitting diode OLED is connected to a node C, and the cathode of the organic light emitting diode OLED is connected to an input terminal of the low-level driving voltage ELVSS.

[0059] The driving transistor DT controls an amount of driving current applied to the organic light emitting diode OLED based on its source-gate voltage V_{sg} . The gate electrode of the driving transistor DT is connected to a node A, its source electrode is connected to a node D, and its drain electrode is connected to a node B.

[0060] The first transistor T1 is connected between a data line 14 and the node D, and is turned on/off in response to an n th scan signal SCAN(n). The gate electrode of the first transistor T1 is connected to an n th first scan line to which the n th scan signal SCAN(n) is applied, the source electrode of the first transistor T1 is connected to the data line 14, and the drain electrode of the first transistor T1 is connected to the node D.

[0061] The second transistor T2 is connected between the node D and an input terminal of the high-level driving voltage ELVDD, and is turned on/off in response to an n th emission signal EM(n). The gate electrode of the second transistor T2 is connected to an n th emission line to which the n th emission signal EM(n) is applied, the source electrode of the second transistor T2 is connected to the input terminal of the high-level driving voltage ELVDD, and the drain electrode of the second transistor T2 is connected to the node D.

[0062] The third transistor T3 is connected to the node A and the node B, and is turned on/off in response to the n th scan signal SCAN(n). The gate electrode of the third transistor T3 is connected to the n th scan line to which the n th scan signal SCAN(n) is applied, the source electrode of the third transistor T3 is connected to the node A, and the drain electrode of the third transistor T3 is connected to the node B. Here, the third transistor T3 may be referred to as a sampling transistor.

[0063] The fourth transistor T4 is connected between the node B and the node C, and is turned on/off in response to the n th emission signal EM(n). The gate electrode of the fourth transistor T4 is connected to the n th emission line to which the n th emission signal EM(n) is applied, the source electrode of the fourth transistor T4 is connected to the node B, and the drain electrode of the fourth transistor T4 is connected to the node C. Here, the fourth transistor T4 may be referred to as an emission transistor.

[0064] The fifth transistor T5 is connected between the node A and an input terminal of the initial voltage V_{ini} , and is turned on/off in response to an ($n-1$)th scan signal SCAN($n-1$). The gate electrode of the fifth transistor T5 is connected to the ($n-1$)th first scan line to which the ($n-1$)th scan signal SCAN($n-1$) is applied, the source electrode of the fifth transistor T5 is connected to the node A, and the drain electrode of the fifth transistor T5 is connected to the input terminal of the initial voltage V_{ini} . Here, the fifth transistor T5 may be referred to as a first initial transistor.

[0065] The capacitor Cstg is connected between the node A and the input terminal of the initial voltage V_{ini} .

[0066] Referring to FIGS. 4 to 6, the operation of the pixel of FIG. 3 will be described. FIG. 4 is a waveform diagram showing data signals and gate signals which are applied to the pixel of FIG. 3. FIGS. 5A, 5B, and 5C are equivalent circuit diagrams of the pixel corresponding to the initial period, sampling period, and emission period of FIG. 4. FIG. 6 is a view showing the voltages for nodes A, B, and C of the pixel during the initial period, the sampling period, and the emission period.

[0067] As shown in FIG. 4, one frame may be divided into an initial period P_i in which the node A is initialized, a sampling period P_s in which the threshold voltage of the driving transistor DT is sampled and stored at the node A, an

emission period P_e in which the source-gate voltage of the driving transistor DT is programmed (or adjusted) according to the sampled threshold voltage, and the organic light emitting diode OLED emits light by a driving current corresponding to the programmed source-gate voltage. In FIG. 4, since an initial operation is performed during an $(n-1)$ th horizontal period H_{n-1} , an n th horizontal period H_n may be entirely spent on a sampling operation. This ensures a sufficient sampling period P_s , thus making it possible to sample the threshold voltage of the driving transistor more accurately. The Data $(m-1)$, Data (m) and Data $(m+1)$ refer to the $(m-1)$ th, (m) th, and $(m+1)$ th data signal respectively.

[0068] In FIG. 5A, the transistors that operate (are turned on) during the initial period P_i are indicated by the solid lines, and the transistors that do not operate (are turned off) during this period are indicated by the dotted lines. Referring to FIGS. 4 and 5A, the initial period P_i lasts for an $(n-1)$ th horizontal period H_{n-1} allocated for data writing in an $(n-1)$ th row. In the initial period P_i , the $(n-1)$ th scan signal SCAN $(n-1)$ is applied at low level, and the n th scan signal SCAN (n) and the n th emission signal EM (n) are applied at high level. Here, the low level is an ON level LON, and the high level is an OFF level LOFF. For convenience of explanation, the low level will be hereinafter referred to as an ON level and the high level as an OFF level.

[0069] In the initial period P_i , as the fifth transistor T5 is turned on in response to the $(n-1)$ th scan signal SCAN $(n-1)$, the node A is initialized to the initial voltage V_{ini} . Here, the fifth transistor T5 may be referred to as a first initial transistor. As the gate electrode of the first initial transistor T5 is connected to the $(n-1)$ th scan line to which the $(n-1)$ th scan signal SCAN $(n-1)$ is applied, a sufficient sampling period may be allowed to sample the threshold voltage V_{th} of the driving transistor DT, thus improving the accuracy of compensation of the threshold voltage V_{th} . By thus initializing the node A prior to the sampling operation, the sampling reliability can be improved, and unnecessary light emission by the organic light emitting diode OLED can be avoided. To this end, the initial voltage V_{ini} may be chosen from a range of voltages well lower than operating voltage of the organic light emitting diode OLED, and the initial voltage V_{ini} may be set equal to or lower than the low-level driving voltage ELVSS. Also, the node D holds the data voltage $V_{data}(n)$ of the previous frame during the initial period P_i .

[0070] In FIG. 5B, the transistors that operate during the sampling period P_s are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. Referring to FIGS. 4 and 5B, the sampling period P_s lasts for an n th horizontal period H_n allocated for data writing in an n th row. In the sampling period P_s , the n th scan signal SCAN (N) is applied at an ON level, and the $(n-1)$ th scan signal SCAN $(n-1)$ and the n th emission signal EM (n) are applied at an OFF level. In the sampling period P_s , as the first and third transistors T1 and T3 turn on in response to the n th scan signal SCAN (n) , the driving transistor DT is diode-connected (that is, the gate electrode and the drain electrode are shorted so that the driving transistor DT acts as a diode), and the data voltage $V_{data}(n)$ is applied to the node D.

[0071] In the sampling period P_s , a current I_{ds} flows between the source electrode and drain electrode of the driving transistor DT, and this current I_{ds} causes the voltage at the node A to rise from the initial voltage V_{ini} to $V_{data}(n)-V_{th}$, obtained by subtracting the threshold voltage of the driving transistor DT from the data voltage $V_{data}(n)$. The initial voltage V_{ini} is equal to or lower than the low-level driving voltage ELVSS. As the voltage at the node A, which is connected to the gate electrode of the driving transistor DT, is adjusted according to the threshold voltage V_{th} of the driving transistor DT, a driving current may be generated in a subsequent emission period P_e , irrespective of the threshold voltage V_{th} of the driving transistor DT.

[0072] In FIG. 5C, the transistors that operate during the emission period P_e are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. Referring to FIGS. 4 and 5C, the emission period P_e corresponds to the remaining portion of one frame, excluding the initial period P_i and the sampling period P_s . In the emission period P_e , the n th emission signal EM (n) is applied at an ON level, and the $(n-1)$ th scan signal SCAN $(n-1)$ and the n th scan signal SCAN (n) are applied at an OFF level.

[0073] In the emission period P_e , as the second transistor T2 is turned on in response to the n th emission signal EM (n) , the high-level driving voltage ELVDD is connected to the source electrode of the driving transistor DT. Also, as the fourth transistor T4 is turned on in response to the n th emission signal EM (n) , the voltage across the nodes B and C becomes substantially equal to the operating voltage V_{oled} of the organic light emitting diode OLED.

[0074] The fourth transistor T4 is connected to the anode of the organic light emitting diode OLED and is turned off during the initial period P_i and the sampling period P_s , but not during the emission period P_e , thus preventing a leakage current flowing through the organic light emitting diode OLED at times other than the emission period P_e . Here, the fourth transistor T4 may be referred to as an emission transistor.

[0075] The relational expression for the driving current I_{oled} flowing through the organic light emitting diode OLED during the emission period P_e is represented by the following Equation 1. The organic light emitting diode OLED emits light by a driving current, thereby displaying a desired gray level.

[0095] [Equation 1]

$$\begin{aligned}
 \text{[0096]} \quad I_{\text{oled}} &= k/2(V_{\text{s}} - V_{\text{th}})^2 = k/2(V_{\text{s}} - V_{\text{g}} - V_{\text{th}})^2 = k/2(V_{\text{DD}} - V_{\text{data}} + V_{\text{th}} - V_{\text{th}})^2 = \\
 &k/2(V_{\text{DD}} - V_{\text{data}})^2
 \end{aligned}$$

where $k/2$ indicates a proportional constant determined by the electron mobility, parasitic capacitance, and channel capacity of the driving transistor DT.

[0076] The mathematical expression for the driving current I_{oled} is $k/2(V_{\text{s}} - V_{\text{th}})^2$. V_{s} , which is programmed in the emission period P_{e} , is already adjusted according to the threshold voltage component V_{th} of the driving transistor DT. Thus, the threshold voltage component V_{th} of the driving transistor DT does not affect the driving current I_{oled} according to the relational expression, as shown in Equation 1. This minimizes the effect of a change in threshold voltage V_{th} on the driving current I_{oled} .

[0077] FIG. 6 shows a table of voltages that are applied to the nodes A, B, and C during the initial, sampling, and emission periods P_{i} , P_{s} , and P_{e} explained in FIGS. 5A to 5C. After passing through the sampling period P_{s} , a voltage of the node A is adjusted according to the threshold voltage V_{th} of the driving transistor DT, and when the organic light emitting diode OLED emits light in the emission period P_{e} , the driving current I_{oled} of the driving transistor DT allows for displaying a desired gray level, irrespective of the threshold voltage V_{th} of the driving transistor DT.

[0078] FIG. 7 is an equivalent circuit diagram showing a modification embodiment of the pixel structure of FIG. 3. FIG. 8 is a waveform diagram showing data signals and gate signals which are applied to the pixel of FIG. 7. FIGS. 9A, 9B, and 9C are equivalent circuit diagrams of the pixel corresponding to an initial period, a sampling period, and an emission period of FIG. 7. FIG. 10 is a view showing the voltages for nodes A, B, and C of the pixel during the initial period, the sampling period, and the emission period.

[0079] The pixel PXL of FIG. 7 further comprises a sixth transistor T6, in addition to the elements of the pixel PXL of FIG. 3. In the pixel PXL of FIG. 7, the sixth transistor T6 is connected between the input terminal of the initial voltage V_{ini} and the node C. A gate electrode of the sixth transistor T6 is connected to an $(n-1)$ th first scan line to which the $(n-1)$ th scan signal SCAN(N-1) is applied, a source electrode of the sixth transistor T6 is connected to the node C, and a drain electrode of the sixth transistor T6 is connected to the input terminal of the initial voltage V_{ini} . By adding the sixth transistor T6 as shown in FIG. 7, the voltage at the node C can be fixed, thereby improving the sampling accuracy. Accordingly, the stability of circuit operation can be improved. Here, the sixth transistor T6 may be referred to as a second initial transistor.

[0080] All the other elements of FIG. 7 except the sixth transistor T6 are substantially identical to those explained with reference to FIG. 3.

[0081] A description of how the pixel of FIG. 7 works will be made with reference to FIGS. 7 to 10. FIG. 8 is a waveform diagram showing data signals and gate signals which are applied to the pixel of FIG. 7. FIGS. 9A, 9B, and 9C are equivalent circuit diagrams of the pixel corresponding to the initial period, the sampling period, and the emission period of FIG. 7. FIG. 10 is a view showing the voltages for nodes A, B, and C of the pixel during the initial period, the sampling period, and the emission period.

[0082] As shown in FIG. 8, one frame may be divided into an initial period P_{i} in which the node A and the node C are initialized, a sampling period P_{s} in which the threshold voltage of the driving transistor DT is sampled and stored at the node A, an emission period P_{e} in which the source-gate voltage of the driving transistor DT is programmed (or adjusted) according to the sampled threshold voltage, and the organic light emitting diode OLED emits light by a driving current corresponding to the programmed source-gate voltage. In FIG. 8, since an initial operation is performed during an $(n-1)$ th horizontal period H_{n-1} , an n th horizontal period H_n may be entirely spent on a sampling operation. This ensures a sufficient sampling period P_{s} , thus making it possible to sample the threshold voltage of the driving transistor more accurately.

[0083] In FIG. 9A, the transistors that operate during the initial period P_{i} are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. Referring to FIGS. 8 and 9A, in the initial period P_{i} , the $(n-1)$ th scan signal SCAN($n-1$) is applied at an ON level, and the n th scan signal SCAN(n) and the n th emission signal EM(n) are applied at an OFF level. In the initial period P_{i} , as the fifth and sixth transistors T5 and T6 turn on in response to the $(n-1)$ th scan signal SCAN($n-1$), the node A and the node C are initialized to the initial voltage V_{ini} . As the gate electrodes of the fifth and sixth transistors T5 and T6 are connected to the $(n-1)$ th scan line to which the $(n-1)$ th scan signal SCAN($n-1$) is applied, a sufficient sampling period may be allowed to sample the threshold voltage V_{th} of the driving transistor DT, thus improving the accuracy of compensation of the threshold voltage V_{th} . In other words, by initializing the node A and the node C prior to the sampling operation, the sampling reliability can be improved, and unnecessary light emission by the organic light emitting diode OLED can be avoided.

[0084] In FIG. 9B, the transistors that operate during the sampling period P_s are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. Referring to FIGS. 8 and 9B, in the sampling period P_s , the n th scan signal $SCAN(N)$ is applied at an ON level, and the $(n-1)$ th scan signal $SCAN(n-1)$ and the n th emission signal $EM(n)$ are applied at an OFF level. In the sampling period P_s , as the first and third transistors T1 and T3 turn on in response to the n th scan signal $SCAN(n)$, the driving transistor DT is diode-connected (that is, the gate electrode and the drain electrode are shorted so that the driving transistor DT acts as a diode), and the data voltage $V_{data}(n)$ is applied to the node D.

[0085] Accordingly, in the sampling period P_s , a current I_{ds} flows between the source electrode and drain electrode of the driving transistor DT, and this current I_{ds} causes the voltage at the node A to rise from the initial voltage V_{ini} to $V_{data}(n)-V_{th}$, obtained by subtracting the threshold voltage of the driving transistor DT from the data voltage $V_{data}(n)$. The initial voltage V_{ini} is equal to or lower than the low-level driving voltage $ELVSS$. As the voltage at the node A, which is connected to the gate electrode of the driving transistor DT, is adjusted according to the threshold voltage V_{th} of the driving transistor DT, a driving current may be generated in a subsequent emission period P_e , irrespective of the threshold voltage V_{th} of the driving transistor DT.

[0086] In FIG. 9C, the transistors that operate during the emission period P_e are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. Referring to FIGS. 8 and 9C, in the emission period P_e , the n th emission signal $EM(n)$ is applied at an ON level, and the $(n-1)$ th scan signal $SCAN(n-1)$ and the n th scan signal $SCAN(n)$ are applied at an OFF level. In the emission period P_e , as the second transistor T2 is turned on in response to the n th emission signal $EM(n)$, the high-level driving voltage $ELVDD$ is connected to the source electrode of the driving transistor DT. Also, as the fourth transistor T4 is turned on in response to the n th emission signal $EM(n)$, the voltage across the nodes B and C becomes substantially equal to the operating voltage V_{oled} of the organic light emitting diode OLED.

[0087] The fourth transistor T4 is connected to the anode of the organic light emitting diode OLED and is turned off during the initial period P_i and the sampling period P_s , but not during the emission period P_e , thus preventing a leakage current flowing through the organic light emitting diode OLED at times other than the emission period P_e . The relational expression for the driving current I_{oled} flowing through the organic light emitting diode OLED during the emission period P_e is represented by the following Equation 2. The organic light emitting diode OLED emits light according to a driving current, thereby displaying a desired gray level.

[00110] [Equation 2]

$$I_{oled} = k/2(V_{sg}-V_{th})^2 = k/2((V_s-V_g)-V_{th})^2 = k/2((V_{DD}-V_{data}+V_{th}) - V_{th})^2 = k/2(V_{DD}-V_{data})^2$$

where $k/2$ indicates a proportional constant determined by the electron mobility, parasitic capacitance, and channel capacity of the driving transistor DT.

[0088] The mathematical expression for the driving current I_{oled} is $k/2(V_{sg}-V_{th})^2$. V_{sg} , which is programmed in the emission period P_e , is already adjusted according to the threshold voltage V_{th} of the driving transistor DT. Thus, the threshold voltage V_{th} of the driving transistor DT does not affect the driving current I_{oled} according to the relational expression, as shown in Equation 2. This minimizes the effect of a change in threshold voltage V_{th} on the driving current I_{oled} .

[0089] FIG. 10 shows a table of voltages that are applied to the nodes A, B, and C during the initial, sampling, and emission periods P_i , P_s , and P_e explained in FIGS. 9A to 9C. After the sampling period P_s , a voltage at the node A is adjusted according to the threshold voltage V_{th} of the driving transistor DT, and when the organic light emitting diode OLED emits light in the emission period P_e , the driving current I_{oled} of the driving transistor DT allows for displaying a desired gray level, irrespective of the threshold voltage V_{th} of the driving transistor DT.

[0090] FIG. 11 is an equivalent circuit diagram showing a modification embodiment of the pixel structure of FIG. 7. FIG. 11 shows a modification of the connection relationship among the second transistor T2, third transistor T3, and fifth transistor T5 shown in FIG. 7.

[0091] The driving transistor DT controls an amount of the driving current applied to the organic light emitting diode OLED based on its source-gate voltage V_{sg} . The gate electrode of the driving transistor DT is connected to a node A, the source electrode of the driving transistor DT is connected to a node D, and the drain electrode of the driving transistor DT is connected to a node B.

[0092] The first transistor T1 is connected to a data line 14 and the node D, and is turned on/off in response to an n th scan signal $SCAN(n)$. The gate electrode of the first transistor T1 is connected to an n th scan line to which the n th scan

signal SCAN(n) is applied, the source electrode of the first transistor T1 is connected to the data line 14, and the drain electrode of the first transistor T1 is connected to the node D.

[0093] The second transistor T2 is connected between the node D and an input terminal of the high-level driving voltage ELVDD, and is turned on/off in response to an nth emission signal EM(n). The gate electrode of the second transistor T2 is connected to an nth emission line to which the nth emission signal EM(n) is applied, the source electrode of the second transistor T2 is connected to the input terminal of the high-level driving voltage ELVDD, and the drain electrode of the second transistor T2 is connected to the node D.

[0094] The third transistor T3 is connected to the node A and the node B, and is turned on/off in response to the nth scan signal SCAN(n). The gate electrode of the third transistor T3 is connected to the nth first scan line to which the nth scan signal SCAN(n) is applied, the source electrode of the third transistor T3 is connected to the node B, and the drain electrode of the third transistor T3 is connected to the node A.

[0095] The fourth transistor T4 is connected to the node B and the node C, and is turned on/off in response to the nth emission signal EM(n). The gate electrode of the fourth transistor T4 is connected to the nth emission line to which the nth emission signal EM(n) is applied, the source electrode of the fourth transistor T4 is connected to the node B, and the drain electrode of the fourth transistor T4 is connected to the node C.

[0096] The fifth transistor T5 is connected between the node A and an input terminal of the initial voltage Vini, and is turned on/off in response to an (n-1)th scan signal SCAN(n-1). The gate electrode of the fifth transistor T5 is connected to the (n-1)th first scan line to which the (n-1)th scan signal SCAN(n-1) is applied, the drain electrode of the fifth transistor T5 is connected to the node A, and the source electrode of the fifth transistor T5 is connected to the input terminal of the initial voltage Vini.

[0097] The sixth transistor T6 is connected between the input terminal of the initial voltage Vini and the node C, and is turned on/off in response to the nth scan signal SCAN(n). The gate electrode of the sixth transistor T6 is connected to the nth scan line to which the nth scan signal SCAN(n) is applied, the source electrode of the sixth transistor T6 is connected to the node C, and the drain electrode of the sixth transistor T6 is connected to the input terminal of the initial voltage Vini.

[0098] The capacitor Cstg is connected between the node A and the input terminal of the initial voltage Vini.

[0099] The waveform diagram in FIG. 8 is also adjusted in the equivalent circuit diagram of FIG. 11. As shown in FIG. 8, one frame may be divided into an initial period Pi in which the node A and the node C are initialized, a sampling period Ps in which the threshold voltage of the driving transistor DT is sampled and stored at the node A, an emission period Pe in which the source-gate voltage of the driving transistor DT is programmed (or adjusted) according to the sampled threshold voltage, and the organic light emitting diode OLED emits light by a driving current corresponding to the programmed source-gate voltage. The gate voltage of the driving transistor DT is initialized during an (n-1)th horizontal period Hn-1, and a sampling operation, along with the initializing of the organic light emitting diode OLED, is performed during an nth horizontal period Hn. That is, the initial period Pi and the sampling period Ps are included in the nth horizontal period Hn.

[0100] In the initial period Pi, the (n-1)th scan signal SCAN(n-1) is applied at an ON level, and the nth scan signal SCAN(n) and the nth emission signal EM(n) are applied at an OFF level. In the initial period Pi, as the fifth transistor T5 is turned on in response to the (n-1)th scan signal SCAN(n-1), the node A is initialized to the initial voltage Vini. Accordingly, by initializing the node A prior to the sampling operation, the reliability of sampling of the threshold voltage Vth of the driving transistor DT can be improved.

[0101] In the sampling period Ps, the nth scan signal SCAN(N) is applied at an ON level, and the (n-1)th scan signal SCAN(n-1) and the nth emission signal EM(n) are applied at an OFF level. In the sampling period Ps, as the first, third, and sixth transistors T1, T3, and T6 turn on in response to the nth scan signal SCAN(n), the driving transistor DT is diode-connected (that is, the gate electrode and the drain electrode are shorted so that the driving transistor DT acts as a diode), and the data voltage Vdata(n) is applied to the node D. Accordingly, in the sampling period Ps, a current Ids flows between the source electrode and drain electrode of the driving transistor DT, and this current Ids causes the voltage at the node A to rise from the initial voltage Vini to Vdata(n)-Vth, obtained by subtracting the threshold voltage of the driving transistor DT from the data voltage Vdata(n). The initial voltage Vini is equal to or lower than the low-level driving voltage ELVSS. As the voltage at the node A, which is connected to the gate electrode of the driving transistor DT, is adjusted according to the threshold voltage Vth of the driving transistor DT, a driving current may be generated in a subsequent emission period Pe, irrespective of the threshold voltage Vth of the driving transistor DT. Also, by initializing the node C prior to the sampling operation, unnecessary light emission by the organic light emitting diode OLED can be prevented.

[0102] The emission period Pe corresponds to the remaining portion of one frame, excluding the initial period Pi and the sampling period Ps. In the emission period Pe, the nth emission signal EM(n) is applied at an ON level, and the (n-1)th scan signal SCAN(n-1) and the nth scan signal SCAN(n) are applied at an OFF level. In the emission period Pe, as the second transistor T2 is turned on in response to the nth emission signal EM(n), the high-level driving voltage ELVDD is connected to the source electrode of the driving transistor DT. Also, as the fourth transistor T4 is turned on

in response to the nth emission signal EM(n), the voltage across the nodes B and C becomes substantially equal to the operating voltage V_{oled} of the organic light emitting diode OLED.

[0103] The fourth transistor T4 is connected to the anode of the organic light emitting diode OLED and is turned off during the initial period P_i and the sampling period P_s , but not during the emission period P_e , thus preventing a leakage current flowing through the organic light emitting diode OLED at times other than the emission period P_e .

[0104] The relational expression for the driving current I_{oled} flowing through the organic light emitting diode OLED during the emission period P_e is represented by the above Equation 2 explained with reference to FIG. 9C. Accordingly, the organic light emitting diode OLED emits light by a driving current, thereby displaying a desired gray level. Referring to Equation 2, the mathematical expression for the driving current I_{oled} is $k/2(V_{sg}-V_{th})^2$. The source-gate voltage V_{sg} , which is programmed in the emission period P_e , is already adjusted according to the threshold voltage V_{th} of the driving transistor DT. Thus, the threshold voltage V_{th} of the driving transistor DT does not affect the driving current I_{oled} according to the relational expression, as shown in Equation 2. This minimizes the effect of a change in threshold voltage V_{th} on the driving current I_{oled} .

[0105] FIG. 12 is an equivalent circuit diagram showing a modification of the pixel structure of FIG. 3. FIG. 13 is a waveform diagram showing data signals and gate signals which are applied to the pixel of FIG. 12. FIGS. 14A, 14B, and 14C are equivalent circuit diagrams of the pixel corresponding to the initial period, sampling period, and emission period of FIG. 12.

[0106] Referring to FIG. 12, each pixel PXL arranged in an nth row (n is a natural number) comprises an organic light emitting diode OLED, a driving transistor DT, a first transistor T1, a second transistor T2, a third transistor T3, a fourth transistor T4, a fifth transistor T5, a sixth transistor T6, and a capacitor Cstg.

[0107] The organic light emitting diode OLED emits light by a driving current supplied from the driving transistor DT. The organic light emitting diode OLED comprises multiple layers of organic compounds between an anode and a cathode. The anode of the organic light emitting diode OLED is connected to a node C, and the cathode of the organic light emitting diode OLED is connected to an input terminal of the low-level driving voltage ELVSS.

[0108] The driving transistor DT controls the driving current applied to the organic light emitting diode OLED based on its source-gate voltage V_{sg} . The gate electrode of the driving transistor DT is connected to a node A, its source electrode is connected to an input terminal of the high-level driving voltage ELVDD, and its drain electrode is connected to a node B.

[0109] The first transistor T1 is connected between a data line 14 and the node D, and is turned on/off in response to an nth scan signal SCAN(n). The gate electrode of the first transistor T1 is connected to an nth scan line to which the nth scan signal SCAN(n) is applied, the source electrode of the first transistor T1 is connected to the data line 14, and the drain electrode of the first transistor T1 is connected to the node D.

[0110] The second transistor T2 is connected to the node A and the node B, and is turned on/off in response to the nth scan signal SCAN(n). The gate electrode of the second transistor T2 is connected to the nth scan line to which the nth scan signal SCAN(n) is applied, the source electrode of the second transistor T2 is connected to the node B, and the drain electrode of the second transistor T2 is connected to the node A.

[0111] The third transistor T3 is connected between the node D and an input terminal of the initial voltage V_{ini} , and is turned on/off in response to an nth emission signal EM(n). The gate electrode of the third transistor T3 is connected to an nth emission line to which the nth emission signal EM(n) is applied, the drain electrode of the third transistor T3 is connected to the node D, and the source electrode of the third transistor T3 is connected to the input terminal of the initial voltage V_{ini} .

[0112] The fourth transistor T4 is connected between the node B and the node C, and is turned on/off in response to the nth emission signal EM(n). The gate electrode of the fourth transistor T4 is connected to the nth emission line to which the nth emission signal EM(n) is applied, the source electrode of the fourth transistor T4 is connected to the node B, and the drain electrode of the fourth transistor T4 is connected to the node C.

[0113] The fifth transistor T5 is connected between the node A and an input terminal of the initial voltage V_{ini} , and is turned on/off in response to an (n-1)th scan signal SCAN(n-1). The gate electrode of the fifth transistor T5 is connected to the (n-1)th first scan line to which the (n-1)th scan signal SCAN(n-1) is applied, the source electrode of the fifth transistor T5 is connected to the node A, and the drain electrode of the fifth transistor T5 is connected to the input terminal of the initial voltage V_{ini} .

[0114] The sixth transistor T6 is connected between the node C and the input terminal of the initial voltage V_{ini} , and is turned on/off in response to the (n-1)th scan signal SCAN(n-1) signal. The gate electrode of the sixth transistor T6 is connected to the (n-1)th first scan line to which the (n-1)th scan signal SCAN(n-1) is applied, the source electrode of the sixth transistor T6 is connected to the node C, and the drain electrode of the sixth transistor T6 is connected to the input terminal of the initial voltage V_{ini} .

[0115] The capacitor Cstg is connected to the node A and the node D.

[0116] As described above, as the pixel PXL of FIG. 12 comprises a capacitor Cstg between the node A and the node D, the voltage applied to the node A changes with the voltage applied to the node D. Therefore, the driving transistor

DT determines the amount of electric current supplied to the organic light emitting diode OLED in response to a change in voltage across the node A. As such, the stability of circuit operation can be improved, and the luminance of the organic light emitting diode OLED can be easily controlled.

5 [0117] Moreover, using the pixel PXL of FIG. 12, a shorting of the data voltage V_{data} and the initial voltage V_{ini} during the initial period can be avoided, and the sampling period for pixel compensation is increased, leading to an improvement in compensation capability.

[0118] The operation of the pixel of FIG. 12 will be described with reference to FIGS. 13 to 14C.

10 [0119] One frame may be divided into an initial period P_i in which the node A and the node C are initialized, a sampling period P_s in which the data voltage $V_{data}(n)$ is stored and the driving transistor DT operates until the source-gate voltage of the driving transistor DT becomes substantially equal to the threshold voltage, and an emission period P_e in which the organic light emitting diode OLED emits light by the driving current of the driving transistor DT that is driven in response to a voltage change at the node A. In FIG. 13, since an initial operation is performed during an $(n-1)$ th horizontal period H_{n-1} , an n th horizontal period H_n may be entirely spent on a sampling operation. This ensures a sufficient sampling period P_s , thus making it possible to sample the threshold voltage of the driving transistor more accurately.

15 [0120] In FIG. 14A, the transistors that operate during the initial period P_i are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. Referring to FIGS. 13 and 14A, in the initial period P_i , the $(n-1)$ th scan signal $SCAN(n-1)$ is applied at an ON level, and the n th scan signal $SCAN(n)$ and the n th emission signal $EM(n)$ are applied at an OFF level. In the initial period P_i , as the fifth and sixth transistors T5 and T6 turn on in response to the $(n-1)$ th scan signal $SCAN(n-1)$, the node A and the node C are initialized to the initial voltage V_{ini} .

20 [0121] In the initial period P_i , as the fifth and sixth transistors T5 and T6 turn on in response to the $(n-1)$ th scan signal $SCAN(n-1)$, the node A and the node C are initialized to the initial voltage V_{ini} . By thus initializing the node A and the node C prior to the sampling operation, the sampling reliability can be improved, and unnecessary light emission by the organic light emitting diode OLED can be avoided. To this end, the initial voltage V_{ini} may be chosen from a range of
25 voltages lower than operating voltage of the organic light emitting diode OLED, and the initial voltage V_{ini} may be set equal to or lower than the low-level driving voltage ELVSS.

[0122] In FIG. 14B, the transistors that operate during the sampling period P_s are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. Referring to FIGS. 13 and 14B, in the sampling period P_s , the n th scan signal $SCAN(N)$ is applied at an ON level, and the $(n-1)$ th scan signal $SCAN(n-1)$ and the n th emission signal $EM(n)$ are applied at an OFF level. In the sampling period P_s , as the first and second transistors T1 and T2 turn on in response to the n th scan signal $SCAN(n)$, the driving transistor DT is diode-connected (that is, the gate electrode and the drain electrode are shorted so that the driving transistor DT acts as a diode), the data voltage $V_{data}(n)$ is applied to the node D, and the high-level driving voltage ELVDD is applied to the node A. In this case, different voltages may be applied to the node D and the node A since the capacitor C_{stg} is placed between the node D and the
35 node A.

[0123] Accordingly, in the sampling period P_s , the driving transistor DT operates until the source-gate voltage becomes substantially equal to the threshold voltage, and the high-level driving voltage ELVDD is applied to the node D while the driving transistor DT operates.

40 [0124] In FIG. 14C, the transistors that operate during the emission period P_e are indicated by the solid lines, and the transistors that do not operate during this period are indicated by the dotted lines. Referring to FIGS. 13 and 14C, in the emission period P_e , the n th emission signal $EM(n)$ is applied at an ON level, and the $(n-1)$ th scan signal $SCAN(n-1)$ and the n th scan signal $SCAN(n)$ are applied at an OFF level. In the emission period P_e , as the third transistor T3 is turned on in response to the n th emission signal $EM(n)$, the initial voltage V_{ini} is applied to the node D. The voltage across the capacitor C_{stg} corresponding to the change in potential $V_{data}-V_{ini}$ across the node D is applied to the node A. In other
45 words, the source-gate voltage V_{sg} of the driving transistor DT is programmed with the change in potential across the node D being applied to the node A. Accordingly, the driving transistor DT determines the amount of current supplied to the organic light emitting diode OLED in response to a change in voltage across the node A.

[0125] Also, as the fourth transistor T4 turns on in response to the n th emission signal $EM(n)$, the voltage across the node C becomes equal to the operating voltage V_{oled} of the organic light emitting diode OLED.

50 [0126] The relational expression for the driving current I_{oled} flowing through the organic light emitting diode OLED during the emission period P_e is represented by the following Equation 3. The organic light emitting diode OLED emits light by a driving current, thereby displaying a desired gray level.

[0127] The fourth transistor T4 is connected to the anode of the organic light emitting diode OLED and is turned off during the initial period P_i and the sampling period P_s , but not during the emission period P_e , thus preventing a leakage
55 current flowing through the organic light emitting diode OLED at other times than the emission period P_e .

[Equation 3]

$$I_{oled} = k/2(V_{sg} - V_{th})^2 = k/2((V_s - V_g) - V_{th})^2 = k/2((V_{DD} - (V_{DD} - (V_{data} - V_{ini}) - V_{th}) - V_{th})^2 = k/2(V_{data} - V_{ini})^2$$

where $k/2$ indicates a proportional constant determined by the electron mobility, parasitic capacitance, and channel capacity of the driving transistor DT.

[0128] The mathematical expression for the driving current I_{oled} is $k(V_{sg} - V_{th})^2$. V_{sg} , which is programmed in the emission period P_e , is already adjusted according to the threshold voltage V_{th} of the driving transistor DT. Thus, the threshold voltage V_{th} of the driving transistor DT does not affect the driving current I_{oled} according to the relational expression, as shown in Equation 3. This minimizes the effect of a change in threshold voltage V_{th} on the driving current I_{oled} .

[0129] Although the above description has been given of a frame that is divided into an initial period P_i , a sampling period P_s , and an emission period P_e , the present disclosure is not limited thereto, and as shown in FIG. 15, a frame may further comprise a hold period P_h between the initial period P_i and the emission period P_e .

[0130] In the hold period P_h , the n th scan signal $SCAN(n)$ is applied at an OFF level, and the $(n-1)$ th scan signal $SCAN(n-1)$ and the n th emission signal $EM(n)$ are applied at an OFF level.

[0131] In this way, in the hold period P_h , the n th emission signal $EM(n)$ is not applied at an ON level but is held at an OFF level for a certain amount of time while the n th scan signal $SCAN(n)$ is applied at an ON level. Accordingly, it is possible to prevent noise caused by a current change or voltage change, which may occur when the n th scan signal $SCAN(n)$ and the n th emission signal $EM(n)$ are synchronized. The other elements shown in FIG. 15 are substantially identical to those explained in FIG. 8.

[0132] Conventionally, each pixel is driven with an n th first scan signal $SCAN1(n)$, an n th second scan signal $SCAN2(n)$, and n th emission signal $EM(n)$. Thus, three GIP blocks are used per pixel. On the contrary, the pixel structure of this specification explained with respect to FIGS. 2 through 15 is driven with the $(n-1)$ th scan signal $SCAN(n-1)$, n th scan signal $SCAN(n)$, and n th emission signal $EM(n)$. Accordingly, the pixel structure of this specification can be driven using a GIP consisting of two blocks. This can reduce the width of a GIP forming area, thereby achieving a narrow bezel.

[0133] FIGS. 16 to 18 are views showing various examples of implementing a scan driver's shift registers and inverters of an emission driver in a gate drive circuit.

[0134] FIG. 16 is a view illustrating the gate drive circuit 13 of FIG. 2 in detail. Referring to FIG. 16, the gate drive circuit may comprise a scan driver $S1(n)$ and an emission driver $EM\ Inv.(n)$.

[0135] The scan driver may generate a scan signal and provide it to the scan lines on a line-sequential basis, in order to drive at least one scan line connected to each pixel row. The scan driver comprises shift registers. Each shift register comprises A stages $S1(1)$ to $S1(n+1)$ connected in cascade. The emission driver may generate an emission signal and provide it to the emission lines, in order to drive at least one emission line connected to each pixel row. The emission driver comprises inverters. Each inverter comprises B stages $EM\ Inv.(1)$ to $EM\ Inv.(n+1)$ connected in cascade.

[0136] The A stages $S1(1)$ to $S1(n+1)$ and the B stages $EM\ Inv.(1)$ to $EM\ Inv.(n+1)$ may be disposed on both sides of an active area where an image is displayed, and be symmetrically disposed with respect to the active area.

[0137] The A stages $S1(n-1)$ simultaneously output an $(n-1)$ th scan signal $SCAN(n-1)$ in response to a start pulse $S1VST$. Apart from the $(n-1)$ th scan signal $SCAN(n-1)$, the A stages $S1(n-1)$ may output a carry signal and supply it as a start pulse $S1VST$ simultaneously to the next A stages $S1(n)$. The carry signal may be input as a start pulse for the next stage.

[0138] As the $(n-1)$ th scan signal $SCAN(n-1)$ is supplied simultaneously to an $(n-1)$ th scan line of $(n-1)$ th pixels and an $(n-1)$ th scan line of an n th pixels, the $(n-1)$ th scan signal $SCAN(n-1)$ is supplied to the B stages $EM\ Inv.(n)$ and the A stages $S1(n)$.

[0139] Upon receiving the $(n-1)$ th scan signal $SCAN(n-1)$, the B stages $EM\ Inv.(n)$ simultaneously supply an n th emission signal $EM(n)$, which is synchronized with the $(n-1)$ th scan signal $SCAN(n-1)$ and is inverted from the $(n-1)$ th scan signal $SCAN(n-1)$, to an emission line of the n th pixel.

[0140] Upon receiving the $(n-1)$ th scan signal $SCAN(n-1)$ or upon receiving the $(n-1)$ th scan signal $SCAN(n-1)$ and a carry signal, the A stages $S1(n)$ simultaneously supply an n th scan signal $SCAN(n)$ to an n th scan line of the n th pixel in response to scan timing control signals such as a start signal Vst and a clock $GCLK$.

[0141] As the n th scan signal $SCAN(n)$ is supplied simultaneously to the n th scan line of the n th pixel and an n th scan line of an $(n+1)$ th pixel, the n th scan signal $SCAN(n)$ is supplied to the B stages $EM\ Inv.(n+1)$ and the A stages $S1(n+1)$.

[0142] Upon receiving the n th scan signal $SCAN(n)$, the B stages $EM\ Inv.(n+1)$ simultaneously supply an $(n+1)$ th emission signal $EM(n+1)$, which is synchronized with the n th scan signal $SCAN(n)$ and is inverted from the n th scan

signal SCAN(n), to an emission line of an (n+1)th pixel.

[0143] Upon receiving the nth scan signal SCAN(n) or upon receiving the nth scan signal SCAN(n) and a carry signal, the A stages S1(n+1) simultaneously supply an (n+1)th scan signal SCAN(n+1) to an (n+1)th scan line of the (n+1)th pixel in response to scan timing control signals such as a start signal Vst and a clock GCLK.

[0144] Generally, the gate drive circuit includes a first scan driver, a second scan driver, and an emission driver, in order to drive the pixels. Also, the gate drive circuit requires at least three blocks of A to C stages to drive the pixels. In contrast, in this exemplary embodiment, the pixels may be driven with the scan driver and the emission driver without an additional driver. Thus, in this exemplary embodiment, the pixels may be driven with the A stages and the B stages without an additional driver. Accordingly, a narrow bezel can be achieved according to this exemplary embodiment since the pixels are driven using only 2/3 of the space compared to the conventional art.

[0145] Referring to FIG. 17, odd numbered A stages S1(1) to S1(2n-1) among A stages S1(1) to S1(2n) and odd numbered B stages EM Inv.(1) to EM Inv.(2n-1) among B stages EM Inv.(1) to EM Inv.(2n) may be disposed on one portion of the active area, and even-numbered A stages S1(2) to S1(2n) among A stages S1(1) to S1(2n) and even numbered B stages EM Inv.(2) to EM Inv.(2n) among B stages EM Inv.(1) to EM Inv.(2n) may be disposed on the other portion of the active area,

[0146] Accordingly, the first set of A stages S1(1) to S1(2n-1) and B stages EM Inv.(1) to EM Inv.(2n-1) disposed on one portion of the active area operate first, and then the second set of A stages S1(2) to S1(2n) and B stages EM Inv.(2) to EM Inv.(2n) disposed on the other portion of the active area operate. In other words, the A stages S1(1) to S1(2n) and the B stages EM Inv.(1) to EM Inv.(2n) may operate sequentially in a zigzag manner.

[0147] The A stage S1(2n-1) disposed on one portion of the active area outputs a (2n-1)th scan signal SCAN(2n-1) in response to a start pulse S1VST, and the B stage EM Inv.(2n-1) outputs a (2n-1)th emission signal EM(2n-1) in response to the start pulse S1VST. The scan signal SCAN(2n-1) output from the A stage S1(2n-1) is applied to the A stage S1(2n) and B stage EM Inv.(2n) disposed on the other portion of the active area, the A stage S1(2n) and B stage EM Inv.(2n) output a scan signal SCAN(2n) and an emission signal EM(2n), respectively, in response to the scan signal SCAN(2n-1), and the output scan signal SCAN(2n) is applied to the A stage S1(2n+1) and B stage EM Inv.(2n+1) disposed on one portion of the active area.

[0148] As described above, this exemplary embodiment can improve the degree of freedom of space utilization and achieve a narrow bezel by disposing the odd-numbered A and B stages and the even-numbered A and B stages, separately.

[0149] Referring to FIG. 18, the A stages S1(1) to S1(n+1) may be disposed on one portion of the active area, and the B stages EM Inv.(1) to EM Inv.(n+1) may be disposed on the other portion of the active area.

[0150] Accordingly, the B stages EM Inv.(1) to EM Inv.(n+1) disposed on the other portion of the active area correspond to the A stages S1(1) to S1(n+1) disposed on one portion of the active area. The A stages S1(1) to S1(n+1) disposed on one portion of the active area and the B stages EM Inv.(1) to EM Inv.(n+1) disposed on the other portion of the active area may operate sequentially.

[0151] The A stages S1(1) to S1(n+1) and B stages EM Inv.(1) to EM Inv.(n+1) disposed on one and the other portions of the active area respectively may apply signals to the pixels in response to different start signals SVST and EVST.

[0152] The A stage S1(n) may apply a scan signal SCAN(n) to the nth pixel and the (n+1)th pixel simultaneously in response to a start signal SVST, and may apply a scan signal SCAN(n) to the A stage S1(n+1). At the same time, the B stage EM Inv.(n) may apply an emission signal EM(n) to the nth pixel in response to a start signal EVST, and may apply a signal to the B stage EM Inv.(n+1). In this way, the A stages and the B stages may operate simultaneously and sequentially.

[0153] As described above, this exemplary embodiment can improve the degree of freedom of space utilization and achieve a narrow bezel by disposing the A stages S1(1) to S1(n+1) and the B stages EM Inv.(1) to EM Inv.(n+1), separately.

[0154] FIG. 19 is a view showing the array configuration of nodes connected to two electrodes of the capacitor Cstg in the pixel of FIG. 7.

[0155] Referring to FIG. 19, the fifth transistor T5 comprises a semiconductor layer 210, a gate electrode 220, a drain electrode 221, and a source electrode, the sixth transistor T6 comprises a semiconductor layer 210, a gate electrode 220, a drain electrode 221, and a source electrode, and the capacitor Cstg comprises a first electrode 225 and a second electrode. The first electrode 225 of the capacitor Cstg is connected to an initial voltage line Vini, which is for receiving signals from the input terminal of the initial voltage Vini, and the drain electrodes 221 of the fifth and sixth transistors T6, and the second electrode corresponds to the gate electrode 235 of the driving transistor DT. Accordingly, a capacitance may be formed at an overlap portion between the first and second electrodes 225 and 235. The source electrode of the fifth transistor T5 may be connected to the gate electrode 235 of the driving transistor DT through a contact hole 271, and the source electrode of the sixth transistor T6 may be connected to the anode of the organic light emitting diode. The semiconductor layer 250 of the driving transistor DT may be formed below the gate electrode 235, and a source contact hole 261 and a drain contact hole 263 may be connected to a source electrode and a drain electrode, each of

a respective transistor.

[0156] The first electrode 225 of the capacitor Cstg may be larger in size than the gate electrode 235 of the driving transistor DT. In this way, the initial voltage Vini is applied to the first electrode 225, thus suppressing the effect of a mobile charge in the substrate 110. This can improve the reduction in the driving current of the driving transistor DT caused by the mobile charge. The initial voltage Vini may be a negative voltage.

[0157] Moreover, the first electrode 225 of the capacitor Cstg is connected to the gate electrode 235 of the driving transistor DT and disposed in an area corresponding to a semiconductor layer of the third transistor T3 that operates in the sampling period, thereby decreasing the effect of the mobile charge on the semiconductor layer of the third transistor T3. In other exemplary embodiments as well, the first electrode 225 of the capacitor Cstg may be disposed in the same way as in FIG. 7.

[0158] Alternatively, a metal layer 114 may be positioned under the semiconductor layer 250 of the driving transistor DT to suppress the effect of the mobile charge on the semiconductor layer 250 of the driving transistor DT. The metal layer 114 may be the same size as or larger than the semiconductor layer 250 of the driving transistor DT.

[0159] The metal layer 114 may be formed of a semiconductor, such as silicon (Si), or a conductive metal; for example, at least one among molybdenum (Mo), aluminum (Al), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), copper (Cu), and an alloy of two or more thereof.

[0160] Also, the first electrode of the capacitor Cstg is not connected to a high-level voltage line VDD that receives signals from the high-level driving voltage input terminal ELVDD, but is connected to the initial voltage line Vini, thereby reducing the number of contact holes.

[0161] FIG. 21 shows a comparative example in which one electrode of the capacitor Cstg of FIG. 7 is not connected to the initial voltage line Vini but is connected to the high-level voltage line VDD.

[0162] Referring to FIG. 21, the second transistor T2 is connected to the high-level voltage line VDD via a contact hole 282, and the first electrode 225 of the capacitor Cstg is connected to the high-level voltage line VDD via another contact hole 281. In other words, the contact hole 281 is added to connect the capacitor Cstg and the high-level voltage line VDD. By the way, in a case where one electrode of the capacitor Cstg is connected to the initial voltage line Vini, as shown in FIGS. 7 and 19, the first electrode 225 of the capacitor Cstg is connected to the drain electrodes of the fifth and sixth transistors T5 and T6 and the initial voltage line Vini via a single contact hole, thereby reducing the number of contact holes compared to the comparative example of FIG. 21. By connecting one electrode of the capacitor Cstg to the initial voltage line Vini, rather than to the high-level voltage line VDD, the number of contact holes can be reduced, resulting in sufficient pixel design margin.

[0163] A cross-sectional view taken along line I-I' of FIG. 19 will be explained below with reference to FIG. 20.

[0164] Referring to FIG. 20, a first buffer layer 120 is positioned on the substrate 110. The first buffer layer 120 may be formed of one among silicon oxide (SiOx), silicon nitride (SiNx), and a multi-layer thereof.

[0165] The substrate 110 may be a glass, metal, plastic, or polyimide insulating layer, and may be composed of two or more layers. A flexible organic light emitting display may be made of a flexible material such as plastic. Also, when organic light emitting diodes that allow for easy fabrication of flexible displays are used in vehicle lighting or vehicle displays, the vehicle lighting or vehicle displays may have various designs and offer design freedom depending on their structure or appearance.

[0166] The metal layer 114 is positioned on the first buffer layer 120. A second buffer layer 130 is positioned on the metal layer 114. The second buffer layer 130 may be formed of one among silicon oxide (SiOx), silicon nitride (SiNx), or a multi-layer thereof.

[0167] The semiconductor layer 210 is positioned on the second buffer layer 130. The semiconductor layer 210 may consist of silicon semiconductor or oxide semiconductor. The semiconductor layer 210 of the sixth transistor T6 comprises a drain region 215, a source region, lightly-doped regions 213, and a channel region 211 positioned between the lightly-doped regions 213. The semiconductor layer 210 may be doped with at least one p-type impurity such as boron (B), aluminum (Al), gallium (Ga), or indium (In). The semiconductor layers of the driving transistor DT and fifth transistor T5 may be formed by the same process as the semiconductor layer 210 of the sixth transistor T6.

[0168] A first insulating layer 140 is positioned on the semiconductor layer 210. The first insulating layer 140 may be formed of one among silicon oxide (SiOx), silicon nitride (SiNx), or a multi-layer thereof.

[0169] A gate electrode 220 of the sixth transistor T6 is positioned above the channel region 211 of the semiconductor layer 210. The gate electrode 220 may be formed of any one among molybdenum (Mo), aluminum (Al), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), copper (Cu), and an alloy of two or more thereof. The gate electrodes 235 of the driving transistor DT and fifth transistor T5 may be formed by the same process as the gate electrode 220 of the sixth transistor T6.

[0170] A second insulating layer 150 is positioned on the gate electrodes 220 and 235. The second insulating layer 150 may be formed of one among silicon oxide (SiOx), silicon nitride (SiNx), or a multi-layer thereof.

[0171] The first electrode 225 of the capacitor Cstg connected to the initial voltage line Vini is positioned on the second insulating layer 150.

[0172] That is, the first electrode 225 connected to the initial voltage line Vini and the second electrode 235 connected to the gate electrode 235 of the driving transistor DT are disposed to overlap, forming the capacitor Cstg. Also, the first electrode 225 is larger in size than the second electrode 235, thus decreasing the effect of a mobile charge on the semiconductor layer of the driving transistor DT.

5 [0173] A third insulating layer 160 is positioned on the first electrode 225 of the capacitor Cstg. The third insulating layer 160 may be formed of one among silicon oxide (SiOx), silicon nitride (SiNx), or a multi-layer thereof.

[0174] After forming the third insulating layer 160, the first to third insulating layers 140, 150, and 160 and the first electrode 225 of the capacitor Cstg are selectively etched to form a contact hole 223. Part of the semiconductor layer 210 of the sixth transistor T6 is exposed through the contact hole 223.

10 [0175] The drain electrode 221 of the sixth transistor T6 formed in the contact hole 223 is positioned on the third insulating layer 160. The drain electrode 221 of the sixth transistor T6 shares the same contact hole 223 with the drain electrode of the fifth transistor T5, and is connected to the initial voltage line Vini and the first electrode 225 of the capacitor Cstg. The drain electrode 221 may be made of any one among molybdenum (Mo), aluminum (Al), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), copper (Cu), and an alloy of two or more thereof. The drain electrode 221 may be a two-layer structure of molybdenum/aluminum-neodymium or a three-layer structure of titanium/aluminum/titanium, molybdenum/aluminum/molybdenum, or molybdenum/aluminum-neodymium/molybdenum.

15 [0176] A fourth insulating layer 170 is positioned on the drain electrode 221. The fourth insulating layer 170 may be a planarizing layer for alleviating the unevenness of the underlying structure, and may be formed of an organic material such as polyimide, benzocyclobutene series resin, or acrylate.

20 [0177] The source and drain electrodes of the aforementioned transistors may be used interchangeably - especially, in case of the first to sixth transistors that function to turn on and off, apart from the driving transistor DT.

[0178] An organic light emitting display of this specification may be used in applications such as TV, mobile, tablet PCs, monitors, smartwatches, laptop computers, vehicle displays, etc. An organic light emitting display of this specification also may be used in displays of various shapes such as flat displays, bendable displays, foldable displays, and rollable displays.

25 [0179] The exemplary embodiments of this disclosure can block leakage current flowing to the organic light emitting diode at times other than the emission period by connecting an emission transistor to the anode of the organic light emitting diode.

[0180] Moreover, the exemplary embodiments of this disclosure can improve the lifetime of the organic light emitting diode because the initial voltage Vini applied during the initial period is lower than the low-level driving voltage ELVSS.

30 [0181] Moreover, the exemplary embodiments of this disclosure can avoid a short between the data voltage Vdata and the initial voltage Vini during the initial period and improve compensation capability because of the longer sampling period for pixel compensation.

[0182] Moreover, the exemplary embodiments of this disclosure can improve the accuracy of threshold voltage compensation because a sufficient sampling period for the threshold voltage of the driving transistor is ensured by connecting the gate electrode of the first initial transistor for initializing the driving transistor of an nth pixel to an (n-1)th scan line to which an (n-1)th scan signal SCAN(n-1) is applied in an (n-1)th pixel.

35 [0183] Moreover, the exemplary embodiments of this disclosure can reduce the number of contact holes and ensure pixel design margin by connecting one electrode of the capacitor to the initial voltage input terminal, rather than the high-level driving voltage.

[0184] Furthermore, the exemplary embodiments of this disclosure can reduce the effect of a mobile charge on the semiconductor layer of the driving transistor by placing a metal layer under the semiconductor layer of the driving transistor.

40 [0185] Furthermore, the exemplary embodiments of this disclosure can reduce the effect of a mobile charge on the semiconductor layer of the driving transistor because one electrode of the capacitor has a larger area than the gate electrode of the driving transistor.

[0186] Furthermore, the exemplary embodiments of this disclosure can reduce the effect of a mobile charge on the semiconductor layer of transistors by placing one electrode of the capacitor in an area corresponding to the semiconductor layer of the transistors that operate during the sampling period.

45 [0187] Furthermore, the exemplary embodiments of this disclosure can prevent distortion in luminescence intensity caused by leakage current because at least one of the transistors connected to the capacitor comprises at least two series-connected transistors.

[0188] Furthermore, the exemplary embodiments of this disclosure can drive the pixels through a gate drive circuit comprising only a scan driver and an emission driver by initializing the driving transistor or the organic light emitting diode during the sampling period of the pixel in the previous row. Accordingly, a narrow bezel can be achieved easily since the pixels are driven using only 2/3 of the space compared to the conventional art.

50 [0189] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure. More particularly, numerous variations and

modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

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Claims

1. An organic light emitting display comprising:

10 a display panel (10) having a plurality of pixels (PXL);
 a gate drive circuit (13) that drives scan lines and emission lines on the display panel (10); and
 a data drive circuit (12) that drives data lines (14) on the display panel (10),
 wherein each of the pixels (PXL) arranged in an nth row (n is a natural number) comprises:

15 an organic light emitting diode (OLED) having an anode connected to a node C and a cathode connected to a low-level driving voltage input terminal,
 a driving transistor (DT) having a gate electrode connected to a node A, a source electrode connected to a node D, and a drain electrode connected to a node B, the driving transistor (DT) controlling a driving current applied to the organic light emitting diode (OLED),
 20 a first transistor (T1) that is connected between a data line (14) and the node D,
 a second transistor (T2) that is connected between the node D and a high-level driving voltage input terminal,
 a third transistor (T3) that is connected to the node A and the node B,
 a fourth transistor (T4) that is connected to the node B and the node C,
 a fifth transistor (T5) that is connected between the node A and an initial voltage input terminal, and
 25 a capacitor (Cstg) that is connected between the node A and the initial voltage input terminal.

2. The organic light emitting display of claim 1, wherein one frame comprises an initial period in which the node A is initialized, a sampling period in which a threshold voltage of the driving transistor (DT) is sampled and stored at the node A, an emission period in which a source-gate voltage of the driving transistor (DT) is programmed to have the sampled threshold voltage, and the organic light emitting diode (OLED) emits light by a driving current corresponding to the programmed source-gate voltage,

30 wherein a gate electrode of the fifth transistor (T5) is connected to an (n-1)th scan line to which an (n-1)th scan signal (SCAN(n-1)) is applied, a gate electrode of the first transistor (T1) and a gate electrode of the third transistor (T3) are connected to an nth scan line to which an nth scan signal (SCAN(n)) is applied, and a gate electrode of the second transistor (T2) and a gate electrode of the fourth transistor (T4) are connected to an nth emission line to which an nth emission signal (EM(n)) is applied,
 35 wherein in the initial period, the (n-1)th scan signal (SCAN(n-1)) is applied at an ON level, and the nth scan signal (SCAN(n)) and the nth emission signal (EM(n)) are applied at an OFF level,
 wherein in the sampling period, the nth scan signal (SCAN(n)) is applied at the ON level, and the (n-1)th scan signal (SCAN(n-1)) and the nth emission signal (EM(n)) are applied at the OFF level, and
 40 wherein in the emission period, the nth emission signal (EM(n)) is applied at the ON level, and the (n-1)th scan signal (SCAN(n-1)) and the nth scan signal (SCAN(n)) are applied at the OFF level.

3. The organic light emitting display of claim 1, further comprising a sixth transistor (T6) connected between the initial voltage input terminal and the node C.

45 4. The organic light emitting display of claim 3, wherein one frame comprises an initial period in which the node A and the node C are initialized, a sampling period in which a threshold voltage of the driving transistor (DT) is sampled and stored at the node A, an emission period in which a source-gate voltage of the driving transistor (DT) is programmed to have the sampled threshold voltage, and the organic light emitting diode (OLED) emits light by a driving current corresponding to the programmed source-gate voltage,
 50 wherein a gate electrode of the fifth transistor (T5) and a gate electrode of the sixth transistor (T6) are connected to an (n-1)th scan line to which an (n-1)th scan signal (SCAN(n-1)) is applied, a gate electrode of the first transistor (T1) and a gate electrode of the third transistor (T3) are connected to an nth scan line to which an nth scan signal (SCAN(n)) is applied, and a gate electrode of the second transistor (T2) and a gate electrode of the fourth transistor (T4) are connected to an nth emission line to which an nth emission signal (EM(n)) is applied,
 55 wherein in the initial period, the (n-1)th scan signal (SCAN(n-1)) is applied at an ON level, and the nth scan signal (SCAN(n)) and the nth emission signal (EM(n)) are applied at an OFF level,

wherein in the sampling period, the n th scan signal (SCAN(n)) is applied at the ON level, and the ($n-1$)th scan signal (SCAN($n-1$)) and the n th emission signal (EM(n)) are applied at the OFF level, and wherein in the emission period, the n th emission signal (EM(n)) is applied at the ON level, and the ($n-1$)th scan signal (SCAN($n-1$)) and the n th scan signal (SCAN(n)) are applied at the OFF level.

5

5. The organic light emitting display of claim 3, wherein one frame comprises an initial period in which the node A and the node C are initialized, a sampling period in which a threshold voltage of the driving transistor (DT) is sampled and stored at the node A, an emission period in which a source-gate voltage of the driving transistor (DT) is programmed to have the sampled threshold voltage, and the organic light emitting diode (OLED) emits light by a driving current corresponding to the programmed source-gate voltage,

10

wherein a gate electrode of the fifth transistor (T5) is connected to an ($n-1$)th scan line to which an ($n-1$)th scan signal (SCAN($n-1$)) is applied, a gate electrode of the first transistor (T1), a gate electrode of the third transistor (T3), and a gate electrode of the sixth transistor (T6) are connected to an n th scan line to which an n th scan signal (SCAN(n)) is applied, and a gate electrode of the second transistor (T2) and a gate electrode of the fourth transistor (T4) are connected to an n th emission line to which an n th emission signal (EM(n)) is applied,

15

wherein in the initial period, the ($n-1$)th scan signal (SCAN($n-1$)) is applied at an ON level, and the n th scan signal (SCAN(n)) and the n th emission signal (EM(n)) are applied at an OFF level,

wherein in the sampling period, the n th scan signal (SCAN(n)) is applied at the ON level, and the ($n-1$)th scan signal (SCAN($n-1$)) and the n th emission signal (EM(n)) are applied at the OFF level, and

20

wherein in the emission period, the n th emission signal (EM(n)) is applied at the ON level, and the ($n-1$)th scan signal (SCAN($n-1$)) and the n th scan signal (SCAN(n)) are applied at the OFF level.

6. The organic light emitting display of any one of claims 2, 4, and 5, wherein the initial period is included in an ($n-1$)th horizontal period, and the sampling period is included in an n th horizontal period.

25

7. The organic light emitting display of any one of claims 1 to 6, wherein, in each pixel (PXL), each transistor whose source electrode or drain electrode is connected to one electrode of the capacitor (Cstg) comprises at least two series-connected transistors (T3A, T3B; T5A, T5B), which are switched on by a same control signal.

30

8. The organic light emitting display of claim 3, wherein a first electrode (225) of the capacitor (Cstg) is positioned between insulating layers (150, 160) that are disposed between a semiconductor layer (210) and a source electrode of the fifth transistor (T5), and the first electrode (225) of the capacitor (Cstg) is connected via a contact hole (223) to a drain electrode (221) of the fifth transistor (T5) and to a drain electrode of the sixth transistor (T6).

35

9. The organic light emitting display of any one of claims 1 to 8, further comprising a metal layer (114) under a semiconductor layer (250) of the driving transistor (DT).

10. The organic light emitting display of any one of claims 1 to 7, wherein a first electrode (225) of the capacitor (Cstg) that receives an initial voltage (Vini) from the initial voltage input terminal is disposed corresponding to the gate electrode (235) of the driving transistor (DT).

40

11. The organic light emitting display of any one of claims 1 to 7, wherein a first electrode (225) of the capacitor (Cstg) that receives an initial voltage (Vini) from the initial voltage input terminal is disposed in an area corresponding to a semiconductor layer of the third transistor (T3) that operates during a sampling period.

45

12. The organic light emitting display of any one of claims 1 to 7, wherein a first electrode (225) of the capacitor (Cstg) is the gate electrode of the driving transistor (DT) connected to the node A, a second electrode of the capacitor (Cstg) corresponds to an electrode connected to the initial voltage input terminal, and the second electrode is not connected to a high-level driving voltage input terminal and is connected to the initial voltage input terminal.

50

13. An organic light emitting display comprising:

a display panel (10) having a plurality of pixels (PXL);

a gate drive circuit (13) that drives scan lines and emission lines on the display panel (10); and

55

a data drive circuit (12) that drives data lines (14) on the display panel (10),

wherein each of the pixels (PXL) arranged in an n th row (n is a natural number) comprises:

an organic light emitting diode (OLED) having an anode connected to a node C and a cathode connected

to a low-level driving voltage input terminal,
 a driving transistor (DT) having a gate electrode connected to a node A, a source electrode connected to a high-level driving voltage input terminal, and a drain electrode connected to a node B, the driving transistor (DT) controlling a driving current applied to the organic light emitting diode (OLED),
 5 a first transistor (T1) that is connected between a data line and a node D,
 a second transistor (T2) that is connected to the node A and the node B,
 a third transistor (T3) that is connected between the node D and an initial voltage input terminal,
 a fourth transistor (T4) that is connected to the node B and the node C,
 10 a fifth transistor (T5) that is connected between the node A and the initial voltage input terminal,
 a sixth transistor (T6) that is connected between the initial voltage input terminal and the node C, and
 a capacitor (Cstg) that is connected to the node A and the node D.

14. The organic light emitting display of claim 13, wherein one frame comprises an initial period in which the node A and the node C are initialized, a sampling period in which a threshold voltage of the driving transistor (DT) is sampled and stored at the node A, an emission period in which a source-gate voltage of the driving transistor (DT) is programmed to have the sampled threshold voltage, and the organic light emitting diode (OLED) emits light by a driving current corresponding to the programmed source-gate voltage,
 15 wherein a gate electrode of the fifth transistor (T5) and a gate electrode of the sixth transistor (T6) are connected to an (n-1)th scan line to which an (n-1)th scan signal (SCAN(n-1)) is applied, a gate electrode of the first transistor (T1) and a gate electrode of the second transistor (T2) are connected to an nth scan line to which an nth scan signal (SCAN(n)) is applied, and a gate electrode of the third transistor and a gate electrode of the fourth transistor (T4) are connected to an nth emission line to which an nth emission signal (EM(n)) is applied,
 20 wherein in the initial period, the (n-1)th scan signal (SCAN(n-1)) is applied at an ON level, and the nth scan signal (SCAN(n)) and the nth emission signal (EM(n)) are applied at an OFF level,
 25 wherein in the sampling period, the nth scan signal (SCAN(n)) is applied at the ON level, and the (n-1)th scan signal (SCAN(n-1)) and the nth emission signal (EM(n)) are applied at the OFF level, and
 wherein in the emission period, the nth emission signal (EM(n)) is applied at the ON level, and the (n-1)th scan signal (SCAN(n-1)) and the nth scan signal (SCAN(n)) are applied at the OFF level.

15. The organic light emitting display of claim 13 or 14, wherein the initial period is included in an (n-1)th horizontal period, and the sampling period is included in an nth horizontal period,
 30 wherein, the second transistor (T2) comprises at least two series-connected transistors (T2A, T2b), which are switched on by a same control signal.

16. The organic light emitting display of any one of claims 3 to 5, wherein the capacitor (Cstg) comprises an electrode (225) connected to the initial voltage input terminal, and a contact hole (223) for connecting a drain electrode or a source electrode of the fifth transistor (T5) and the initial voltage input terminal,
 35 wherein a drain electrode or a source electrode of the sixth transistor (T6) for providing a negative voltage is connected to at least one electrode of the organic light emitting diode via the contact hole (223).

17. The organic light emitting display of any one of claims 1 to 16, wherein the capacitor (Cstg) comprises:

a first electrode that receives an initial voltage (Vini); and
 a second electrode connected to the driving transistor (DT),
 45 wherein the first electrode is larger in size than the second electrode.

18. The organic light emitting display of any one of claims 13 to 15, wherein a first electrode (225) of the capacitor (Cstg) is disposed in an area corresponding to a semiconductor layer of the third transistor (T3).

FIG. 1

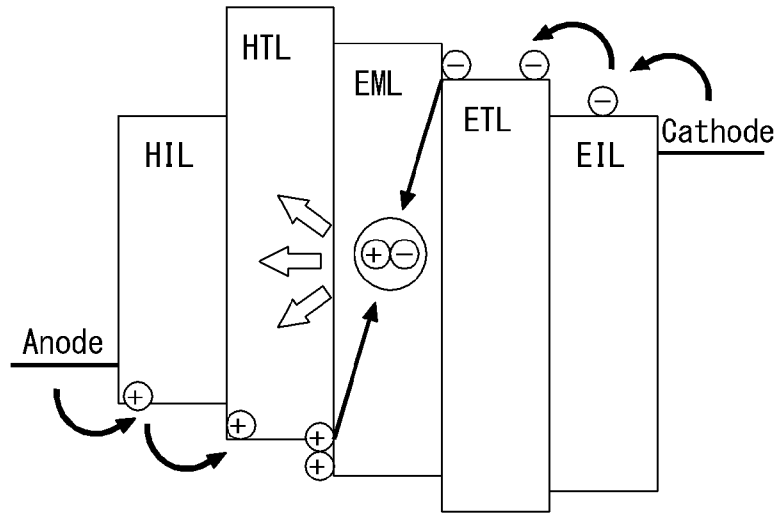


FIG. 2

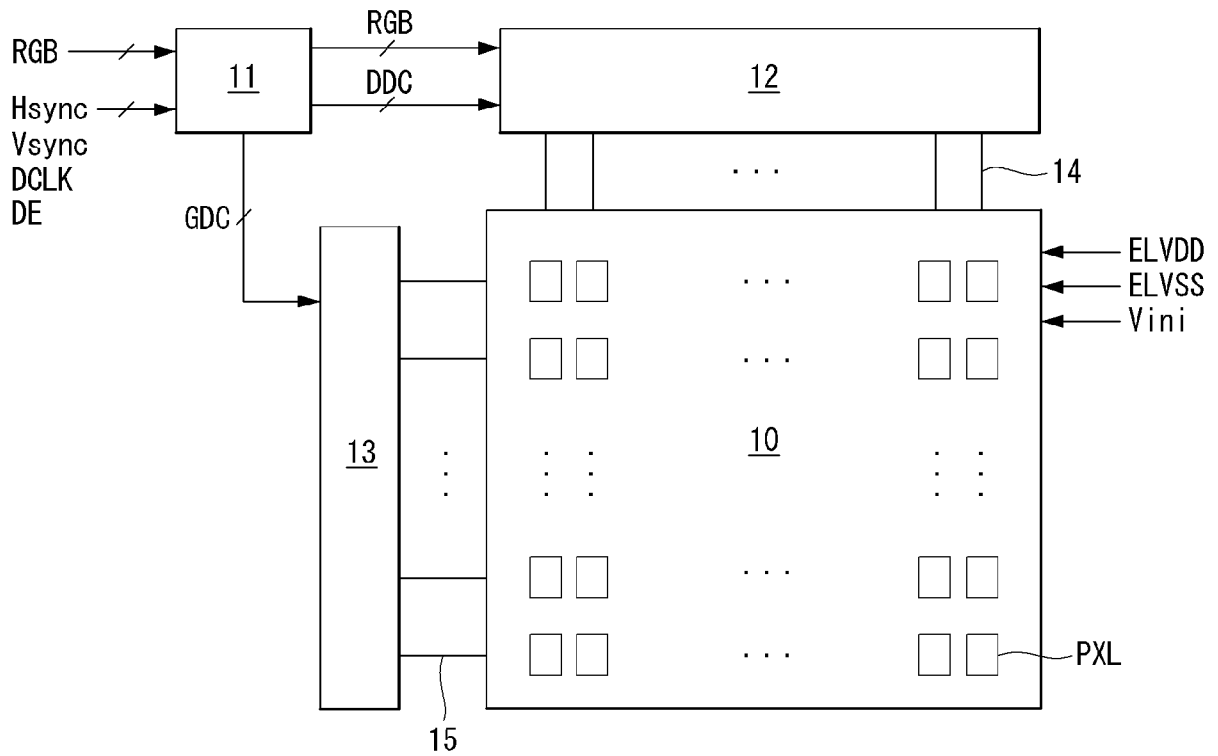


FIG. 3

PXL

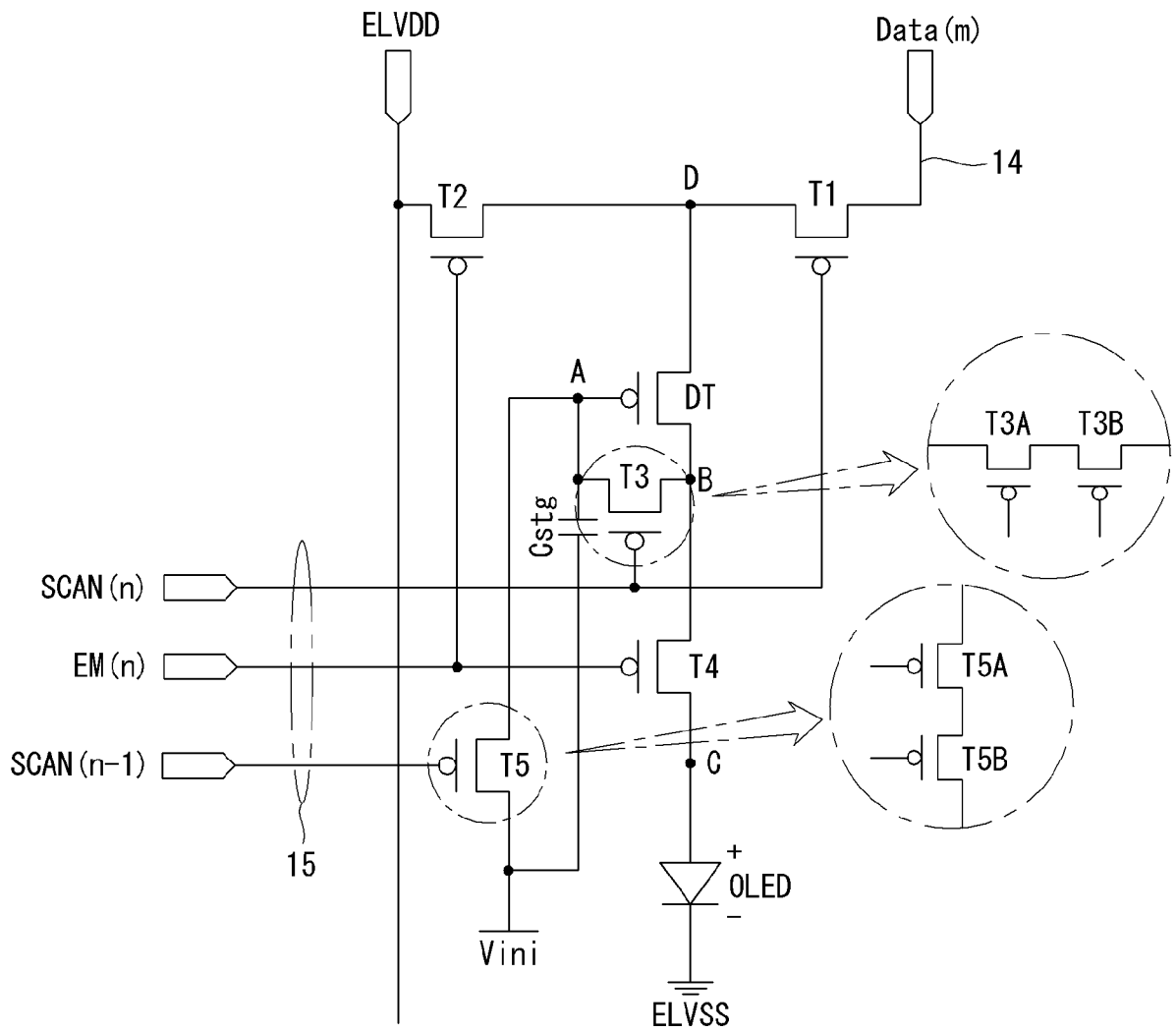


FIG. 4

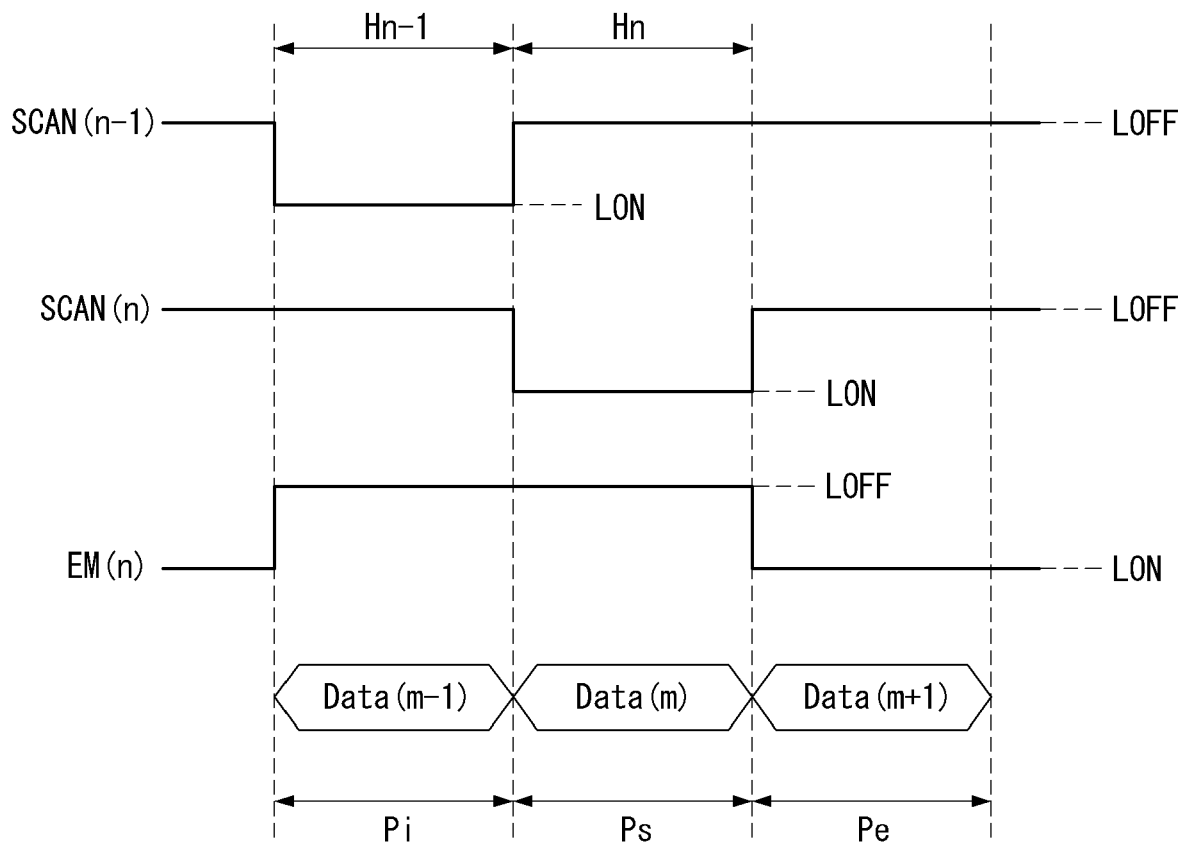


FIG. 5A

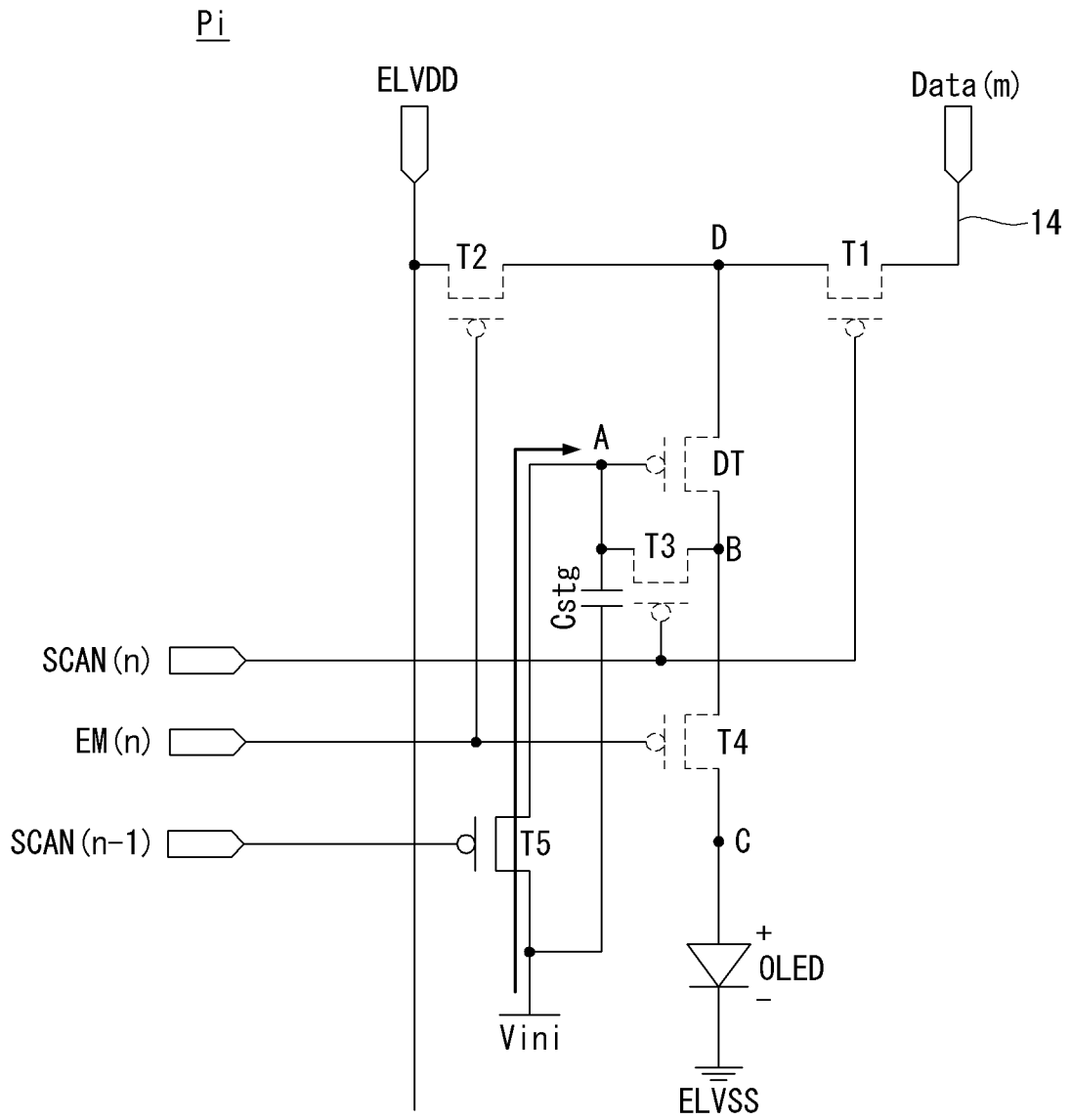


FIG. 5B

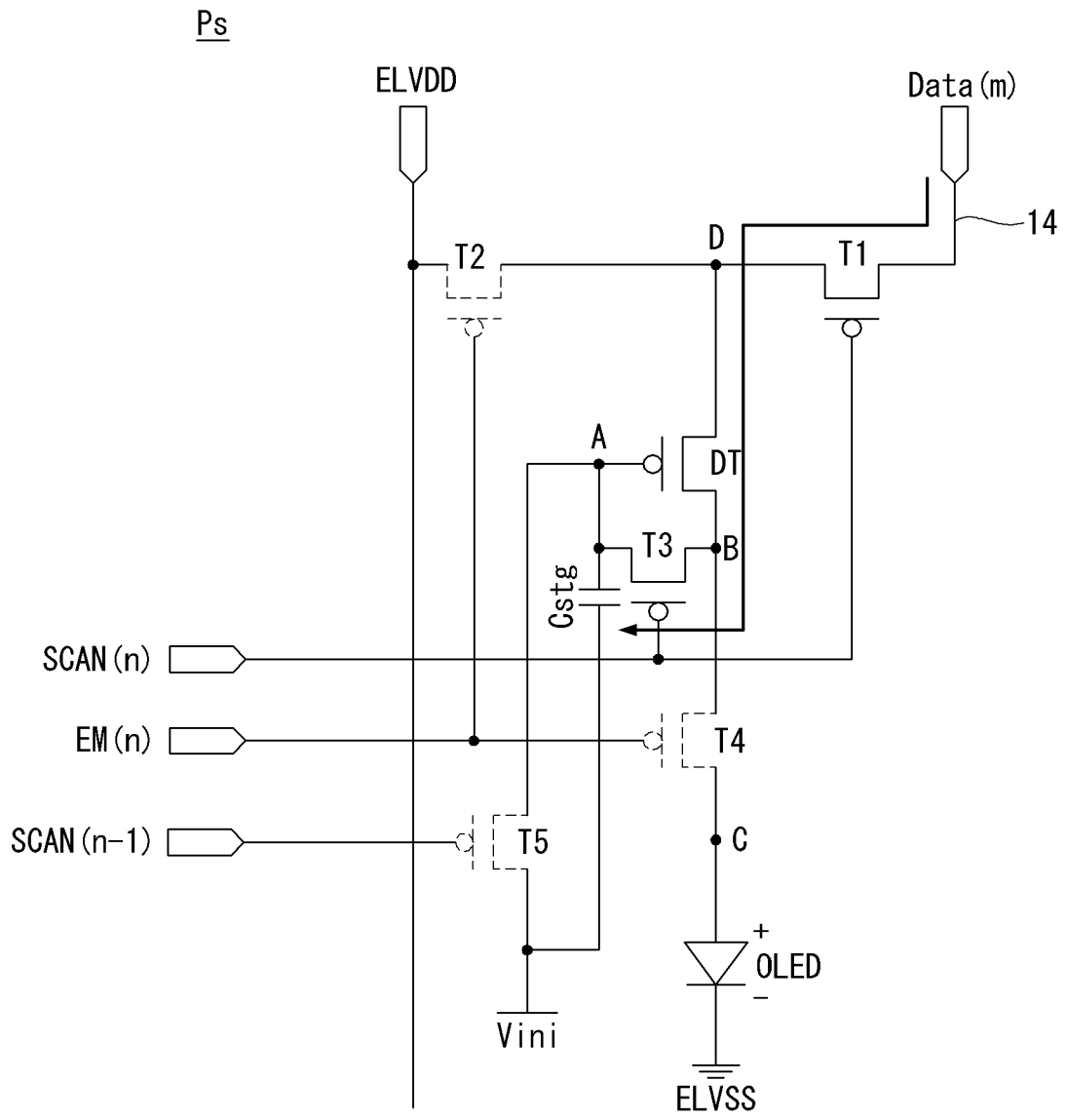


FIG. 5C

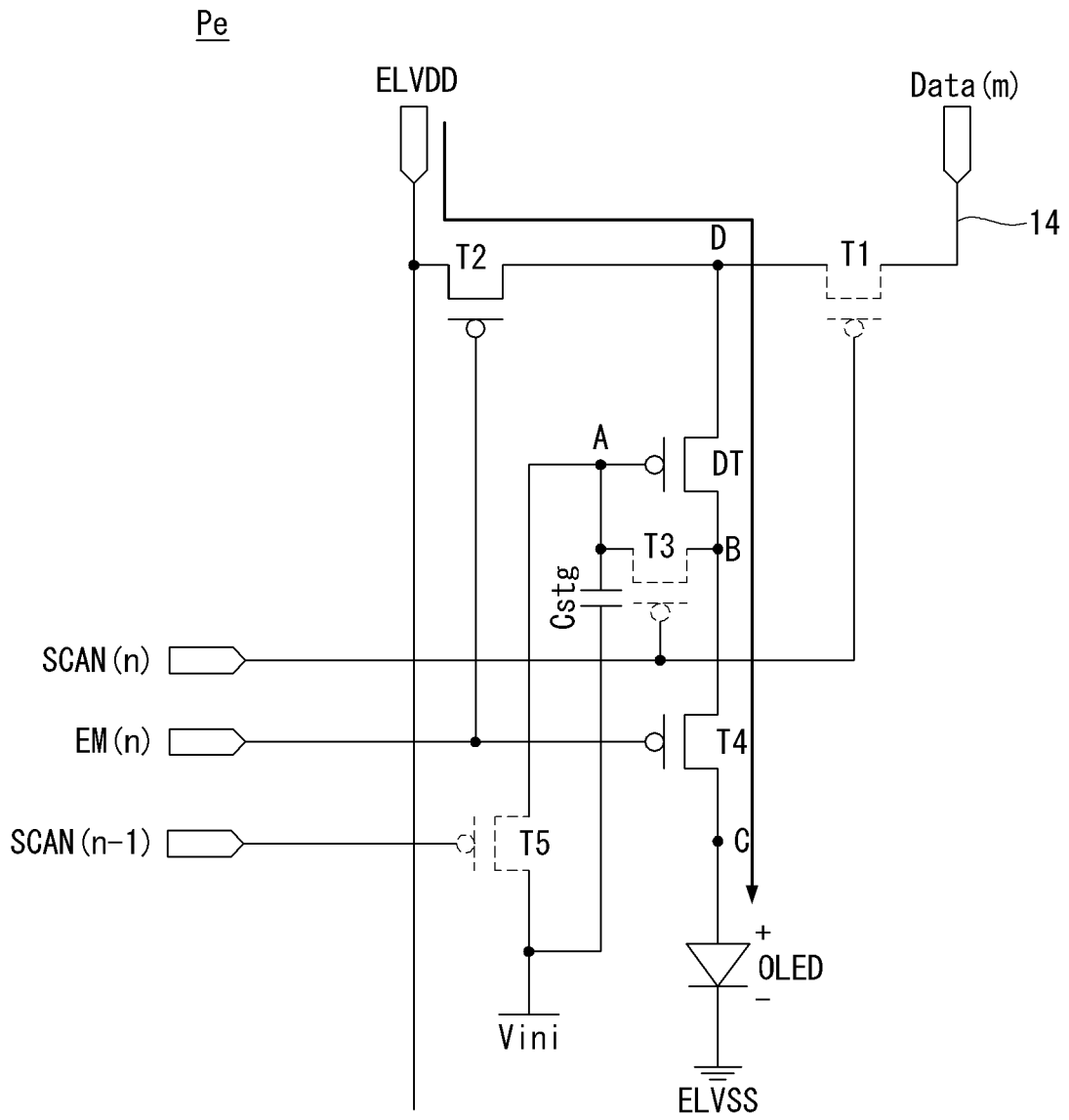


FIG. 6

| Node \ Period | Pi | Ps | Pe |
|---------------|-------|-----------|-----------|
| A | Vini | Vdata-Vth | Vdata-Vth |
| B | VOLED | Vdata | VOLED |
| C | VOLED | VOLED | VOLED |

FIG. 7

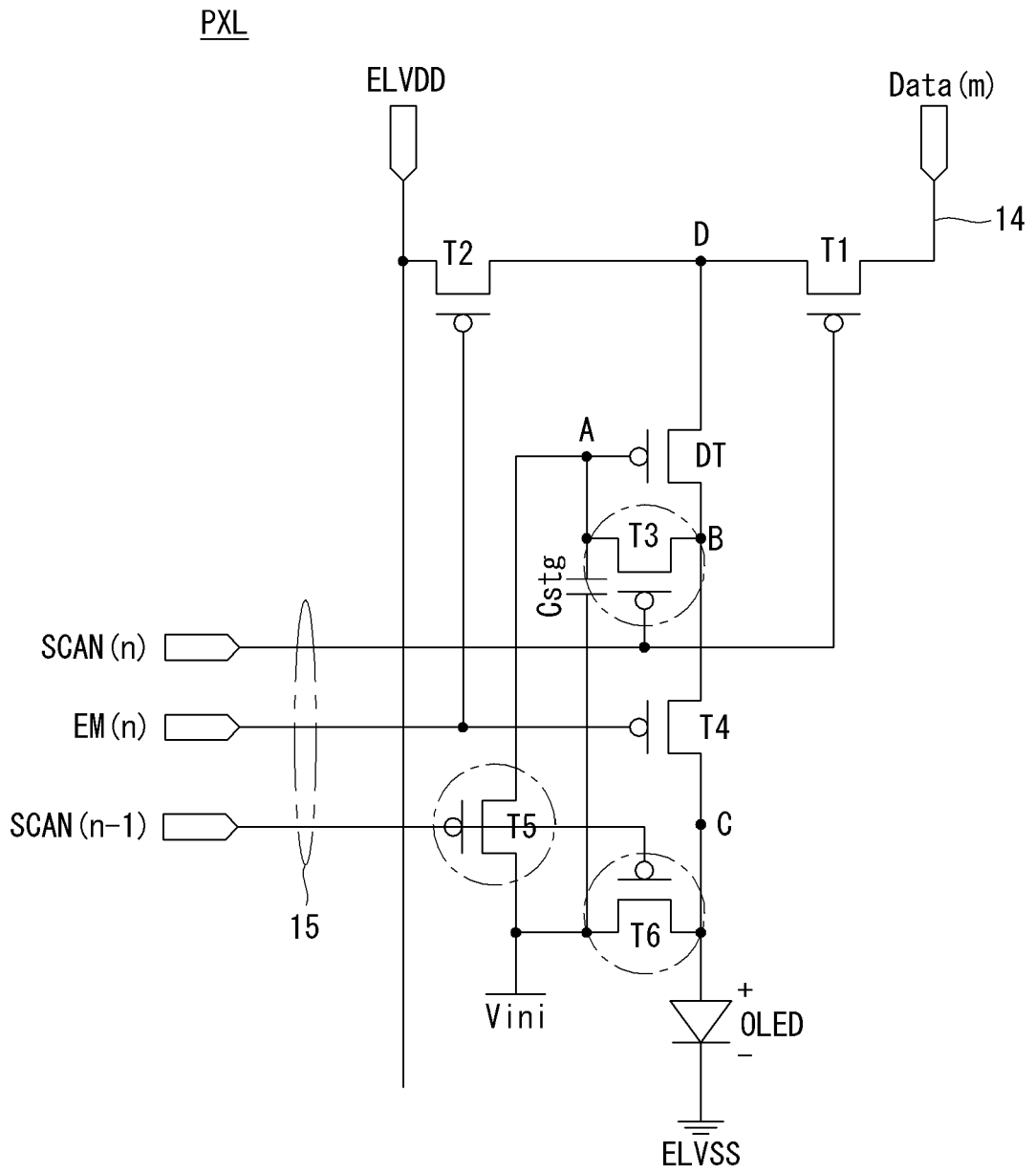


FIG. 8

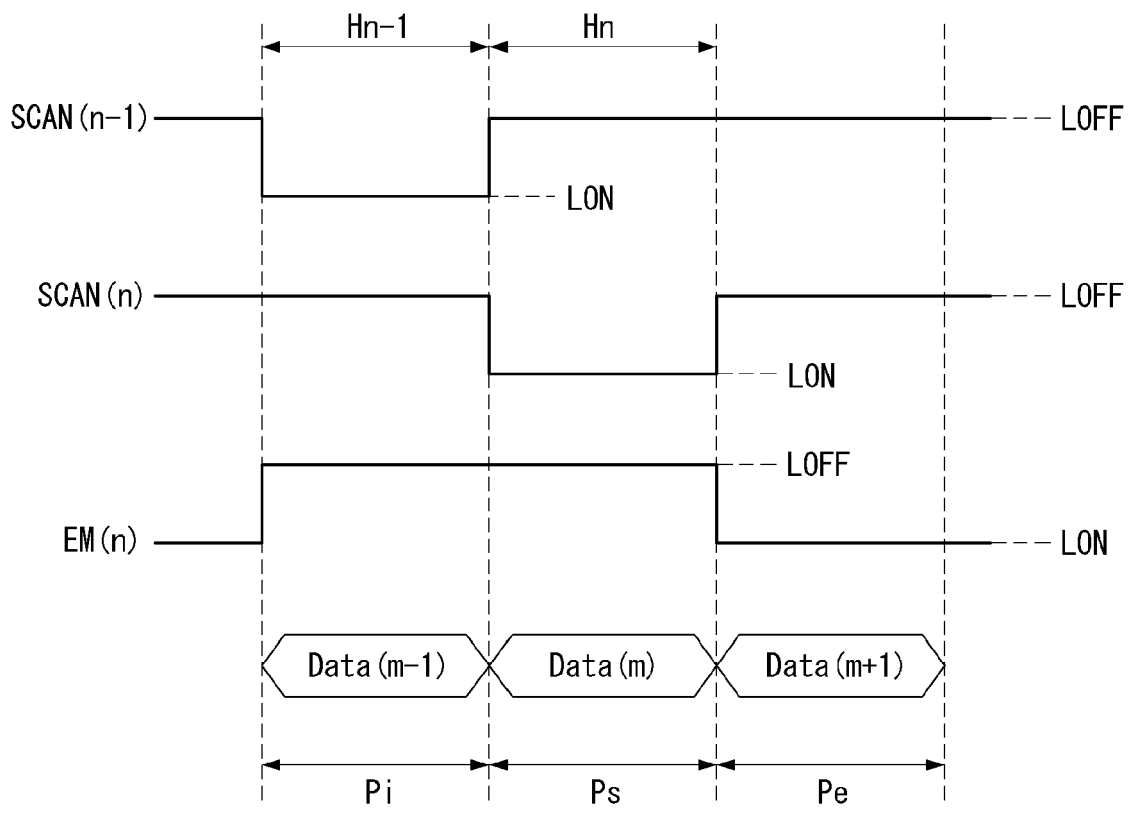


FIG. 9A

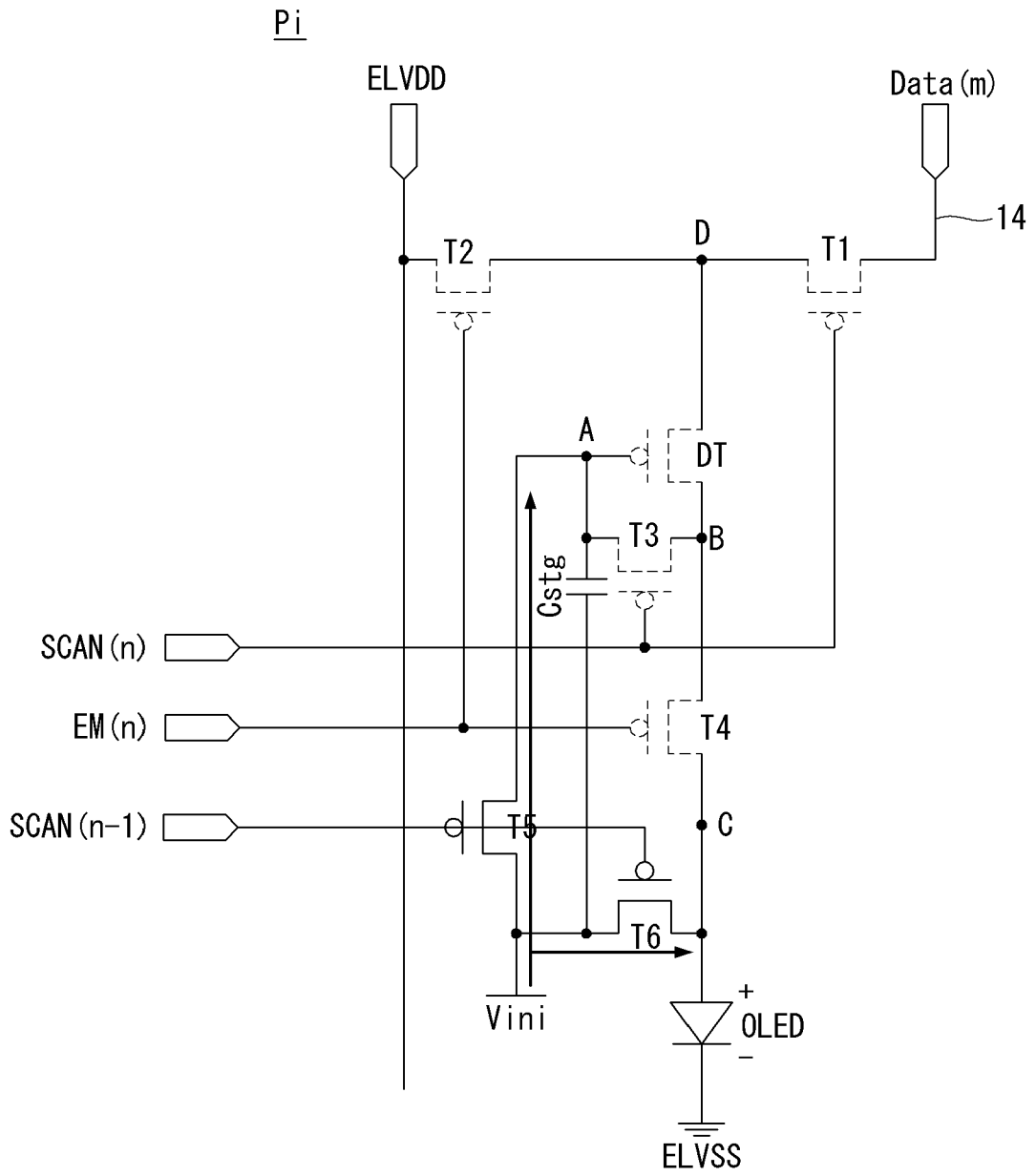


FIG. 9C

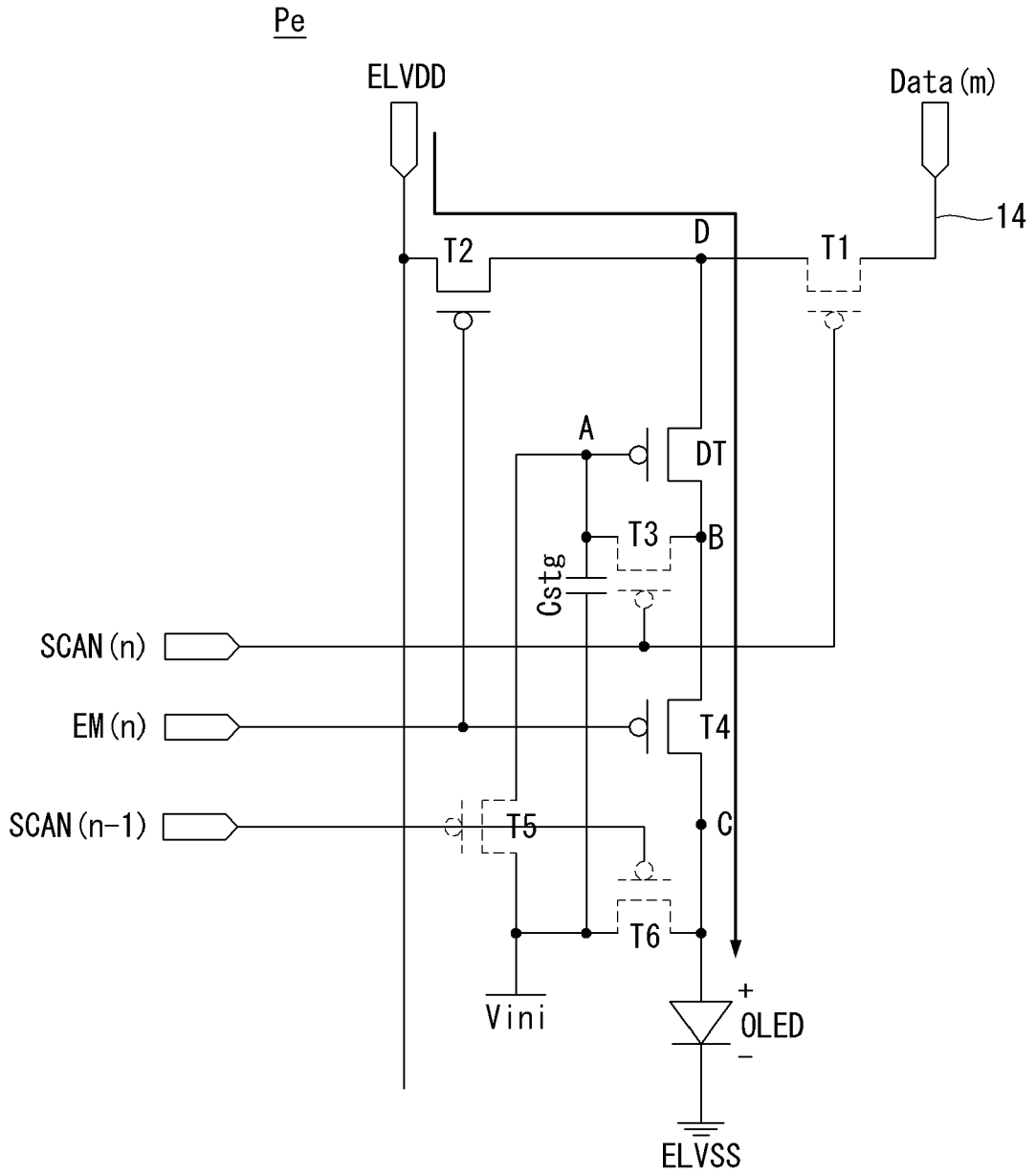


FIG. 10

| Node \ Period | Pi | Ps | Pe |
|---------------|-------|-----------|-----------|
| A | Vini | Vdata-Vth | Vdata-Vth |
| B | VOLED | Vdata | VOLED |
| C | VOLED | Vinit | VOLED |

FIG. 11

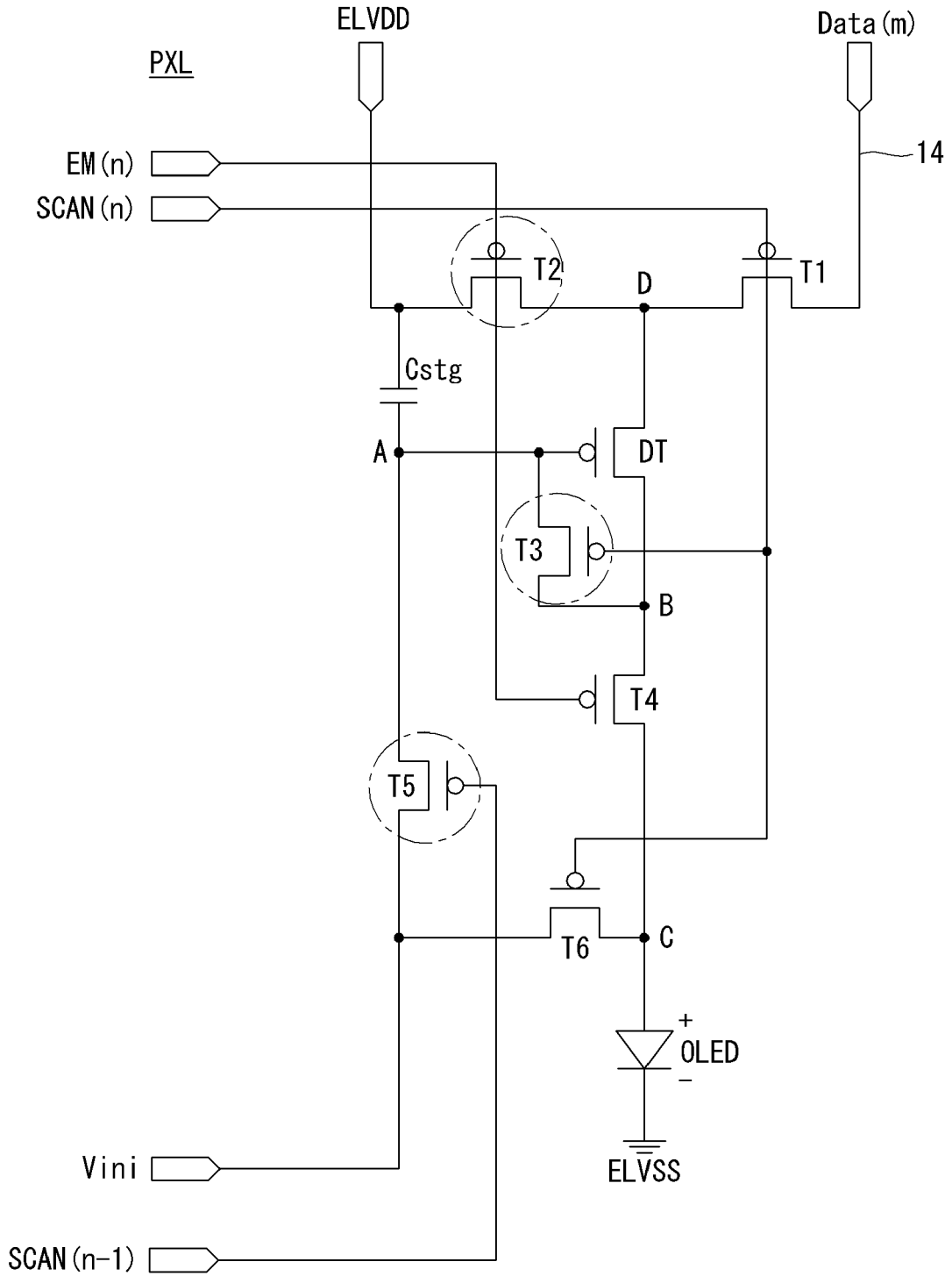


FIG. 12

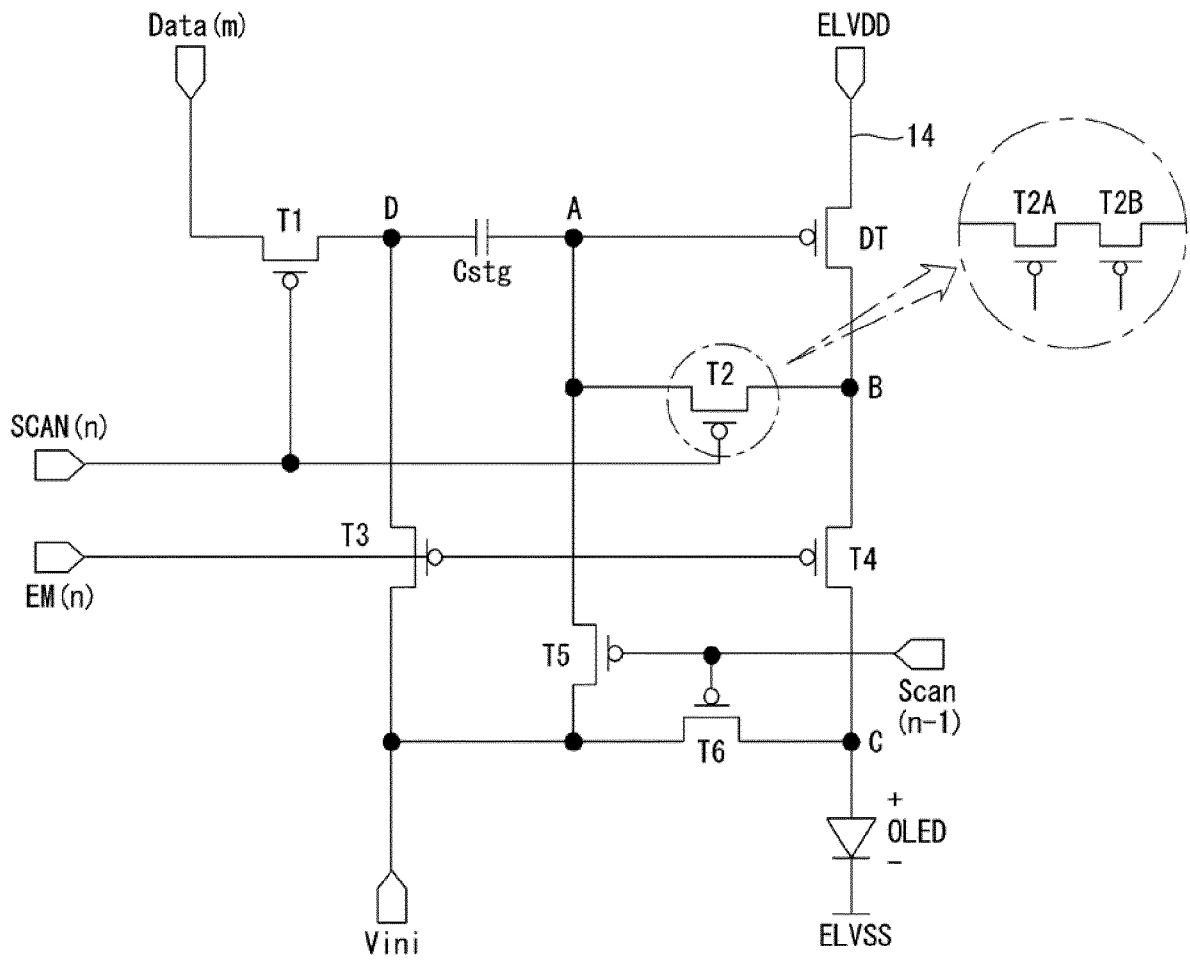


FIG. 13

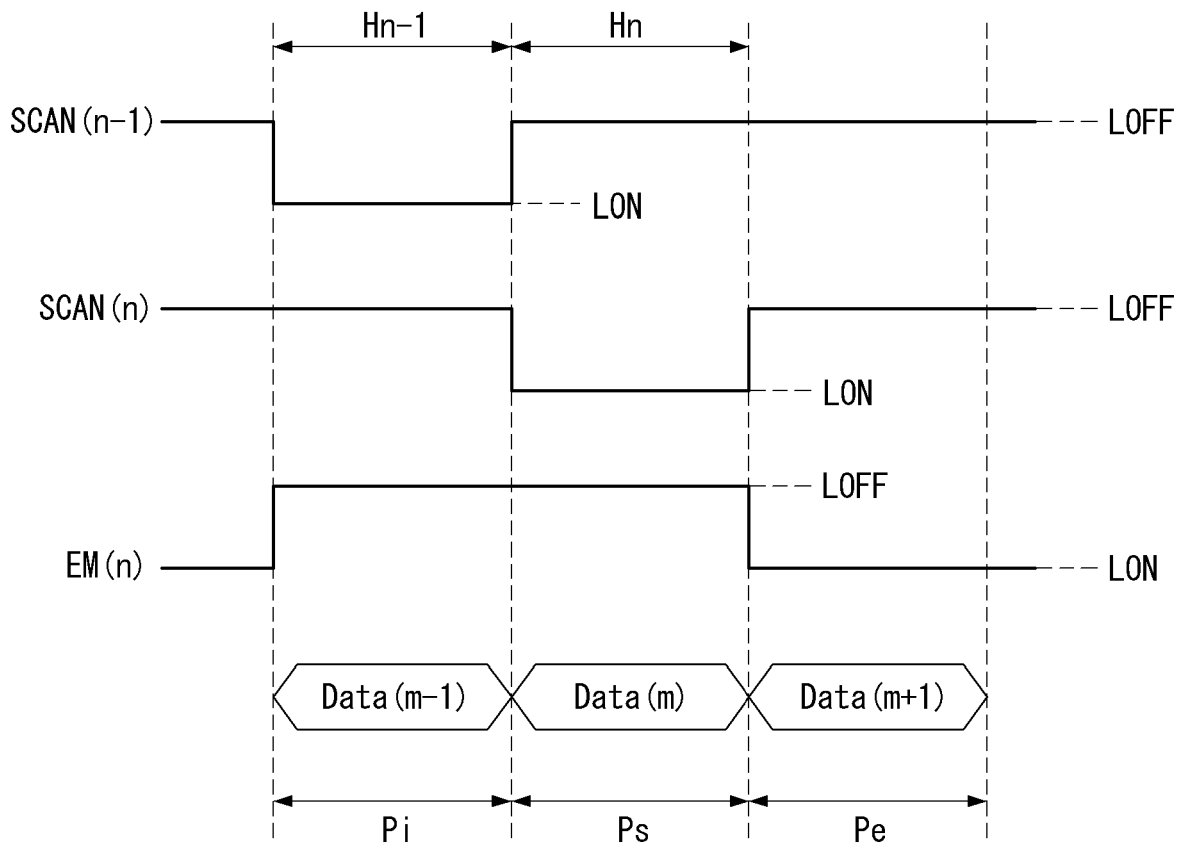


FIG. 14B

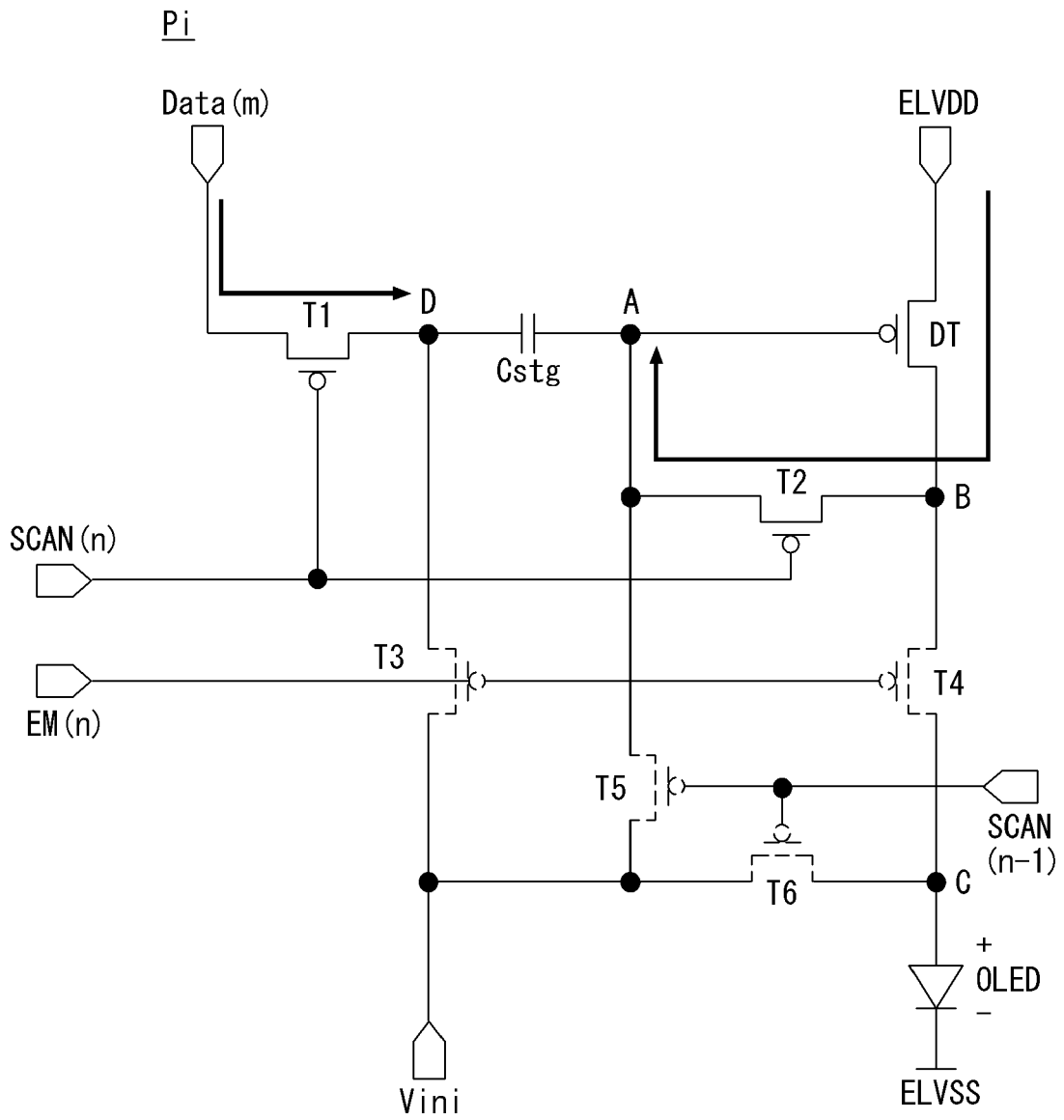


FIG. 14C

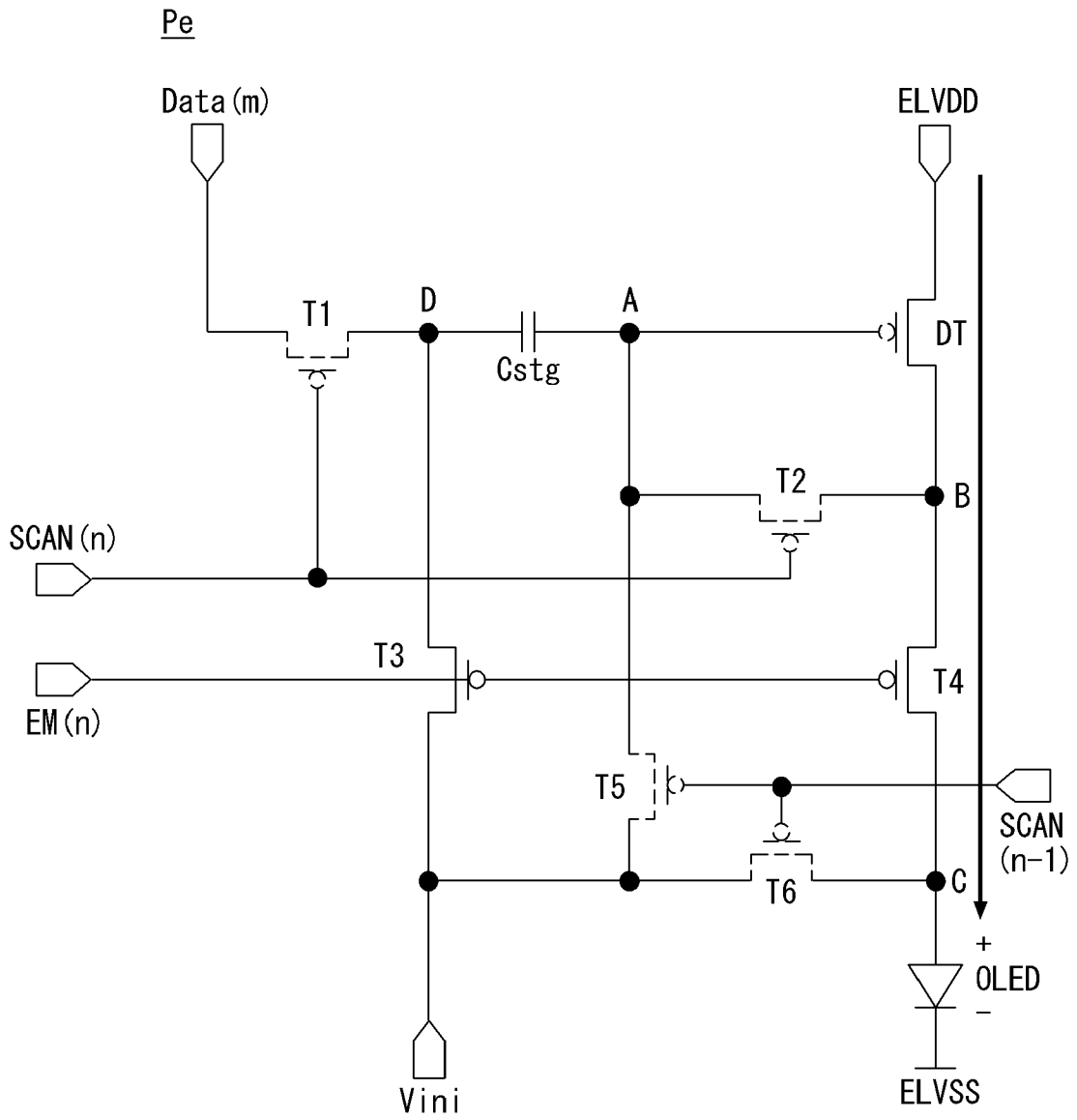


FIG. 15

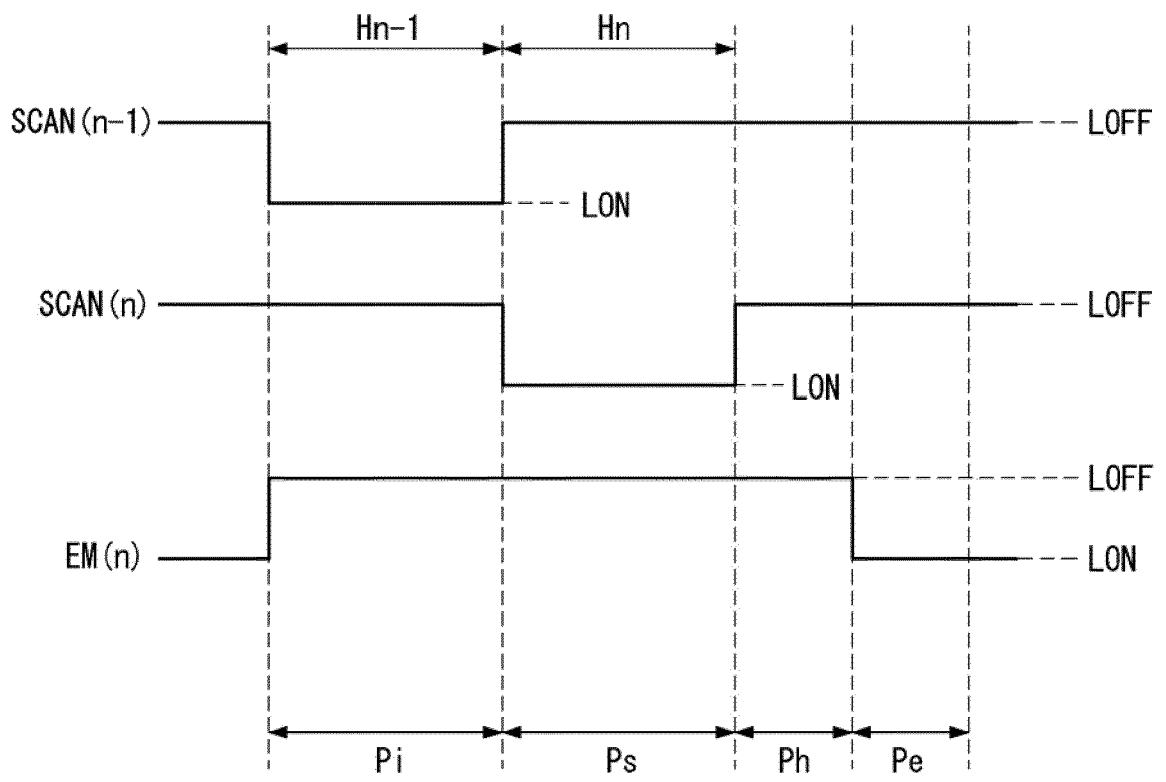


FIG. 16

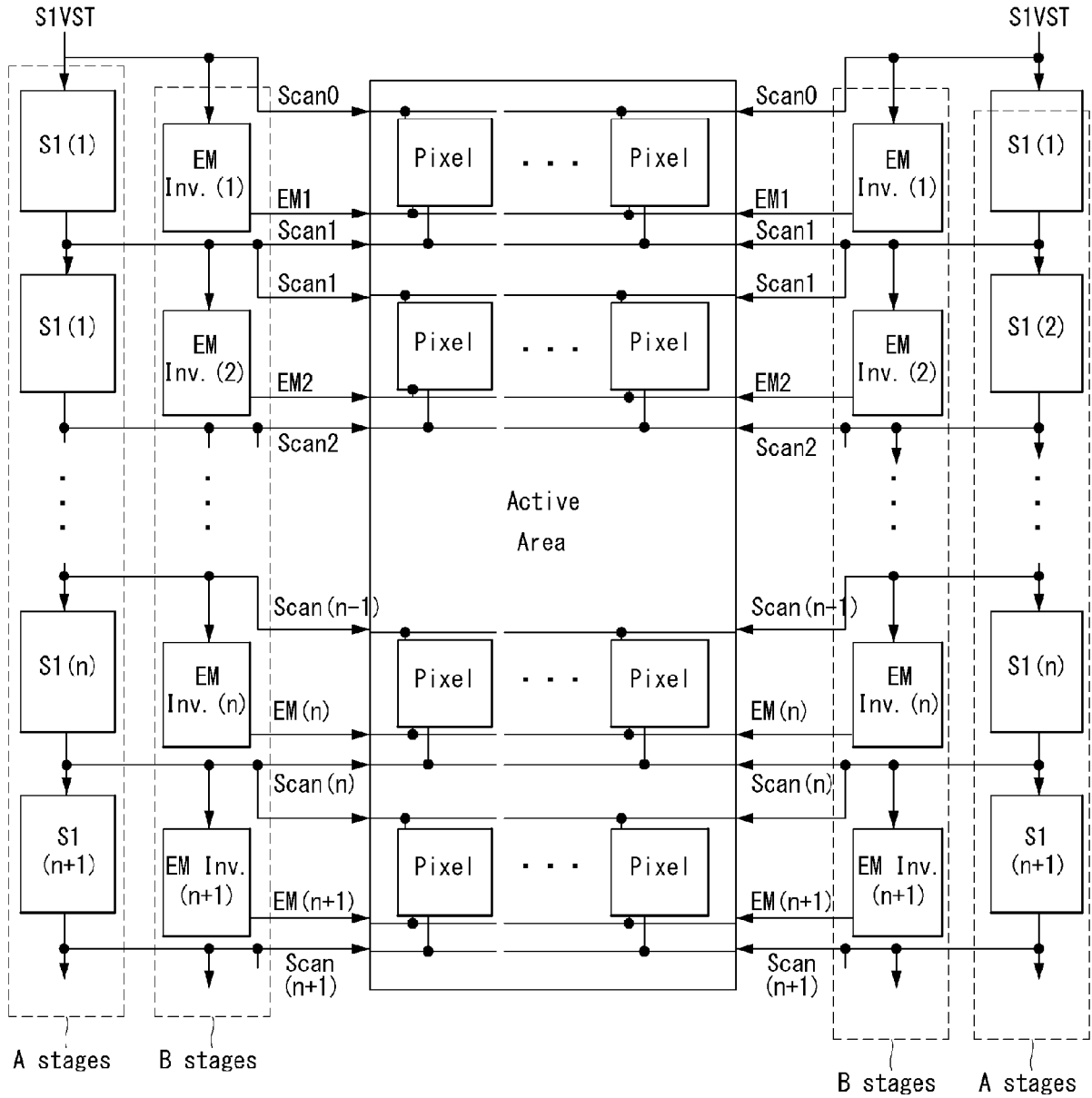


FIG. 17

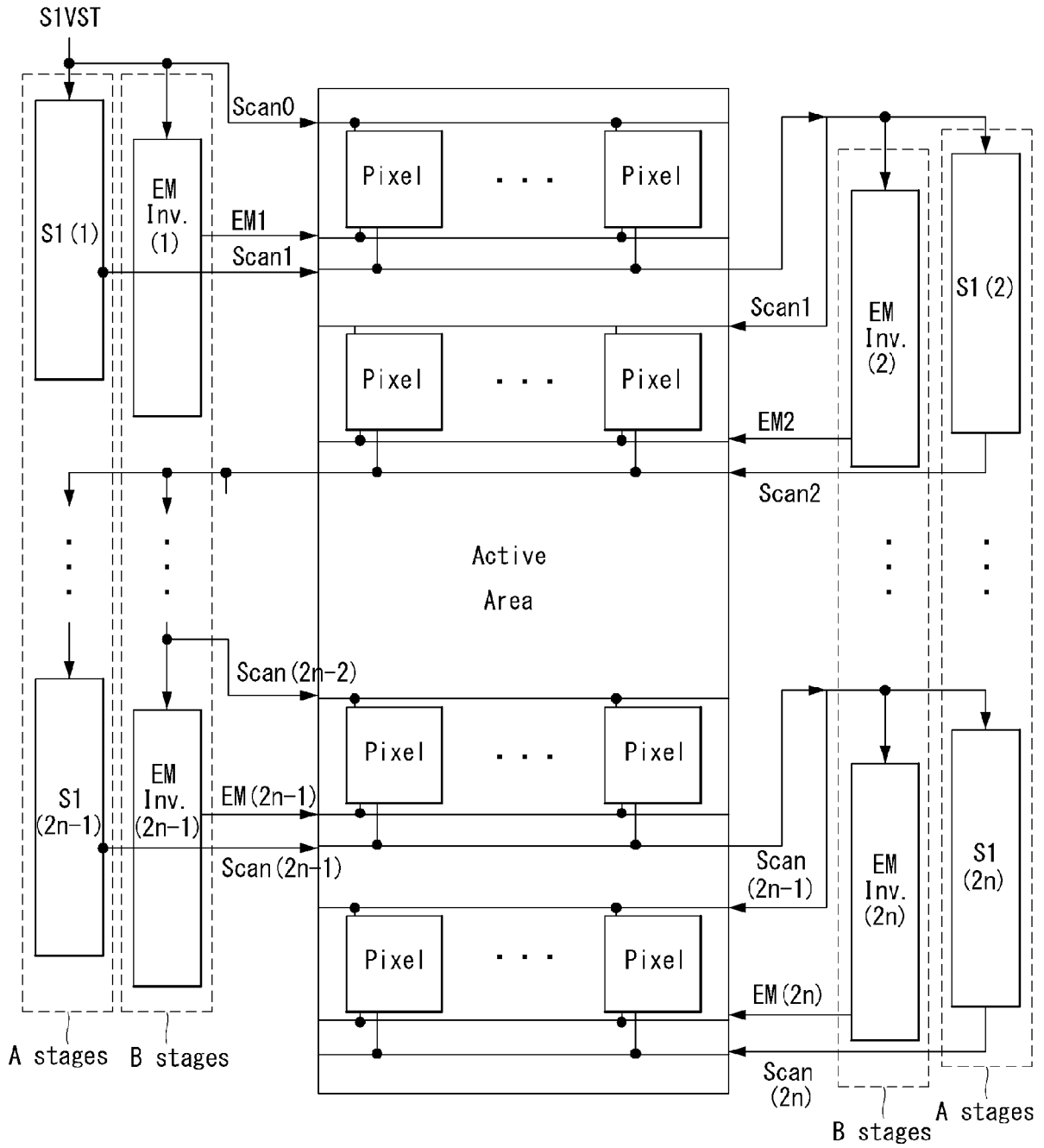


FIG. 18

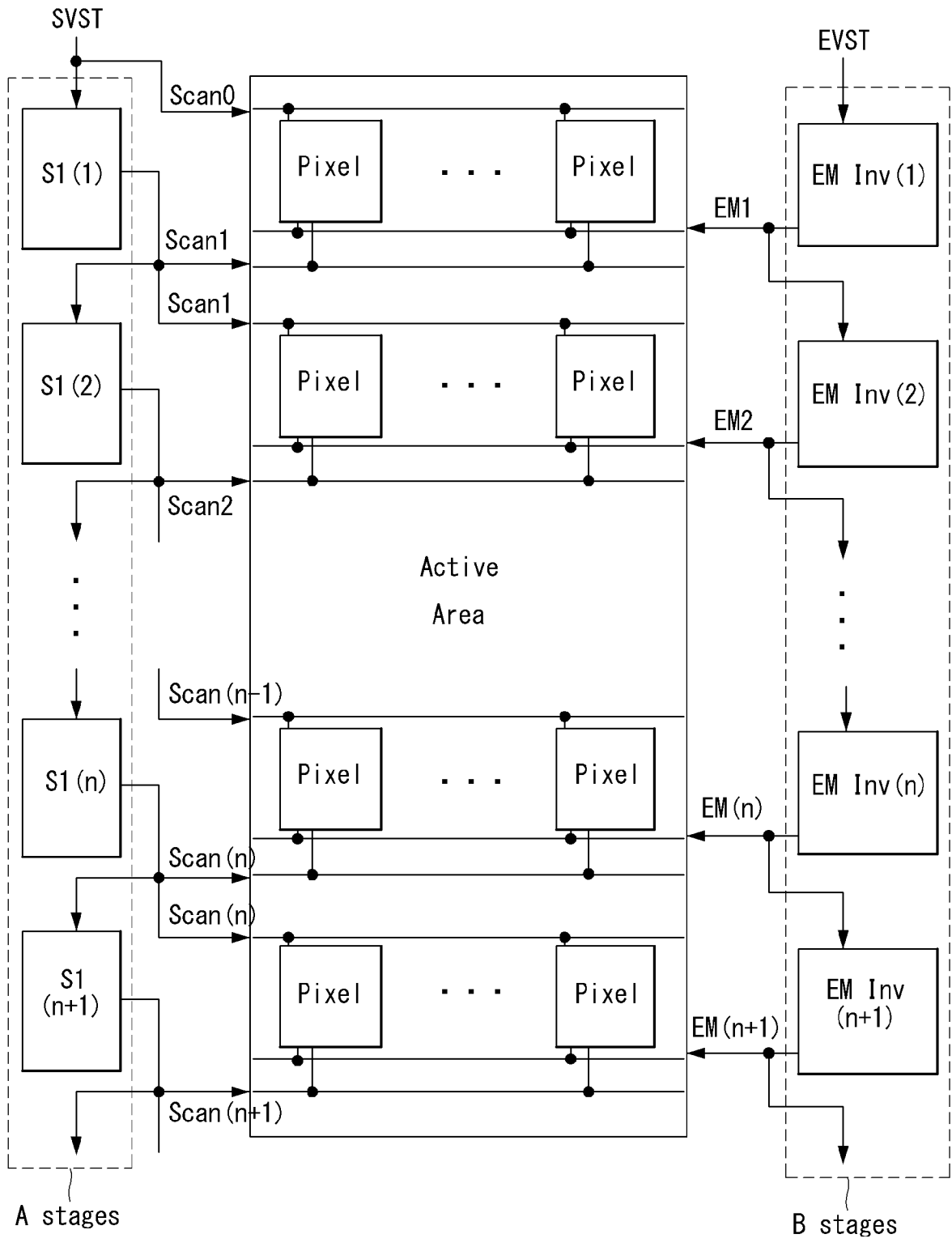


FIG. 19

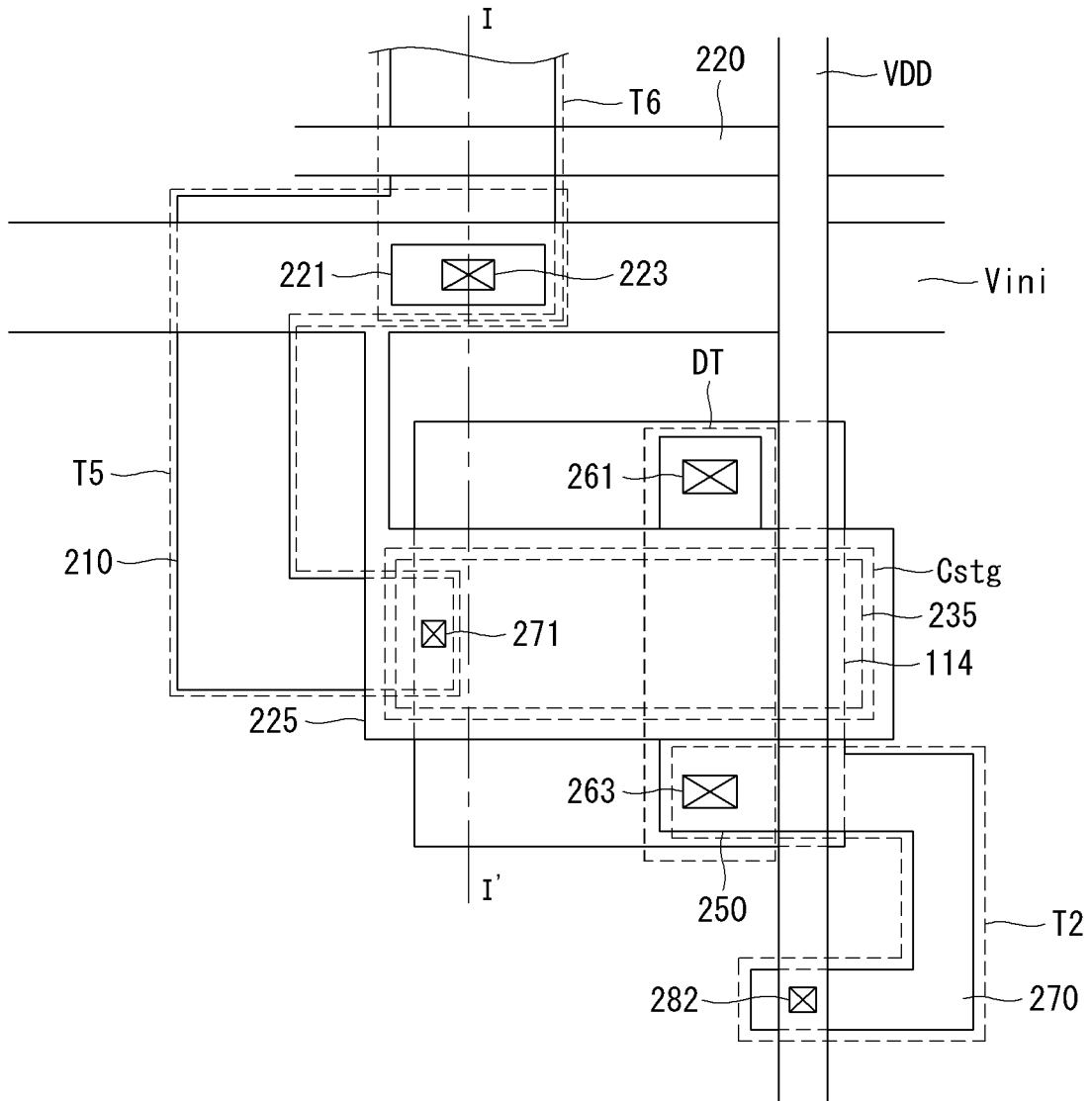


FIG. 20

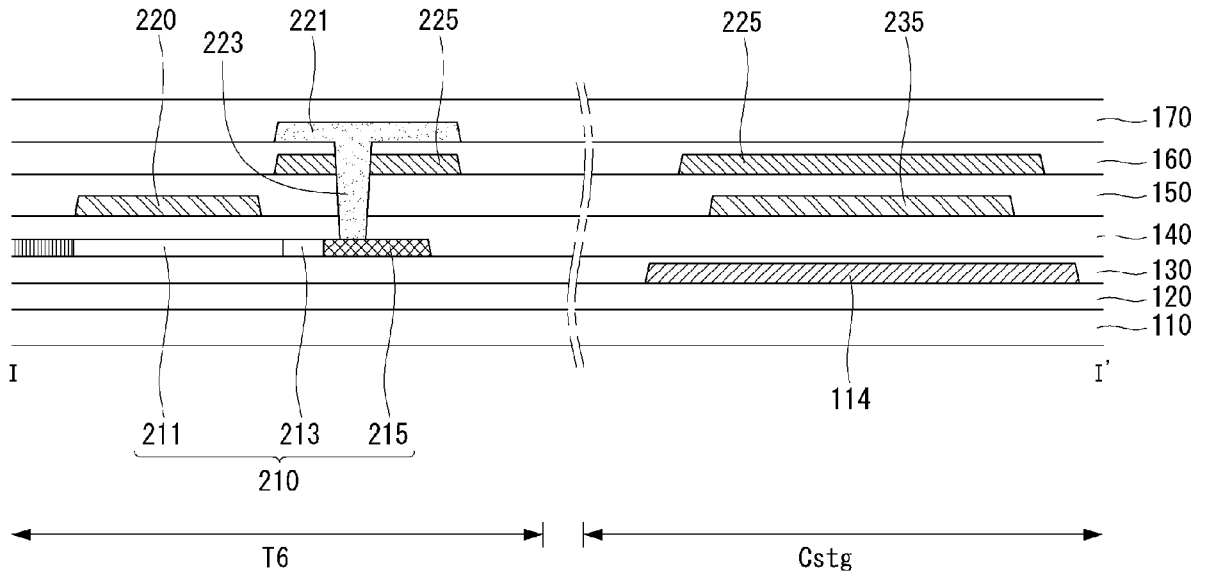
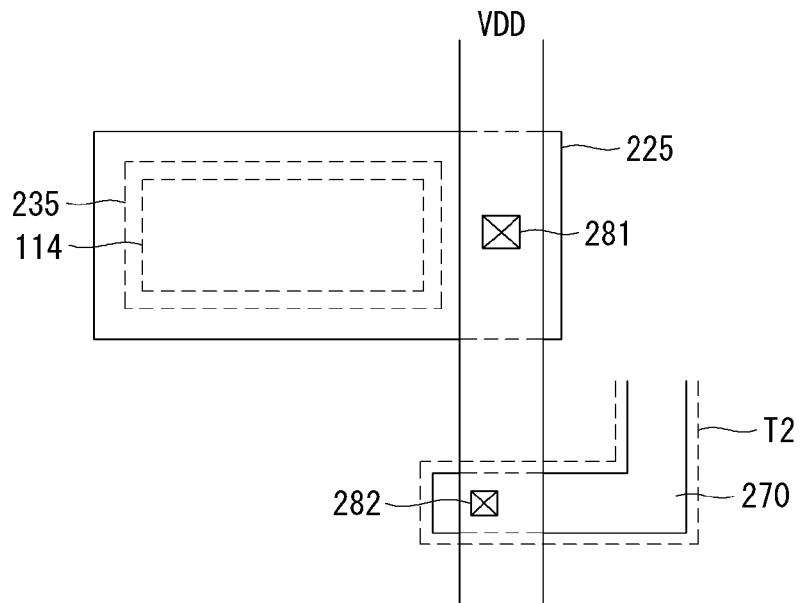


FIG. 21



| | | | |
|----------------|--|---------|------------|
| 专利名称(译) | 有机发光显示器 | | |
| 公开(公告)号 | EP3098804A2 | 公开(公告)日 | 2016-11-30 |
| 申请号 | EP2016171255 | 申请日 | 2016-05-25 |
| [标]申请(专利权)人(译) | 乐金显示有限公司 | | |
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| 当前申请(专利权)人(译) | LG DISPLAY CO. , LTD. | | |
| [标]发明人 | KIM DAEKYU KIM JUNGCHUL KANG HEEKWANG KWON JUNYOUNG | | |
| 发明人 | KIM, DAEKYU KIM, JUNGCHUL KANG, HEEKWANG KWON, JUNYOUNG | | |
| IPC分类号 | G09G3/3233 | | |
| CPC分类号 | G09G3/3225 H01L27/3244 H01L27/3248 G09G3/3233 G09G2300/0819 G09G2300/0861 G09G2310/0251 G09G2310/0256 G09G2310/0262 G09G2320/0238 G09G2320/043 G09G3/3241 G09G3/3266 G09G3/3291 G09G2300/0426 G09G2300/043 G09G2300/0814 G09G2310/0278 | | |
| 优先权 | 1020150075339 2015-05-28 KR 1020150169474 2015-11-30 KR 1020160053639 2016-04-30 KR | | |
| 其他公开文献 | EP3098804A3 | | |
| 外部链接 | Espacenet | | |

摘要(译)

有机发光显示器包括具有多个像素 (PXL) 的显示面板 (10) ;栅极驱动电路 (13) , 用于驱动显示面板 (10) 上的扫描线和发射线;以及驱动显示面板 (10) 上的数据线 (14) 的数据驱动电路 (12) , 布置在第n行 (n为自然数) 的每个像素 (PXL) 包括 : 有机发光二极管 (OLED) 具有连接到节点C的阳极和连接到低电平驱动电压输入端子的阴极;驱动晶体管 (DT) , 其栅极连接到节点A , 源极连接到节点D , 漏极连接到节点B , 驱动晶体管 (DT) 控制施加到有机物的驱动电流发光二极管 (OLED) ;第一晶体管 (T1) , 连接在数据线 (14) 和节点D之间;第二晶体管 (T2) , 连接在节点D和高电平驱动电压输入端之间;第三晶体管 (T3) , 连接到节点A和节点B;第四晶体管 (T4) , 连接到节点B和节点C;第五晶体管 (T5) , 连接在节点A和初始电压输入端之间;电容器 (Cstg) 连接在节点A和初始电压输入端子之间。

