



(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
16.11.2016 Bulletin 2016/46

(51) Int Cl.:
G09G 3/32 (2006.01) **G09G 3/3241** (2016.01)
G09G 3/3233 (2016.01)

(21) Application number: **16176868.4**

(22) Date of filing: **16.01.2014**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

- **Lee, Tak-Young**
Yongin-City, Gyeonggi-Do (KR)
- **In, Hai-Jung**
Yongin-City, Gyeonggi-Do (KR)
- **Chung, Bo-Yong**
Yongin-City, Gyeonggi-Do (KR)
- **Choi, Min-Hyuk**
Yongin-City, Gyeonggi-Do (KR)
- **Kim, Yong-Jae**
Yongin-City, Gyeonggi-Do (KR)

(30) Priority: **17.01.2013 KR 20130005453**
17.01.2013 KR 20130005454
28.06.2013 KR 20130075336

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
14151419.0 / 2 757 548

(74) Representative: **Gulde & Partner**
Patent- und Rechtsanwaltskanzlei mbB
Wallstraße 58/59
10179 Berlin (DE)

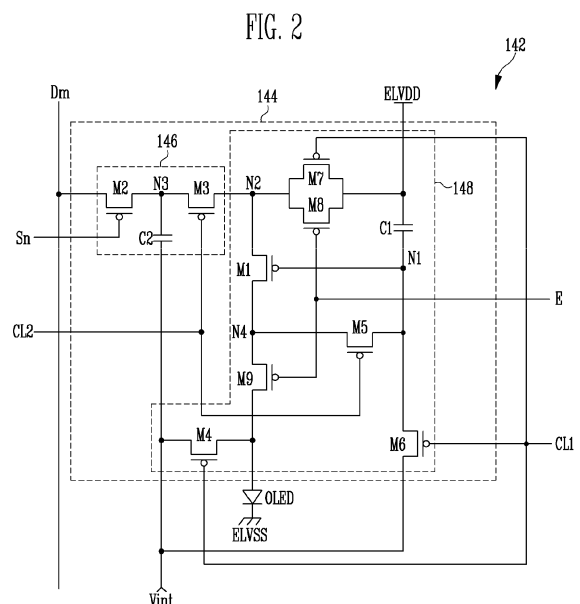
(71) Applicant: **Samsung Display Co., Ltd.**
Gyeonggi-do 17113 (KR)

(72) Inventors:
• **Park, Yong-Sung**
Yongin-City, Gyeonggi-Do (KR)

Remarks:
This application was filed on 29.06.2016 as a divisional application to the application mentioned under INID code 62.

(54) **PIXEL AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME**

(57) A pixel (142) includes an organic light emitting diode (OLED), a first driver (146) and a second driver (148). The second driver (148) controls an amount of current supplied from a first power source (ELVDD) to the organic light emitting diode (OLED), corresponding to a previous data signal. The first driver (146) stores a current data signal supplied from a data line (Dm) and supplies the previous data signal to the second driver (148). In the pixel (142), the second driver (148) includes a sixth transistor (M6) coupled between an initialization power source (Vinit) and a first node (N1), the sixth transistor (M6) being configured to turn on when a first control signal is supplied to a first control line (C11); and a seventh transistor (M7) coupled between the first power source (ELVDD) and a second node (N2) commonly coupled to the first and second drivers (146, 148), the seventh transistor (M7) being configured to turn on when the first control signal is supplied.



Description**BACKGROUND**

- 5 **[0001]** Embodiments of the present invention relate to a pixel and an organic light emitting display using the same.
[0002] With the recent advances in information technologies, the importance of a display as a mode of presenting information has increased. Accordingly, flat panel displays (FPDs) such as a liquid crystal display (LCD), an organic light emitting display and a plasma display panel (PDP) are being increasingly used.
10 **[0003]** An organic light emitting display displays images using organic light emitting diodes that emit light through recombination of electrons and holes. The organic light emitting display has a fast response speed and has low power consumption. Background prior art in the field is disclosed in US 2012/113077A1, EP 2 463 849 A1, EP 2 146 337 A1, US 2011/279484 A1, US 2008/243498 A1 und US 2011/090200 A1, for instance.

SUMMARY

- 15 **[0004]** The present invention provides a pixel according to claim 1 and an organic light emitting display according to claim 10 using the same, which can be at least driven at a low frequency. Advantageous embodiments are provided in the dependent claims.
[0005] Among them there is an embodiment, which can improve display quality by compensating for degradation of an organic light emitting diode.
20 **[0006]** According to an embodiment of the present invention, there is provided a pixel including: an organic light emitting diode; a second driver configured to control an amount of current supplied from a first power source to the organic light emitting diode, corresponding to a previous data signal; and a first driver configured to store a current data signal supplied from a data line and supply the previous data signal to the second driver, wherein the second driver includes: a sixth transistor coupled between an initialization power source and a first node coupled to a gate electrode of a first transistor, the sixth transistor being configured to turn on when a first control signal is supplied to a first control line; and a seventh transistor coupled between the first power source and a second node commonly coupled to the first and second drivers, the seventh transistor being configured to turn on when the first control signal is supplied.
25 **[0007]** The initialization power source may be set to a voltage lower than the data signal supplied to the data line.
[0008] The first driver may include a second transistor coupled between the data line and a third node, the second transistor being configured to turn on when a scan signal is supplied to a scan line; a third transistor coupled between the third and second nodes, the third transistor being configured to turn on when a second control signal is supplied; and a second capacitor coupled between the third node and the initialization power source.
30 **[0009]** The third and sixth transistors may have turn-on periods not overlapped with each other.
[0010] The second transistor may have a turn-on period not overlapped with those of the third and sixth transistors.
[0011] The second driver may include an eighth transistor coupled between the first power source and the second node coupled to a first electrode of the first transistor, the eighth transistor being configured to turn off when an emission control signal is supplied and to turn on otherwise; a fifth transistor coupled between the first node and a second electrode of the first transistor, the fifth transistor being configured to turn on when the second control signal is supplied; a ninth transistor coupled between the second electrode of the first transistor and an anode electrode of the organic light emitting diode, the ninth transistor being configured to turn off when the emission control signal is supplied and to turn on otherwise; and a first capacitor coupled between the first node and the first power source.
35 **[0012]** The eighth transistor may have a turn-on period not overlapped with those of the fifth and sixth transistors.
[0013] The fifth and sixth transistors may have turn-on periods not overlapped with each other.
[0014] The second driver may further include a fourth transistor coupled between the anode electrode of the organic light emitting diode and the initialization power source, the fourth transistor being configured to turn on when the first control signal is supplied.
40 **[0015]** The second driver may further include a fourth transistor coupled between the anode electrode of the organic light emitting diode and the initialization power source, the fourth transistor being configured to turn on when the second control signal is supplied.
[0016] The second driver may further include a fourth transistor positioned between the anode electrode of the organic light emitting diode and a second control line to which the second control signal is supplied, the fourth transistor having a gate electrode coupled to the second control line.
[0017] The second driver may further include a photodiode coupled in parallel to the first capacitor between the first node and the first power source.
45 **[0018]** The photodiode may control the increment of the voltage at the first node, corresponding to the luminance of the organic light emitting diode.
[0019] The photodiode may control the increment of the voltage at the first node, in proportion to the luminance of the
50
55

organic light emitting diode.

[0020] The second driver may further include a third capacitor coupled between the anode electrode of the organic light emitting diode and the second node.

[0021] According to an embodiment of the present invention, there is provided an organic light emitting display, including: a control driver configured to supply a first control signal to a first control line, and to supply a second control signal to a second control line during a first period in one frame; a scan driver configured to supply an emission control line to an emission control line during the first period, a second period and a third period in the one frame, and progressively supply a scan signal to scan lines during a fourth period in the one frame; a data driver configured to supply a data signal to data lines, in synchronization with the scan signal, during the fourth period in the one frame; and pixels positioned in an area defined by the scan lines and the data lines, the pixels storing a current data signal during a period in which the pixels emit light, corresponding to a previous data signal.

[0022] The previous data signal may be a data signal supplied in a previous frame, and the current data signal may be a data signal supplied in a current frame.

[0023] The scan driver may concurrently supply a scan signal to the scan lines during the third period.

[0024] The data driver may supply a reset voltage to the data lines during the third period.

[0025] The reset voltage may be set to a voltage in a voltage range of the data signal.

[0026] Each pixel may control an amount of current flowing from a first power source to a second power source via an organic light emitting diode, corresponding to the previous data signal.

[0027] The first power source may be set to a first voltage during the fourth period, and may be set to a second voltage different from the first voltage during the first to third periods.

[0028] The second voltage may be a voltage lower than the first voltage.

[0029] Each pixel may include an organic light emitting diode; a second driver configured according to an amount of current supplied from the first power source to the organic light emitting diode, corresponding to the previous data signal; and a first driver configured to store the current data signal, and to supply the previous data signal to the second driver.

[0030] The first driver may include a second transistor coupled between a corresponding one of the data lines and a third node, the second transistor being configured to turn on when a scan signal is supplied to a corresponding one of the scan lines; a third transistor coupled between the third node and a second node commonly coupled to the first and second drivers, the third transistor being configured to turn on when the second control signal is supplied; and a second capacitor coupled between the third node and an initialization power source.

[0031] The second driver may include a first transistor configured to have a first electrode coupled to the first power source via the second node commonly coupled to the first and second drivers, the first transistor having a gate electrode coupled to a first node; a fifth transistor coupled between a second electrode of the first transistor and the first node, the fifth transistor being configured to turn on when the second control signal is supplied; a sixth transistor coupled between the first node and the initialization power source, the sixth transistor being configured to turn on when the first control signal is supplied; a seventh transistor coupled between the second node and the first power source, the seventh transistor being configured to turn on when the first control signal is supplied; an eighth transistor coupled between the second node and the first power source, the eighth transistor being configured to turn off when the emission control signal is supplied and to turn on otherwise; and a ninth transistor coupled between the second electrode of the first transistor and an anode electrode of the organic light emitting diode, the ninth transistor being configured to turn off when the emission control signal is supplied and to turn on otherwise.

[0032] The initialization power source may be set to a voltage lower than the data signal.

[0033] The second driver may further include a fourth transistor coupled between the anode electrode of the organic light emitting diode and the initialization power source, the fourth transistor being configured to turn on when the first control signal is supplied.

[0034] The second driver may further include a fourth transistor coupled between the anode electrode of the organic light emitting diode and the initialization power source, the fourth transistor being configured to turn on when the second control signal is supplied.

[0035] The second driver may further include a fourth transistor positioned between the anode electrode of the organic light emitting diode and the second control line, the fourth transistor having a gate electrode coupled to the second control line.

[0036] The second driver may further include a photodiode coupled in parallel with the first capacitor between the first node and the first power source.

[0037] The photodiode may control the increment of the voltage at the first node, corresponding to the luminance of the organic light emitting diode.

[0038] According to an embodiment of the present invention, there is provided a pixel including an organic light emitting diode; a second driver configured to control an amount of current supplied from a first power source to the organic light emitting diode, corresponding to a previous data signal; and a first driver configured to store a current data signal supplied from a data line and to supply the previous data signal to the second driver, wherein the second driver comprises: a

fourth transistor coupled between an anode electrode of the organic light emitting diode and an initialization power source, the fourth transistor being configured to turn on when a first control signal is supplied; and a seventh transistor coupled between the first power source and a second node commonly coupled to the first and second drivers, the seventh transistor being configured to turn on when the first control signal is supplied.

5 [0039] The first driver may further include a second transistor coupled between the data line and a third node, the second transistor being configured to turn on when a scan signal is supplied to a scan line; a third transistor coupled between the third and second nodes, the third transistor being configured to turn on when a second control signal is supplied; and a second capacitor coupled between the third node and the initialization power source.

10 [0040] The second driver may further include a fifth transistor coupled between a first node coupled to a gate electrode of a first transistor and a second electrode of the first transistor, the fifth transistor being configured to turn on when a second control signal is supplied; a sixth transistor coupled between the initialization power source and the first node, the sixth transistor being configured to turn on when the first control signal is supplied; an eighth transistor coupled between the first power source and the second node, the second node being coupled to a first electrode of the first transistor, the eighth transistor being configured to turn off when an emission control signal is supplied and to turn on otherwise; a ninth transistor coupled between the second electrode of the first transistor and the anode electrode of the organic light emitting diode, the ninth transistor being configured to turn off when the emission control signal is supplied and to turn on otherwise; and a first capacitor coupled between the first node and the first power source.

15 [0041] The eighth transistor may have a turn-on period not overlapped with those of the fifth and sixth transistors.

[0042] The fifth and sixth transistors may have turn-on periods not overlapped with each other.

20 [0043] The photodiode may control the increment of the voltage at the first node, in proportion to the luminance of the organic light emitting diode.

[0044] The second driver may further include a third capacitor coupled between the anode electrode of the organic light emitting diode and the second node.

25 BRIEF DESCRIPTION OF THE DRAWINGS

[0045] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

30 [0046] In the drawing figures, dimensions may be exaggerated for clarity of illustration. It will be understood that when an element is referred to as being "between" two elements, it can be the only element between the two elements, or one or more intervening elements may also be present. Like reference numerals refer to like elements throughout.

35 FIG. 1 is a diagram illustrating an organic light emitting display according to an embodiment of the present invention.

FIG. 2 is a circuit diagram illustrating a pixel according to a first embodiment of the present invention.

FIG. 3 is a waveform diagram illustrating a driving method according to an embodiment of the present invention.

FIG. 4 is a waveform diagram illustrating a driving method according to another embodiment of the present invention.

40 FIG. 5 is a waveform diagram illustrating a driving method according to still another embodiment of the present invention.

FIG. 6 is a diagram illustrating an embodiment of a driving frequency in 3D driving.

FIG. 7 is a circuit diagram illustrating a pixel according to a second embodiment of the present invention.

FIG. 8 is a circuit diagram illustrating a pixel according to a third embodiment of the present invention.

45 FIG. 9 is a graph illustrating the increment of the voltage at a first node, corresponding to degradation of an organic light emitting diode.

FIG. 10 is a circuit diagram illustrating a pixel according to a fourth embodiment of the present invention.

FIG. 11 is a circuit diagram illustrating a pixel according to a fifth embodiment of the present invention.

FIG. 12 is a circuit diagram illustrating a pixel according to a sixth embodiment of the present invention.

50 DETAILED DESCRIPTION

[0047] Hereinafter, certain exemplary embodiments according to the present invention will be described with reference to the accompanying drawings. Here, when a first element is described as being coupled to a second element, the first element may be directly coupled to the second element or may be indirectly coupled to the second element via a third element. Further, some of the elements that are not essential to the complete understanding of the invention are omitted for clarity. Also, like reference numerals refer to like elements throughout.

55 [0048] FIG. 1 is a diagram illustrating an organic light emitting display according to an embodiment of the present invention.

[0049] Referring to FIG. 1, the organic light emitting display according to this embodiment includes pixels positioned in an area defined by scan lines S1 to Sn and data lines D1 to Dm, a display unit 140 including the pixels 142, a scan driver 110 for driving the scan lines S1 to Sn and an emission control line E, a control driver 120 for driving first and second control lines CL1 and CL2, a data driver 130 for driving the data lines D1 to Dm, and a timing controller 150 for

5

controlling the scan driver 110, the control driver 120 and the data driver 130.

[0050] The scan driver 110 supplies a scan signal to the scan lines S1 to Sn. For example, the scan driver 110, as shown in FIG. 3, may progressively supply the scan signal to the scan lines S1 to Sn during a fourth period T4 in one frame 1 F. The scan driver 110, as shown in FIG. 4, may concurrently (e.g., simultaneously) supply the scan signal to the scan lines S1 to Sn during a third period T3 in the one frame 1 F.

10

[0051] The scan driver 110 supplies an emission control signal to the emission control line E commonly coupled to the pixels 142. For example, the scan driver 110 may supply the emission control signal to the emission control line E during the other periods T1, T2 and T3 except the fourth period T4 in the one frame 1 F. Here, the scan signal supplied from the scan driver 110 is set to a voltage (e.g., a low voltage) at which transistors included in the pixels 142 are turned on, and the emission control signal is set to a voltage (e.g., a high voltage) at which the transistors are turned off.

15

[0052] The control driver 120 supplies a first control signal to the first control line CL1 commonly coupled to the pixels 142, and supplies a second control signal to the second control line CL2 commonly coupled to the pixels 142. Here, the first and second control signals CL1 and CL2 are not overlapped with each other. For example, the control driver 120 supplies the first control signal to the first control line CL1 during a first period T1 in the one frame 1 F, and supplies the second control signal to the second control line CL2 during a second period T2 in the one frame 1 F. Here, the first and second control signals are set to a voltage (e.g., a low voltage) at which the transistors can be turned on.

20

[0053] The data driver 130 supplies a data signal to the data lines D1 to Dm so in synchronization with the scan signal supplied to the scan lines S1 to Sn during the fourth period T4 in the one frame 1 F.

[0054] Here, the data driver 130 may alternately supply left and right data signals every frame for the purpose of 3D driving. Additionally, the data driver 130 may supply a reset voltage Vr to the data lines D1 to Dm during the third period T3 in the one frame 1 F. Here, the reset voltage Vr may be set to a voltage in a voltage range of the data signal.

25

[0055] The timing controller 150 controls the scan driver 110, the control driver 120 and the data driver 130, corresponding to a synchronization signal supplied from the outside of the organic light emitting display.

[0056] The display unit 140 includes the pixels 142 positioned in the area defined by the scan lines S1 to Sn and the data lines D1 to Dm. The pixels 142, during the fourth period T4, charge a data signal (current data signal) of a current frame and concurrently (e.g., simultaneously) emit light corresponding to a data signal (e.g., a previous data signal) of a previous frame. To this end, the pixels 142, during the fourth period T4, control an amount of current flowing from a first power source ELVDD to a second power source ELVSS via organic light emitting diodes.

30

[0057] Although it has been illustrated in FIG. 1 that, for convenience of illustration, the emission control line E is coupled to the scan driver 110, and the control lines CL1 and CL2 are coupled to the control driver 120, the present invention is not limited thereto. In practice, the emission control line E and the control lines CL1 and CL2 may be coupled to various drivers. For example, the emission control line E and the control lines CL1 and CL2 may be commonly coupled to the scan driver 110.

35

[0058] FIG. 2 is a circuit diagram illustrating a pixel according to a first embodiment of the present invention. For convenience of illustration, a pixel coupled to an m-th data line Dm and an n-th scan line Sn will be shown in FIG. 2.

40

[0059] Referring to FIG. 2, the pixel 142 according to this embodiment includes an organic light emitting diode OLED and a pixel circuit 144 that controls an amount of current supplied to the organic light emitting diode OLED.

[0060] An anode electrode of the organic light emitting diode OLED is coupled to the pixel circuit 144, and a cathode electrode of the organic light emitting diode OLED is coupled to the second power source ELVSS. The organic light emitting diode OLED generates light (e.g., light having a predetermined luminance) corresponding to an amount of current supplied from the pixel circuit 144. The second power source ELVSS is set to a voltage lower than that of the first power source ELVDD so that a current can flow through the organic light emitting diode OLED.

45

[0061] The pixel circuit 144 includes a first driver 146 for storing the current data signal, and a second driver 148 for controlling an amount of the current supplied to the organic light emitting diode OLED, corresponding to the previous data signal.

50

[0062] The first driver 146 stores the current data signal supplied from the data line Dm and concurrently (e.g., simultaneously) supplies the previous data signal stored in the previous frame to the second driver 148. To this end, the first driver 146 includes a second transistor M2, a third transistor M3 and a second capacitor C2.

[0063] A first electrode of the second transistor M2 is coupled to the data line Dm, and a second electrode of the second transistor M2 is coupled to a third node N3. A gate electrode of the second transistor M2 is coupled to the scan line Sn. The second transistor M2 is turned on when the scan signal is supplied to the scan line Sn, to supply the data signal from the data line Dm to the third node N3.

55

[0064] A first electrode of the third transistor M3 is coupled to the third node N3, and a second electrode of the third transistor M3 is coupled to the second driver 148 (e.g., at a second node N2). A gate electrode of the third transistor M3

is coupled to the second control line CL2. The third transistor M3 is turned on when the second control signal is supplied to the second control line CL2, to allow the third and second nodes N3 and N2 to be electrically coupled to each other.

[0065] The second capacitor C2 is coupled between the third node N3 and a fixed voltage source (e.g., an initialization power source Vint). The second capacitor C2 charges a voltage corresponding to the current data signal during a period in which the second transistor M2 is turned on.

[0066] The second driver 148 charges a voltage corresponding to the previous data signal supplied from the first driver 146, and controls an amount of current flowing from the first power source ELVDD to the second power source ELVSS via the organic light emitting diode OLED, corresponding to the charged voltage. To this end, the second driver 148 includes a first transistor M1, fourth to ninth transistors M4 to M9, and a first capacitor C1.

[0067] A first electrode of the first transistor (e.g., a driving transistor) M1 is coupled to the second node N2, and a second electrode of the first transistor M1 is coupled to a fourth node N4. A gate electrode of the first transistor M1 is coupled to a first node N1. The first transistor M1 controls an amount of current supplied to the organic light emitting diode OLED, corresponding to a voltage applied to the first node N1.

[0068] A first electrode of the fourth transistor M4 is coupled to the anode electrode of the organic light emitting diode OLED, and a second electrode of the fourth transistor M4 is coupled to the initialization power source Vint. A gate electrode of the fourth transistor M4 is coupled to the first control line CL1. The fourth transistor M4 is turned on when the first control signal is supplied to the first control line CL1, to supply the voltage of the initialization power source Vint to the anode electrode of the organic light emitting diode OLED. Here, the initialization power source Vint is set to a voltage lower than the data signal. For example, the initialization power source Vint may be set to a voltage lower than that obtained by subtracting the absolute threshold voltage of the first transistor M1 from the data signal having the lowest voltage.

[0069] A first electrode of the fifth transistor M5 is coupled to the fourth node N4, and a second electrode of the fifth transistor M5 is coupled to the first node N1. A gate electrode of the fifth transistor M5 is coupled to the second control line CL2. The fifth transistor M5 is turned on when the second control signal is supplied to the second control line CL2, to allow the first and fourth nodes N1 and N4 to be electrically coupled to each other. When the first and fourth nodes N1 and N4 are electrically coupled to each other, the first transistor M1 is diode-coupled.

[0070] A first electrode of the sixth transistor M6 is coupled to the first node N1, and a second electrode of the sixth transistor M6 is coupled to the initialization power source Vint. A gate electrode of the sixth transistor M6 is coupled to the first control line CL1. The sixth transistor M6 is turned on when the first control signal is supplied to the first control line CL1, to supply the voltage of the initialization power source Vint to the first node N1.

[0071] A first electrode of the seventh transistor M7 is coupled to the first power source ELVDD, and a second electrode of the seventh transistor M7 is coupled to the second node N2. A gate electrode of the seventh transistor M7 is coupled to the first control line CL1. The seventh transistor M7 is turned on when the first control signal is supplied to the first control line CL1, to supply the voltage of the first power source ELVDD to the second node N2.

[0072] A first electrode of the eighth transistor M8 is coupled to the first power source ELVDD, and a second electrode of the eighth transistor M8 is coupled to the second node N2. A gate electrode of the eighth transistor M8 is coupled to the emission control line E. The eighth transistor M8 is turned off when the emission control signal is supplied to the emission control line E, and is turned on when the emission control signal is not supplied.

[0073] A first electrode of the ninth transistor M9 is coupled to the fourth node N4, and a second electrode of the ninth transistor M9 is coupled to the anode electrode of the organic light emitting diode OLED. A gate electrode of the ninth transistor M9 is coupled to the emission control line E.

[0074] The ninth transistor M9 is turned off when the emission control signal is supplied to the emission control line E, and is turned on when the emission control signal is not supplied.

[0075] The first capacitor C1 is coupled between the first power source ELVDD and the first node N1.

[0076] The first capacitor C1 charges a voltage corresponding to the previous data signal and the threshold voltage of the first transistor M1.

[0077] FIG. 3 is a waveform diagram illustrating a driving method according to an embodiment of the present invention.

[0078] Referring to FIG. 3, one frame according to this embodiment is divided into first to fourth periods T1 to T4.

[0079] First, the emission control signal is supplied during the first to third periods T1 to T3, and the emission control signal is not supplied during the fourth period T4. When the emission control signal is supplied, the eighth and ninth transistors M8 and M9 are turned off. When the ninth transistor M9 is turned off, the first transistor M1 and the organic light emitting diode OLED are electrically decoupled from each other, and accordingly, the organic light emitting diode OLED is set in the non-emission state during the first to third periods T1 to T3.

[0080] The first control signal is supplied to the first control line CL1 during the first period T1. When the first control signal is supplied to the first control line CL1, the fourth, sixth and seventh transistors M4, M6 and M7 are turned on.

[0081] When the fourth transistor M4 is turned on, the voltage of the initialization power source Vint is supplied to the anode electrode of the organic light emitting diode OLED. When the voltage of the initialization power source Vint is supplied to the anode electrode of the organic light emitting diode OLED, the voltage charged in a parasitic capacitor

(not shown) equivalently formed in the organic light emitting diode OLED is discharged.

[0082] When the sixth transistor M6 is turned on, the voltage of the initialization power source Vint is supplied to the first node N1. When the seventh transistor M7 is turned on, the voltage of the first power source ELVDD is supplied to the second node N2. Here, the initialization power source Vint is set to a voltage lower than the data signal, and hence the first transistor M1 is set in an on-bias state during the first period T1. Then, the first transistor M1 is initialized in the on-bias state, thereby improving display quality.

[0083] The second control signal is supplied to the second control line CL2 during the second period T2. When the second control signal is supplied to the second control line CL2, the third and fifth transistors M3 and M5 are turned on. When the fifth transistor M5 is turned on, the first transistor M1 is diode-coupled. When the third transistor M3 is turned on, the voltage of the previous data signal stored in the second capacitor C2 is supplied to the second node N2. In this case, the voltage at the first node N1 is initialized as the voltage of the initialization power source Vint, lower than the data signal, and hence the first transistor M1 is turned on.

[0084] When the first transistor M1 is turned on, the voltage of the data signal, applied to the second node N2, is supplied to the first node N1 via the diode-coupled first transistor M1. In this case, the first capacitor C1 stores a voltage corresponding to the data signal and the threshold voltage of the first transistor M1.

[0085] The supply of the emission control signal to the emission control line E is maintained during the third period T3.

[0086] The supply of the emission control signal to the emission control line E is stopped during the fourth period T4. When the supply of the emission control signal to the emission control line E is stopped, the eighth and ninth transistors M8 and M9 are turned on. When the eighth transistor M8 is turned on, the first power source ELVDD and the second node N2 are electrically coupled to each other. When the ninth transistor M9 is turned on, the fourth node N4 and the organic light emitting diode OLED are electrically coupled to each other. Then, the first transistor M1 controls an amount of the current flowing from the first power source ELVDD to the second power source ELVSS via the organic light emitting diode OLED, corresponding to the voltage applied to the first node N1. In this case, the organic light emitting diode OLED generates light (e.g., light having a predetermined luminance) corresponding to the amount of current supplied thereto.

[0087] The scan signal is progressively supplied to the scan lines S1 to Sn during the fourth period T4.

[0088] When the scan signal is progressively supplied to the scan lines S1 to Sn, the second transistor M2 included in each pixel 142 for each horizontal line is turned on. When the second transistor M2 is turned on, the current data signal from a data line (any one of D1 to Dm) is supplied to the third node N3 included in each pixel 142. In this case, the second capacitor C2 charges a voltage corresponding to the current data signal. In practice, according to embodiments of the present invention, images are displayed by repeating the aforementioned procedure.

[0089] FIG. 4 is a waveform diagram illustrating a driving method according to another embodiment of the present invention. In reference to FIG. 4, detailed descriptions of components that are substantially identical to those of FIG. 3 will be omitted.

[0090] Referring to FIG. 4, during the third period T3 in the driving method according to this embodiment, the scan signal is concurrently (e.g., simultaneously) supplied to the scan lines S1 to Sn, and the reset voltage Vr is supplied to the data lines D1 to Dm in synchronization with the scan signal.

[0091] When the scan signal is supplied to the n-th scan line Sn during the third period T3, the second transistor M2 is turned on. When the second transistor M2 is turned on, the reset voltage Vr is supplied to the third node N3. That is, the voltage at the third node N3 included in each pixel 142 is initialized as the reset voltage Vr during the third period T3.

[0092] Subsequently, the scan signal is progressively supplied to the scan lines S1 to Sn during the fourth period T4. When the scan signal is supplied to the n-th scan line Sn, the second transistor M2 is turned on. When the second transistor M2 is turned on, the current data signal from the data line Dm is supplied to the third node N3. In this case, the second capacitor C2 charges a voltage corresponding to the current data signal.

[0093] Here, the third node N3 is initialized with the reset voltage Vr during the third period T3, and hence a uniform voltage corresponding to the current data signal may be charged in the second capacitor C2 during the fourth period T4.

[0094] For example, the voltage at the third node N3 included in each pixel 142 is set corresponding to the voltage of the previous data signal after the second period T2. That is, the voltages at the third nodes N3 included in the respective pixels 142 are set different from one another, corresponding to the previous data signal. Thus, in a case where the voltage at the third node N3 is not initialized, the voltage of the current data signal stored in the second capacitor C2 is altered by the voltage of the previous data signal, and accordingly, a crosstalk phenomenon may occur.

[0095] FIG. 5 is a waveform diagram illustrating a driving method according to still another embodiment of the present invention. In reference to FIG. 5, detailed descriptions of components that are substantially identical to those of FIG. 4 will be omitted.

[0096] Referring to FIG. 5, in the driving method according to this embodiment, the voltage of the first power source ELVDD is changed. That is, the first power source ELVDD is set to a first voltage VDD1 during the fourth period T4 in which the pixels 142 emit light, and is set to a second voltage VDD2 lower than the first voltage VDD1 during the first to third periods T1 to T3 in which the pixels 142 do not emit light. Here, the second voltage VDD2 is set to a voltage

higher than that of the initialization power source Vint so that the first transistor M1 is set in the on-bias state during the first period T1.

[0097] For example, the first power source ELVDD is set to the second voltage VDD2 during the first to third periods T1 to T3. The voltage of the first power source ELVDD is raised to the first voltage VDD1 during the fourth period T4.

[0098] When the voltage of the first power source ELVDD is raised to the first voltage VDD1 during the fourth period T4, the voltage at the first node N1, which is set in a floating state, is also raised.

[0099] When the voltage at the first node N1 is raised as described above, it is possible to improve the ability to express (or represent) black.

[0100] For example, the first capacitor C1 is charged using the voltage charged in the second capacitor C2 during the second period T2. In this case, the voltage charged in the first capacitor C1 is set to a voltage lower than a desired voltage, and therefore, the organic light emitting diode OLED emits a small amount of light when the black is expressed (or represented). Accordingly, in this embodiment, the voltage of the first power source ELVDD and the voltage at the first node N1 corresponding thereto are raised during the fourth period T4, so that it is possible to prevent the organic light emitting diode OLED from emitting a small amount of light when the black is expressed (or represented).

[0101] FIG. 6 is a diagram illustrating an embodiment of a driving frequency in 3D driving.

[0102] Referring to FIG. 6, the organic light emitting display according to embodiments of the present invention receives a data signal during an emission period. That is, the pixels 142 store a voltage corresponding to the right (or left) data signal during a period in which an image corresponding to the left (or right) data signal. Thus, in embodiments of the present invention, a 3D image can be implemented at a driving frequency of 120Hz. In FIG. 6, RD represents a right data signal, and LD represents a left data signal. In addition, R represents emission corresponding to the right data signal, and L represents emission corresponding to the left data signal.

[0103] FIG. 7 is a circuit diagram illustrating a pixel according to a second embodiment of the present invention. In FIG. 7, components that are substantially identical to those of FIG. 2 are designated by like reference numerals, and their detailed descriptions will be omitted.

[0104] Referring to FIG. 7, the pixel 142 according to this embodiment includes a pixel circuit 200 and the organic light emitting diode OLED.

[0105] The pixel circuit 200 includes the first driver 146 for storing the current data signal, and a second driver 202 for controlling an amount of the current supplied to the organic light emitting diode OLED, corresponding to the previous data signal.

[0106] The second driver 202 includes a fourth transistor M4' coupled between the anode electrode of the organic light emitting diode OLED and the initialization power source Vint. A gate electrode of the fourth transistor M4' is coupled to the second control line CL2. The fourth transistor M4' is turned on when the second control signal is supplied to the second control line CL2, to supply the voltage of the initialization power source Vint to the anode electrode of the organic light emitting diode OLED. The operating process of the pixel according to this embodiment, except the fourth transistor M4', is substantially the same as that of the pixel according to the first embodiment, and therefore, its detailed description will be omitted.

[0107] FIG. 8 is a circuit diagram illustrating a pixel according to a third embodiment of the present invention. In FIG. 8, components that are substantially identical to those of FIG. 2 are designated by like reference numerals, and their detailed descriptions will be omitted.

[0108] Referring to FIG. 8, the pixel 142 according to this embodiment includes a pixel circuit 210 and the organic light emitting diode OLED.

[0109] The pixel circuit 210 includes the first driver 146 for storing the current data signal, and a second driver 212 for controlling an amount of the current supplied to the organic light emitting diode OLED, corresponding to the previous data signal.

[0110] The second driver 212 includes a photodiode PD coupled in parallel to the first capacitor C1 between the first power source ELVDD and the first node N1. The photodiode PD controls an amount of current supplied from the first power source ELVDD to the first node N1, i.e., the voltage at the first node N1, corresponding to the brightness of the organic light emitting diode OLED. In practice, the photodiode PD controls the voltage at the first node N1 so that the degradation of the organic light emitting diode OLED can be compensated for.

[0111] The operating process of the pixel will be described. During the fourth period T4, the photodiode PD controls an amount of current flowing from the first power source ELVDD to the first node N1, i.e., an increment of the voltage at the first node N1, in proportion to the luminance of the organic light emitting diode OLED. In other words, the photodiode PD controls the voltage at the first node N1 to be increased as the luminance of the organic light emitting diode OLED increases.

[0112] For example, as the organic light emitting diode OLED is degraded, the organic light emitting diode OLED generates light with a low luminance, corresponding to the same gray level. Thus, the voltage at the first node N1 is changed by the photodiode PD, corresponding to the degradation of the organic light emitting diode OLED. That is, although a data signal with the same gray level is supplied, an increment of the voltage at the first node N1 is changed

by the photodiode PD.

[0113] In a case where the organic light emitting diode OLED emits light, corresponding to a specific gray level j (j is a natural number), the increment of the voltage at the first node N1 when the organic light emitting diode OLED is degraded is set lower by a first voltage $V1$ than that of the voltage at the first node N1 when the organic light emitting diode OLED is not degraded. That is, in the described embodiment of the present invention, the increment of the voltage at the first node N1 is set low as the organic light emitting diode OLED is degraded, and accordingly, it is possible to compensate for a decrease in luminance, caused by the degradation of the organic light emitting diode OLED.

[0114] In practice, according to embodiments of the present invention, an amount of current supplied to the organic light emitting diode OLED may be represented as shown in Equation 1.

Equation 1

$$I_{oled} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (ELVDD - V_{N1} - |V_{th}|)^2$$

$$I_{oled} = \frac{1}{2} \mu C_{ox} \frac{W}{L} \left(ELVDD - \frac{C2Vdata + C1Vint}{C2 + C1} - \Delta V_{PD} \right)^2$$

[0115] In Equation 1, μ denotes the mobility of the first transistor M1, C_{ox} denotes the gate capacitance of the first transistor, V_{th} denotes the threshold voltage of the first transistor M1, and W and L denote the channel width/length ratio of the first transistor M1. In addition, $Vdata$ denotes the voltage of the data signal, and ΔV_{PD} denotes a variation in voltage, caused by the photodiode PD. Referring to Equation 1, an amount of the current supplied to the organic light emitting diode OLED is determined by the voltage of the data signal and the variation in voltage, caused by the photodiode PD. In the variation in voltage, caused by the photodiode PD, an increment of the voltage at the first node N1 is set low as the organic light emitting diode OLED is degraded. Accordingly, it is possible to compensate for a decrease in luminance of the organic light emitting diode OLED.

[0116] The operating process of the pixel 142 according to this embodiment, except that the photodiode PD is added so that the degradation of the organic light emitting diode OLED is compensated for, is substantially identical to that of the pixel in the first embodiment shown in FIG. 2. In practice, the pixel 142 according to this embodiment can be driven with the driving waveforms shown in FIGS. 3 to 5.

[0117] FIG. 10 is a circuit diagram illustrating a pixel according to a fourth embodiment of the present invention. In FIG. 10, components that are substantially identical to those of FIG. 7 are designated by like reference numerals, and their detailed descriptions will be omitted.

[0118] Referring to FIG. 10, the pixel 142 according to this embodiment includes a pixel circuit 220 and the organic light emitting diode OLED.

[0119] The pixel circuit 220 includes the first driver 146 for storing the current data signal, and a second driver 222 for controlling an amount of the current supplied to the organic light emitting diode OLED, corresponding to the previous data signal.

[0120] The second driver 222 includes a photodiode PD coupled in parallel to the first capacitor C1 between the first power source ELVDD and the first node N1. The photodiode PD controls an amount of current supplied from the first power source ELVDD to the first node N1, i.e., the voltage at the first node N1, corresponding to the brightness of the organic light emitting diode OLED. In practice, the photodiode PD controls the voltage at the first node N1 so that the degradation of the organic light emitting diode OLED can be compensated for.

[0121] FIG. 11 is a circuit diagram illustrating a pixel according to a fifth embodiment of the present invention. In FIG. 11, components that are substantially identical to those of FIG. 7 are designated by like reference numerals, and their detailed descriptions will be omitted.

[0122] Referring to FIG. 11, the pixel 142 according to this embodiment includes a pixel circuit 230 and the organic light emitting diode OLED.

[0123] The pixel circuit 230 includes the first driver 146 for storing the current data signal, and a second driver 232 for controlling an amount of the current supplied to the organic light emitting diode OLED, corresponding to the previous data signal.

[0124] The second driver 232 includes a third capacitor C3 coupled between the second node N2 and the anode electrode of the organic light emitting diode OLED. The third capacitor C3 controls the voltage at the second node N2, corresponding to the voltage at the anode electrode of the organic light emitting diode OLED. For example, the third capacitor C3 controls the voltage at the second node N2 so that the degradation of the organic light emitting diode OLED is compensated for. The pixel 142 according to this embodiment can be driven with any one of the driving waveforms shown in FIGS. 3 to 5.

[0125] The operating process of the pixel will be described in conjunction with the driving waveform of FIG. 3. The emission control signal is supplied to the emission control line E during the first to third periods T1 to T3, and the emission control signal is not supplied to the emission control line E during the fourth period T4. When the emission control signal is supplied to the emission control line E, the eighth and ninth transistors M8 and M9 are turned off. Then, the first transistor M1 and the organic light emitting diode OLED are electrically decoupled from each other, and accordingly, the organic light emitting diode OLED is set in the non-emission state during the first to third periods T1 to T3. When the ninth transistor M9 is turned off, the anode electrode of the organic light emitting diode OLED is set to a voltage (e.g., a predetermined voltage) *Voled*.

[0126] The first control signal is supplied to the first control line CL1 during the first period T1 so that the sixth and seventh transistors M6 and M7 are turned on. When the sixth transistor M6 is turned on, the voltage of the initialization power source *Vint* is supplied to the first node N1. When the seventh transistor M7 is turned on, the voltage of the first power source ELVDD is supplied to the second node N2. In this case, the first transistor M1 is initialized in an on-bias state.

[0127] The second control signal is supplied to the second control line CL2 during the second period T2.

[0128] When the second control signal is supplied to the second control line CL2, the third, fourth and fifth transistors M3, M4' and M5 are turned on.

[0129] When the fifth transistor M5 is turned on, the first transistor M1 is diode-coupled. When the third transistor M3 is turned on, the voltage of the previous data signal stored in the second capacitor C2 is supplied to the second node N2. When the fourth transistor M4' is turned on, the voltage *Voled* at the anode electrode of the organic light emitting diode OLED is dropped to the voltage of the initialization power source *Vint*. In this case, the voltage at the second node N2 is dropped, corresponding to a decrement of the voltage at the anode electrode of the organic light emitting diode OLED, by coupling of the third capacitor C3.

[0130] When the voltage of the previous data signal is supplied to the second node N2, the first transistor M1 is turned on. When the first transistor M1 is turned on, the voltage applied to the second node N2 is supplied to the first node N1 via the diode-coupled first transistor M1. In this case, the first capacitor C1 stores a voltage corresponding to the previous data signal, the threshold voltage of the first transistor M1 and the degradation of the organic light emitting diode OLED.

[0131] For example, when the fourth transistor M4' is turned on, the voltage at the anode electrode of the organic light emitting diode OLED is changed as shown in Equation 2.

Equation 2

$$\Delta Voled = Voled - (Vint)$$

[0132] In Equation 2, *Voled* denotes the voltage at the anode electrode of the organic light emitting diode OLED, applied during the first period T1. Referring to Equation 2, the voltage at the anode electrode of the organic light emitting diode OLED during the second period T2 is dropped from the voltage *Voled* applied during the first period T1 to the voltage of the initialization power source *Vint*.

[0133] In this case, the variation ($\Delta Voled$) in the voltage at the anode electrode of the organic light emitting diode OLED is determined by the degradation of the organic light emitting diode OLED. In practice, as the organic light emitting diode OLED is degraded, the resistance of the organic light emitting diode OLED is increased. Accordingly, as the organic light emitting diode OLED is degraded, the variation ($\Delta Voled$) in the voltage at the anode electrode of the organic light emitting diode OLED is increased.

[0134] For example, the resistance of the organic light emitting diode OLED is increased corresponding to the degradation of the organic light emitting diode OLED. When the resistance of the organic light emitting diode OLED is increased, the voltage *Voled* at the anode electrode of the organic light emitting diode OLED, which is applied during the first period T1, is increased. Thus, as the organic light emitting diode OLED is degraded, a decrement of the voltage at the second node N2 is increased, and accordingly, the degradation of the organic light emitting diode OLED can be compensated for. In other words, when the voltage at the second node N2 is dropped, the voltage at the first node N1 is also dropped. Accordingly, as the organic light emitting diode OLED is degraded, an amount of the current supplied to the organic light emitting diode OLED is increased, thereby compensating for the degradation of the organic light emitting diode OLED.

[0135] The supply of the emission control signal to the emission control line E is maintained during the third period T3.

[0136] The supply of the emission control signal to the emission control line En is stopped during the fourth period T4, so that the eighth and ninth transistors M8 and M9 are turned on. When the eighth transistor M8 is turned on, the first power source ELVDD and the second node N2 are electrically coupled to each other. When the ninth transistor M9 is turned on, the fourth node N4 and the anode electrode of the organic light emitting diode OLED are electrically connected to each other. Then, the first transistor M1 controls an amount of the current flowing from the first power source ELVDD to the second power source ELVSS via the organic light emitting diode OLED, corresponding to the voltage applied to the first node N1. In this case, the organic light emitting diode OLED generates light (e.g., light with a predetermined

luminance) corresponding to an amount of current supplied thereto.

5 [0137] The scan signal is progressively supplied to the scan lines S1 to Sn during the fourth period T4. When the scan signal is progressively supplied to the scan lines S1 to Sn, the second transistor M2 included in each pixel 142 is turned on for each horizontal line. When the second transistor M2 is turned on, the current data signal from a data line (any one of D1 to Dm) is supplied to the third node N3 included in each pixel 142. In this case, the second capacitor C2 charges a voltage corresponding to the current data signal. In practice, in embodiments according to the present invention, images are displayed by repeating the aforementioned procedure.

10 [0138] FIG. 12 is a circuit diagram illustrating a pixel according to a sixth embodiment of the present invention. In FIG. 12, components that are substantially identical to those of FIG. 11 are designated by like reference numerals, and their detailed descriptions will be omitted.

[0139] Referring to FIG. 12, the pixel according to this embodiment includes a pixel circuit 240 and the organic light emitting diode OLED.

15 [0140] The pixel circuit 240 includes the first driver 146 for storing the current data signal, and a second driver 242 for controlling an amount of the current supplied to the organic light emitting diode OLED, corresponding to the previous data signal.

20 [0141] The second driver 242 includes a fourth transistor M4" coupled between the second control line CL2 and the organic light emitting diode OLED. A gate electrode of the fourth transistor M4" is coupled to the second control line CL2. That is, the fourth transistor M4" is diode-coupled. The fourth transistor M4" allows the voltage at the anode electrode of the organic light emitting diode OLED to be dropped to approximately the voltage of the second control signal when the second control signal is supplied to the second control line CL2.

[0142] That is, the operating process of the pixel according to this embodiment, except that the voltage Voled at the anode electrode of the organic light emitting diode OLED is dropped to the voltage of the second control signal other than that of the initialization power source Vint, is substantially identical to that of the pixel according to the fifth embodiment shown in FIG. 11. Therefore, its detailed description will be omitted.

25 [0143] Although it has been described in embodiments according to the present invention that the transistors are shown as PMOS transistors for convenience of illustration, the present invention is not limited thereto. In other words, the transistors may be formed as NMOS transistors.

30 [0144] In embodiments of the present invention, the organic light emitting diode OLED may generate red, green and blue light, corresponding to an amount of current supplied from the driving transistor, or may generate white light, corresponding to the amount of the current supplied from the driving transistor. In a case where the organic light emitting diode OLED generates white light, a color image is implemented using a separate color filter or the like.

35 [0145] By way of summation and review, an organic light emitting display includes a plurality of pixels arranged in a matrix form at crossing regions of a plurality of data lines, a plurality of scan lines and a plurality of power lines. Each pixel generally includes an organic light emitting diode, two or more transistors including a driving transistor, and one or more capacitors.

[0146] In order to implement a 3D image, the organic light emitting display includes four frames during a period of 16.6 ms. A left image is displayed in a first frame among the four frames, and a right image is displayed in a third frame among the four frames. In addition, a black image is displayed in second and fourth frames among the four frames.

40 [0147] In shutter glasses, a left lens receives light during the first frame, and a right lens receives light during the third frame. In this case, a user wearing the shutter glasses recognizes, as a 3D image, an image supplied through the shutter glasses. The left and right lenses switch from either receiving light to not receiving light or from not receiving light to receiving light while the black image is being displayed during the second and fourth frames, and thus it is possible to prevent the occurrence of a crosstalk phenomenon.

45 [0148] However, in the related art organic light emitting display, the four frames are included in the period of 16.6 ms, and accordingly, the organic light emitting display is driven at a driving frequency of 240Hz. In a case where the organic light emitting display is driven at a high frequency, the power consumption of the organic light emitting display is increased, and the stability of the organic light emitting display is lowered. Further, the manufacturing cost of the organic light emitting display is increased. Since the black image is displayed during the second and fourth frames, the peak current for expressing a gray scale is increased, and accordingly, the lifespan of the organic light emitting diode is lowered.

50 [0149] In the pixel and the organic light emitting display using the same according to embodiments of the present invention, the pixels emit light, and concurrently (e.g., simultaneously), the data signal can be charged. Accordingly, the organic light emitting display is driven at a low frequency, thereby implementing a 3D image. Further, the driving transistor included in each pixel is initialized in an on-bias state before the data signal is supplied, thereby displaying a uniform image.

55 [0150] Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated.

Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

5 **Claims**

1. A pixel (142) comprising:

an organic light emitting diode (OLED);
 10 a second driver (148, 202, 212, 222) configured to control an amount of current supplied from a first power source (ELVDD) to the organic light emitting diode (OLED), corresponding to a previous data signal; and
 a first driver (146) configured to store a current data signal supplied from a data line (D1, ..., Dn) and to supply the previous data signal to the second driver (148, 202, 212, 222),

15 wherein the second driver (148, 202, 212, 222) comprises:

a sixth transistor (M6) coupled between an initialization power source (Vinit) and a first node (N1) coupled to a gate electrode of a first transistor (M1), the sixth transistor (M6) being configured to turn on when a first control signal is supplied via a first control line (C1); and
 20 a seventh transistor (M7) coupled between the first power source (ELVDD) and a second node (N2) commonly coupled to the first and second drivers (146, 148, 202, 212, 222), the seventh transistor (M7) being configured to turn on when the first control signal is supplied.

2. The pixel of claim 1, wherein the initialization power source (Vinit) has a voltage lower than that of a data signal supplied to the data line (Dm).
 25

3. The pixel of claim 1 or 2, wherein the second driver (148, 202, 212, 222, 232, 242) further comprises a fourth transistor (M4) coupled between the anode electrode of the organic light emitting diode (OLED) and the initialization power source (Vinit), the fourth transistor (M4) being configured to turn on when the first control signal is supplied.
 30

4. The pixel of claim 1 or 2, wherein the second driver (148, 202, 212, 222, 232, 242) further comprises a fourth transistor (M4) coupled between the anode electrode of the organic light emitting diode (OLED) and the initialization power source (Vinit), the fourth transistor (M4) being configured to turn on when a second control signal is supplied to a second control line (C12).
 35

5. The pixel of claim 1 or 2, wherein the second driver (212, 222) further comprises a photodiode (PD) and a first capacitor (C1) both coupled in parallel between the first node (N1) and the first power source (ELVDD).

6. The pixel of claim 5, wherein the photodiode (PD) is configured to control an increment of a voltage at the first node (N1), corresponding to a luminance of the organic light emitting diode (OLED).
 40

7. The pixel of claim 5, wherein the photodiode (PD) is configured to control an increment of a voltage at the first node (N1), in proportion to a luminance of the organic light emitting diode (OLED).

8. The pixel of one of the preceding claims, wherein the second driver (148, 202, 212, 222) further comprises:
 45

an eighth transistor (M8) coupled between the first power source (ELVDD) and the second node (N2), the second node (N2) being coupled to a first electrode of the first transistor (M1), the eighth transistor (M8) being configured to turn off when an emission control signal is supplied via an emission control line (E);
 50 a fifth transistor (M5) coupled between the first node (N1) and a second electrode of the first transistor (M1), the fifth transistor (M5) being configured to turn on when a second control signal is supplied via a second control line (C12);
 a ninth transistor (M9) coupled between the second electrode of the first transistor (M1) and an anode electrode of the organic light emitting diode (OLED), the ninth transistor (M9) being configured to turn off when the emission control signal is supplied; and
 55 a first capacitor (C1) coupled between the first node (N1) and the first power source (ELVDD).

9. The pixel of one of the preceding claims, wherein the first driver (146) comprises:

a second transistor (M2) coupled between the data line (Dm) and a third node (N3), the second transistor (M2) being configured to turn on when a scan signal is supplied via a scan line (Sn);
 a third transistor (M3) coupled between the second and third nodes (N2, N3), the third transistor (M3) being configured to turn on when a second control signal is supplied; and
 a second capacitor (C2) coupled between the third node (N3) and the initialization power source (Vinit).

10. An organic light emitting display comprising:

a control driver (120) configured to supply a first control signal to a first control line (Cl1) during a first period in one frame comprising not overlapping first to fourth periods, and to supply a second control signal to a second control line (Cl2) during the second period in the one frame;
 a scan driver (110) configured to supply an emission control signal to an emission control line (E) during the first period, the second period, and the third period in the one frame, and to progressively supply a scan signal to scan lines (S1 ... Sn) during the fourth period in the one frame;
 a data driver (130) configured to supply a data signal to data lines (D1 ... Dm), in synchronization with the scan signal, during the fourth period in the one frame; and
 pixels (142) according to one of the preceding claims connected to the data lines (D1 ... Dm), the scan lines (S1 ... Sn), the emission control line (E), the first control line (Cl1) and the second control line (Cl2).

11. The organic light emitting display of claim 10, wherein the scan driver (110) is configured to further supply the scan signal concurrently to the scan lines (S1 ... Sn) during the third period.

12. The organic light emitting display of claim 10 or 11, wherein the data driver (130) is configured to supply a reset voltage to the data lines (D1 ... Dm) during the third period.

13. The organic light emitting display of claim 10, 11 or 12, wherein the first power source (ELVDD) is set to a first voltage during the fourth period, and is set to a second voltage different from the first voltage during the first to third periods.

FIG. 1

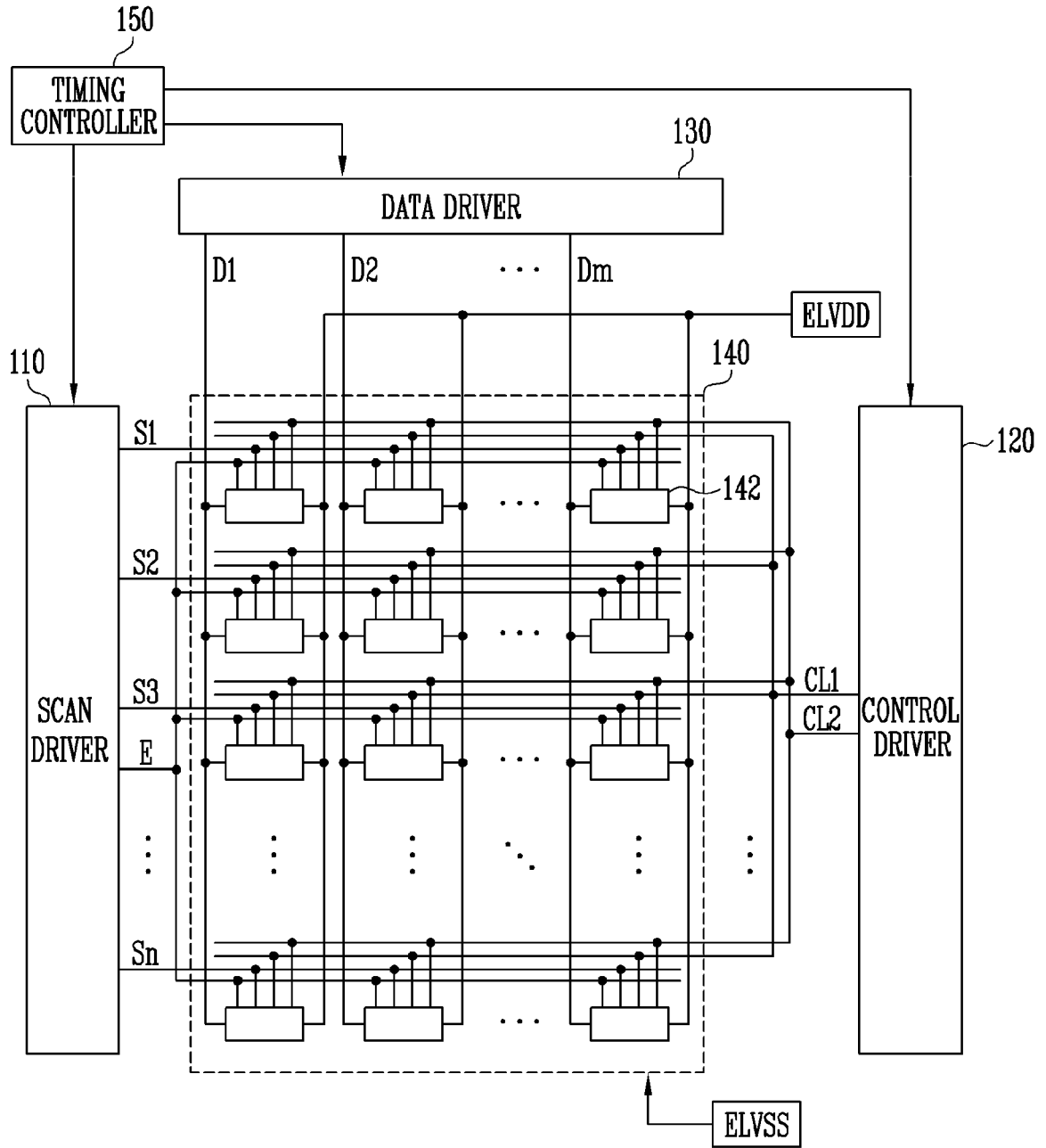


FIG. 2

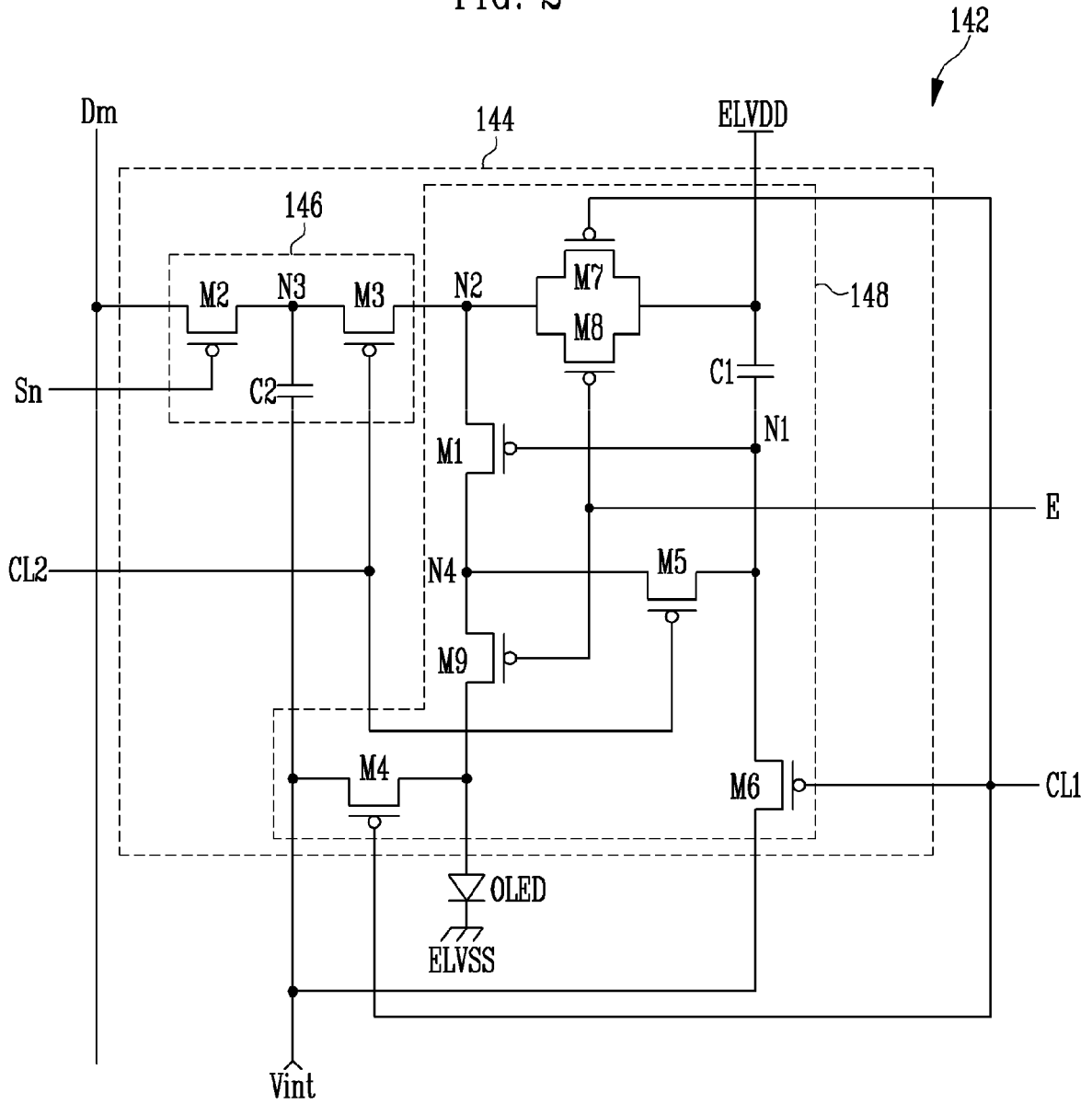


FIG. 3

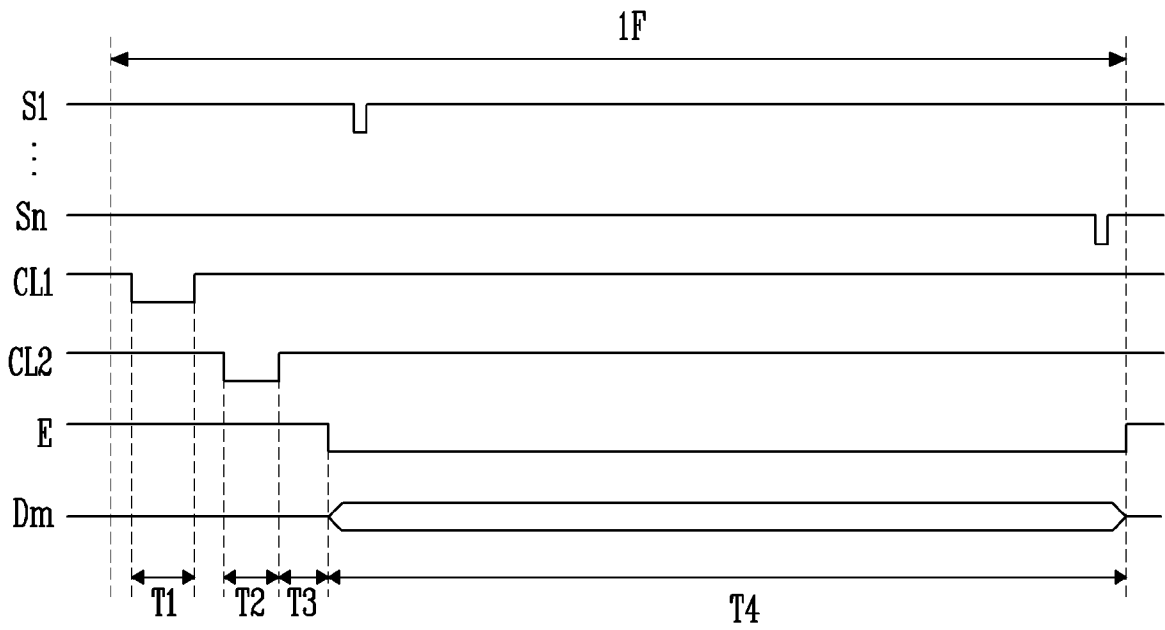


FIG. 4

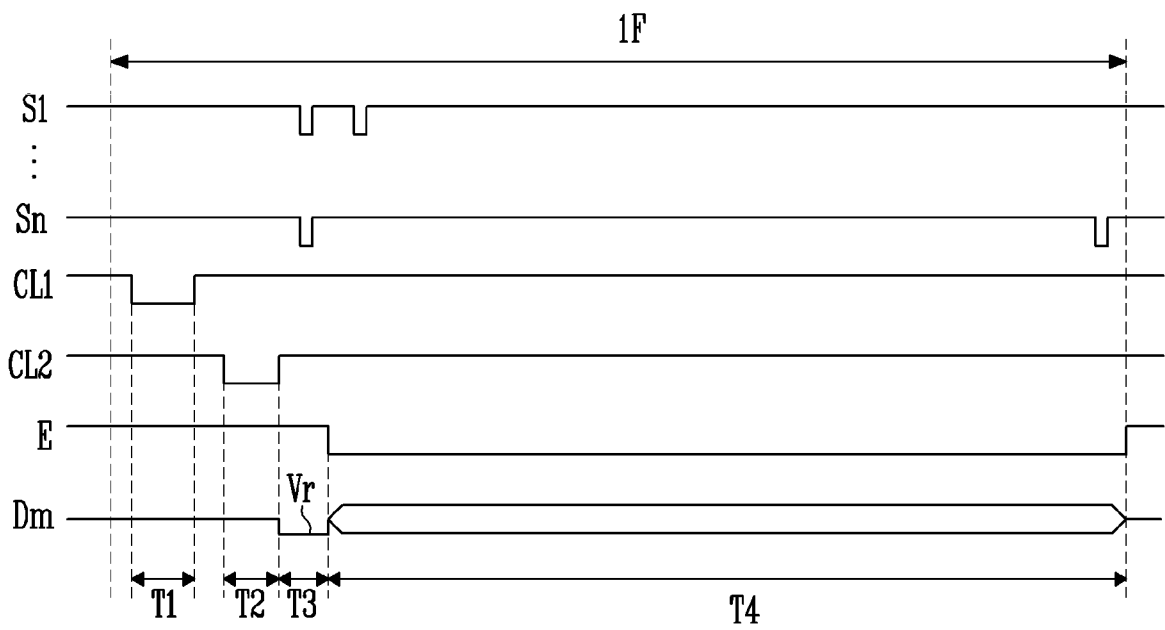


FIG. 5

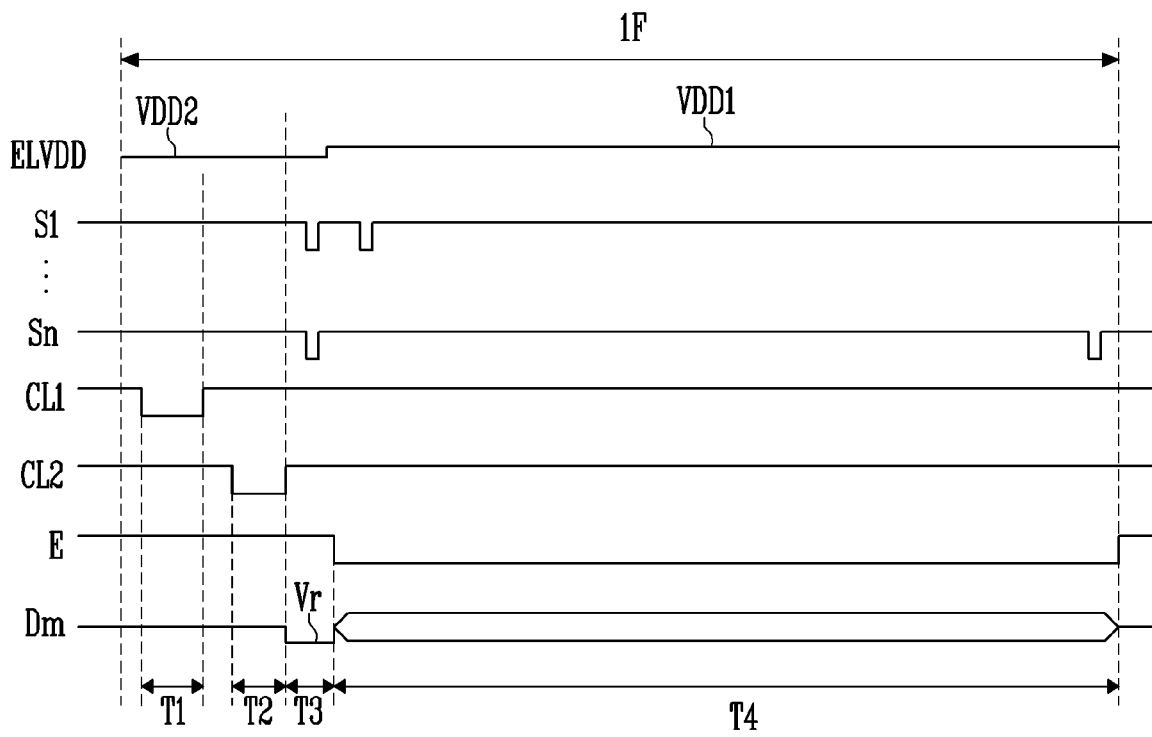


FIG. 6

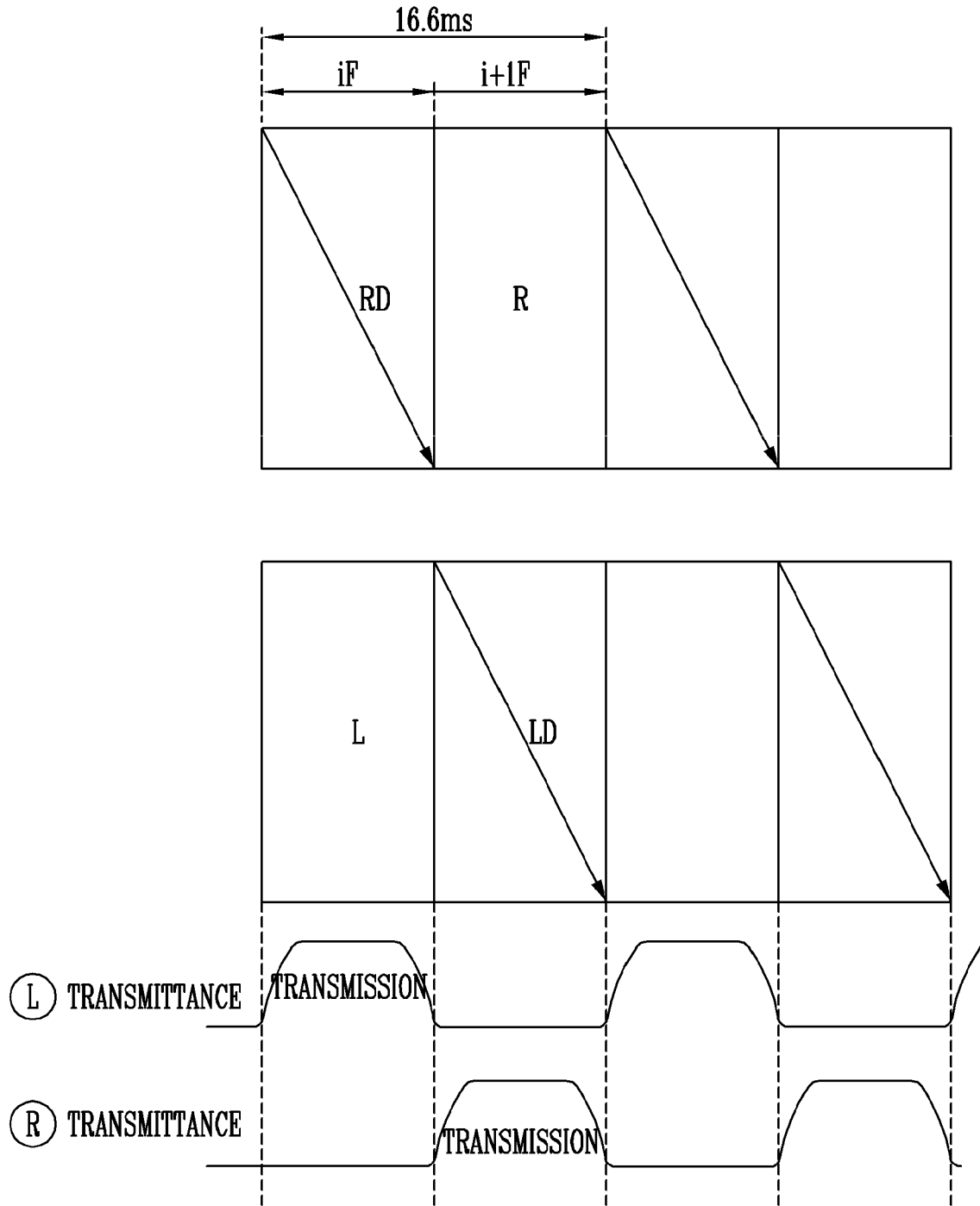


FIG. 7

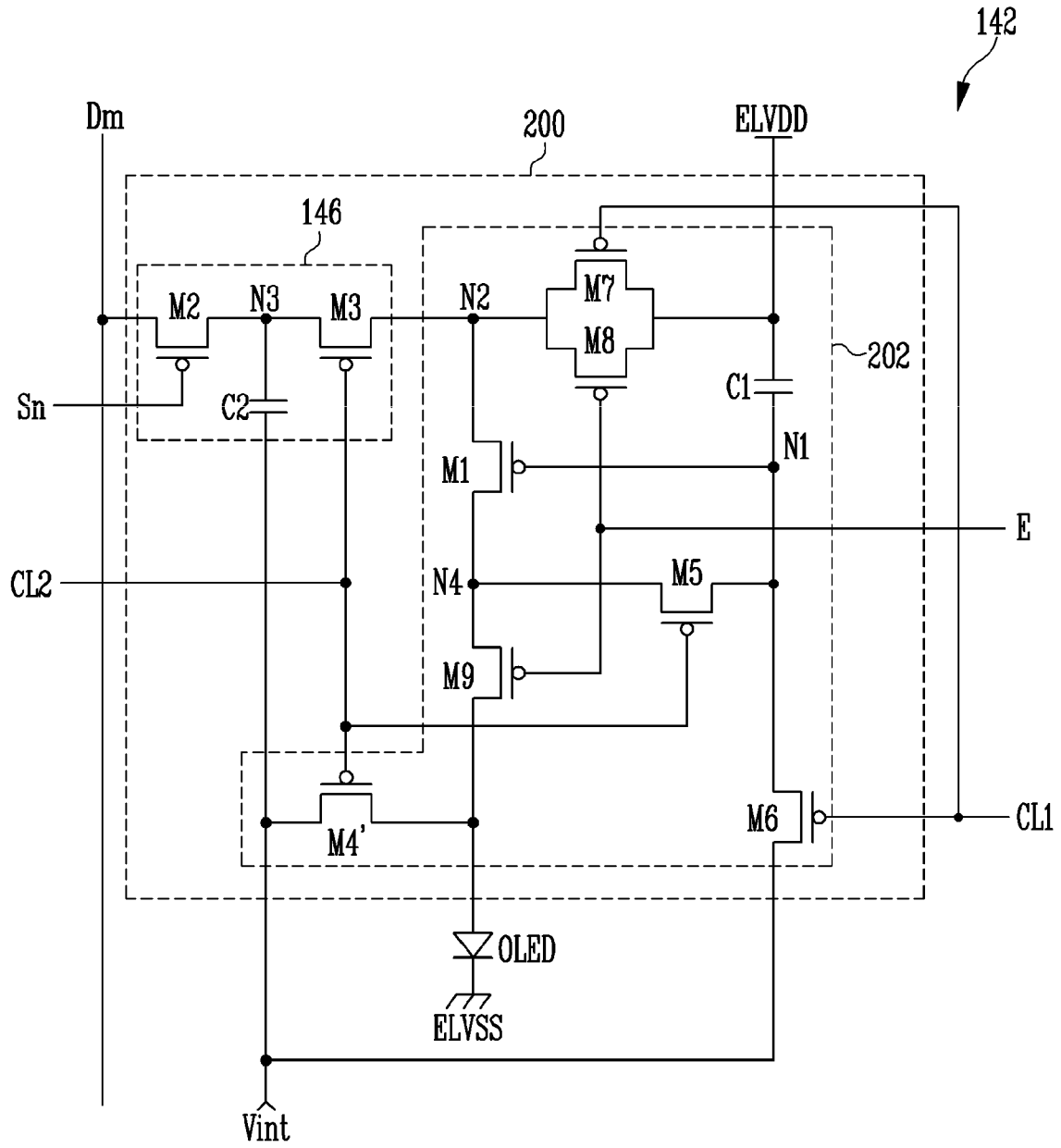


FIG. 8

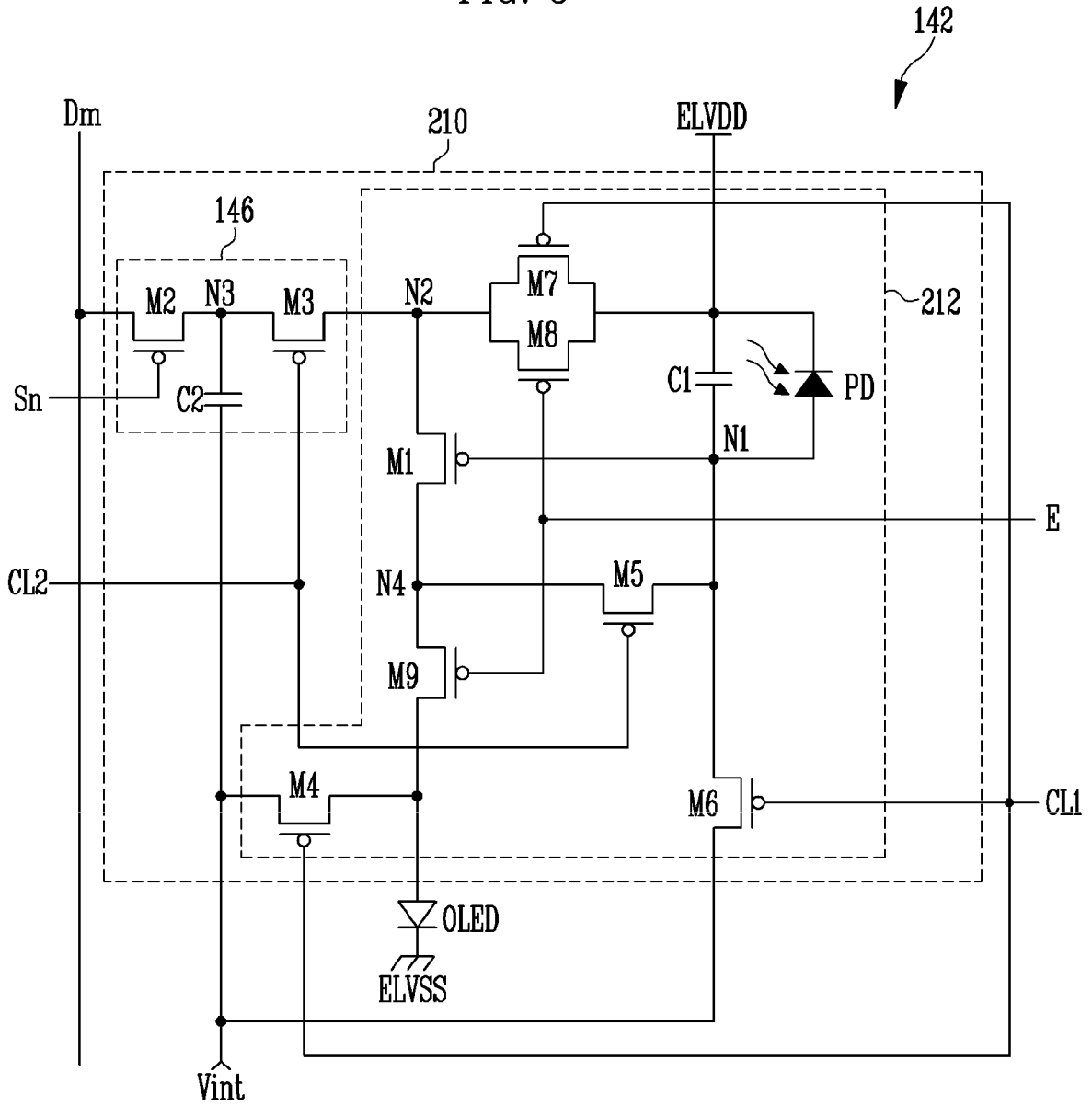


FIG. 9

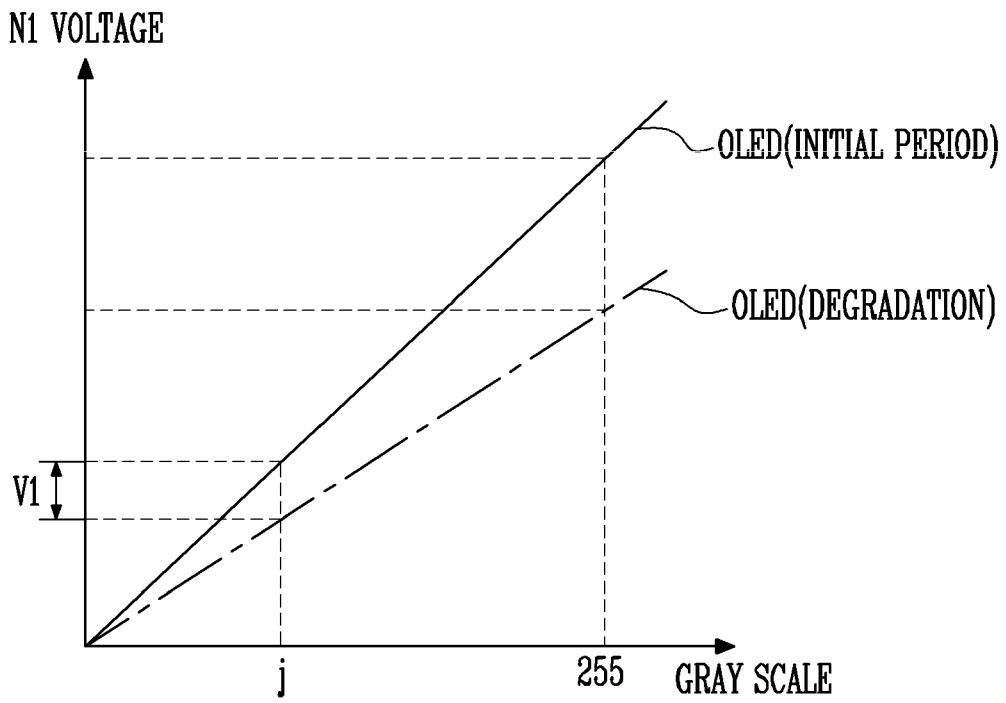


FIG. 10

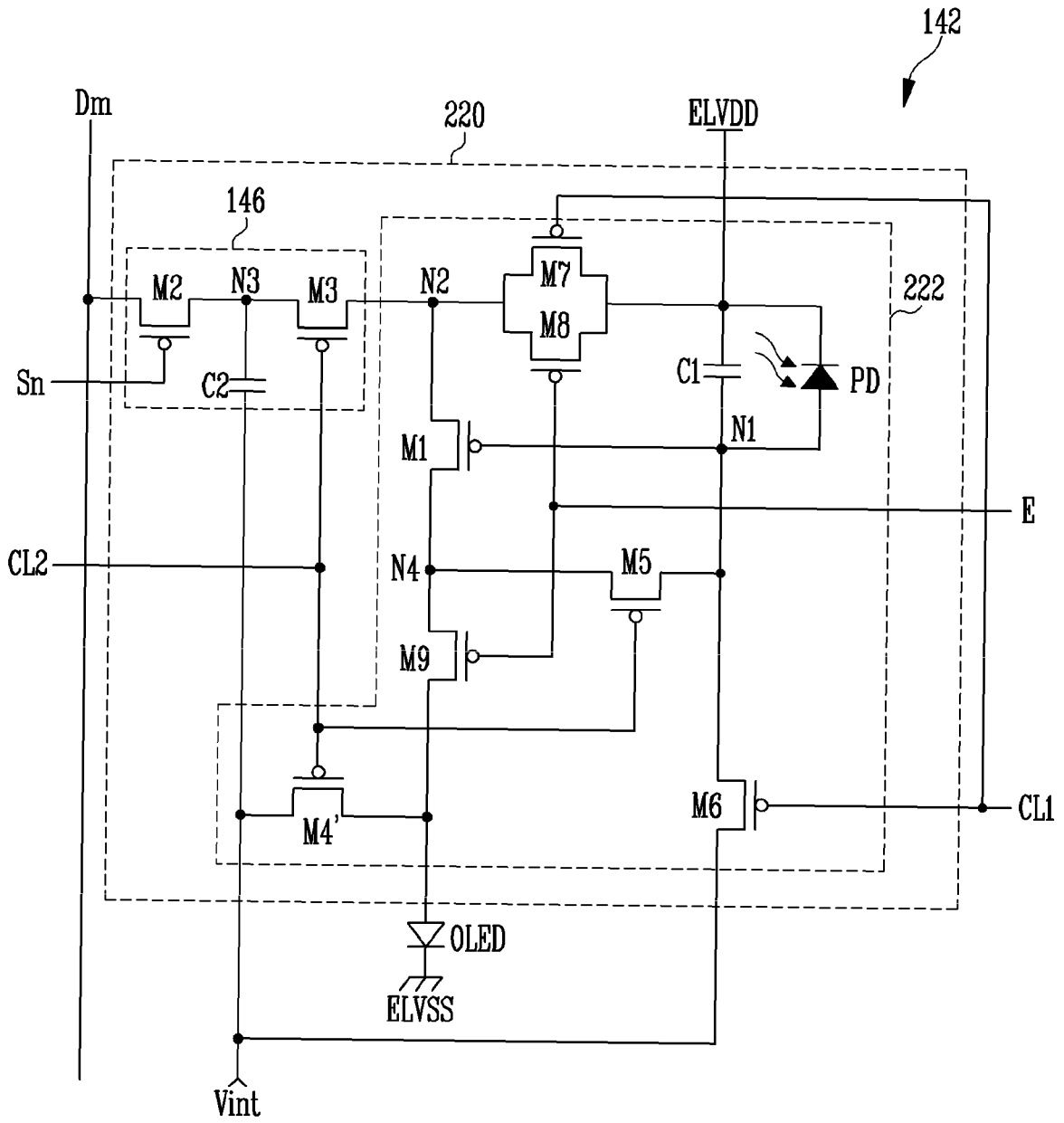
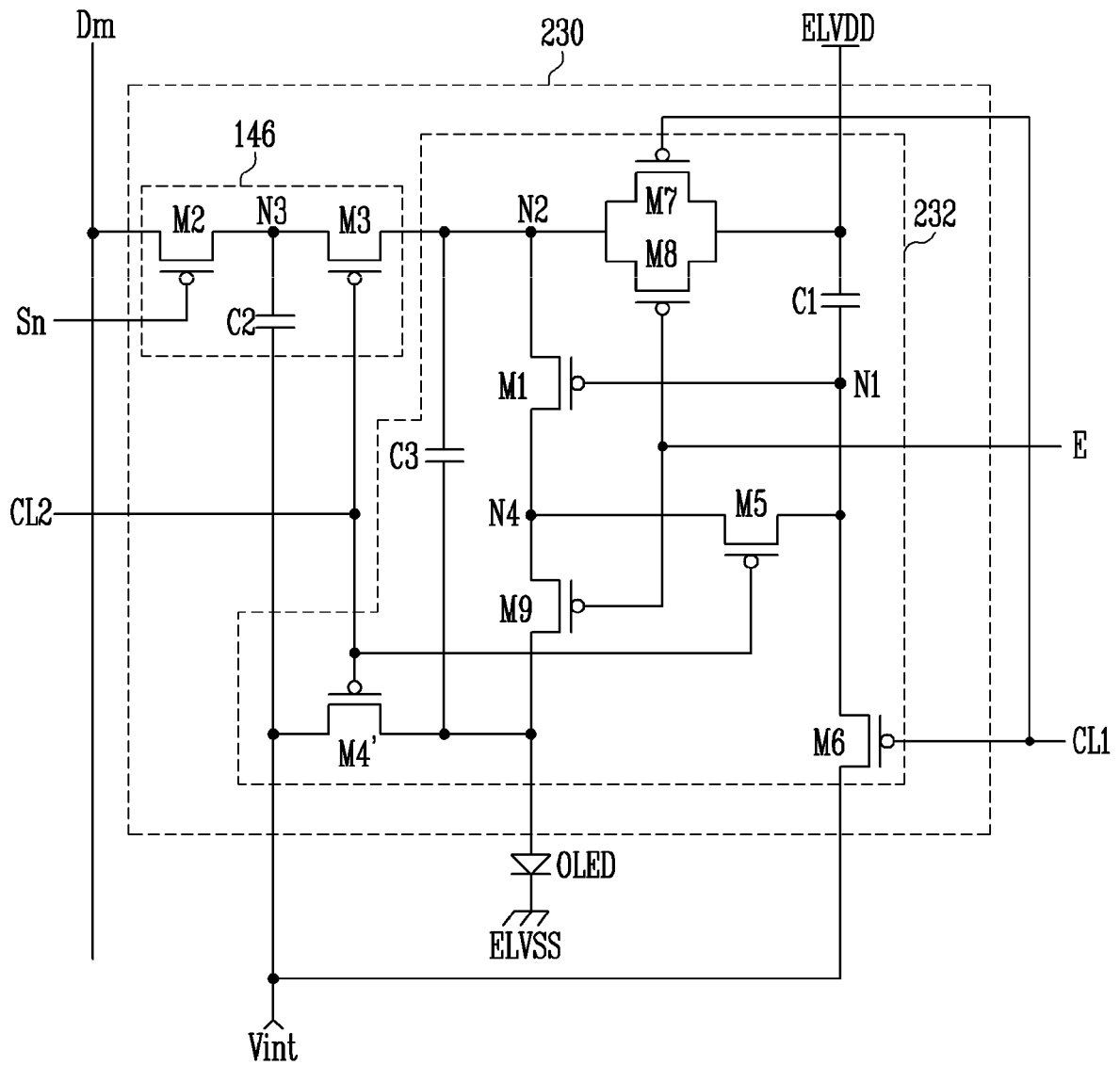


FIG. 11

142





EUROPEAN SEARCH REPORT

Application Number
EP 16 17 6868

5

10

15

20

25

30

35

40

45

50

55

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	US 2012/113077 A1 (KANG CHUL-KYU [KR]) 10 May 2012 (2012-05-10) * paragraphs [0060] - [0077]; figures 8,9 *	1-13	INV. G09G3/32 G09G3/3241 G09G3/3233
Y	EP 2 463 849 A1 (SAMSUNG MOBILE DISPLAY CO LTD [KR]) 13 June 2012 (2012-06-13) * paragraphs [0097] - [0102]; figures 3,4 *	1-10	
Y	EP 2 146 337 A1 (SAMSUNG MOBILE DISPLAY CO LTD [KR]) 20 January 2010 (2010-01-20) * paragraph [0050]; figure 2 *	3	
Y	US 2011/279484 A1 (HAN SANG-MYEON [KR] ET AL) 17 November 2011 (2011-11-17) * figures 6a-7 *	4	
Y	US 2009/243498 A1 (CHILDS MARK J [GB] ET AL) 1 October 2009 (2009-10-01) * paragraphs [0049], [0050]; figure 2 *	5-7	
Y	US 2011/090200 A1 (CHOI SANG-MOO [KR] ET AL) 21 April 2011 (2011-04-21) * paragraph [0057]; figure 4B *	11-13	TECHNICAL FIELDS SEARCHED (IPC) G09G
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 14 September 2016	Examiner Giancane, Iacopo
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03.02 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.

EP 16 17 6868

5 This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

14-09-2016

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012113077 A1	10-05-2012	JP 5901880 B2	13-04-2016
		JP 2012103660 A	31-05-2012
		KR 20120048294 A	15-05-2012
		US 2012113077 A1	10-05-2012
		US 2016171927 A1	16-06-2016

EP 2463849 A1	13-06-2012	CN 102568374 A	11-07-2012
		EP 2463849 A1	13-06-2012
		JP 2012128386 A	05-07-2012
		KR 20120065137 A	20-06-2012
		US 2012147060 A1	14-06-2012

EP 2146337 A1	20-01-2010	CN 101630481 A	20-01-2010
		EP 2146337 A1	20-01-2010
		JP 2010026488 A	04-02-2010
		KR 20100009219 A	27-01-2010
		US 2010013816 A1	21-01-2010

US 2011279484 A1	17-11-2011	KR 101082234 B1	09-11-2011
		US 2011279484 A1	17-11-2011
		US 2014071110 A1	13-03-2014

US 2009243498 A1	01-10-2009	CN 1833268 A	13-09-2006
		US 2009243498 A1	01-10-2009

US 2011090200 A1	21-04-2011	KR 20110042516 A	27-04-2011
		US 2011090200 A1	21-04-2011

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 2012113077 A1 [0003]
- EP 2463849 A1 [0003]
- EP 2146337 A1 [0003]
- US 2011279484 A1 [0003]
- US 2008243498 A1 [0003]
- US 2011090200 A1 [0003]

