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(54) **Organic light emitting display and method of compensation for threshold voltage thereof**

Organische lichtemittierende Anzeige und Verfahren zur Kompensierung von deren Schwellenspannung

Affichage électroluminescent organique et procédé de compensation pour sa tension de seuil

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Description

BACKGROUND

Field of the Invention

[0001] Embodiments of the invention relate to an active matrix organic light emitting display, and more particularly, to an organic light emitting display and a method of compensating for a threshold voltage thereof.

Discussion of the Related Art

[0002] An active matrix organic light emitting display includes organic light emitting diodes (hereinafter, abbreviated as "OLEDs") capable of emitting light. Such an active matrix organic light emitting display has advantages of a fast response time, a high light emitting efficiency, a high luminance, a wide viewing angle, and the like.

[0003] The OLED serving as a self-emitting element typically includes an anode electrode, a cathode electrode, and an organic compound layer formed between the anode electrode and the cathode electrode. The organic compound layer includes a hole injection layer HIL, a hole transport layer HTL, a light emitting layer EML, an electron transport layer ETL, and an electron injection layer EIL. When a driving voltage is applied to the anode electrode and the cathode electrode, holes passing through the hole transport layer HTL and electrons passing through the electron transport layer ETL move to the light emitting layer EML and form excitons. As a result, the light emitting layer EML generates visible light.

[0004] The organic light emitting display arranges pixels, each including an OLED, in a matrix form, and adjusts a luminance of the pixels depending on a gray scale of video data. Each pixel typically includes a driving thin film transistor (TFT) for controlling a driving current flowing in the OLED. It is preferable that electrical characteristics (including a threshold voltage, mobility, etc.) of the driving TFT are equally designed in all of the pixels. However, in practice, the electrical characteristics of the driving TFTs of the pixels are not uniform due to various causes. A deviation between the electrical characteristics of the driving TFTs results in a luminance deviation between the pixels.

[0005] Various compensation methods of compensating for the threshold voltage of the driving TFT are known. FIGs. 1 and 2 show one of the various compensation methods. An external compensation method illustrated in FIGs. 1 and 2 operates a driving TFT DT in a source follower manner and senses a threshold voltage Vth of the driving TFT DT. The source follower manner determines a change in the threshold voltage Vth based on a sensing value input to an analog-to-digital converter (ADC). However, accurate sensing of the threshold voltage Vth of the driving TFT DT using the source follower manner has to be performed after the driving TFT DT is turned off and a drain-source current Ids of the driving TFT DT becomes zero. Therefore, a long time Tx is required to sense the threshold voltage Vth.

[0006] More specifically, a sensing data voltage Vdata greater than the threshold voltage Vth is applied to a gate electrode of the driving TFT DT, so as to sense the threshold voltage Vth. When an initialization voltage Vref is applied to a source electrode of the driving TFT DT, the driving TFT DT is turned on because a gate-source voltage Vgs of the driving TFT DT is greater than the threshold voltage Vth. In this instance, the drain-source current Ids of the driving TFT DT depends on a difference Vgs between a gate voltage Vg (VN1) of the driving TFT DT and a source voltage Vs (VN2) of the driving TFT DT. In an initial sensing period, in which the source voltage Vs (VN2) of the driving TFT DT starts to increase, because the gate-source voltage Vgs of the driving TFT DT is large, a channel resistance of the driving TFT DT is small. As a result, the drain-source current Ids of the driving TFT DT is large. However, as the source voltage Vs (VN2) of the driving TFT DT gradually increases, the gate-source voltage Vgs of the driving TFT DT decreases. Therefore, the channel resistance of the driving TFT DT increases. As a result, the drain-source current Ids of the driving TFT DT decreases. When the drain-source current Ids of the driving TFT DT decreases, a charge amount accumulated in a sensing capacitor Cx decreases. Therefore, a time required for the gate-source voltage Vgs of the driving TFT DT to become the threshold voltage Vth increases. As the sensing time of the threshold voltage Vth increases, the amount of time available for displaying an image (e.g., the image display time) is reduced. Thus, in order to increase the image display time, the sensing time of the threshold voltage Vth needs to be reduced.

US 2013/201173 A1 discloses a three-transistor type driver circuit as part of a data extraction system. The organic light emitting display comprises a display panel including a plurality of pixels, a gate driving circuit configured to generate a threshold voltage sensing gate pulse supplied to a gate line or select input which is connected to the gates of a first and a second switching transistor in a first and a third period of a sensing period, a data driving circuit configured to supply a data voltage signal to the pixels in response to the threshold voltage sensing gate pulse, a read out circuit to detect a source voltage of a driving thin film transistor of each pixel as an output voltage proportional to the threshold voltage of the driving transistor in response to the threshold voltage sensing gate pulse, and a controller configured to modulate input digital video data for the image display based on a change in a threshold voltage of the driving transistor and to generate digital compensation data. Here, the display is configured to determine the threshold voltage of the driving transistor based on the sensed output voltage. The sensing period for sensing the threshold voltage of the driving transistor is divided into a first pre-charge period, a second integrate period and a third read period. A gate voltage of the driving transistor of each pixel is

held at a level high enough to turn the driving transistor on in the first pre-charge period of the sensing period and is held at a second level low enough to keep the driving transistor off in the third read period of the sensing period. US 2013/050292 A1 discloses an OLED display device which can sense a current of each pixel at high speed by a simple structure in order to compensate the luminance non-uniformity. The OLED display device includes a display panel having a plurality of pixels each including a light emitting element and a pixel circuit, and a data driver. The pixel circuit includes a driver transistor, the gate of which is connected to a data line via a switching transistor. The source of the driving transistor is connected to the gate by means of a capacitor and to a reference line via a second switching transistor. The data line and the reference line can be alternatively connected to a data driver via an output channel line. The data driver comprises a digital to analogue converter and a sample and hold circuit which can be alternatively connected to the data line and the reference line, respectively, via the output channel. Here, a sensing mode period comprises three periods, i.e. a data supply period, a pre-charge period and a sensing period. During the data supply period, a single level data voltage is supplied to the gate of the driving transistor via a first switching transistor which is turned off during the pre-charge period and the sensing period.

SUMMARY

[0007] The object of the present invention is to provide an organic light emitting display according to claim 1 and a method of compensating for a threshold voltage according to claim 7.

The dependent claims define further advantageous embodiments.

[0008] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0009] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of embodiments of the invention. In the drawings:

FIG. 1 is an equivalent circuit diagram of a pixel operating in a related art source follower manner;

FIG. 2 is a waveform diagram showing changes in a gate-source voltage of a driving thin film transistor (TFT) shown in FIG. 1 when a threshold voltage of the driving TFT is sensed;

FIG. 3 is a block diagram of an organic light emitting display according to an example embodiment of the invention;

FIG. 4 shows a pixel array of a display panel;

FIG. 5 illustrates a connection structure of a timing controller, a data driving circuit, and pixels along with a detailed configuration of an external compensation pixel of a source follower manner;

FIG. 6 shows a timing chart illustrating an image display period and non-display periods disposed on both sides of the image display period;

FIG. 7 shows a timing diagram illustrating, as a method for holding a gate voltage of a driving TFT at a high level in a first period of a sensing period, and holding the gate voltage of the driving TFT at a reference level in a second period following the first period, an example of inputting a threshold voltage sensing data voltage at a first level in the first period and inputting the threshold voltage sensing data voltage at a second level lower than the first level in the second period;

FIG. 8 shows a timing diagram illustrating, as another method for holding a gate voltage of a driving TFT at a high level in a first period of a sensing period, and holding the gate voltage of the driving TFT at a reference level in a second period following the first period, an example of inputting a threshold voltage sensing gate pulse at a first level in the first period and inputting the threshold voltage sensing gate pulse at a second level lower than the first level in the second period;

FIGs. 9A to 9C are waveform diagrams showing changes in a gate-source voltage of a driving TFT according to an example embodiment of the invention;

FIGs. 10 and 11 show a method for generating a first threshold voltage sensing gate pulse at a multi-on level, FIG. 10 illustrating a timing diagram and FIG. 11 showing a circuit diagram; and

FIG. 12 shows a reduction in a sensing time required to sense a threshold voltage of a driving TFT according to an example embodiment of the invention, as compared with related art.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0011] Reference will now be made in detail to embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same or like reference numbers will be used throughout the drawings to refer to the same or like parts. Detailed description of known art may be omitted if it is determined

that the art can mislead the embodiments of the invention.

[0012] Example embodiments of the invention will be described with reference to FIGs. 3 to 12.

[0013] FIG. 3 is a block diagram of an organic light emitting display according to an example embodiment of the invention. FIG. 4 shows a pixel array of a display panel.

[0014] As shown in FIGs. 3 and 4, the organic light emitting display according to the embodiment may include a display panel 10, a data driving circuit 12, a gate driving circuit 13, and a timing controller 11.

[0015] The display panel 10 may include a plurality of data lines 14, a plurality of gate lines 15 crossing the data lines 14, and a plurality of pixels P respectively arranged at crossings of the data lines 14 and the gate lines 15 in a matrix form.

[0016] The data lines 14 may include m data voltage supply lines 14A_1 to 14A_m and m sensing voltage readout lines 14B_1 to 14B_m, where m is a positive integer. The gate lines 15 may include n first gate lines 15A_1 to 15A_n and n second gate lines 15B_1 to 15B_n, where n is a positive integer.

[0017] Each pixel P may be connected to one of the data voltage supply lines 14A_1 to 14A_m, one of the sensing voltage readout lines 14B_1 to 14B_m, one of the first gate lines 15A_1 to 15A_n, and one of the second gate lines 15B_1 to 15B_n. Each pixel P may receive a data voltage through the data voltage supply line, may receive a first threshold voltage sensing gate pulse through the first gate line, may receive a second threshold voltage sensing gate pulse through the second gate line, and may output a sensing voltage through the sensing voltage readout line. For example, in a pixel array shown in FIG. 4, the pixels P sequentially operate based on each of horizontal lines L#1 to L#n in response to the first threshold voltage sensing gate pulse received from the first gate lines 15A_1 to 15A_n in a line sequential manner and the second threshold voltage sensing gate pulse received from the second gate lines 15B_1 to 15B_n in the line sequential manner. The pixels P on the same horizontal line, on which an operation is activated, may receive a threshold voltage sensing data voltage from the data voltage supply lines 14A_1 to 14A_m and output the sensing voltage to the sensing voltage readout lines 14B_1 to 14B_m.

[0018] Each pixel P may receive a high potential driving voltage EVDD and a low potential driving voltage EVSS from a power generator (not shown). Each pixel P according to an embodiment of the invention may include an organic light emitting diode (OLED), a driving thin film transistor (TFT), first and second switch TFTs, and a storage capacitor for the external compensation. The TFTs constituting the pixel P may be implemented as a p-type or an n-type. Further, semiconductor layers of the TFTs constituting the pixel P may contain amorphous silicon, polycrystalline silicon, or oxide.

[0019] In a sensing drive for sensing a threshold voltage of the driving TFT, the data driving circuit 12 may supply the threshold voltage sensing data voltage to the pixels P in response to the first threshold voltage sensing gate pulse. Further, the data driving circuit 12 may convert the sensing voltages received from the display panel 10 through the sensing voltage readout lines 14B_1 to 14B_m into digital values and supply the digital sensing voltages to the timing controller 11. In an image display drive for the image display, the data driving circuit 12 may convert digital compensation data MDATA received from the timing controller 11 into an image display data voltage based on a data control signal DDC and supply the image display data voltage to the data voltage supply lines 14A_1 to 14A_m.

[0020] The gate driving circuit 13 may generate a gate pulse based on a gate control signal GDC. The gate pulse may include the first threshold voltage sensing gate pulse, the second threshold voltage sensing gate pulse, a first image display gate pulse, and a second image display gate pulse. In the sensing drive of the threshold voltage, the gate driving circuit 13 may supply the first threshold voltage sensing gate pulse to the first gate lines 15A_1 to 15A_n in the line sequential manner and also may supply the second threshold voltage sensing gate pulse to the second gate lines 15B_1 to 15B_n in the line sequential manner. In the image display drive, the gate driving circuit 13 may supply the first image display gate pulse to the first gate lines 15A_1 to 15A_n in the line sequential manner and also may supply the second image display gate pulse to the second gate lines 15B_1 to 15B_n in the line sequential manner. The gate driving circuit 13 may be directly formed on the display panel 10 through a gate driver-in panel (GIP) process.

[0021] The timing controller 11 may generate the data control signal DDC for controlling operation timing of the data driving circuit 12 and the gate control signal GDC for controlling operation timing of the gate driving circuit 13 based on timing signals, such as a vertical sync signal Vsync, a horizontal sync signal Hsync, a data enable signal DE, and a dot clock DCLK. Further, the timing controller 11 may modulate input digital video data DATA based on the digital sensing voltages received from the data driving circuit 12 and generate the digital compensation data MDATA for compensating for a deviation between the threshold voltages of the driving TFTs. The timing controller 11 may then supply the digital compensation data MDATA to the data driving circuit 12.

[0022] The timing controller 11 according to an embodiment of the invention may divide a sensing period for sensing the threshold voltage into a first period and a second period following the first period. The timing controller 11 may control an operation of the data driving circuit 12 and an operation of the gate driving circuit 13 in the first and second periods, thereby reducing the time required to sense the threshold voltage. For this, an embodiment of the invention may not uniformly hold a gate voltage of the driving TFT included in the pixel P at a predetermined level throughout the sensing period, in contrast to the related art. For example, an embodiment

of the invention may hold the gate voltage of the driving TFT at one or more high levels in the first period of the sensing period, and may hold the gate voltage of the driving TFT at a reference level lower than the high level in the second period of the sensing period. Furthermore, the embodiment may increase a gate-source voltage of the driving TFT and reduces a channel resistance of the driving TFT in the first period of the sensing period, thereby increasing an amount of a current flowing between a drain electrode and a source electrode of the driving TFT. As the amount of the current flowing between the drain electrode and the source electrode of the driving TFT increases, the source voltage of the driving TFT may rapidly increase. Therefore, the time it takes for the gate-source voltage of the driving TFT to reach a threshold voltage of the driving TFT may be reduced.

[0023] FIG. 5 illustrates an example connection structure of the timing controller, the data driving circuit, and the pixels along with a detailed configuration of an external compensation pixel of a source follower manner. FIG. 6 shows an example image display period and non-display periods disposed on both sides of the image display period.

[0024] As shown in FIG. 5, the pixel P may include an OLED, a driving TFT DT, a storage capacitor Cst, a first switch TFT ST1, and a second switch TFT ST2.

[0025] The OLED may include an anode electrode connected to a second node N2, a cathode electrode connected to an input terminal of a low potential driving voltage EVSS, and an organic compound layer positioned between the anode electrode and the cathode electrode.

[0026] The driving TFT DT may control a driving current Ioled flowing in the OLED depending on a gate-source voltage Vgs of the driving TFT DT. The driving TFT DT may include a gate electrode connected to a first node N1, a drain electrode connected to an input terminal of a high potential driving voltage EVDD, and a source electrode connected to the second node N2.

[0027] The storage capacitor Cst may be connected between the first node N1 and the second node N2.

[0028] In the sensing drive, the first switch TFT ST1 may apply a threshold voltage sensing data voltage Vdata charged to the data voltage supply line 14A to the first node N1 in response to a first threshold voltage sensing gate pulse SCAN. In the image display drive, the first switch TFT ST1 may apply an image display data voltage Vdata charged to the data voltage supply line 14A to the first node N1 in response to a first image display gate pulse SCAN. The first switch TFT ST1 may include a gate electrode connected to the first gate line 15A, a drain electrode connected to the data voltage supply line 14A, and a source electrode connected to the first node N1.

[0029] In the sensing drive, the second switch TFT ST2 may turn on a current flow between the second node N2 and the sensing voltage readout line 14B in response to a second threshold voltage sensing gate pulse SEN, thereby storing a source voltage of the second node N2, which is changed by following a gate voltage of the first node N1 in the source follower manner, in a sensing capacitor Cx of the sensing voltage readout line 14B. In one example, the sensing capacitor Cx may be implemented by a parasitic capacitor of the sensing voltage readout line 14B. In the image display drive, the second switch TFT ST2 may turn on a current flow between the second node N2 and the sensing voltage readout line 14B in response to a second image display gate pulse SEN, thereby resetting a source voltage of the driving TFT DT to an initialization voltage Vpre. A gate electrode of the second switch TFT ST2 may be connected to the second gate line 15B, a drain electrode of the second switch TFT ST2 may be connected to the second node N2, and a source electrode of the second switch TFT ST2 may be connected to the sensing voltage readout line 14B.

[0030] The data driving circuit 12 may be connected to the pixel P through the data voltage supply line 14A and the sensing voltage readout line 14B. The sensing capacitor Cx for storing the source voltage of the second node N2 as the sensing voltage Vsen may be formed on the sensing voltage readout line 14B. The data driving circuit 12 may include a digital-to-analog converter (DAC), an analog-to-digital converter (ADC), an initialization switch SW1, and a sampling switch SW2.

[0031] In the first and second periods of the sensing period, the DAC may generate the threshold voltage sensing data voltages Vdata at the same level or different levels under the control of the timing controller 11 and may output the threshold voltage sensing data voltages Vdata to the data voltage supply line 14A. In an image display period, the DAC may convert digital compensation data into an image display data voltage Vdata under the control of the timing controller 11 and may output the image display data voltage Vdata to the data voltage supply line 14A.

[0032] The initialization switch SW1 may turn on a current flow between an input terminal of the initialization voltage Vpre and the sensing voltage readout line 14B. The sampling switch SW2 may turn on a current flow between the sensing voltage readout line 14B and the ADC. The ADC may convert the analog sensing voltage Vsen stored in the sensing capacitor Cx into a digital value and supplies this digital sensing voltage Vsen to the timing controller 11.

[0033] A process for detecting the sensing voltage Vsen deciding a change in the threshold voltage of the driving TFT DT from each pixel P is additionally described below with reference to FIGs. 5 and 6.

[0034] When the first and second threshold voltage sensing gate pulses SCAN and SEN of an on-level Lon are applied to the pixel P for the sensing drive of the threshold voltage, the first switch TFT ST1 and the second switch TFT ST2 may be turned on. In this example, the initialization switch SW1 inside the data driving circuit 12 is turned on. When the first switch TFT ST1 is turned on, the threshold voltage sensing data voltages Vdata is supplied to the first node N1. When the initialization switch SW1 and the second switch TFT ST2 are turned

on, the initialization voltage Vpre is supplied to the second node N2. In this example, because the gate-source voltage Vgs of the driving TFT DT is greater than the threshold voltage Vth of the driving TFT DT, the current Ioled (Ids) flows between the drain electrode and the source electrode of the driving TFT DT. A source voltage VN2 of the driving TFT DT charged to the second node N2 gradually increases due to the current Ioled (Ids). Hence, until the gate-source voltage Vgs of the driving TFT DT becomes the threshold voltage Vth of the driving TFT DT, the source voltage VN2 of the driving TFT DT follows a gate voltage VN1 of the driving TFT DT.

[0035] The gradually increasing source voltage VN2 of the driving TFT DT at the second node N2 may be stored in the sensing capacitor Cx formed on the sensing voltage readout line 14B as the sensing voltage Vsen via the second switch TFT ST2. The sensing voltage Vsen may be detected when the sampling switch SW2 inside the data driving circuit 12 is turned on in the sensing period, in which the second threshold voltage sensing gate pulse SEN is maintained at the on-level Lon. The detected sensing voltage Vsen may be supplied to the ADC.

[0036] In the external compensation using the source follower manner, an embodiment of the invention may hold the gate voltage of the driving TFT at one or more high levels in the first period of the sensing period, thereby reducing the sensing time of the threshold voltage. For this, an example embodiment of the invention may modulate the threshold voltage sensing data voltage Vdata as shown in FIG. 7, or may modulate the first threshold voltage sensing gate pulse SCAN as shown in FIG. 8. This is described in detail below with reference to FIGs. 7 and 8.

[0037] As shown in FIG. 6, the threshold voltage sensing according to an embodiment of the invention may be performed in at least one of a first non-display period X1 arranged prior to an image display period X0 and a second non-display period X2 arranged after the image display period X0. Furthermore, because the sensing period of the threshold voltage according to an embodiment of the invention may be greatly reduced as compared with the related art, the sensing of the threshold voltage may be partially performed in vertical blank periods VB belonging to the image display period X0. In example embodiments disclosed herein, the vertical blank periods VB are defined as periods between adjacent display frames DF. The first non-display period X1 may be defined as a period until several tens to several hundreds of frames passed from an application time point of a driving power enable signal PON. The second non-display period X2 may be defined as a period until several tens to several hundreds of frames passed from an application time point of a driving power disable signal POFF.

[0038] FIG. 7 shows a method for holding the gate voltage of the driving TFT at the high level in the first period of the sensing period and holding the gate voltage of the driving TFT at the reference level in the second period following the first period. FIG. 8 shows another method for holding the gate voltage of the driving TFT at the high level in the first period of the sensing period and holding the gate voltage of the driving TFT at the reference level in the second period following the first period. FIGs. 9A to 9C are waveform diagrams showing changes in the gate-source voltage of the driving TFT according to an example embodiment of the invention.

[0039] An example embodiment of the invention may increase the gate-source voltage of the driving TFT in an initial sensing period and reduce the channel resistance of the driving TFT. Further, the example embodiment may increase the drain-source current of the driving TFT in the initial sensing period, so that the source voltage of the driving TFT rapidly follows the gate voltage of the driving TFT. Hence, the time required to sense the threshold voltage of the driving TFT may be reduced.

[0040] Example embodiments of the invention may use at least one of the methods shown in FIGs. 7 and 8, so as to increase the gate-source voltage of the driving TFT in the initial sensing period.

[0041] As shown in FIG. 7, an embodiment of the invention may input the threshold voltage sensing data voltage Vdata at a first level L1 in a first period T1 of a sensing period, and may input the threshold voltage sensing data voltage Vdata at a second level L2 lower than the first level L1 in a second period T2 of the sensing period. In an example, the first threshold voltage sensing gate pulse SCAN may be input at the same on-level in the first and second periods T1 and T2 of the sensing period. The threshold voltage sensing data voltage Vdata of the first level L1 is applied to the gate electrode of the driving TFT DT in the first period T1 and thus makes the gate voltage VN1 (Vg) of the driving TFT DT at a high level as shown in FIGs. 9A to 9C. In example embodiments disclosed herein, the high level may be implemented as one voltage level as shown in FIG. 9A, or may be implemented as a plurality of voltage levels as shown in FIGs. 9B and 9C. The gate voltage VN1 (Vg) of the driving TFT DT may be maintained at a reference level lower than the high level in the second period T2 of the sensing period.

[0042] As shown in FIG. 8, an embodiment of the invention may input the first threshold voltage sensing gate pulse SCAN at a first on-level Lon1 in the first period T1 of the sensing period, and may input the first threshold voltage sensing gate pulse SCAN at a second on-level Lon2 lower than the first on-level Lon1 in the second period T2 of the sensing period. In an example, the threshold voltage sensing data voltage Vdata may be input at the same level in the first and second periods T1 and T2 of the sensing period. The first threshold voltage sensing gate pulse SCAN of the first on-level Lon1 is applied to the gate electrode of the first switch TFT ST1 and reduces the channel resistance of the first switch TFT ST1, thereby increasing an amount of the drain-source current of the first switch TFT ST1. Thus, the threshold voltage sensing data voltage Vdata applied to the gate electrode of the driving TFT DT through the first switch TFT ST1

in the first period T1 may be relatively larger than that in the second period T2. As a result, the gate voltage VN1 (Vg) of the driving TFT DT in the first period T1 has the high level as shown in FIGs. 9A to 9C. In an embodiment disclosed herein, the high level may be implemented as one voltage level as shown in FIG. 9A, or may be implemented as a plurality of voltage levels as shown in FIGs. 9B and 9C. The gate voltage VN1 (Vg) of the driving TFT DT may be maintained at the reference level lower than the high level in the second period T2 of the sensing period.

[0043] According to embodiments of the invention, a threshold voltage sensing period Tx' may be much shorter than the related art threshold voltage sensing period Tx (FIG. 2) through the above description.

[0044] FIGs. 10 and 11 show a method for generating the first threshold voltage sensing gate pulse at a multi-on level.

[0045] As shown in FIGs. 10 and 11, the gate driving circuit according to an example embodiment of the invention may generate the first threshold voltage sensing gate pulse SCAN of a multi-on level based on adjacent clock signals S(N-1) and S(N), which partially overlap each other. For this, the gate driving circuit according to the example embodiment may include an inverter INV, a first AND gate AND1, a second AND gate AND2, a first level shifter L/S 1, a second level shifter L/S 2, and a waveform synthesizer.

[0046] In this example, the inverter INV inverts the (N-1)th clock signal S(N-1) of a TTL level. The first AND gate AND1 performs an AND operation on the (N-1)th clock signal S(N-1) passing through the inverter INV and the Nth clock signal S(N). The second AND gate AND2 performs an AND operation on the (N-1)th clock signal S(N-1), which does not pass through the inverter INV, and the Nth clock signal S(N). The first level shifter L/S 1 level-shifts an operation result of the second AND gate AND2 having the TTL level into a first on-level VGH1 and an off-level VGL. The second level shifter L/S 2 level-shifts an operation result of the first AND gate AND1 having the TTL level into a second on-level VGH2 and the off-level VGL. In example embodiments disclosed herein, the first on-level VGH1 is higher than the second on-level VGH2. The waveform synthesizer synthesizes a signal received from the first level shifter L/S 1 and a signal received from the second level shifter L/S 2 and generates the first threshold voltage sensing gate pulse SCAN of the multi-on level having the first on-level VGH1 and the second on-level VGH2.

[0047] FIG. 12 shows a reduction in a sensing time required to sense the threshold voltage of the driving TFT according to an example embodiment of the invention, as compared with the related art.

[0048] As shown in FIG. 12, related art changes the source voltage Vg using the source follower manner in a state where the gate voltage Vg of the driving TFT is uniformly held at a predetermined level (for example, 9V), and senses the threshold voltage Vth of the driving TFT. As a result, in the example related art shown here, the time required to sense the threshold voltage Vth of the driving TFT was 4.12 msec, which is relatively long.

[0049] On the other hand, example embodiments of the invention do not uniformly hold the gate voltage of the driving TFT at a predetermined level throughout the sensing period. For example, an example embodiment holds the gate voltage of the driving TFT at the high level (for example, 11V) in the initial period of the sensing period and holds the gate voltage of the driving TFT at the reference level (for example, 9V) lower than the high level in the remaining period of the sensing period. As a result, in the example embodiment, the time required to sense the threshold voltage Vth of the driving TFT may be 2.77 msec, which is greatly reduced as compared with the related art.

[0050] As described above, embodiments of the invention control the gate voltage of the driving TFT at the multi-level when sensing the threshold voltage of the driving TFT using the source follower manner, thereby greatly reducing time required to sense the threshold voltage of the driving TFT.

[0051] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the scope of the invention, as defined by the appended claims.

Claims

1. An organic light emitting display comprising:

- a display panel (10) including a plurality of pixels (P), each pixel (P) comprising:
  - a driving TFT (DT) including a gate electrode connected to a first node (N1), a source electrode connected to a second node (N2), and a drain electrode connected to an input terminal of a high potential driving voltage (EVDD);
  - an organic light emitting diode (OLED) connected between the second node (N2) and an input terminal of a low potential driving voltage (EVSS);
  - a storage capacitor (Cst) connected between the first node (N1) and the second node (N2);
  - a first switch TFT (ST1) which is connected between a data voltage supply line (14A) chargeable to a threshold voltage sensing data voltage (V_{data}) and the first node (N1) and is turned on or off in response to a first threshold voltage sensing gate pulse (SCAN); and
  - a second switch TFT (ST2) which is con-

nected between a sensing voltage readout line (14B) for charging the sensing voltage (V_{sen}) and the second node (N2) and is turned on or off in response to a second threshold voltage sensing gate pulse (SEN),
- wherein both the first and second switch TFTs (ST1, ST2) are continuously turned on in the first and second periods (T1, T2) of a sensing period;

- a gate driving circuit (13) configured to generate both the first threshold voltage sensing gate pulse (SCAN) and the second threshold voltage sensing gate pulse (SEN) each at an on-level (L_{on}) in the sensing period;
- a data driving circuit (12) configured to supply the threshold voltage sensing data voltage (V_{data}) to the pixels (P) in response to the first threshold voltage sensing gate pulse (SCAN), and to detect a source voltage (Vs) of the driving thin film transistor, TFT, (DT) of each pixel as the sensing voltage (V_{sen}) in response to the second threshold voltage sensing gate pulse (SEN); and
- a timing controller (11) configured to modulate input digital video data (DATA) for the image display based on a change in a threshold voltage of the driving TFT (DT), and generate digital compensation data,
- wherein the display is configured to determine the threshold voltage of the driving TFT (DT) based on the sensing voltage (V_{sen}),
- wherein the sensing period for sensing the threshold voltage of the driving TFT (DT) is divided into a first period (T1) and a second period (T2) following the first period (T1), and
- wherein a gate voltage (V_g) of the driving TFT (DT) of each pixel (P) is held at one or more voltage levels in the first period (T1) of the sensing period, and is held at a reference level lower than said one or more voltage levels but higher than the source voltage (V_s) in the second period (T2) of the sensing period.

2. The organic light emitting display of claim 1, wherein:

- the data driving circuit (12) is further configured to supply the threshold voltage sensing data voltage (V_{data}) of the one or more voltage levels to the pixel (P) in the first period (T1) of the sensing period and the threshold voltage sensing data voltage (V_{data}) of the reference level lower than said one or more voltage levels in the second period (T2) of the sensing period; and
- the gate driving circuit (13) is further configured to generate the first threshold voltage sensing gate pulse (SCAN) at the same on-level in the first and second periods (T1, T2) of the sensing period.

3. The organic light emitting display of claim 1, wherein:

- the gate driving circuit (13) is further configured to generate the first threshold voltage sensing gate pulse (SCAN) at a first on-level (L_{on1}) in the first period (T1) of the sensing period and at a second on-level (L_{on2}) different from the first on-level (L_{on1}) in the second period (T2) of the sensing period; and
- the data driving circuit (12) is further configured to supply the threshold voltage sensing data voltage (V_{data}) of the same level to the pixel (P) in the first and second periods (T1, T2) of the sensing period.

4. The organic light emitting display of claim 3, wherein the gate driving circuit (13) is further configured to generate the first threshold voltage sensing gate pulse (SCAN) at the first on-level (L_{on1}) in the first period (T1) of the sensing period, and to generate the first threshold voltage sensing gate pulse (SCAN) at the second on-level (L_{on2}) lower than the first on-level (L_{on1}) in the second period (T2) of the sensing period.

5. The organic light emitting display of claim 1, wherein the display is further configured to sense the sensing voltage (V_{sen}) at the end of the sensing period to thereby determine the threshold voltage.

6. The organic light emitting display of claim 1, wherein the pixels (P) are operated in a source follower manner.

7. A method of compensating for a threshold voltage of an organic light emitting display including a display panel (10) including a plurality of pixels (P), each pixel (P) comprising:

- a driving TFT (DT) including a gate electrode connected to a first node (N1), a source electrode connected to a second node (N2), and a drain electrode connected to an input terminal of a high potential driving voltage (EVDD);
- an organic light emitting diode (OLED) connected between the second node (N2) and an input terminal of a low potential driving voltage (EVSS);
- a storage capacitor (Cst) connected between the first node (N1) and the second node (N2);
- a first switch TFT (ST1) which is connected between a data voltage supply line (14A) chargeable to a threshold voltage sensing data voltage (V_{data}) and the first node (N1) and is turned on or off in response to a first threshold

voltage sensing gate pulse (SCAN); and
- a second switch TFT (ST2) which is connected between a sensing voltage readout line (14B) for charging the sensing voltage (V_{sen}) and the second node (N2) and is turned on or off in response to a second threshold voltage sensing gate pulse (SEN),
- wherein both the first and second switch TFTs (ST1, ST2) are continuously turned on in the first and second periods (T1, T2) of a sensing period, the method comprising:

- generating both the first threshold voltage sensing gate pulse (SCAN) and the second threshold voltage sensing gate pulse (SEN) each t an on-level (L_{on}) in the sensing period;
- supplying the threshold voltage sensing data voltage (V_{data}) to the pixels (P) in response to the first threshold voltage sensing gate pulse (SCAN);
- detecting a source voltage (V_s) of the driving thin film transistor (TFT) (DT) of each pixel (P) as the sensing voltage (V_{sen}) in response to the second threshold voltage sensing gate pulse (SEN); and
- modulating input digital video data (DATA) for the image display based on a change in a threshold voltage of the driving TFT (DT) and generating digital compensation data,

- wherein the threshold voltage of the driving TFT (DT) is determined based on the sensing voltage (V_{sen}),
- wherein the sensing period for sensing the threshold voltage of the driving TFT (DT) is divided into a first period (T1) and a second period (T2) following the first period (T1), and
- wherein a gate voltage of the driving TFT (DT) of each pixel (P) is held at one or more voltage levels (L1) in the first period (T1) of the sensing period and is held at a reference level (L2) lower than the one or more voltage levels (L1) but higher than the source voltage (V_s) in the second period (T2) of the sensing period.

8. The method of claim 7, wherein:

- the threshold voltage sensing data voltage (V_{data}) is supplied to the pixel (P) at the one or more voltage levels (L1) in the first period (T1) of the sensing period and at the reference level (L2) lower than the the one or more voltage levels (L1) in the second period (T2) of the sensing period; and
- the first threshold voltage sensing gate pulse (SCAN) is generated at the same on-level (L_{on}) in the first and second periods (T1, T2) of the sensing period.

9. The method of claim 7, wherein:

- the first threshold voltage sensing gate pulse (SCAN) is generated at a first on-level (L_{on1}) in the first period (T1) of the sensing period and at a second on-level (L_{on2}) different from the first on-level (L_{on1}) in the second period (T2) of the sensing period; and
- the threshold voltage sensing data voltage (V_{data}) is supplied to the pixel (P) at the same level in the first and second periods (T1, T2) of the sensing period.

10. The method of claim 9, wherein the first threshold voltage sensing gate pulse (SCAN) is generated at a first on-level (L_{on1}) in the first period (T1) of the sensing period and is generated at a second on-level (L_{on2}) lower than the first on-level (L_{on1}) in the second period (T2) of the sensing period.

11. The method of claim 7, wherein the pixels (P) are operated in a source follower manner.

12. The method of claim 7, further comprising:

- sensing the sensing voltage (V_{sen}) at the end of the sensing period to determine the threshold voltage.

Patentansprüche

1. Organische lichtemittierende Anzeige, umfassend:

- ein Anzeigefeld (10), das eine Vielzahl von Pixeln (P) aufweist, wobei jedes Pixel (P) umfasst:

- einen Treiber-TFT (DT), der eine Gate-Elektrode, die mit einem ersten Knoten (N1) verbunden ist, eine Source-Elektrode, die mit einem zweiten Knoten (N2) verbunden ist, und eine Drain-Elektrode, die mit einem Eingangsanschluss einer Treibspannung mit hohem Potential (EVDD) verbunden ist, aufweist;
- eine organische lichtemittierende Diode (OLED), die zwischen dem zweiten Knoten (N2) und einem Eingangsanschluss einer Treibspannung mit niedrigem Potential (EVSS) angeschlossen ist;
- einen Speicherkondensator (Cst), der zwischen dem ersten Knoten (N1) und dem zweiten Knoten (N2) angeschlossen ist;
- einen ersten Schalter-TFT (ST1), der zwischen einer Daten-Spannungszufuhrleitung (14A), die auf eine Schwellenspan-

nungs-Abfühldatenspannung (V_{data}) geladen werden kann, und dem ersten Knoten (N1) angeschlossen ist und ein oder ausgeschaltet wird ansprechend auf einen ersten Schwellenspannungs-Abfühl-Gate-Impuls (SCAN); und

- einen zweiten Schalter-TFT (ST2), der zwischen einer Abfühlspannungs-Ausleseleitung (14B) zum Laden der Abfühlspannung (V_{sen}) und dem zweiten Knoten (N2) angeschlossen ist und ein oder ausgeschaltet wird ansprechend auf einen zweiten Schwellenspannungs-Abfühl-Gate-Impuls (SEN);

wobei sowohl der erste als auch zweite Schalter-TFT (ST1, ST2) kontinuierlich in der ersten und zweiten Periode (T1, T2) einer Abfühlperiode ein geschaltet sind;

- eine Gate-Treiberschaltung (13), die ausgelegt ist, sowohl den ersten Schwellenspannungs-Abfühl-Gate-Impuls (SCAN) als auch den zweiten Schwellenspannungs-Abfühl-Gate-Impuls (SEN) jeweils auf einem Ein-Pegel (L_{on}) in der Abfühlperiode zu generieren;
- eine Datentreiberschaltung (12), die ausgelegt ist, die Schwellenspannungs-Abfühldatenspannung (V_{data}) den Pixeln (P) ansprechend auf den ersten Schwellenspannungs-Abfühl-Gate-Impuls (SCAN) zuzuführen, und eine Source-Spannung (V_s) des Treiber-Dünnfilmtransistors, TFT, (DT) jedes Pixels als Abfühlspannung (V_{sen}) ansprechend auf den zweiten Schwellenspannungs-Abfühl-Gate-Impuls (SEN) zu detektieren; und
- eine Zeitsteuereinheit (11), die ausgelegt ist, eingegebene digitale Videodaten (DATA) für die Bildanzeige auf der Basis einer Änderung in einer Schwellenspannung des Treiber-TFT (DT) zu modulieren, und digitale Kompensationsdaten zu generieren;

wobei die Anzeige ausgelegt ist, die Schwellenspannung des Treiber-TFT (DT) auf der Basis der Abfühlspannung (V_{sen}) zu bestimmen;

wobei die Abfühlperiode zum Abfühlen der Schwellenspannung des Treiber-TFT (DT) in eine erste Periode (T1) und eine zweite Periode (T2) nach der ersten Periode (T1) geteilt ist; und

wobei eine Gate-Spannung (V_g) des Treiber-TFT (DT) jedes Pixels (P) auf einem oder mehreren Spannungspegeln in der ersten Periode (T1) der Abfühlperiode gehalten wird, und auf einem Referenzpegel, der niedriger ist als der eine oder die mehreren Spannungspegel, jedoch höher als die Source-Spannung (V_s), in der zweiten Periode (T2) der Abfühlperiode gehalten wird.

2. Organische lichtemittierende Anzeige nach Anspruch 1, wobei:

die Datentreiberschaltung (12) ferner ausgelegt ist, die Schwellenspannungs-Abfühldatenspannung (V_{data}) des einen oder der mehreren Spannungspegel dem Pixel (P) in der ersten Periode (T1) der Abfühlperiode zuzuführen, und die Schwellenspannungs-Abfühldatenspannung (V_{data}) des Referenzpegels, der niedriger ist als der eine oder die mehreren Spannungspegel, in der zweiten Periode (T2) der Abfühlperiode; und die Gate-Treiberschaltung (13) ferner ausgelegt ist, den ersten Schwellenspannungs-Abfühl-Gate-Impuls (SCAN) auf demselben Ein-Pegel in der ersten und zweiten Periode (T1, T2) der Abfühlperiode zu generieren.

3. Organische lichtemittierende Anzeige nach Anspruch 1, wobei:

die Gate-Treiberschaltung (13) ferner ausgelegt ist, den ersten Schwellenspannungs-Abfühl-Gate-Impuls (SCAN) auf einem ersten Ein-Pegel (L_{on1}) in der ersten Periode (T1) der Abfühlperiode und auf einem zweiten Ein-Pegel (L_{on2}), der von dem ersten Ein-Pegel (L_{on1}) verschieden ist, in der zweiten Periode (T2) der Abfühlperiode zu generieren; und

die Datentreiberschaltung (12) ferner ausgelegt ist, die Schwellenspannungs-Abfühldatenspannung (V_{data}) auf demselben Pegel dem Pixel (P) in der ersten und zweiten Periode (T1, T2) der Abfühlperiode zuzuführen.

4. Organische lichtemittierende Anzeige nach Anspruch 3, wobei die Gate-Treiberschaltung (13) ferner ausgelegt ist, den ersten Schwellenspannungs-Abfühl-Gate-Impuls (SCAN) auf dem ersten Ein-Pegel (L_{on1}) in der ersten Periode (T1) der Abfühlperiode zu generieren, und den ersten Schwellenspannungs-Abfühl-Gate-Impuls (SCAN) auf dem zweiten Ein-Pegel (L_{an2}), der niedriger ist als der erste Ein-Pegel (L_{on1}), in der zweiten Periode (T2) der Abfühlperiode zu generieren.

5. Organische lichtemittierende Anzeige nach Anspruch 1, wobei die Anzeige ferner ausgelegt ist, die Abfühlspannung (V_{sen}) am Ende der Abfühlperiode abzufühlen, um dadurch die Schwellenspannung zu bestimmen.

6. Organische lichtemittierende Anzeige nach Anspruch 1, wobei die Pixel (P) in einer Source-Folger-Weise betrieben werden.

7. Verfahren zum Kompensieren einer Schwellenspannung einer organischen lichtemittierenden An-

zeige, umfassend ein Anzeigefeld (10), das eine Vielzahl von Pixeln (P) aufweist, wobei jedes Pixel (P) umfasst:

- einen Treiber-TFT (DT), der eine Gate-Elektrode, die mit einem ersten Knoten (N1) verbunden ist, eine Source-Elektrode, die mit einem zweiten Knoten (N2) verbunden ist, und eine Drain-Elektrode, die mit einem Eingangsanschluss einer Treibspannung mit hohem Potential (EVDD) verbunden ist, aufweist;
- eine organische lichtemittierende Diode (OLED), die zwischen dem zweiten Knoten (N2) und einem Eingangsanschluss einer Treibspannung mit niedrigem Potential (EVSS) angeschlossen ist;
- einen Speicherkondensator (Cst), der zwischen dem ersten Knoten (N1) und dem zweiten Knoten (N2) angeschlossen ist;
- einen ersten Schalter-TFT (ST1), der zwischen einer Daten-Spannungszufuhrleitung (14A), die auf eine Schwellenspannungs-Abfühldatenspannung (V_{data}) geladen werden kann, und dem ersten Knoten (N1) angeschlossen ist und ein oder ausgeschaltet wird ansprechend auf einen ersten Schwellenspannungs-Abfühl-Gate-Impuls (SCAN); und
- einen zweiten Schalter-TFT (ST2), der zwischen einer Abfühlspannungs-Ausleseleitung (14B) zum Laden der Abfühlspannung (V_{sen}) und dem zweiten Knoten (N2) angeschlossen ist und ein oder ausgeschaltet wird ansprechend auf einen zweiten Schwellenspannungs-Abfühl-Gate-Impuls (SEN);

wobei sowohl der erste als auch zweite Schalter-TFT (ST1, ST2) kontinuierlich in der ersten und zweiten Periode (T1, T2) einer Abfühlperiode ein geschaltet sind;
wobei das Verfahren umfasst:

- Generieren sowohl des ersten Schwellenspannungs-Abfühl-Gate-Impulses (SCAN) als auch des zweiten Schwellenspannungs-Abfühl-Gate-Impulses (SEN) jeweils auf einem Ein-Pegel (L_{on}) in der Abfühlperiode;
- Zuführen der Schwellenspannungs-Abfühldatenspannung (V_{data}) zu den Pixeln (P) ansprechend auf den ersten Schwellenspannungs-Abfühl-Gate-Impuls (SCAN);
- Detektieren einer Source-Spannung (V_s) des Treiber-Dünnfilmtransistors (TFT) (DT) jedes Pixels (P) als Abfühlspannung (V_{sen}) ansprechend auf den zweiten Schwellenspannungs-Abfühl-Gate-Impuls (SEN); und
- Modulieren von eingegebenen digitalen Videodaten (DATA) für die Bildanzeige auf der Basis einer Änderung in einer Schwellenspannung des Treiber-TFT (DT), und Generieren von digitalen Kompensationsdaten;

wobei die Schwellenspannung des Treiber-TFT (DT) auf der Basis der Abfühlspannung (V_{sen}) bestimmt wird;
wobei die Abfühlperiode zum Abfühlen der Schwellenspannung des Treiber-TFT (DT) in eine erste Periode (T1) und eine zweite Periode (T2) nach der ersten Periode (T1) geteilt wird; und
wobei eine Gate-Spannung des Treiber-TFT (DT) jedes Pixels (P) auf einem oder mehreren Spannungspegeln (L1) in der ersten Periode (T1) der Abfühlperiode gehalten wird, und auf einem Referenzpegel (L2), der niedriger ist als der eine oder die mehreren Spannungspegel, jedoch höher als die Source-Spannung (V_s), in der zweiten Periode (T2) der Abfühlperiode gehalten wird.

8. Verfahren nach Anspruch 7, wobei:

die Schwellenspannungs-Abfühldatenspannung (V_{data}) dem Pixel (P) auf dem einen oder den mehreren Spannungspegeln (L1) in der ersten Periode (T1) der Abfühlperiode zugeführt werden, und auf dem Referenzpegel (L2), der niedriger ist als der eine oder die mehreren Spannungspegel (L1), in der zweiten Periode (T2) der Abfühlperiode; und
der erste Schwellenspannungs-Abfühl-Gate-Impuls (SCAN) auf demselben Ein-Pegel (L_{on}) in der ersten und zweiten Periode (T1, T2) der Abfühlperiode generiert wird.

9. Verfahren nach Anspruch 7, wobei:

der erste Schwellenspannungs-Abfühl-Gate-Impuls (SCAN) auf einem ersten Ein-Pegel (L_{on1}) in der ersten Periode (T1) der Abfühlperiode und auf einem zweiten Ein-Pegel (L_{on2}), der von dem ersten Ein-Pegel (L_{on1}) verschieden ist, in der zweiten Periode (T2) der Abfühlperiode generiert wird; und
die Schwellenspannungs-Abfühldatenspannung (V_{data}) auf demselben Pegel dem Pixel (P) in der ersten und zweiten Periode (T1, T2) der Abfühlperiode zugeführt wird.

10. Verfahren nach Anspruch 9, wobei der erste Schwellenspannungs-Abfühl-Gate-Impuls (SCAN) auf einem ersten Ein-Pegel (L_{on1}) in der ersten Periode (T1) der Abfühlperiode generiert wird, und auf einem zweiten Ein-Pegel (L_{on2}), der niedriger ist als der erste Ein-Pegel (L_{on1}), in der zweiten Periode (T2) der Abfühlperiode generiert wird.

11. Verfahren nach Anspruch 7, wobei die Pixel (P) in einer Source-Folger-Weise betrieben werden.

12. Verfahren nach Anspruch 7, ferner umfassend: Abfühlen der Abfühlspannung (V_{sen}) am Ende der Abfühlperiode, um dadurch die Schwellenspannung zu bestimmen.

Revendications

1. Dispositif d'affichage électroluminescent organique comprenant :

- un panneau d'affichage (10) comprenant une pluralité de pixels (P), chaque pixel (P) comprenant :
  - un TFT d'attaque (DT) comprenant une électrode de grille reliée à un premier noeud (N1), une électrode de source reliée à un second noeud (N2) et une électrode de drain reliée à une borne d'entrée d'une tension de commande à potentiel élevé (EVDD) ;
  - une diode électroluminescente organique (OLED) reliée entre le second noeud (N2) et une borne d'entrée d'une tension de commande à bas potentiel (EVSS) ;
  - un condensateur de stockage (Cst) relié entre le premier noeud (N1) et le second noeud (N2) ;
  - un premier TFT de commutation (ST1) qui est relié entre une ligne d'alimentation en tension de données (14A) qui peut être chargée à une tension de données de détection de tension seuil (V_{data}) et le premier noeud (N1) et qui est allumé ou éteint en réponse à une première impulsion de grille de détection de tension seuil (SCAN) ; et
  - un second TFT de commutation (ST2) qui est relié entre une ligne de lecture de voltage de détection (14B) permettant de charger la tension de détection (V_{sen}) et le second noeud (N2) et qui est allumé ou éteint en réponse à une seconde impulsion de grille de détection de tension seuil (SEN),
- dans lequel les deux premier et second TFT de commutation (ST1, ST2) sont allumés en continu pendant la première et la seconde période (T1, T2) d'une période de détection ;
- un circuit d'attaque de grille (13) conçu pour générer à la fois la première impulsion de grille de détection de tension seuil (SCAN) et la seconde impulsion de détection de tension seuil (SEN) chacune à un niveau allumé (L_{on}) dans la période de détection ;
- un circuit d'attaque de données (12) conçue pour fournir la tension de données de détection de tension seuil (V_{data}) aux pixels (P) en réponse à la première impulsion de grille de détection de tension seuil (SCAN), et pour détecter une tension source (V_s) du transistor à couche minces, TFT, d'attaque (DT) de chaque pixel comme la tension de détection (V_{sen}) en réponse à la seconde impulsion de grille de détection de tension seuil (SEN) ; et
- un contrôleur de temporisation (11) conçu pour moduler des données de vidéo digitale d'entrée (DATA) pour l'affichage d'image en fonction d'un changement dans la tension seuil du TFT d'attaque (DT), et pour générer des données de compensation digitales,
- dans lequel l'affichage est conçu pour déterminer la tension seuil du TFT d'attaque (DT) en fonction de la tension de détection (V_{sen}),
- dans lequel la période de détection destinée à la détection de la tension seuil du TFT d'attaque (DT) est divisée en une première période (T1) et en une seconde période (T2) suivant la première période (T1), et
- dans lequel une tension de grille (V_g) du TFT d'attaque (DT) de chaque pixel (P) est maintenue à un ou plusieurs niveaux de tension dans la première période (T1) de la période de détection, et est maintenue à un niveau de référence inférieur auxdits un ou plusieurs niveaux de tension mais supérieur à la tension source (V_s) dans la seconde période (T2) de la période de détection.

2. Dispositif d'affichage électroluminescent organique selon la revendication 1, dans lequel :

- le circuit d'attaque de données (12) est en outre conçu pour fournir la tension de données de détection de tension seuil (V_{data}) de l'un ou de plusieurs niveaux de tension au pixel (P) dans la première période (T1) de la période de détection et la tension de données de détection de tension seuil (V_{data}) du niveau de référence inférieure auxdits un ou plusieurs niveaux de tension dans la seconde période (T2) de la période de détection ; et
- le circuit d'attaque de grille (13) est en outre conçu pour générer la première impulsion de grille de détection de tension seuil (SCAN) au même niveau allumé dans la première et la seconde période (T1, T2) de la période de détection.

3. Dispositif d'affichage électroluminescent organique selon la revendication 1, dans lequel :

- le circuit d'attaque de grille (13) est en outre conçu pour générer la première impulsion de grille de détection de tension seuil (SCAN) à un premier niveau allumé (L_{on1}) dans la première

période (T1) de la période de détection et à un second niveau allumé (L_{on2}) différent du premier niveau allumé (L_{on1}) dans la seconde période (T2) de la période de détection ; et
- le circuit d'attaque de données (12) est en outre conçu pour fournir la tension de données de détection de tension seuil (V_{data}) du même niveau au pixel (P) dans la première et la seconde période (T1, T2) de la période de détection.

4. Dispositif d'affichage électroluminescent organique selon la revendication 3, dans lequel le circuit d'attaque de grille (13) est en outre configuré pour générer la première impulsion de grille de détection de tension seuil (SCAN) au premier niveau allumé (Lon1) dans la première période (T1) de la période de détection, et pour générer la première impulsion de grille de détection de tension seuil (SCAN) au second niveau allumé (L_{on2}) inférieur au premier niveau allumé (L_{on1}) dans la seconde période (T2) de la période de détection.

5. Dispositif d'affichage électroluminescent organique selon la revendication 1, dans lequel l'affichage est en outre conçu pour détecter la tension de détection (V_{sen}) à la fin de la période de détection pour ainsi déterminer la valeur seuil.

6. Dispositif d'affichage électroluminescent organique selon la revendication 1, dans lequel les pixels (P) sont exploités d'une manière suiveuse de source.

7. Procédé de compensation pour une tension seuil d'un dispositif d'affichage électroluminescent organique comprenant un panneau d'affichage (10) comprenant une pluralité de pixels (P), chaque pixel (P) comprenant :

- un TFT d'attaque (DT) comprenant une électrode de grille reliée à un premier noeud (N1), une électrode de source reliée à un second noeud (N2) et une électrode de drain reliée à une borne d'entrée d'une tension de commande à potentiel élevé (EVDD) ;
- une diode électroluminescente organique (OLED) reliée entre le second noeud (N2) et une borne d'entrée d'une tension de commande à bas potentiel (EVSS) ;
- un condensateur de stockage (Cst) relié entre le premier noeud (N1) et le second noeud (N2) ;
- un premier TFT de commutation (ST1) qui est relié entre une ligne d'alimentation en tension de données (14A) qui peut être chargée à une tension de données de détection de tension seuil (V_{data}) et le premier noeud (N1) et qui est allumé ou éteint en réponse à une première impulsion de grille de détection de tension seuil (SCAN) ; et
- un second TFT de commutation (ST2) qui est relié entre une ligne de lecture de voltage de détection (14B) permettant de charger la tension de détection (V_{sen}) et le second noeud (N2) et qui est allumé ou éteint en réponse à une seconde impulsion de grille de détection de tension seuil (SEN),
- dans lequel les deux premier et second TFT de commutation (ST1, ST2) sont allumés en continu pendant la première et la seconde période (T1, T2) d'une période de détection, le procédé comprenant :

  - la génération à la fois de la première impulsion des grilles de détection de tension seuil (SCAN) et de la seconde impulsion de grille de détection de tension seuil (SEN) chacune à un niveau allumé (L_{on}) dans la période de détection ;
  - la fourniture de la tension de données de détection de tension seuil (V_{data}) aux pixels (P) en réponse à la première impulsion de grille de détection de tension seuil (SCAN) ;
  - la détection d'une tension de source (V_s) du transistor à couche minces (TFT) d'attaque (DT) de chaque pixel (P) comme la tension de détection (V_{sen}) en réponse à la seconde impulsion de grille de détection de tension seuil (SEN) ; et
  - la modulation de données de vidéo digitale d'entrée (DATA) pour l'affichage d'image en fonction d'un changement dans une tension seuil du TFT d'attaque (DT), et la génération de données de compensation digitales,

- dans lequel la tension seuil du TFT d'attaque (DT) est déterminée en fonction de la tension de détection (V_{sen}),
- dans lequel la période de détection destinée à la détection de la tension seuil du TFT d'attaque (DT) est divisée en une première période (T1) et en une seconde période (T2) suivant la première période (T1), et
- dans lequel une tension de grille du TFT d'attaque (DT) de chaque pixel (P) est maintenue à un ou plusieurs niveaux de tension dans la première période (T1) de la période de détection, et est maintenue à un niveau de référence (L2) inférieur à l'un ou plusieurs niveaux de tension (L1) mais supérieur à la tension source (V_s) dans la seconde période (T2) de la période de détection.

8. Procédé selon la revendication 7, dans lequel :

- la tension de données de détection de tension seuil (V_{data}) est fournie au pixel (P) à l'un ou plusieurs niveaux de tension (L1) dans la pre-

mière période (T1) de la période de détection et au niveau de référence (L2) inférieur à l'un ou plusieurs niveau de tension (L1) dans la seconde période (T2) de la paire de détection ; et
- la première impulsion de grille de détection de tension seuil (SCAN) est généré au même niveau allumé (L_{on}) dans la première et la seconde période (T1, T2) de la période de détection.

9. Procédé selon la revendication 7, dans lequel :

- la première impulsion de grille de détection de tension seuil (SCAN) est générée à un premier niveau allumé (L_{on1}) dans la première période (T1) de la période de détection et à un second niveau allumé (L_{on2}) différent du premier niveau allumé (L_{on1}) dans la seconde période (T2) de la période de détection ; et
- la tension de données de détection de tension seuil (V_{data}) est fournie au pixel (P) au même niveau dans la première et la seconde période (T1, T2) de la période de détection.

10. Procédé selon la revendication 9, dans lequel la première impulsion de grille de détection de tension seuil (SCAN) est générée à un premier niveau allumé (L_{on1}) dans la première période (T1) de la période de détection et est générée à un second niveau allumé (L_{on2}) inférieur au premier niveau allumé (L_{on1}) dans la seconde période (T2) de la période de détection.

11. Procédé selon la revendication 7, dans lequel les pixels (P) sont exploités d'une manière suiveuse de source.

12. Procédé selon la revendication 7, comprenant en outre :

- la détection de la tension de détection (V_{sen}) à la fin de la période de détection afin de déterminer la tension seuil.

FIG. 1

(RELATED ART)

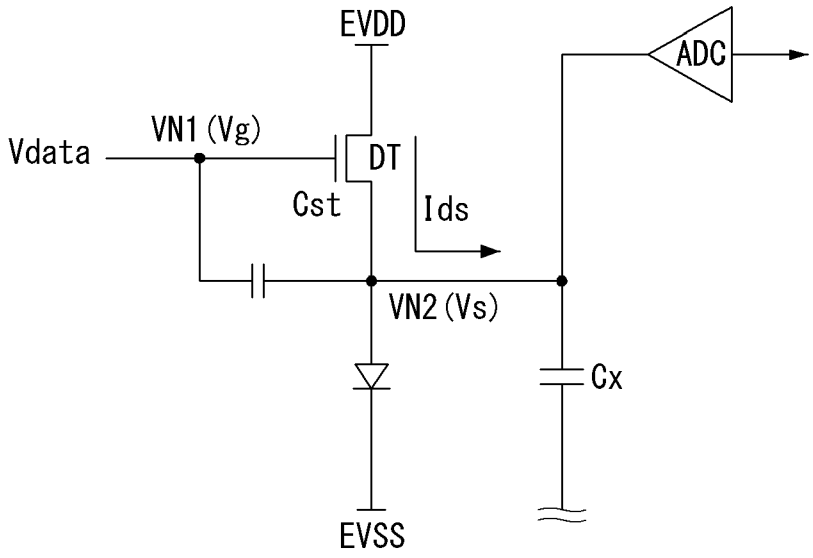


FIG. 2

(RELATED ART)

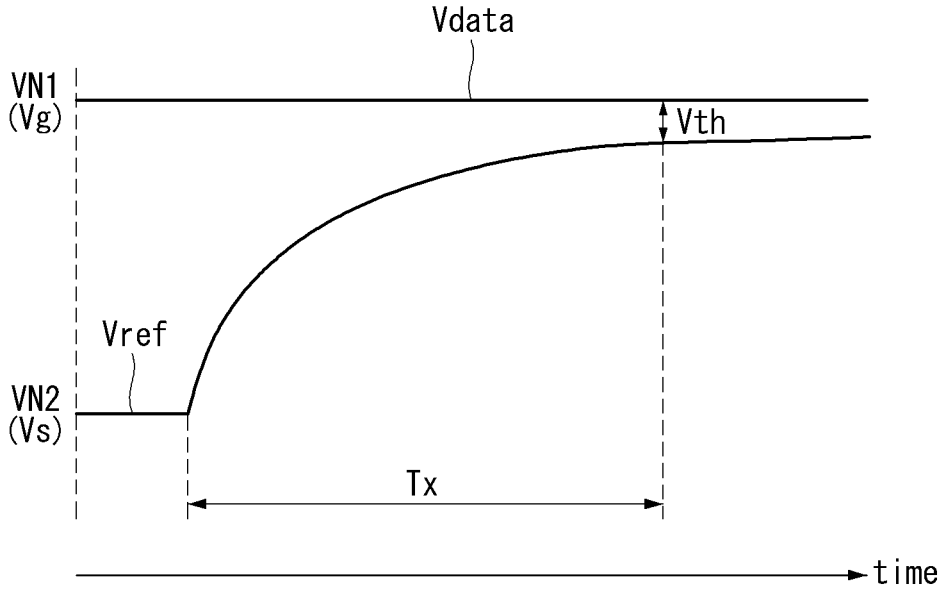


FIG. 3

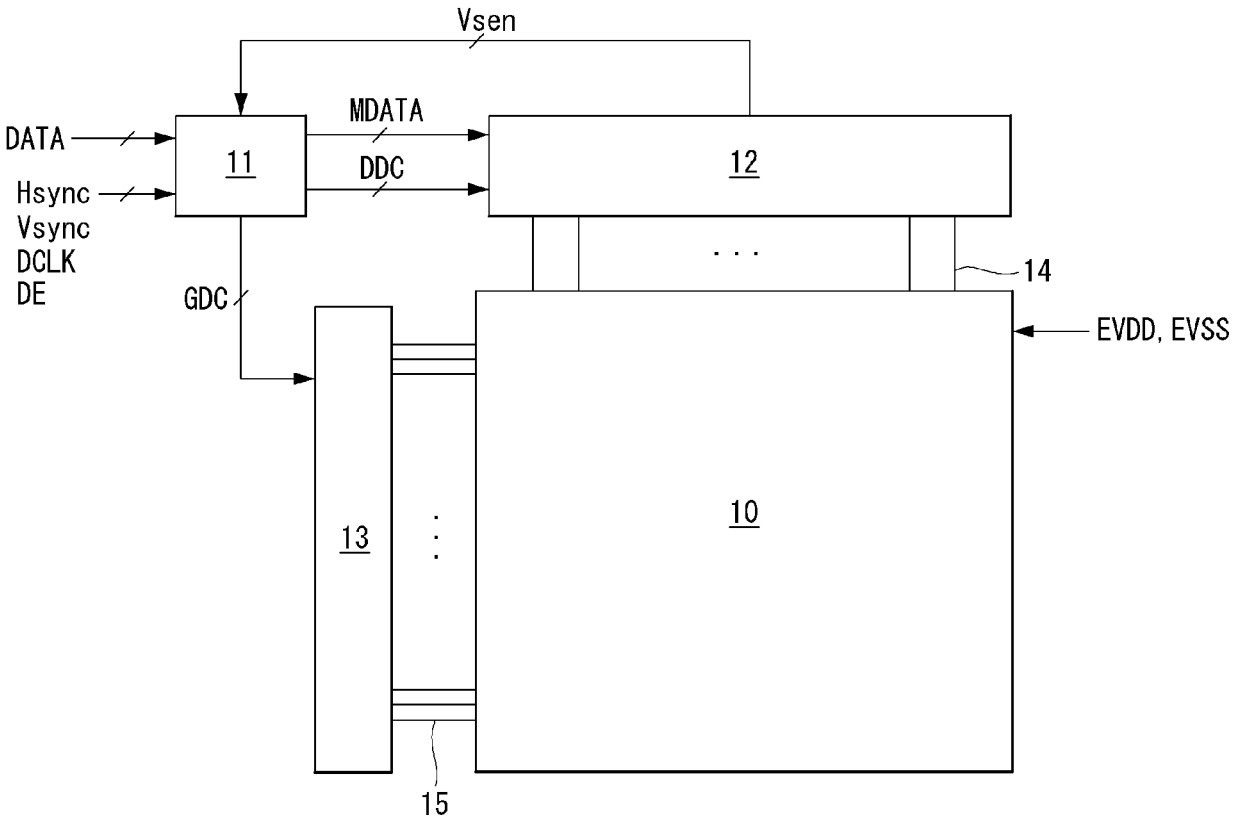

Vsen
DATA
Hsync
Vsync
DCLK
DE
11
MDATA
DDC
12
GDC
14
EVDD, EVSS
13
10
15

FIG. 4

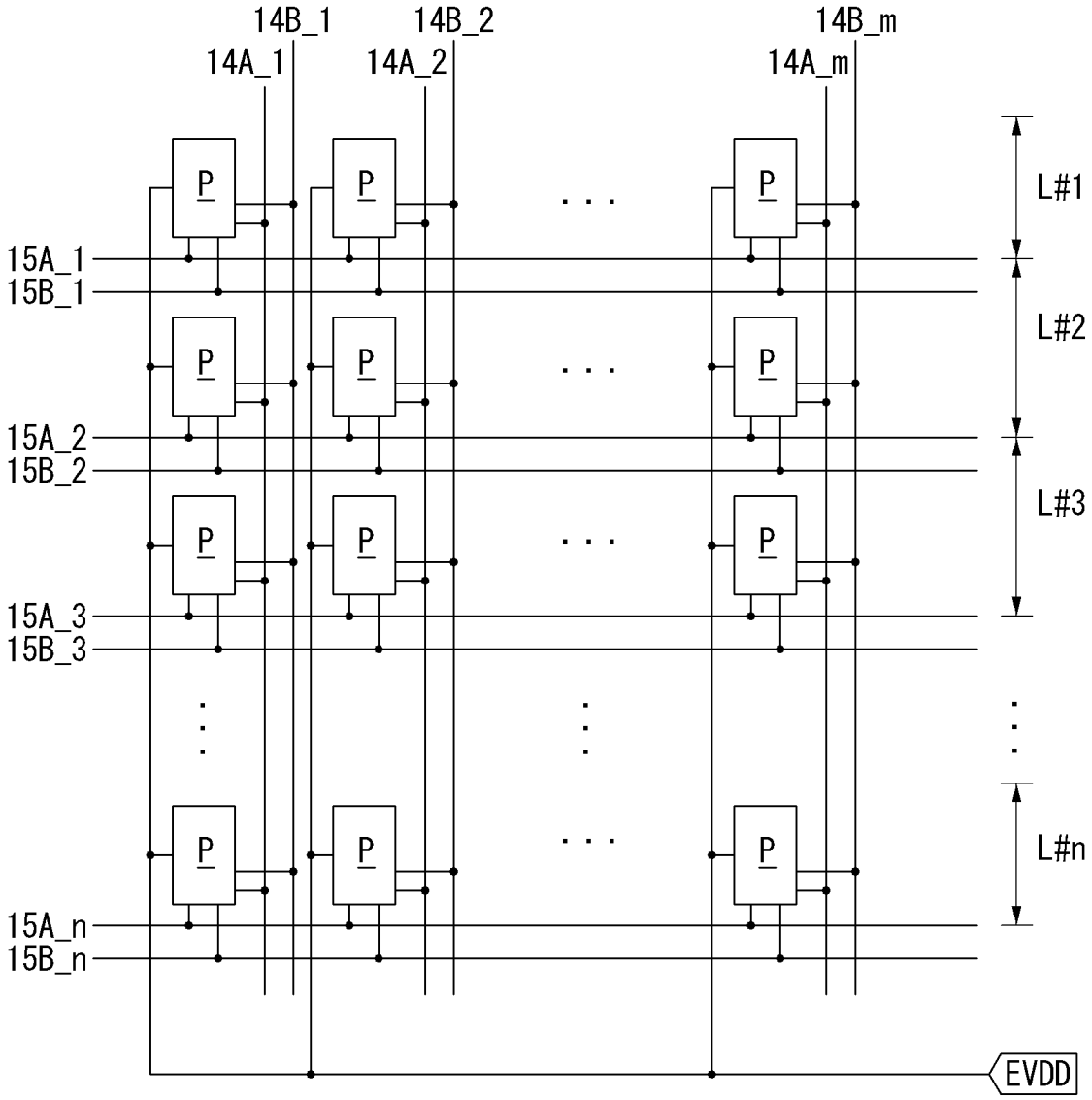

14B_1
14B_2
14B_m
14A_1
14A_2
14A_m
P
15A_1
15B_1
15A_2
15B_2
15A_3
15B_3
15A_n
15B_n
L#1
L#2
L#3
L#n
EVDD

FIG. 5

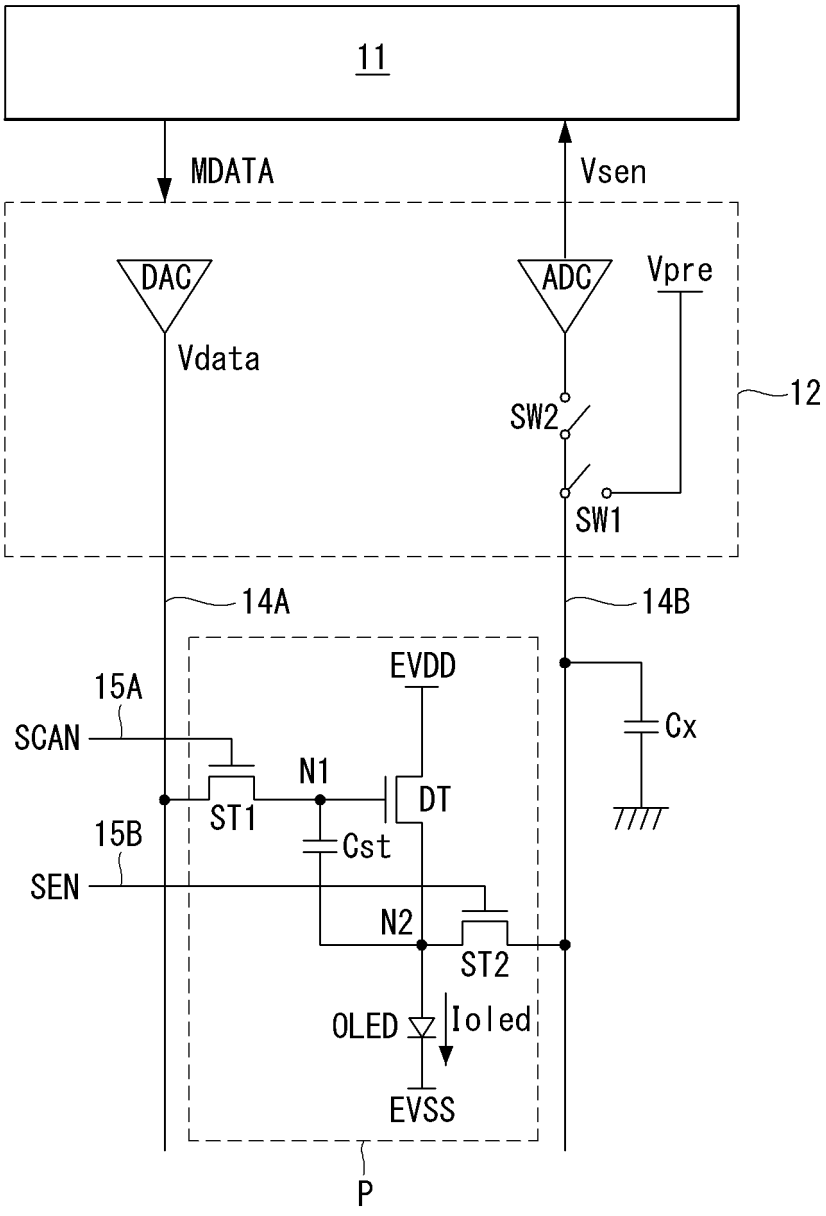

11
MDATA
Vsen
DAC
Vdata
ADC
Vpre
SW2
SW1
12
14A
14B
15A
SCAN
EVDD
Cx
N1
ST1
DT
15B
Cst
SEN
N2
ST2
OLED
Ioled
EVSS
P

FIG. 6

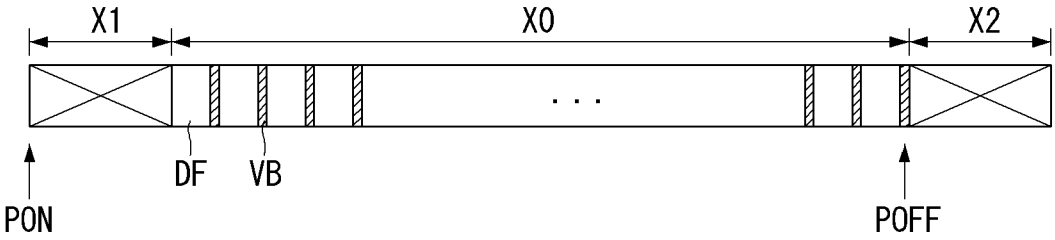

X1
X0
X2
DF
VB
PON
POFF

FIG. 7

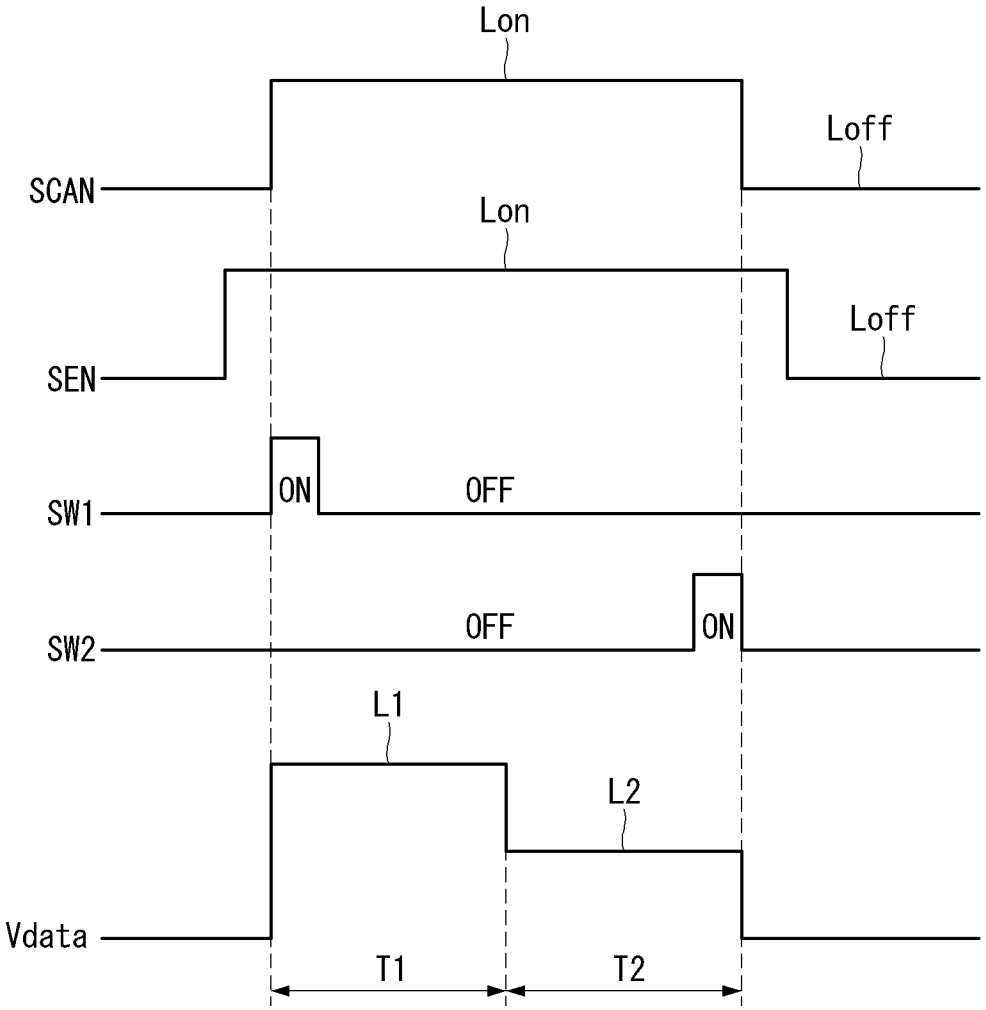

Lon
Loff
SCAN
Lon
Loff
SEN
ON
OFF
SW1
OFF
ON
SW2
L1
L2
Vdata
T1
T2

FIG. 8

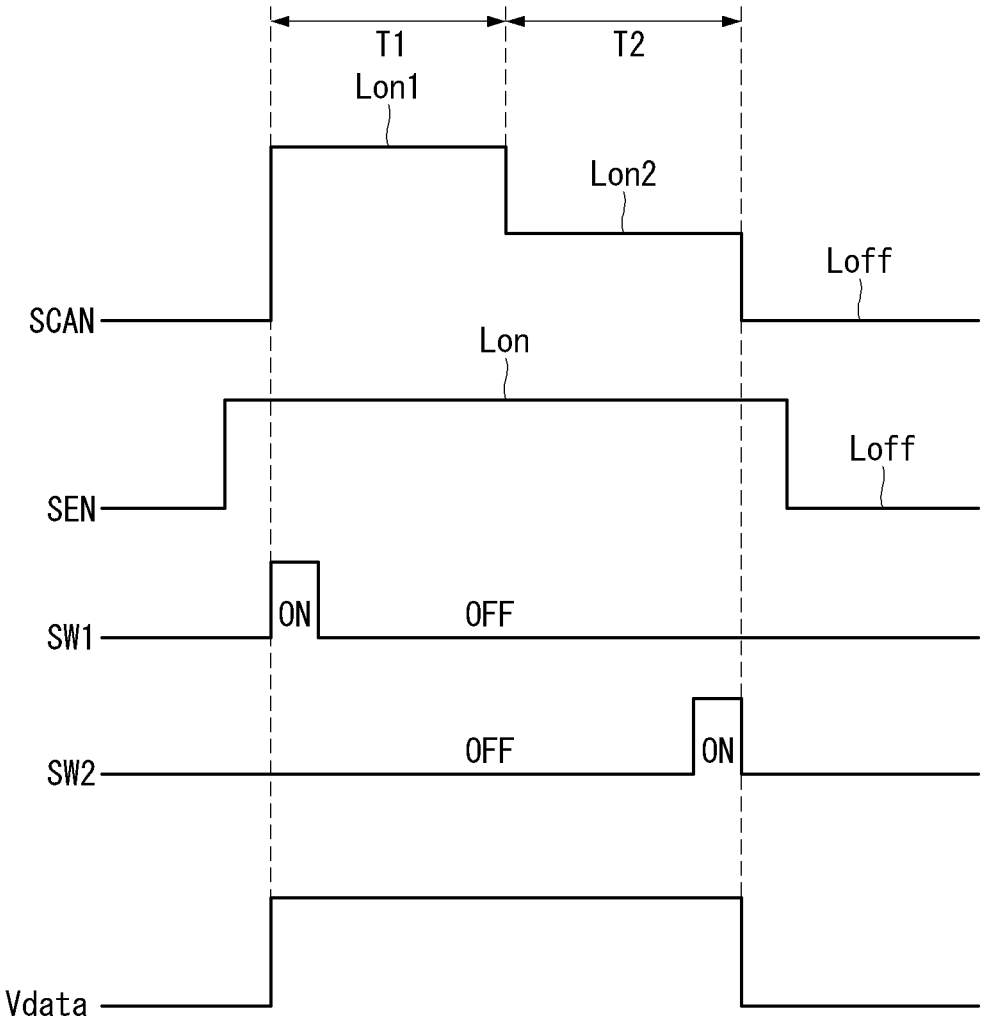

T1
T2
Lon1
Lon2
Loff
SCAN
Lon
Loff
SEN
ON
OFF
SW1
OFF
ON
SW2
Vdata

FIG. 9A

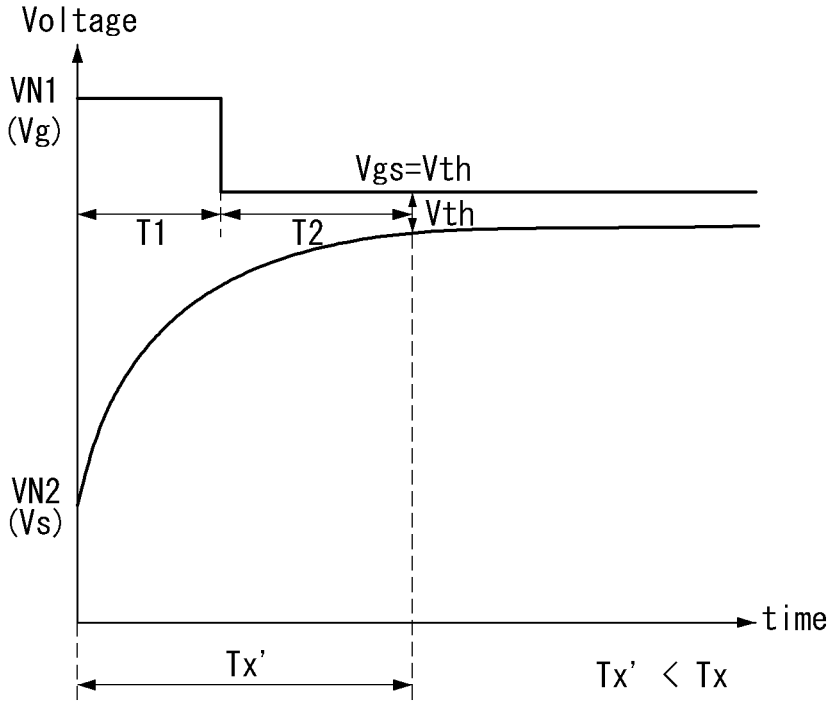


FIG. 9B

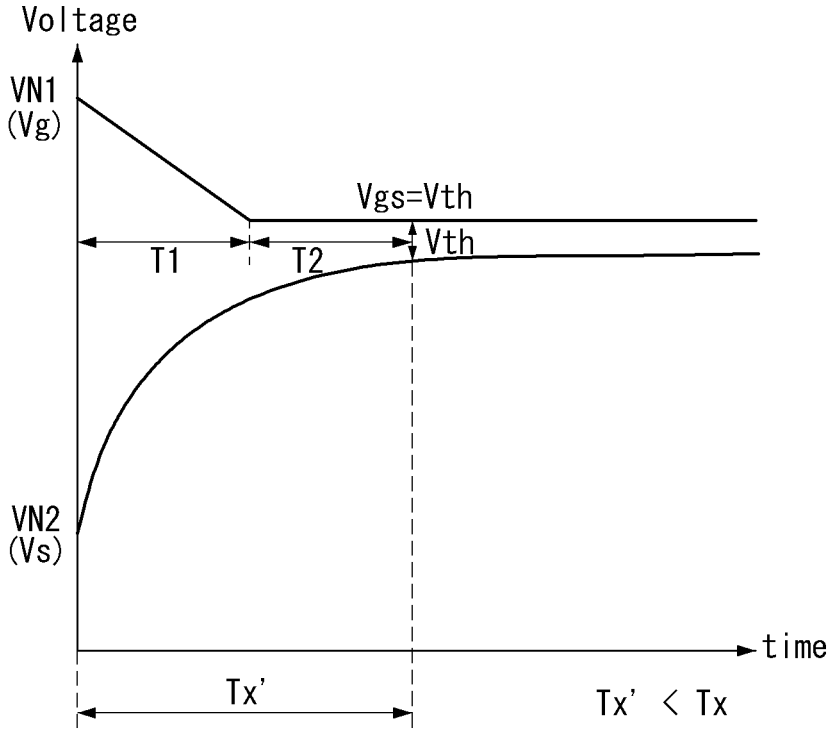


FIG. 9C

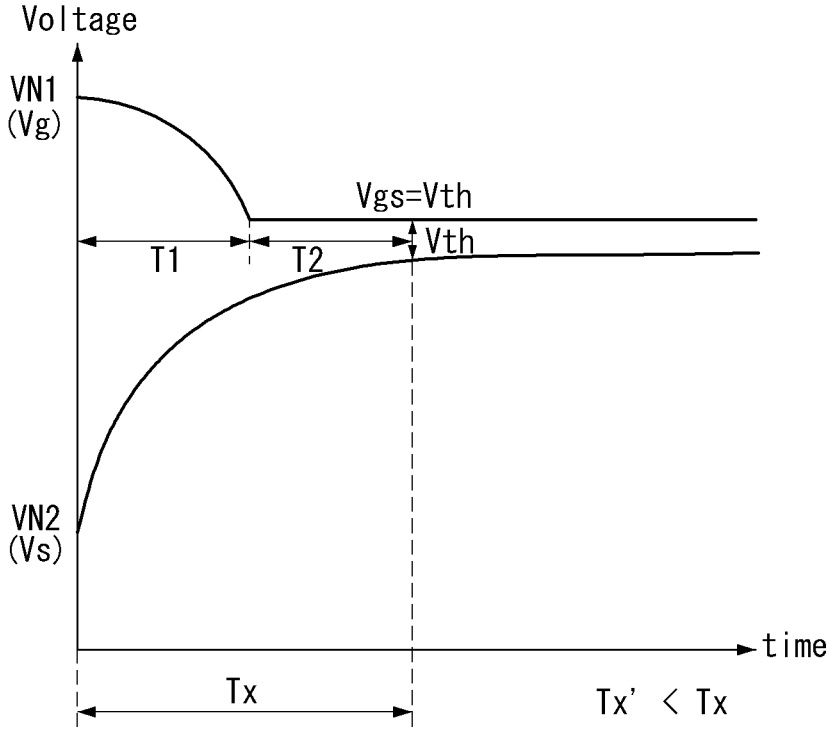


FIG. 10

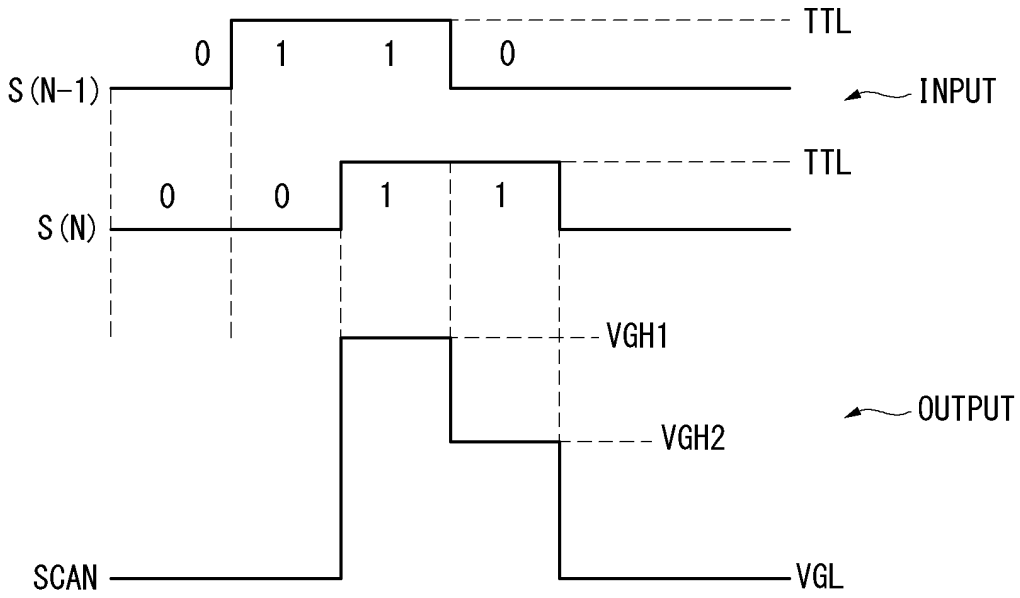

TTL
0
1
1
0
S(N-1)
INPUT
TTL
0
0
1
1
S(N)
VGH1
OUTPUT
VGH2
SCAN
VGL

FIG. 11

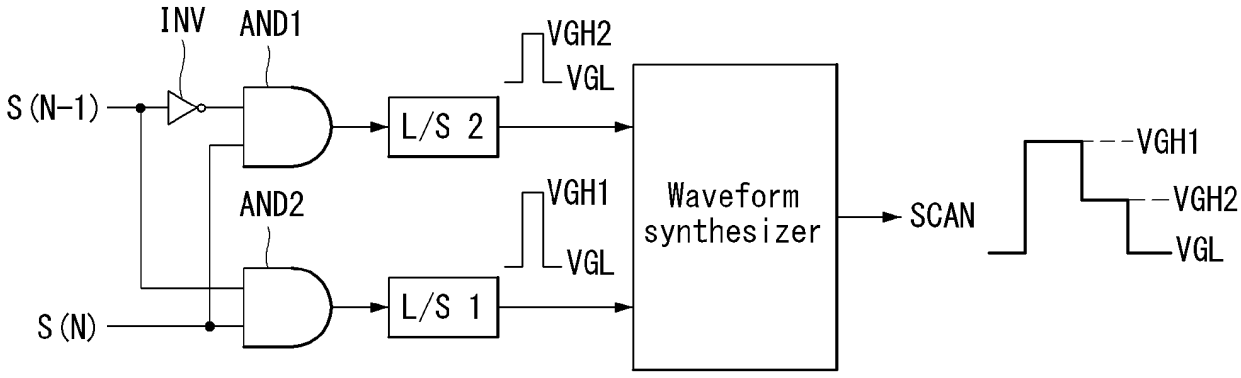
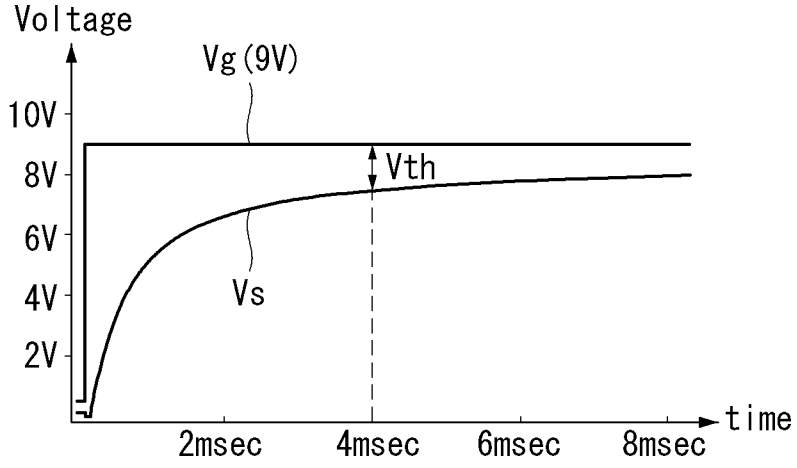
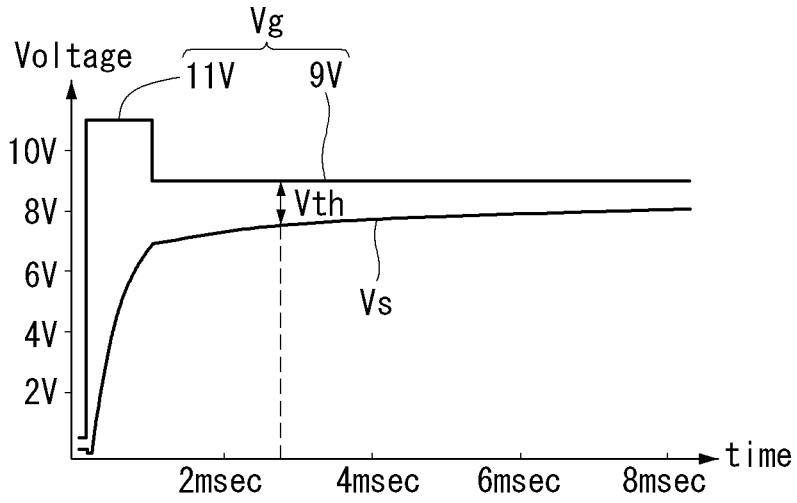

INV
AND1
VGH2
VGL
S(N-1)
L/S 2
AND2
VGH1
VGL
Waveform synthesizer
SCAN
VGH1
VGH2
VGL
L/S 1
S(N)

FIG. 12



(A)Related art



(B)

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2013201173 A1 **[0006]**
- US 2013050292 A1 **[0006]**

专利名称(译)	有机发光显示器及其阈值电压的补偿方法		
公开(公告)号	EP2876634B1	公开(公告)日	2018-10-10
申请号	EP2014192646	申请日	2014-11-11
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	PARK KWANGMO		
发明人	PARK, KWANGMO		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G3/3291 G09G2300/043 G09G2300/0819 G09G2300/0842 G09G2320/0233 G09G3/3258 G09G2310/08		
优先权	1020130141334 2013-11-20 KR		
其他公开文献	EP2876634A1		
外部链接	Espacenet		

摘要(译)

公开了一种有机发光显示器和补偿其阈值电压的方法。有机发光显示器包括：显示面板（10），包括多个像素（P）;栅极驱动电路（13），产生第一和第二阈值电压感测栅极脉冲;数据驱动电路（12），提供阈值电压响应于第一阈值电压感测栅极脉冲感测到像素（P）的数据电压，并且响应于第二阈值电压将每个像素（P）的驱动薄膜晶体管（TFT）的源电压检测为感测电压感测门脉冲和定时控制器（11），其基于感测电压的变化调制用于图像显示的输入数字视频数据并产生数字补偿数据。

FIG. 1

(RELATED ART)