(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 747 062 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
25.06.2014 Bulletin 2014/26

(51) Int Cl.:
G09G 3/00 *(2006.01)* ***H01L 27/00*** *(2006.01)*

(21) Application number: **13194955.4**

(22) Date of filing: **28.11.2013**

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME

(30) Priority: **29.11.2012 KR 20120137356**

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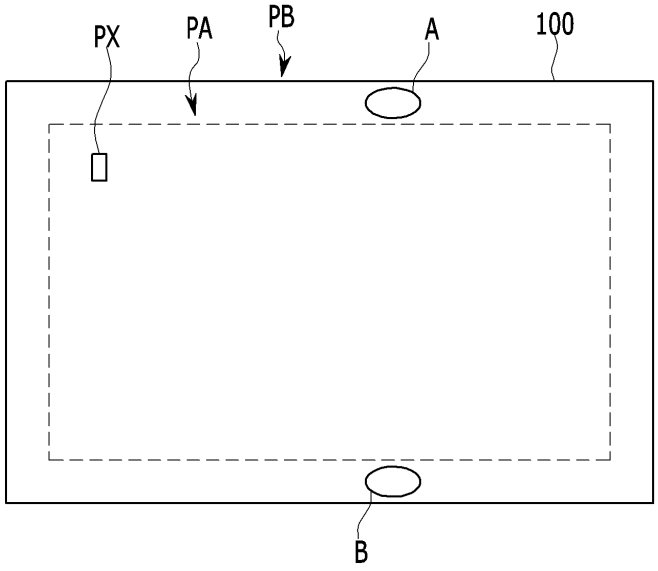
(54) Organic light emitting diode display

(57) Disclosed is an organic light emitting diode display including: a pixel unit including an organic light emitting diode for displaying an image; and a periphery surrounding the pixel unit. The periphery includes a gate common voltage line formed on the substrate and receiving a common voltage from an external circuit, an interlayer insulating layer covering the gate common voltage line and including a common voltage contact hole for exposing a part of the gate common voltage line, a data common voltage line formed on the interlayer insulating layer and contacting the gate common voltage line through the common voltage contact hole, and a plurality of protrusions provided in the common voltage contact hole and formed on the substrate.

FIG. 1



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Description

[0001] The described technology relates generally to an organic light emitting diode (OLED) display.

[0002] An organic light emitting diode display typically includes two electrodes and an organic emission layer interposed therebetween, electrons injected from one electrode (the cathode) and holes injected from the other electrode (the anode) combine in the organic emission layer to form an exciton, and light is emitted while the exciton discharges energy.

[0003] Each pixel of the organic light emitting diode display typically includes a switching thin film transistor, a driving thin film transistor, a capacitor, and an organic light emitting diode. A driving voltage ELVDD is supplied from a driving voltage line to the driving thin film transistor and the capacitor, and the driving thin film transistor serves to control the current flowing to the organic light emitting diode through the driving voltage line. A common voltage line supplies a common voltage ELVSS to the cathode and forms a potential difference between a pixel electrode as an anode and a common electrode, thereby causing a current between the pixel electrode and the common electrode.

[0004] The common voltage ELVSS is transmitted to the common electrode formed on barrier ribs by continuous contact among a gate common voltage contact unit including gate lines, a data common voltage contact unit including data lines, and the common electrode, which are formed in a peripheral region.

[0005] However, because of a thickness of the barrier ribs, during manufacture a developer may not be sufficiently vaporized so a lifting phenomenon may be generated at a border of a contact hole formed in the barrier rib.

[0006] Regarding the lifting phenomenon, a common electrode provided on the barrier rib is passed through the contact hole to deteriorate adherence with a bottom metal film and generate heat.

[0007] The above information disclosed in this Background section is only for enhancement of understanding of the background of the described technology and therefore it may contain information that does not form the prior art that is already known in this country to a person of ordinary skill in the art.

[0008] The described technology has been made in an effort to provide an organic light emitting diode (OLED) display with reduced heat generation.

[0009] An exemplary embodiment provides an organic light emitting diode (OLED) display including: a pixel unit formed on a substrate and including an organic light emitting diode for displaying an image; and a periphery surrounding the pixel unit, wherein the periphery includes a gate common voltage line formed on the substrate and receiving a common voltage from an external circuit, an interlayer insulating layer for covering the gate common voltage line and including a common voltage contact hole for exposing a part of the gate common voltage line, a data common voltage line formed on the interlayer insulating layer and contacting the gate common voltage line through the common voltage contact hole, a barrier rib covering the data common voltage line and including a common voltage opening exposing a part of the data common voltage line, a common electrode formed on the barrier rib and contacting the data common voltage line through the common voltage opening, and a plurality of protrusions provided in the common voltage contact hole and formed on the substrate.

[0010] The organic light emitting diode includes a first electrode, an organic emission layer provided on the first electrode, and a second electrode provided on the organic emission layer, and the common electrode is integrally formed with the second electrode.

[0011] The second electrode is formed on the pixel unit.

[0012] The pixel unit includes a thin film transistor for connecting the first electrode to a drain electrode of the thin film transistor.

[0013] The protrusion is formed with a material that includes a material of a semiconductor of the thin film transistor.

[0014] The organic light emitting diode display further includes a buffer layer formed on the substrate, wherein the protrusion includes a first protrusion made of the same material as the buffer layer, and a second protrusion provided on the first protrusion and made of the same material as the semiconductor.

[0015] The organic light emitting diode display further includes a buffer layer formed on the substrate, wherein the protrusion is made of the same material as the buffer layer.

[0016] The buffer layer includes at least one of silicon nitride and silicon oxide.

[0017] The substrate includes a recess portion provided between neighboring protrusions.

[0018] The pixel unit includes: a gate line formed on the substrate and transmitting a scan signal; a data line and a driving voltage line crossing the gate line in an insulated manner and transmitting a data signal and a driving voltage, respectively; a switching thin film transistor connected to the gate line and the data line; a driving thin film transistor connected to the switching thin film transistor and the driving voltage line; a first electrode connected to the driving thin film transistor; an organic emission layer formed on the first electrode; and a second electrode formed on the organic light emitting diode, wherein the gate common voltage line is formed on the same layer as the gate line, and the data common voltage line is formed on the same layer as the data line.

[0019] According to an aspect of the present invention, there is provided an organic light emitting diode display as set out in claim 1. Preferred features are set out in claims 2 to 11.

[0020] A contact area of the common electrode and the common voltage line is increased by the protrusion of the organic light emitting device according to the em-

bodiments of the invention so contact resistance is reduced. Therefore, generation of heat caused by an increase of resistance according to the lifting phenomenon of the barrier rib can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021]

FIG. 1 shows a top plan view of an organic light emitting diode (OLED) display according to an exemplary embodiment.
FIG. 2 shows an equivalent circuit for a pixel of an organic light emitting diode (OLED) display according to an exemplary embodiment.
FIG. 3 shows a cross-sectional view of a pixel of an organic light emitting diode (OLED) display according to an exemplary embodiment.
FIG. 4 shows a magnified top plan view of a side portion (A) in a periphery of FIG. 1.
FIG. 5 shows a cross-sectional view with respect to a line V-V of FIG. 4.
FIG. 6 shows a magnified top plan view of a side portion (B) in a periphery of FIG. 1.
FIG. 7 shows cross-sectional view with respect to a line VII-VII of FIG. 6.
FIG. 8 shows a cross-sectional view of a side portion (B) in a periphery according to another exemplary embodiment.

[0022] The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown.

[0023] As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the scope of the present invention.

[0024] The drawings and description are to be regarded as illustrative in nature and not restrictive. Like reference numerals designate like elements throughout the specification.

[0025] Further, the size and thickness of each component shown in the drawings are arbitrarily shown for better understanding and ease of description, but the present invention is not limited thereto.

[0026] In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. For understanding and ease of description, the thickness of some layers and areas is exaggerated. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

[0027] In addition, unless explicitly described to the contrary, the word "comprise" and variations such as "comprises" or "comprising" will be understood to imply the inclusion of stated elements but not the exclusion of any other elements. The word "on" means positioned on or below the object portion, but does not essentially mean positioned on the upper side of the object portion based on a gravity direction.

[0028] FIG. 1 shows a top plan view of an organic light emitting diode (OLED) display according to an exemplary embodiment.

[0029] As shown in FIG. 1, the organic light emitting diode (OLED) display includes a substrate 100, a pixel unit (PA) formed on the substrate 100 and including a plurality of pixels (PX) configured by an organic light emitting diode (LD), and a periphery (PB) surrounding the pixel unit (PA).

[0030] The pixel (PX) will now be described with reference to FIG. 2.

[0031] FIG. 2 shows an equivalent circuit for a pixel of an organic light emitting diode (OLED) display according to an exemplary embodiment.

[0032] A detailed configuration of the pixel of the display panel is shown in FIG. 2 and FIG. 3, and the exemplary embodiment is not restricted to the configuration shown in FIG. 2 and FIG. 3. The wire and the organic light emitting diode may be formed in various structures within the range in which those skilled in the art can readily make modifications. For example, the accompanying drawing shows a two-transistors-one-capacitor (2Tr-1Cap) structured active matrix (AM) type of display device in which one pixel includes two thin film transistors (TFTs) and one capacitor, and the embodiment is not limited thereto. Therefore, the display device does not restrict numbers of thin film transistors, capacitors, and wires. In addition, the pixel represents the minimum unit for displaying an image, and the display device uses a plurality of pixels to display the image.

[0033] As shown in FIG. 2, the display device includes a plurality of signal lines 121, 171, and 172 and a plurality of pixels (PX) connected thereto and arranged in a matrix form.

[0034] The signal line includes a plurality of gate lines 121 for transmitting a gate signal (or a scan signal), a plurality of data lines 171 for transmitting a data signal, and a plurality of driving voltage lines 172 for transmitting a driving voltage (ELVDD). The gate lines 121 are provided in a row direction and are substantially parallel with each other, and parts of the data lines 171 and the driving voltage lines 172 in a vertical direction are provided in a column direction and are substantially parallel with each other.

[0035] In this embodiment, the pixel (PX) includes a switching thin film transistor (Qs), a driving thin film transistor (Qd), a storage capacitor (Cst), and an organic light emitting diode (OLED) (LD).

[0036] The switching thin film transistor (Qs) includes a control terminal, an input terminal, and an output terminal, and the control terminal is connected to the gate line 121, the input terminal is connected to the data line 171, and the output terminal is connected to the driving thin film transistor (Qd). The switching thin film transistor

(Qs) responds to the scan signal applied to the gate line 121 to transmit the data signal applied to the data line 171 to the driving thin film transistor (Qd).

[0037] The driving thin film transistor (Qd) includes a control terminal, an input terminal, and an output terminal, and the control terminal is connected to the switching thin film transistor (Qs), the input terminal to the driving voltage line 172, and the output terminal to the organic light emitting diode (LD). The driving thin film transistor (Qd) outputs an output current (I_{LD}) that is variable according to a voltage between the control terminal and the output terminal.

[0038] The capacitor (Cst) is connected between the control terminal of the driving thin film transistor (Qd) and the input terminal. The capacitor (Cst) charges the data signal applied to the control terminal of the driving thin film transistor (Qd) and maintains it when the switching thin film transistor (Qs) is turned off.

[0039] In this embodiment, the organic light emitting diode (LD) includes an anode connected to the output terminal of the driving thin film transistor (Qd) and a cathode connected to a common voltage (ELVSS). The organic light emitting diode (LD) of this embodiment changes intensity and emits light depending on the output current (I_{LD}) of the driving thin film transistor (Qd) to thus display the image.

[0040] An inter-layer structure of an organic light emitting diode (OLED) display according to an exemplary embodiment will now be described with reference to FIG. 2 and FIG. 3.

[0041] FIG. 3 shows a cross-sectional view of a pixel of an organic light emitting diode (OLED) display according to an exemplary embodiment.

[0042] The cross-sectional view of FIG. 3 shows a thin film transistor connected to an organic light emitting diode according to an embodiment.

[0043] As shown in FIG. 2 and FIG. 3, the organic light emitting diode (OLED) display includes a substrate 100, and a buffer layer 120 is formed on the substrate 100.

[0044] The substrate 100 can be a polymer substrate made of a polymer material, or a glass substrate.

[0045] The buffer layer 120 can be formed with a single film of silicon nitride (SiN_x) or a plurality of multilayers that are generated by stacking silicon nitride (SiN_x) and silicon oxide (SiO_2). The buffer layer 120 prevents permeation of undesired components such as impurity or moisture, and smoothes its surface.

[0046] In this embodiment, a semiconductor 135 of polysilicon is formed on the buffer layer 120.

[0047] The semiconductor 135 includes a channel region 1355, and a source region 1356 and a drain region 1357 that are formed on both sides of the channel region 1355. The channel region 1355 of the semiconductor 135 is polysilicon to which an impurity is not doped, that is, an intrinsic semiconductor. The source region 1356 and the drain region 1357 of the semiconductor 135 are polysilicon to which a conductive impurity is doped, that is, an impurity semiconductor.

[0048] The source region 1356 and the drain region 1357 can be one of a p-type impurity and an n-type impurity.

[0049] A gate insulating layer 140 is formed on the semiconductor 135. The gate insulating layer 140 can be formed with a single layer of tetra ethyl ortho silicate (TEOS), silicon oxide (SiO_2), or silicon nitride (SiN_x), or a plurality of multilayers that are formed by stacking silicon oxide (SiO_2) and silicon nitride (SiN_x).

[0050] A gate electrode 155 is formed on the gate insulating layer 140, and the gate electrode 155 overlaps the channel region 1355.

[0051] The gate electrode 155 can be formed with a single layer or multilayers of a low-resistance material such as Al, Ti, Mo, Cu, Ni, or an alloy thereof, or a high-corrosion material.

[0052] A first interlayer insulating layer 160 is formed on the gate electrode 155.

[0053] In a like manner of the gate insulating layer 140, the first interlayer insulating layer 160 can be formed with a single layer of tetra ethyl ortho silicate (TEOS), silicon oxide (SiO_2), or silicon nitride (SiNx), or a plurality of multilayers that are formed by stacking silicon oxide (SiO_2) and silicon nitride (SiNx).

[0054] The first interlayer insulating layer 160 and the gate insulating layer 140 include a source contact hole 166 for exposing the source region 1356 and a drain contact hole 167 for exposing the drain region 1357.

[0055] A source electrode 173 and a drain electrode 175 are formed on the first interlayer insulating layer 160.

[0056] The source electrode 173 and the drain electrode 175 are respectively connected to the source region 1356 and the drain region 1357 through the contact holes 166 and 167.

[0057] The drain electrode 175 can be formed with a single layer or multilayers of a low-resistance material such as Al, Ti, Mo, Cu, Ni, or an alloy thereof, or a high-corrosion material. For example, the drain electrode 175 can be triple layers of Ti/Cu/Ti, Ti/Ag/Ti, or Mo/Al/Mo.

[0058] A second interlayer insulating layer 180 is formed on the drain electrode 175.

[0059] In a like manner of the first interlayer insulating layer, the second interlayer insulating layer 180 can be formed with a single layer of tetra ethyl ortho silicate (TEOS), silicon oxide (SiO_2), or silicon nitride (SiNx), or a plurality of multilayers that are formed by stacking silicon oxide (SiO_2) and silicon nitride (SiNx). The second interlayer insulating layer 180 can also be formed with a low dielectric constant organic material.

[0060] A contact hole 82 for exposing the drain electrode 175 is formed in the second interlayer insulating layer 180.

[0061] A first electrode 710 is formed on the second interlayer insulating layer 180. The first electrode 710 can be the anode of the organic light emitting diode shown in FIG. 2. An interlayer insulating layer is formed between the first electrode 710 and the drain electrode 175, and the first electrode 710 can be formed on the

same layer as the drain electrode 175 and can be integrally formed with the drain electrode 175.

[0062] A barrier rib 190 is formed on the first electrode 710.

[0063] The barrier rib 190 has an opening 195 for exposing the first electrode 710. The barrier rib 190 includes a resin of a polyacrylate or a polyimide and a silica-based inorganic material.

[0064] An organic emission layer 720 is formed in the opening 195 of the barrier rib 190.

[0065] The organic emission layer 720 is formed to be multiple layers including at least one of an emission layer, a hole injection layer (HIL), a hole transport layer (HTL), an electron transport layer (ETL), and an electron injection layer (EIL).

[0066] When the organic emission layer 720 includes all of them, the hole injection layer (HIL) is provided on the first electrode 710, and the anode, the hole transport layer (HTL), the emission layer, the electron transport layer (ETL), and the electron injection layer (EIL) are sequentially stacked thereon.

[0067] A second electrode 730 is formed on the barrier rib 190 and the organic emission layer 720.

[0068] The second electrode 730 becomes the common electrode, which is the cathode of the organic light emitting diode. Therefore, the first electrode 710, the organic emission layer 720, and the second electrode 730 configure an organic light emitting diode 70 in this embodiment.

[0069] The organic light emitting diode (OLED) display according to embodiments of the invention can be a front display type, a rear display type, or a both-side display type according to a direction in which the organic light emitting diode 70 emits light.

[0070] In the case of the front display type, the first electrode 710 is formed to be a reflective layer and the second electrode 730 is formed to be a semi-reflective layer or a transmissive layer. In the case of the rear display type, the first electrode 710 is formed to be a semi-transmissive layer and the second electrode 730 is formed to be a reflective layer. In the case of the both-side display type, the first electrode 710 and the second electrode 730 are formed to be transparent layers or semi-transmissive layer.

[0071] The reflective layer and the semi-transmissive layer are made of at least one metal of magnesium (Mg), silver (Ag), gold (Au), calcium (Ca), lithium (Li), chromium (Cr), and aluminum (Al), or an alloy thereof. The reflective layer and the semi-transmissive layer are determined by thickness, and the semi-transmissive layer can be formed to be less than 200 nm thick. Optical transmittance is increased when the thickness is reduced, but when it is too thin, resistance is increased.

[0072] The transparent layer is made of indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), or indium oxide (In_2O_3).

[0073] An encapsulation layer 130 is formed on the second electrode 730. The encapsulation layer 130 can be formed by alternately stacking at least one organic layer and at least one inorganic layer. There may be multiple inorganic layers or organic layers.

[0074] In this embodiment, the organic layer is formed of a polymer, and desirably it may be a single layer or a deposition layer including one of polyethylene terephthalate, a polyimide, a polycarbonate, an epoxy, polyethylene, and a polyacrylate. Further desirably, the organic layer can be formed with a polyacrylate, and in detail, it includes a polymerized monomer composition including di-acrylate monomer and tri-acrylate monomer. A mono-acrylate monomer can be included in the monomer composition. Also, a photoinitiator such as TPO can be further included in the monomer composition, but is not limited thereto.

[0075] The inorganic layer can be a single layer or a deposition layer including a metal oxide or a metal nitride. In detail, the inorganic layer can include one of SiN_x, Al_2O_3, SiO_2, and TiO_2.

[0076] The externally exposed uppermost layer of the encapsulation layer 130 can be formed with an inorganic layer so as to prevent permeation of vapor into the organic light emitting diode.

[0077] The encapsulation layer can include at least one sandwich configuration in which at least one organic layer is inserted between at least two inorganic layers. Further, the encapsulation layer can include at least one sandwich configuration in which at least one inorganic layer is included between at least two organic layers.

[0078] The encapsulation layer can sequentially include a first inorganic layer, a first organic layer, and a second inorganic layer in order from top to bottom of the display. In addition, the encapsulation layer can sequentially include a first inorganic layer, a first organic layer, a second inorganic layer, a second organic layer, and a third inorganic layer in order from top to bottom of the display. Further, the encapsulation layer can sequentially include a first inorganic layer, a first organic layer, a second inorganic layer, a second organic layer, a third inorganic layer, a third organic layer, and a fourth inorganic layer in order from top to bottom of the display.

[0079] A metal halide layer including LiF can be included between the display unit and the first inorganic layer. The metal halide layer prevents the display unit from being damaged when the first inorganic layer is formed according to a sputtering method or a plasma deposition method.

[0080] In this embodiment, the first organic layer is narrower than the second inorganic layer, and the second organic layer can be narrower than the third inorganic layer. Further, the first organic layer is entirely covered by the second inorganic layer, and the second organic layer can be entirely covered by the third inorganic layer.

[0081] A periphery of an organic light emitting diode (OLED) display according to an exemplary embodiment will now be described.

[0082] FIG. 4 shows a magnified top plan view of a side portion (A) in a periphery of FIG. 1, FIG. 5 shows a

cross-sectional view with respect to a line V-V of FIG. 4, FIG. 6 shows a magnified top plan view of a side portion (B) in a periphery of FIG. 1, and FIG. 7 shows cross-sectional view with respect to a line VII-VII of FIG. 6.

[0083] As shown in FIG. 4 to FIG. 7, a buffer layer 120 is formed on the substrate 100 of the organic light emitting diode (OLED) display.

[0084] For ease of description, a portion in which a contact hole for transmitting a common voltage to a second electrode of a pixel from the outside (or an external circuit) will be called a contact area (LA). The contact area (LA) is provided on a side portion A and a side portion B of the periphery (PB), shown in FIG. 1. Each contact area (LA) is provided on the side portion A and the side portion B in FIG. 4, and a plurality of contact areas (LA) can be formed thereon.

[0085] The buffer layer 120 includes an opening 22 from which a portion of the buffer layer 120 that corresponds to the contact area (LA) is removed, and a plurality of protrusions 600 are formed in the opening 22.

[0086] In this embodiment, each protrusion 600 includes a first protrusion 62 made of the same material as the buffer layer 120, and a second protrusion 64 provided on the first protrusion and made of the same material as the semiconductor. In some embodiments, the first protrusion 62 can be considered to be a first portion of each protrusion 600, and the second protrusion 62 can be considered to be a second portion 64 of each protrusion 600. The protrusion 600 may extend in a direction (e.g., a direction perpendicular to a cutting plane) to form a rib, or may be shaped as an island type protrusion.

[0087] In order to increase steps of each protrusion 600, a plurality of buffer layers 120 can be formed, for example increasing the height of the portion of the protrusion 600 made of the same material as the buffer layers 120. The height (H) of the protrusion 600 can be 300 nm (3000 Å) to 500 nm (5000 Å) in consideration of step coverage of the upper layer. In this instance, the first protrusion 62 is formed to be 300 nm (3000 Å) to 450 nm (4500 Å) thick, and the second protrusion 64 is formed to be 50 nm (500 Å) thick.

[0088] A gate insulating layer 140 is formed on the buffer layer 120 and the protrusions 600. The gate insulating layer 140 is formed along the protrusions 600 to form protrusions and depressions. In this embodiment the protrusions and depressions in the gate insulating layer 140 correspond to the shape of the protrusions 600.

[0089] A gate common voltage line 42 and a gate driving voltage line 52 are formed on the gate insulating layer 140. The gate common voltage line 42 is formed along the protrusions and depressions formed by the protrusions 600 to thus form protrusions and depressions. In this embodiment the protrusions and depressions in the gate common voltage line 42 correspond to the shape of the protrusions 600.

[0090] The gate common voltage line 42 and the gate driving voltage line 52 are formed on the same layer as the gate line, and they can be made of the same material as the gate line.

[0091] The gate common voltage line 42 and the gate driving voltage line 52 respectively receive a common voltage and a driving voltage from a flexible printed circuit (FPC) through pads 4 and 5.

[0092] A first interlayer insulating layer 160 is formed on the gate common voltage line 42 and the gate driving voltage line 52.

[0093] The first interlayer insulating layer 160 includes common voltage contact holes 83 for exposing the gate common voltage line 42 and driving voltage contact holes 85 for exposing the gate driving voltage line 52.

[0094] A data common voltage line 44 connected to the gate common voltage line 42 in the region of the common voltage contact hole 83 and a data driving voltage line 54 connected to the gate driving voltage line 52 through the driving voltage contact hole 85 are formed on the first interlayer insulating layer 160.

[0095] The data common voltage line 44 is formed along the protrusions and depressions of the gate common voltage line 42 to thus form protrusions and depressions. In this embodiment the protrusions and depressions in the data common voltage line 44 correspond to the protrusions and depressions of the gate common voltage line 42. An area that contacts the gate common voltage line 42 is increased by the protrusions and depressions, thereby reducing contact resistance.

[0096] A barrier rib 190 is formed on the data common voltage line 44 and the data driving voltage line 54

[0097] The barrier rib 190 has a common voltage opening 97 for exposing the data common voltage line 44. The common voltage opening 97 is provided in the contact area (LA).

[0098] A second electrode 730 is formed on the barrier rib 190. The second electrode 730 is connected to the data common voltage line 44 in the region of the common voltage opening 97.

[0099] The common voltage applied through the pad 4 is transmitted to the second electrode 730 through a common voltage line 400 configured by the gate common voltage line 42 and the data common voltage line 44.

[0100] A contact area of the second electrode 730 with the data common voltage line 44 is increased by the protrusions and depressions of the contact area (LA) formed by the protrusions 600, so the second electrode 730 and the data common voltage line 44 are strongly combined and contact resistance is reduced. Therefore, heat is not generated when an incised portion of the barrier rib 190 configuring the common voltage opening 97 is lifted.

[0101] The constant voltage applied through the pad 5 is transmitted to the driving voltage line through a driving voltage line 500 configured by the gate driving voltage line 52 and the data driving voltage line 54.

[0102] FIG. 8 shows a cross-sectional view of a side portion (B), shown in FIG. 1, in a periphery according to another exemplary embodiment.

[0103] An interlayer configuration is generally equivalent to that of FIG. 3 to FIG. 7 so different parts will be

described in detail.

[0104] The substrate 100 in the contact area (LA) according to the exemplary embodiment of FIG. 8 has a plurality of recess portions (U). The recess portions (U) are provided between the protrusions 600, and the recess portions (U) increase the step height of the protrusions (600).

[0105] In some embodiments, when the step caused by the protrusions 600 (e.g. formed by using the buffer layer and the semiconductor) is sufficient, the recess portion (U) may not be formed in the substrate 100.

[0106] As discussed above, embodiments of the present invention provide an organic light emitting diode display, comprising: a pixel unit formed on a substrate and including an organic light emitting diode for displaying an image; and a periphery region surrounding the pixel unit, the periphery region comprising: a gate common voltage line formed on the substrate, the gate common voltage line arranged to receive a common voltage from an external circuit, an interlayer insulating layer arranged to cover part of the gate common voltage line and including a common voltage contact hole for exposing a part of the gate common voltage line, a data common voltage line formed on the interlayer insulating layer and contacting the gate common voltage line in the region of the common voltage contact hole, a barrier rib arranged to cover part of the data common voltage line and including a common voltage opening for exposing a part of the data common voltage line, a common electrode formed on the barrier rib and contacting the data common voltage line in the region of the common voltage opening, and a plurality of protrusions provided in the region of the common voltage contact hole and formed on the substrate.

[0107] In such arrangements, in the region of the common voltage contact hole, the gate common voltage line and the data common voltage line contact each other. Furthermore, in the region of the common voltage contact hole, the gate common voltage line and the data common voltage line are both formed over the plurality of protrusions. Thus, the common voltage line and the data common voltage line are formed with a series of protrusions and depressions corresponding to the shape of the plurality of protrusions.

[0108] In some embodiments, the substrate includes a plurality of recess portions respectively provided between neighboring protrusions in the region of the common voltage contact hole. Thus, the plurality of recess portions can increase the effective height of the protrusions.

[0109] In some embodiments, the pixel unit includes a thin film transistor for connecting the second electrode to a drain electrode. In some such embodiments, each protrusion comprises a material that includes a material of a semiconductor of the thin film transistor. For example, the each protrusion can be made out of the semiconductor material used in the thin film transistor. In such arrangements, each protrusion can be deposited at the same time as the semiconductor material.

[0110] In some embodiments, the organic light emitting diode display can comprise a buffer layer formed on the substrate. In some such embodiments, each protrusion can be made of the same material as the buffer layer.

[0111] In some embodiments, each protrusion can include a first portion made of the same material as the buffer layer, and a second portion provided on the first portion and made of the same material as the semiconductor.

[0112] In some embodiments, each protrusion is provided in the form of a rib on the substrate. In other embodiments, the protrusions can take different forms.

[0113] While this disclosure has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

Claims

1. An organic light emitting diode display, comprising:

a pixel unit formed on a substrate and including an organic light emitting diode for displaying an image; and

a periphery region surrounding the pixel unit, the periphery region comprising:

a gate common voltage line formed on the substrate, the gate common voltage line arranged to receive a common voltage from an external circuit,

an interlayer insulating layer arranged to cover part of the gate common voltage line and including a common voltage contact hole for exposing a part of the gate common voltage line,

a data common voltage line formed on the interlayer insulating layer and contacting the gate common voltage line in the region of the common voltage contact hole,

a barrier rib arranged to cover part of the data common voltage line and including a common voltage opening for exposing a part of the data common voltage line,

a common electrode formed on the barrier rib and contacting the data common voltage line in the region of the common voltage opening, and

a plurality of protrusions provided in the region of the common voltage contact hole and formed on the substrate.

2. The organic light emitting diode display of claim 1, wherein in the region of the common voltage contact

hole, the gate common voltage line and the data common voltage line are both formed over the plurality of protrusions, wherein the common voltage line and the data common voltage line respectively comprise a series of protrusions and depressions corresponding to the plurality of protrusions.

3. The organic light emitting diode display of claim 1 or 2, wherein the organic light emitting diode comprises:

a first electrode, an organic emission layer provided on the first electrode, and a second electrode provided on the organic emission layer, and
the common electrode is integrally formed with the second electrode.

4. The organic light emitting diode display of claim 3, wherein the second electrode is formed on the pixel unit.

5. The organic light emitting diode display of claim 3 or 4, wherein the pixel unit includes a thin film transistor for connecting the first electrode to a drain electrode of the thin film transistor.

6. The organic light emitting diode display of claim 5, wherein each protrusion comprises a material that includes a material of a semiconductor of the thin film transistor.

7. The organic light emitting diode display of any one of claims 1 to 6, further comprising a buffer layer formed on the substrate, the protrusion being made of the same material as the buffer layer.

8. The organic light emitting diode display of claim 7 when dependent on claim 6, wherein each protrusion includes a first portion made of the same material as the buffer layer, and a second portion provided on the first portion and made of the same material as the semiconductor.

9. The organic light emitting diode display of claim 7 or 8, wherein the buffer layer includes at least one of silicon nitride and silicon oxide.

10. The organic light emitting diode display of any one of claims 1 to 9, wherein the substrate includes a plurality of recess portions respectively provided between neighboring protrusions.

11. The organic light emitting diode display of any one of claims 1 to 10, wherein the pixel unit includes:

a gate line formed on the substrate, the gate line arranged to transmit a scan signal;
a data line and a driving voltage line crossing the gate line in an insulated manner, the data line arranged to transmitting a data signal and a driving voltage, respectively;
a switching thin film transistor connected to the gate line and the data line;
a driving thin film transistor connected to the switching thin film transistor and the driving voltage line;
a first electrode connected to the driving thin film transistor;
an organic emission layer formed on the first electrode; and
a second electrode formed on the organic light emitting diode, wherein the gate common voltage line is formed on the same layer as the gate line, and the data common voltage line is formed on the same layer as the data line.

FIG. 1

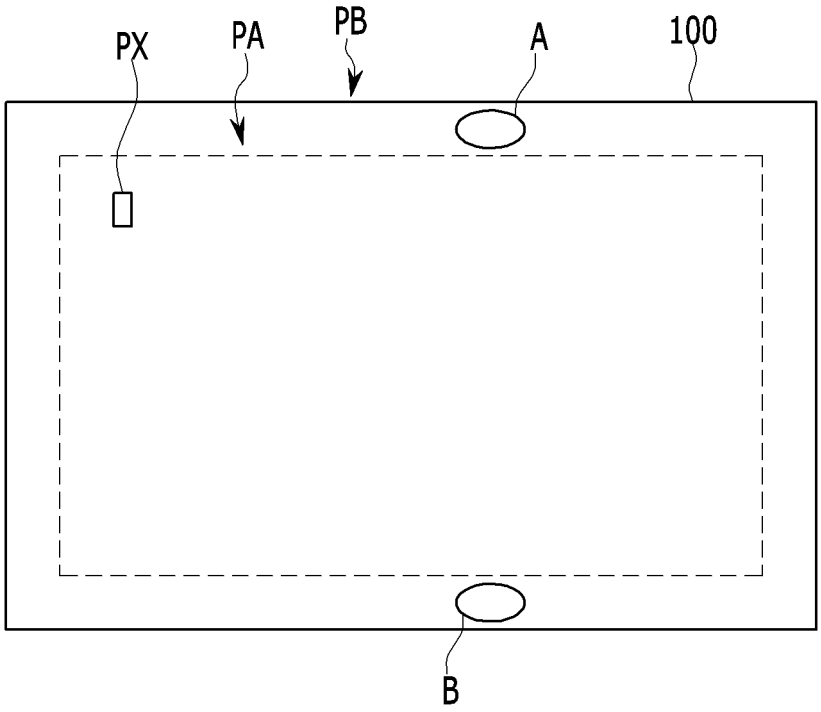


FIG. 2

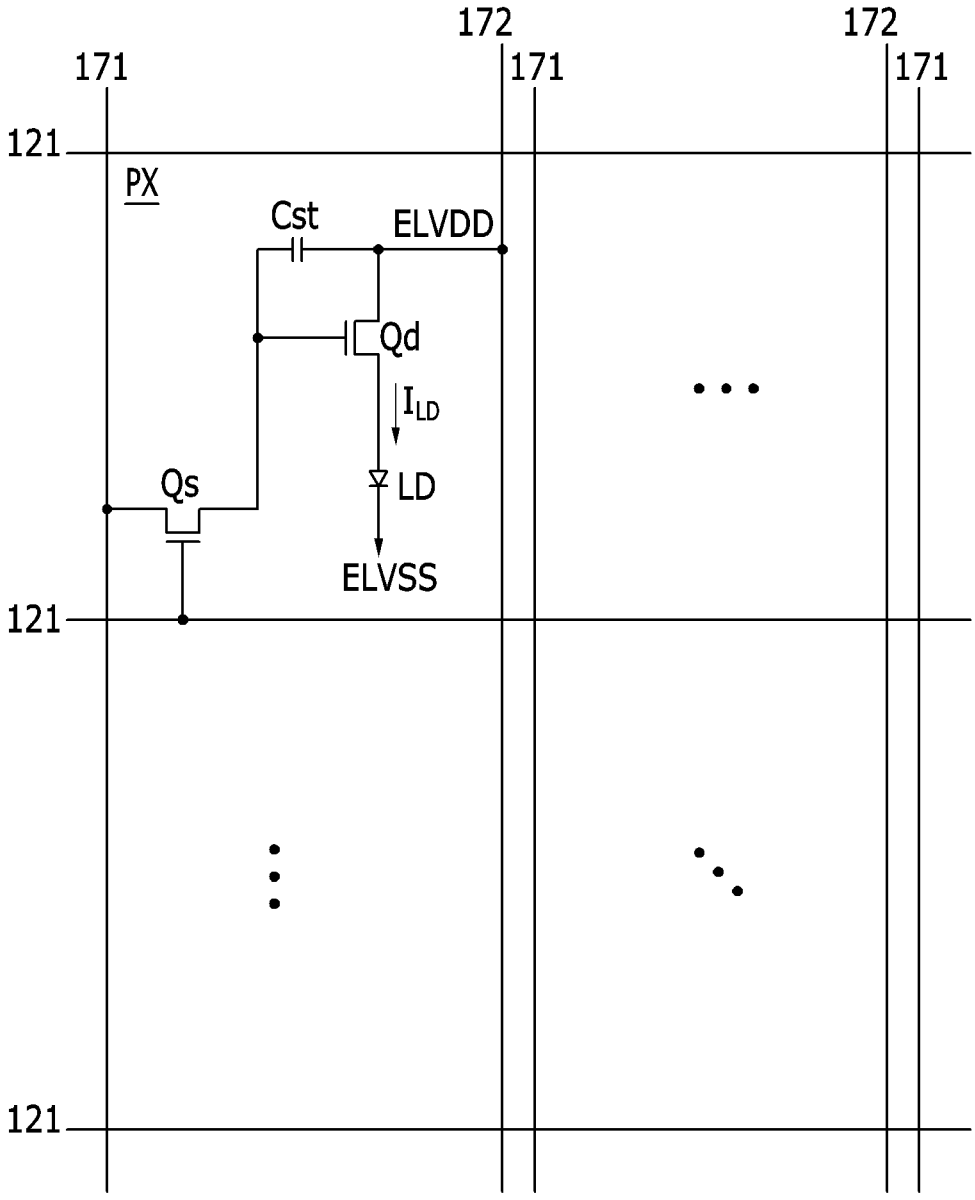


FIG. 3

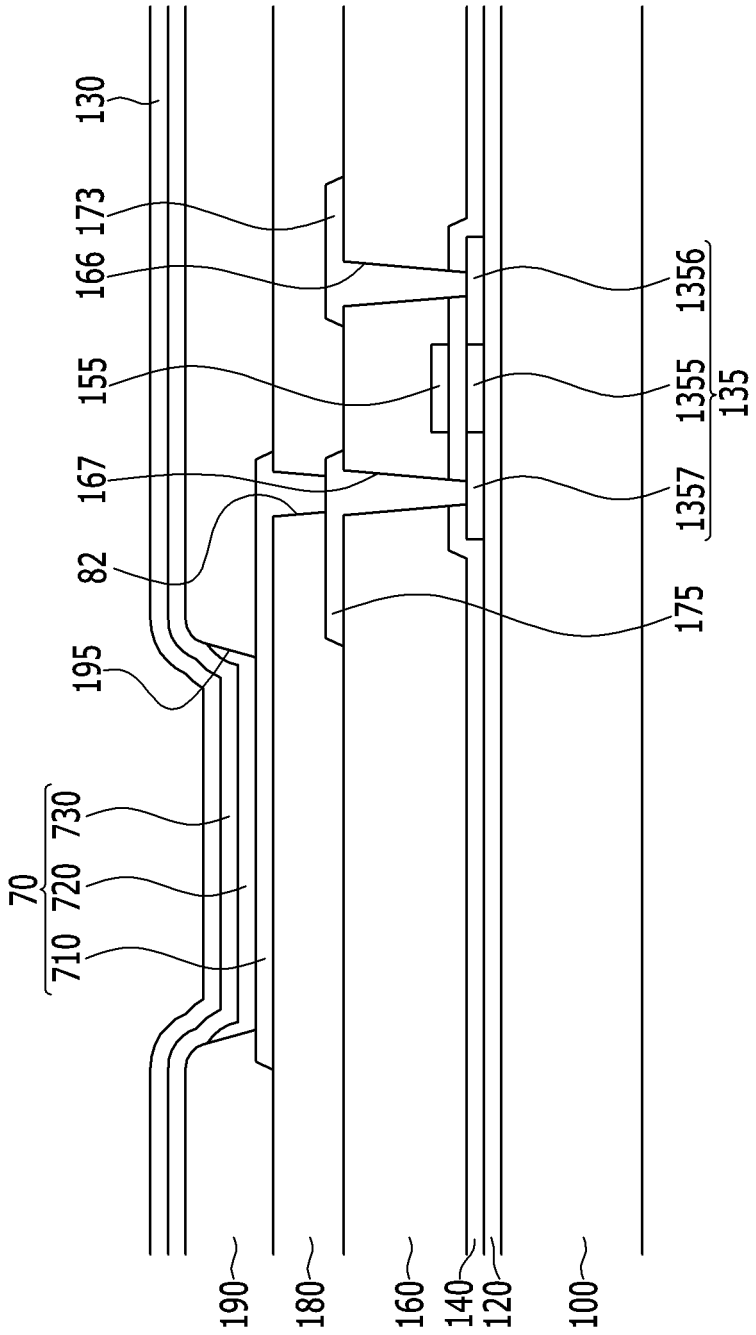

130
173
166
155
167
82
195
730
720
710
70
1356
1355
1357
135
175
190
180
160
140
120
100

FIG. 4

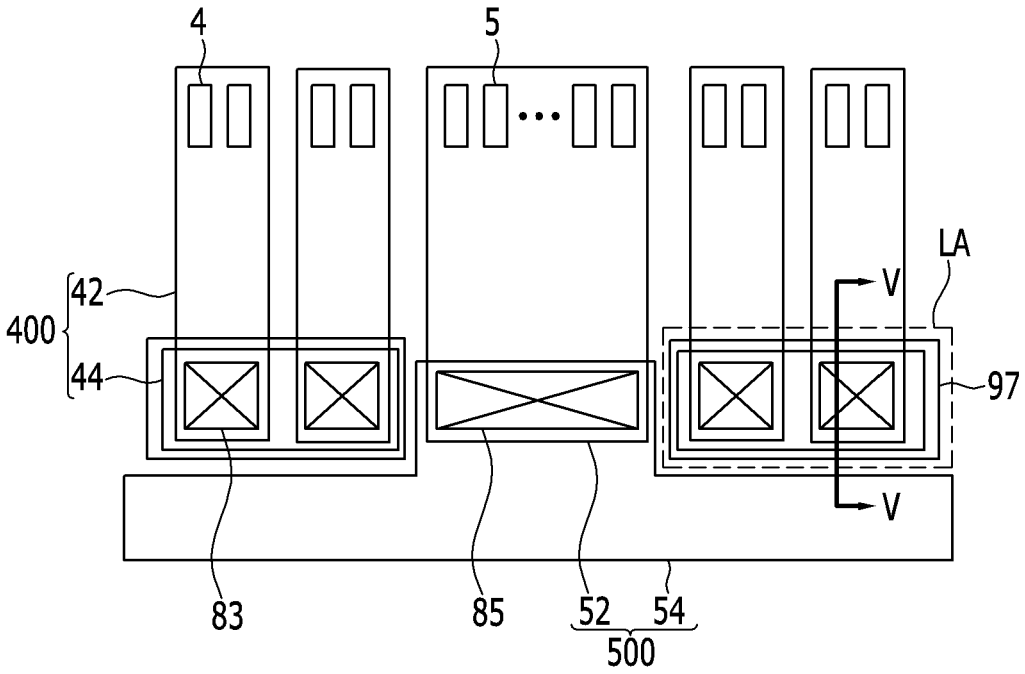


FIG. 5

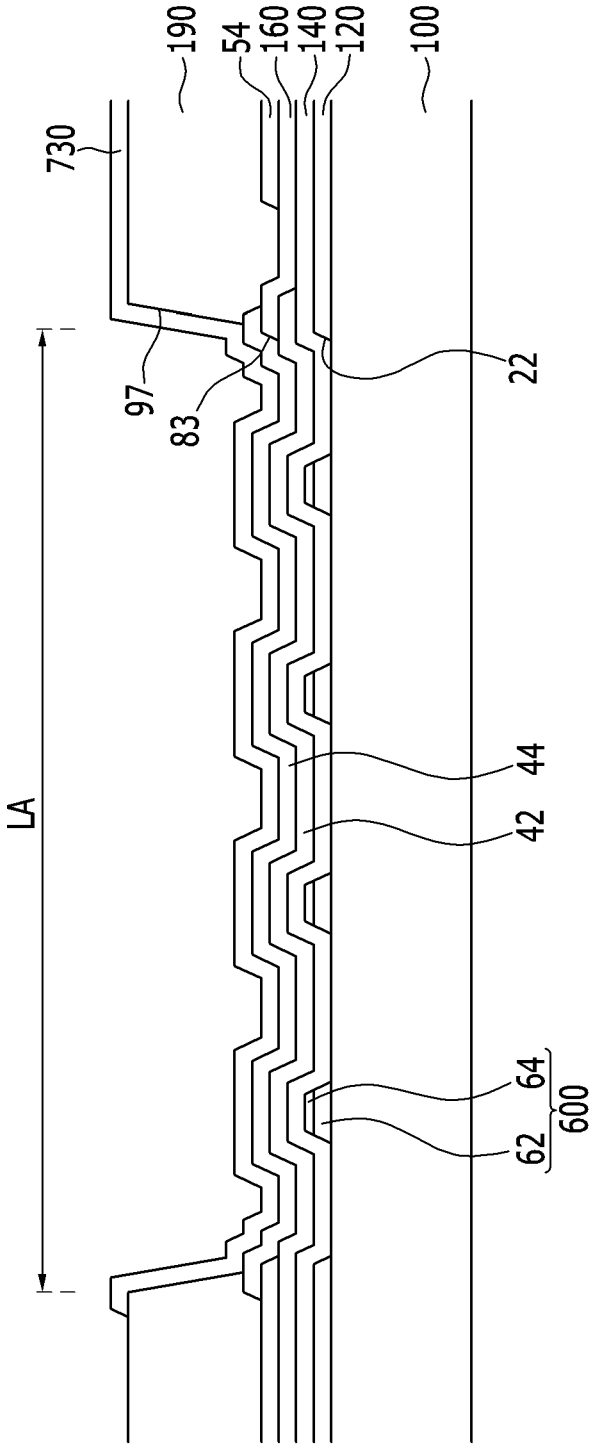


FIG. 6

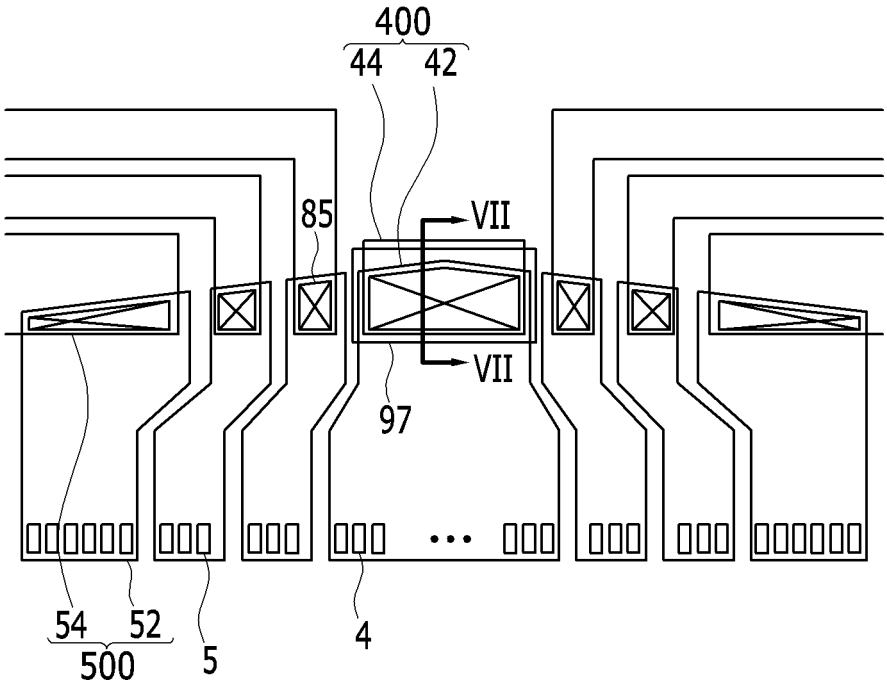


FIG. 7

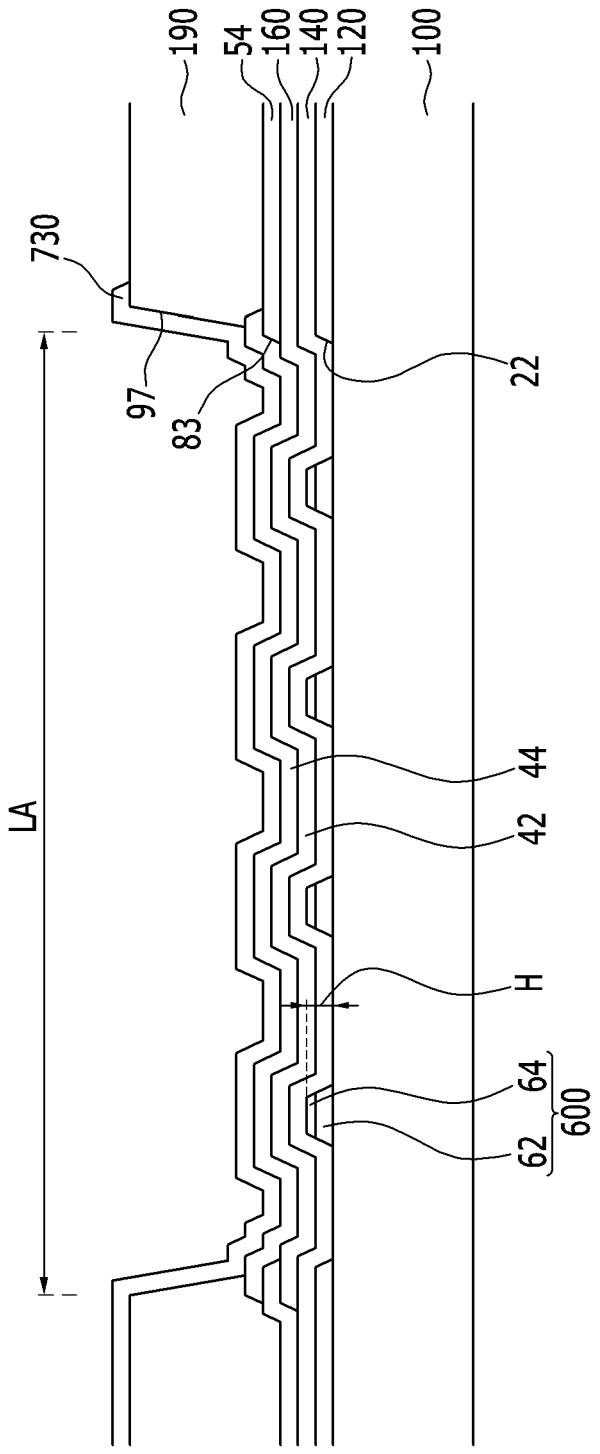
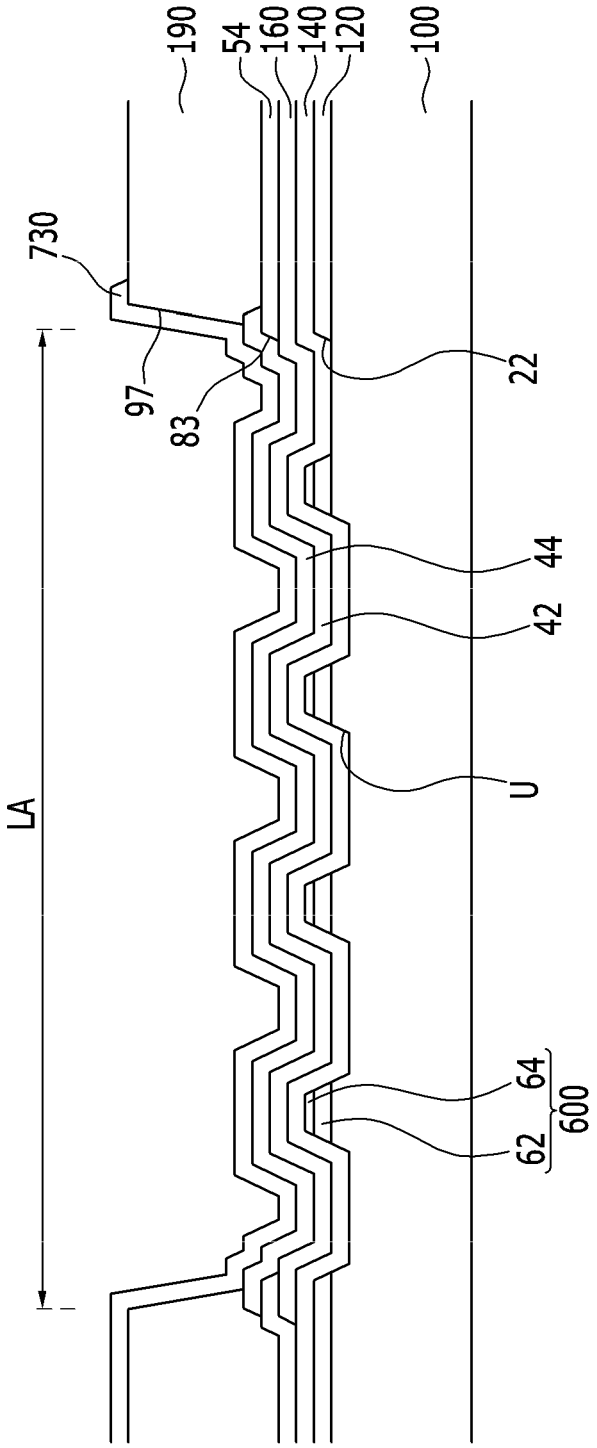


FIG. 8



专利名称(译)	有机发光二极管显示器		
公开(公告)号	EP2747062A2	公开(公告)日	2014-06-25
申请号	EP2013194955	申请日	2013-11-28
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
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发明人	PARK, KYUNG HOON PARK, JONG HYUN HEO, SEONG KWEON		
IPC分类号	G09G3/00 H01L27/00		
优先权	1020120137356 2012-11-29 KR		
其他公开文献	EP2747062A3		
外部链接	Espacenet		

摘要(译)

公开了一种有机发光二极管显示器，包括：像素单元，包括用于显示图像的有机发光二极管;以及围绕像素单元的周边。外围包括形成在基板上并从外部电路接收公共电压的栅极公共电压线，覆盖栅极公共电压线并包括用于暴露栅极公共电压线的一部分的公共电压接触孔的层间绝缘层，数据公共电压线形成在层间绝缘层上并通过公共电压接触孔接触栅极公共电压线，以及多个突起设置在公共电压接触孔中并形成在基板上。

FIG. 1