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(54) **Organic light emitting display device and driving method thereof**

Organische lichtemittierende Anzeigevorrichtung und Verfahren zu ihrer Ansteuerung

Dispositif d'affichage électroluminescent organique et son procédé de commande

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Description

BACKGROUND

1. Field

[0001] An aspect of the present invention relates to an organic light emitting display device and a driving method thereof, and more particularly, to an organic light emitting display device and a driving method thereof, which can improve image quality.

2. Description of the Related Art

[0002] Recently, there have been developed various types of flat panel display devices capable of reducing the disadvantageous weight and volume typical of cathode ray tubes. The flat panel display devices include a liquid crystal display, a field emission display, a plasma display panel, an organic light emitting display device, and the like.

[0003] Among these flat panel display devices, the organic light emitting display device displays images using organic light emitting diodes that emit light through recombination of electrons and holes. The organic light emitting display device has a fast response speed and is driven with low power consumption. In a conventional organic light emitting display device, current corresponding to a data signal is supplied to an organic light emitting diode, using a transistor formed in each pixel, so that the organic light emitting diode emits light.

[0004] EP 1 347 436 A2 is directed to the problem of poor images due to charge redistribution of the capacitors caused by previous data voltage stored in the parasitic capacitors. The problem is solved by precharge voltage supplied into the data lines.

[0005] US 2006/0151745 A1 discloses a display including a demultiplexer and an initialization section as well. Initializing switches coupled to initialization voltage are included in the initialization section.

SUMMARY

[0006] Embodiments are directed to an organic light emitting display device according to claim 1.

[0007] The first initialization power source may be set to a voltage lower than that of the data signals.

[0008] The first switches may be progressively turned on, corresponding to control signals.

[0009] The control signal supplied to the first switch coupled to the first data line may overlap with a scan signal during a partial period.

[0010] A control signal supplied to a first switch coupled to the second set of data lines may completely overlap with the scan signal.

[0011] The second set of data lines may have only one data line.

[0012] The device may further include pixels, and pixels positioned on a j-th (j is a natural number) horizontal line may each include an organic light emitting diode, a first transistor controlling an amount of current supplied to the organic light emitting diode, a second transistor coupled between a first electrode of the first transistor and a data line, the second transistor being turned on when a scan signal is supplied to a j-th scan line, a third transistor coupled between a second electrode and a gate electrode of the first transistor, the third transistor being turned on when the scan signal is supplied to the j-th scan line, a storage capacitor coupled between the gate electrode of the first transistor and a first power source, and a sixth transistor coupled between the gate electrode of the first transistor and a second initialization power source, the sixth transistor being turned on when a scan signal is supplied to a (j-1)-th scan line.

[0013] The second initialization power source may be set to a voltage lower than that of the data signals.

[0014] The second initialization power source may be set to a voltage identical to that of the first initialization power source.

[0015] Each pixel may further include a boosting capacitor coupled between the j-th scan line and the gate electrode of the first transistor.

[0016] The device may further include emission control lines formed for each horizontal line, and the scan driver may supply an emission control signal to a j-th emission control line so that the emission control signal overlaps with the scan signal supplied to the (j-1)-th and j-th scan lines.

[0017] Each pixel may further include a fourth transistor coupled between the first electrode of the first transistor and the first power source, the fourth transistor being turned off when the emission control signal is supplied to the j-th emission control line and otherwise turned on, and a fifth transistor coupled between the second electrode of the first transistor and the organic light emitting diode, the fifth transistor being turned off when the emission control signal is supplied to the j-th emission control line and otherwise turned on.

[0018] Embodiments are also directed to a driving method of an organic light emitting display device according to claim 10. The initialization power source may be set to a voltage lower than that of the data signals.

[0019] The initialization power source may be supplied only during the first period.

[0020] The period when the first data signal is supplied to the specific data line is longer than that when the data signal is supplied to each of the other data lines.

[0021] The scan signal is supplied after the first data signal is supplied to the specific data line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] Features will become apparent to those of skill in the art by describing in detail exemplary embodiments with reference to the attached drawings in which:

FIG. 1 is a block diagram illustrating an organic light emitting display device according to an embodiment.
FIG. 2 is a circuit diagram illustrating a demultiplexer according to an embodiment.
FIG. 3 is a circuit diagram illustrating a pixel according to an embodiment.
FIG. 4 is a circuit diagram illustrating a pixel according to another embodiment.
FIG. 5 is a circuit diagram illustrating an embodiment of the coupling structure between a demultiplexer and a pixel.
FIG. 6 is a waveform diagram illustrating a driving method of the demultiplexer and the pixel, shown in FIG. 5.
FIG. 7 is a circuit diagram illustrating a demultiplexer according to another embodiment.

DETAILED DESCRIPTION

[0023] In the drawing figures, dimensions may be exaggerated for clarity of illustration. It will be understood that when an element is referred to as being "between" two elements, it can be the only element between the two elements, or one or more intervening elements may also be present. Like reference numerals refer to like elements throughout.

[0024] FIG. 1 is a block diagram illustrating an organic light emitting display device according to an embodiment.

[0025] Referring to FIG. 1, the organic light emitting display device according to this embodiment includes a scan driver 110, a data driver 120, a pixel unit 130, a timing controller 150, a demultiplexer unit 160, and a demultiplexer controller 170.

[0026] The pixel unit 130 has pixels 140 positioned at intersection portions of scan lines S1 to Sn and data lines D1 to Dm. Each pixel 140 receives a first power source ELVDD and a second power source ELVSS, supplied from the outside of the pixel unit 130. The pixels 140 receive a data signal while being selected for each horizontal line, corresponding to a scan signal supplied to the scan lines S1 to Sn. Each pixel 140 receiving the data signal generates light with a predetermined luminance while controlling the amount of current flowing from the first power source ELVDD to the second power source ELVSS via an organic light emitting diode (not shown).

[0027] The scan driver 110 generates a scan signal under the control of the timing controller 150, and supplies the generated scan signal to the scan lines S1 to Sn. For example, the scan driver 110 progressively supplies a scan signal to the scan lines S1 to Sn. The scan driver 110 generates an emission control signal under the control of the timing controller 150, and progressively supplies the generated emission control signal to emission control lines E1 to En. Here, the emission control signal supplied to a j-th (j is a natural number) emission control line Ej overlaps with the scan signal supplied to a (j-1)-th scan line Sj-1 and a j-th scan line Sj.

[0028] The data driver 120 progressively supplies a plurality of data signals to output lines O1 to Om/i (m and i may each be a natural number of 2 or more). For example, the data driver 120 progressively supplies i data signals to output lines O1 to Om/i for each horizontal period. Here, data driver 120 supplies the i data signals to overlap with the scan signal.

[0029] The demultiplexer unit 160 includes a plurality of demultiplexers 162 coupled to the respective output lines O1 to Om/i. Each demultiplexer 162 is coupled to i data lines D. The demultiplexer 162 provides, to the i data lines D, i data signals supplied from the output line O for each horizontal period.

[0030] The demultiplexer controller 170 may progressively supply i control signals to each demultiplexer 162. In an example embodiment, the demultiplexer controller 170 supplies the i control signals to each demultiplexer 162 so that the data signal is time-divisionally supplied in the demultiplexer 162. Meanwhile, although the demultiplexer controller 170 has been illustrated as a separate driver in FIG. 1, embodiments are not limited thereto. For example, the timing controller 150 may progressively supply the i control signals to the demultiplexer unit 160.

[0031] The timing controller 150 controls the scan driver 110, a data driver 120, and the demultiplexer controller 170, corresponding to synchronization signals supplied from the outside thereof.

[0032] FIG. 2 is a circuit diagram illustrating a demultiplexer according to an embodiment. For convenience of illustration, a demultiplexer 162 coupled to a first output line O1 is shown in FIG. 2. The demultiplexer 162 is shown as being coupled to three data lines for convenience of explanation.

[0033] Referring to FIG. 2, the demultiplexer 162 includes first switches SW1 respectively coupled between the output line O1 and a first set of data lines D1 to D3, and second switches SW2 respectively coupled between a first initialization power source Vint1 and a second set of data lines, e.g., data lines D2 and D3.

[0034] The first switches SW1 are respectively coupled between the output line O1 and each data line D1 to D3. The first switch SW1 is turned on, corresponding to any one of a first control signal CS1, a second control signal CS2, and a third control signal Cs3. Here, the first, second and third control signals CS1, CS2, and CS3 are progressively supplied so as not to overlap with one another for each horizontal period.

[0035] The second switches SW2 are respectively coupled between the first initialization power source Vint1 and some data lines D2 and D3, e.g., the other data lines D2 and D3 except the data line D1 receiving a first data signal. The second switch SW2 is turned on when the same control signal as that supplied to the first switch SW1 (which is coupled to the data line D1 receiving the first data signal, i.e., the first control signal) is supplied to the second switch SW2. Meanwhile, the first initialization power source Vint1 is used to initialize the voltage of a previous data signal stored in some data lines D2

and D3. To this end, the first initialization power source Vint1 is set to a voltage lower than that of the data signal.

[0036] FIG. 3 is a circuit diagram illustrating a pixel according to an embodiment. A pixel coupled to an n-th scan line Sn and an m-th data line Dm will be shown in FIG. 3.

[0037] Referring to FIG. 3, the pixel 140 according to this embodiment includes an organic light emitting diode OLED, and a pixel unit 142 controlling the amount of current supplied to the organic light emitting diode OLED.

[0038] An anode electrode of the organic light emitting diode OLED is coupled to the pixel circuit 142, and a cathode electrode of the organic light emitting diode OLED is coupled to a second power source ELVSS. The organic light emitting diode OLED generates light with a predetermined luminance, corresponding to the amount of current supplied from the pixel circuit 142.

[0039] The pixel circuit 142 stores a voltage corresponding to a data signal and the threshold voltage of a driving transistor M1, and controls the amount of current supplied to the organic light emitting diode OLED, corresponding to the stored voltage. In the present embodiment, the pixel circuit 142 may be a suitable circuit that compensates for the threshold voltage of the driving transistor M1. For example, the pixel circuit 142 may include first to sixth transistors M1 to M6 and a storage capacitor Cst.

[0040] A first electrode of the first transistor (driving transistor) M1 is coupled to a first node N1, and a second electrode of the first transistor M1 is coupled to a first electrode of the fifth transistor M5. A gate electrode of the first transistor M1 is coupled to a second node N2. The first transistor M1 controls the amount of the current supplied to the organic light emitting diode OLED, corresponding to the voltage stored in the storage capacitor Cst.

[0041] A first electrode of the second transistor M2 is coupled to the data line Dm, and a second electrode of the second transistor M2 is coupled to the first node N1. A gate electrode of the second transistor M2 is coupled to the n-th scan line Sn. When a scan signal is supplied to the n-th scan line Sn, the second transistor M2 is turned on to supply a data signal from the data line Dm to the first node N1.

[0042] A first electrode of the third transistor M3 is coupled to the second electrode of the first transistor M1, and a second electrode of the third transistor M3 is coupled to the second node N2. A gate electrode of the third transistor M3 is coupled to the n-th scan line Sn. When the scan signal is supplied to the n-th scan line Sn, the third transistor M3 is turned on to allow the first transistor M1 to be diode-coupled.

[0043] A first electrode of the fourth transistor M4 is coupled to a first power source ELVDD, and a second electrode of the fourth transistor M4 is coupled to the first node N1. A gate electrode of the fourth transistor M4 is coupled to an emission control line En. When an emission control signal is supplied to the emission control line En, the fourth transistor M4 is turned off, and otherwise, the fourth transistor M4 is turned on.

[0044] The first electrode of the fifth transistor M5 is coupled to the second electrode of the first transistor M1, and a second electrode of the fifth transistor M5 is coupled to the anode electrode of the organic light emitting diode OLED. A gate electrode of the fifth transistor M5 is coupled to the emission control line En. When the emission control signal is supplied to the emission control line En, the fifth transistor M5 is turned off, and otherwise, the fifth transistor M5 is turned on.

[0045] A first electrode of the sixth transistor M6 is coupled to the second node N2, and a second electrode of the sixth transistor M6 is coupled to a second initialization power source Vint2. A gate electrode of the sixth transistor M6 is coupled to an (n-1)-th scan line Sn-1. When the scan signal is supplied to the (n-1)-th scan line Sn-1, the sixth transistor M6 is turned on to supply the voltage of the second initialization power source Vint2 to the second node N2. Here, the voltage of the second initialization power source Vint2 may be set to a voltage lower than that of the data signal, e.g., the same voltage as that of the first initialization power source Vint1.

[0046] The storage capacitor Cst is coupled between the first power source ELVDD and the second node N2. The storage capacitor Cst stores a voltage corresponding to the data signal and the threshold voltage of the first transistor M1.

[0047] In an implementation, as shown in FIG. 4, the pixel circuit 142 may further include a boosting capacitor Cb coupled between the n-th scan line Sn and the second node N2. The boosting capacitor Cb controls the voltage at the second node N2, corresponding to the scan signal supplied to the n-th scan line Sn.

[0048] FIG. 5 is a circuit diagram illustrating an embodiment of the coupling structure between a demultiplexer and a pixel. For convenience of illustration, it is assumed that red (R), green (G), and blue (B) pixels are coupled to the demultiplexer in FIG. 5. FIG. 6 is a waveform diagram illustrating a driving method of the demultiplexer and the pixel, shown in FIG. 5.

[0049] Referring to FIGS. 5 and 6, an emission control signal is first supplied to the emission control line En. If the emission control signal is supplied to the emission control line En, the fourth and fifth transistors M4 and M5 included in each of the pixels 142R, 142G, and 142B are turned off. If the fourth transistor M4 is turned off, the first power source ELVDD and the first node N1 are electrically cut off. If the fifth transistor M5 is turned off, the organic light emitting diode OLED and the first transistor M1 are electrically cut off. Thus, the pixels 142R, 142G, and 142B are set to be in a non-emission state during the period in which the emission control signal is supplied to the emission control line En.

[0050] Subsequently, a scan signal is supplied to the (n-1)-th scan line Sn-1. If the scan signal is supplied to the (n-1)-th scan line Sn-1, the sixth transistor M6 included in each of the pixels 142R, 142G, and 142B is turned

on. If the sixth transistor M6 is turned on, the voltage of the second initialization power source Vint2 is supplied to the second node N2. That is, the second node N2 of each of the pixels 142R, 142G and 142B positioned on an n-th horizontal line is initialized to the voltage of the second initialization power source Vint2 during the period in which the scan signal is supplied to the (n-1)-th scan line Sn-1.

[0051] Subsequently, the first control signal CS1 is supplied during a next horizontal period so that the first switch SW1 coupled to the first data line D1 is turned on. If the first switch SW1 is turned on, the output line O1 and the first data line D1 are electrically coupled to each other. In this case, a data signal corresponding to a current horizontal period is supplied to the first data line D1.

[0052] If the first control signal CS1 is supplied, the second switches SW2 coupled to the second and third data lines D2 and D3 are turned on. If the second switch SW2 is turned on, the voltage of the first initialization power source Vint1 is supplied to the second and third data lines D2 and D3. That is, when the first control signal CS1 is supplied, the second and third data lines D2 and D3 are initialized to the voltage of the first initialization power source Vint1, regardless of the data signal supplied during a previous horizontal period.

[0053] That is, in the present embodiment, when the scan signal is supplied to the (n-1)-th scan line Sn-1, the second node N2 of each of the pixels 142R, 142G, and 142B is initialized to the voltage of the second initialization power source Vint2. Before the scan signal is supplied to the (n-1)-th scan line Sn-1, the data signal corresponding to the current horizontal period is supplied to the first data line D1, and the voltage of the first initialization power source Vint1 is supplied to the second and third data lines D2 and D3. To this end, the first control signal CS1 is set to have a width wider than that of each of the second and third control signals CS2 and CS3 (W1 > W2).

[0054] After the first control signal CS1 is supplied, the scan signal is supplied to the n-th scan line Sn so as to overlap with the first control signal CS1. Thus, the second and third transistors M2 and M3 included in each of the pixels 142R, 142G, and 142B are turned on. If the second and third transistors M2 and M3 included in the pixel 142R are turned on, the data signal supplied to the first data line D1 is supplied to the second node N2 via the diode-coupled first transistor M1. In this case, the storage capacitor Cst included in the pixel 142R charges the data signal and a voltage corresponding to the threshold voltage of the first transistor M1. Meanwhile, since the second and third data lines D2 and D3 are initialized to the voltage of the first initialization power source Vint1, the diode-coupled first transistor M1 included in each of the pixels 142G and 142B is set to be in a turn-off state.

[0055] After a voltage corresponding to the data signal is charged in the pixel 142R, the second control signal CS2 is supplied to the pixel 142R so that the first switch SW1 coupled to the second data line D2 is turned on. If the first switch SW1 is turned on, the data signal from the output line O1 is supplied to the second data line D2. If the data signal is supplied to the second data line D2, the diode-coupled first transistor M1 included in the pixel 142G is turned on. Then, the storage capacitor Cst included in the pixel 142G charges the data signal and the voltage corresponding to the threshold voltage of the first transistor M1.

[0056] After a voltage corresponding to the data signal is charged in the pixel 142G, the third control signal CS3 is supplied to the pixel 142G so that the first switch SW1 coupled to the third data line D3 is turned on. If the first switch SW1 is turned on, the data signal from the output line O1 is supplied to the third data line D3. If the data signal is supplied to the third data line D3, the diode-coupled first transistor M1 included in the pixel 142B is turned on. Then, the storage capacitor Cst included in the pixel 142B charges the data signal and the voltage corresponding to the threshold voltage of the first transistor M1.

[0057] Subsequently, the supply of the emission control signal to the emission control line En is stopped so that the fourth and fifth transistors M4 and M5 included in each of the pixels 142R, 142G, and 142B are turned on. Then, the first transistor M1 included in each of the pixels 142R, 142G, and 142B generates light with a predetermined luminance while controlling the amount of current supplied to the organic light emitting diode OLED, corresponding to the voltage charged in the storage capacitor Cst.

[0058] As described above, in the present embodiment, the scan signal supplied to the scan lines S1 to Sn can overlap with the control signals CS1 to CS3 for controlling the demultiplexer 162. In this case, the data supply time may be maximally secured, and accordingly, it may be possible to improve image quality and implement high resolution. In the present embodiment, the data signal supplied from the output line O1 is not stored in a separate capacitor (e.g., a parasitic capacitor) and then supplied, but directly supplied to the pixel 142. If the data signal from the output line O1 is directly supplied to the pixel 142 as described above, it may be possible to minimize the time required to charge the data signal.

[0059] FIG. 7 is a circuit diagram illustrating a demultiplexer according to another embodiment. FIG. 7 illustrates a case where the demultiplexer 162 is coupled to two data lines.

[0060] Referring to FIG. 7, the demultiplexer 162 according to this embodiment includes first switches SW1 respectively coupled between the output line O1 and the data lines D1 and D2, and a second switch SW2 coupled between the first initialization power source Vint1 and the second data line D2.

[0061] The first switches SW1 are respectively coupled between the output line O1 and the data lines D1 and D2. The first switches SW1 are progressively turned on, corresponding to the control signals CS1 and CS2. Here, the first switch SW1 coupled to the first data line D1 is

turned on, corresponding to the first control signal CS1, and the first switch SW1 coupled to the second data line D2 is turned on, corresponding to the second control signal CS2 supplied after the first control signal is supplied.

[0062] The second switch SW2 is coupled to the demultiplexer 162 so as to be coupled the first initialization power source Vint1 and the other data line D2 except the data line D1 to which the data signal is initially supplied. When the first control signal CS1 is supplied, the second switch SW2 is turned on to supply the voltage of the first initialization power source Vint1 to the second data line D2. The subsequent operation procedure is identical to that in FIG. 5, and therefore, its detailed description will be omitted.

[0063] By way of summation and review, a conventional organic light emitting display device may include a data driver supplying a data signal to data lines, a scan driver progressively supplying a scan signal to scan lines, and a pixel unit having a plurality of pixels coupled to the scan lines and the data lines.

[0064] When a scan signal is supplied from the scan line, the pixel receives a data signal supplied from the data line, and emits light with a predetermined luminance while supplying current corresponding to the data signal to the organic light emitting diode, using a driving transistor. The threshold voltage of the driving transistor may be compensated by allowing the driving transistor to be diode-coupled in order to display a uniform image.

[0065] Meanwhile, a structure in which a demultiplexer is added to be coupled to each output line of the data driver may be considered in order to reduce manufacturing cost. The demultiplexer time-divisionally supplies, to a plurality of data lines, a plurality of data signals supplied to the respective output lines. However, in a case where the demultiplexer is added, one horizontal period may be divided into a data supply period (or a demultiplexer control signal supply period) and a scan signal supply period due to characteristics of the diode-coupled driving transistor.

[0066] More specifically, the gate electrode of a driving transistor in each pixel positioned on the current horizontal line may first be initialized to a predetermined voltage by a data signal supplied to the previous horizontal line. Subsequently, the demultiplexer progressively supplies a plurality of data signals to the plurality of data lines during the data supply period. A scan signal is supplied to the scan line during the scan signal supply period after the data supply period so that the data signal supplied to the data line is input to the pixels positioned on the horizontal lines. In a conventional organic light emitting display device, when the scan signal and the data signal overlap with each other, a desired data signal may not be supplied to the pixel. In other words, the data signal previously charged in the previous period is supplied to the pixel during the period in which the scan signal is supplied.

[0067] Meanwhile, if the horizontal period is divided into the data supply period and the scan signal supply period, the period in which the data signal is supplied to each pixel is decreased. Accordingly, the threshold voltage of the driving transistor may not be compensated, and therefore, the display quality may be deteriorated. Particularly, in a case where the horizontal period is divided in the conventional organic light emitting display device, the period in which the data signal is supplied may decrease, and therefore, it may be difficult to implement a high-resolution panel.

[0068] As described above, embodiments may provide an organic light emitting display device and a driving method thereof that can improve image quality. In the organic light emitting display device and the driving method thereof according to embodiments, the voltage of an initialization power source is supplied to other data lines coupled to a demultiplexer during the period in which a first data signal is supplied to a specific data line in the demultiplexer. That is, the other data lines are initialized from the voltage of a previous data signal to the voltage of the initialization power source during the period in which the first data signal is supplied to the specific data line.

[0069] If the other data lines are initialized to the voltage of the initialization power source, data signals and a scan signal may be supplied while overlapping with each other during a horizontal period, and accordingly, it may be possible to enhance display quality. According to embodiments, the data signals and the scan signal may overlap with each other, thereby enabling high resolution.

[0070] It is clear for a person skilled in the art that the disclosed embodiments can also be combined where possible.

Claims

1. An organic light emitting display device, comprising:

a plurality of scan lines (S1 to Sn) and a plurality of data lines (D1 to Dm);
a scan driver (110) progressively supplying scan signals to the scan lines (S1 to Sn);
a data driver (120) having a plurality of output lines (O1 to Om/i) and supplying data signals to the output lines (O1 to Om/i) of the data driver (120) during a period in which the scan signals are supplied; and
a demultiplexer unit (160) including a plurality of demultiplexers (162), each demultiplexer (162) being coupled to a respective one of the output lines (O1 to Om/i) of the data driver (120), and supplying the data signals to a respective set of i data lines (D1 to Di), wherein i is a natural number ≥ 2, each demultiplexer (162) including:

i first switches (SW1), each first switch (SW1) being coupled between said output line (O1 to Om/i) of the data driver (120) and

a corresponding data line among said set of data lines (D1 to Di), and
[i-1] second switches (SW2), each second switch (SW2) being coupled between a first initialization power source providing a first initialization voltage (Vint1) and a data line (D2 to Di) except a first data line (D1) among said set of data lines (D1 to Di), wherein the first data line (D1) is the data line to which a data signal is supplied first among the set of data lines (D1 to Di);

wherein each of the second switches (SW2) is turned on by the same control signal (CS1) that turns on the first switch (SW1) coupled to the first data line (D1), so that the initialization voltage (Vint1) is supplied to the data lines (D2 to Di) of said set of data lines (D1 to Di) except the first data line (D1) when the data voltage is supplied to the first data line (D1), and
characterized in that
a control signal (CS1) supplied to the first switch (SW1) coupled to the first data line (D1) has a first width (W1) wider than a second width (W2) of a control signal (CS2, CS3) supplied to the first switch (SW1) coupled to the data line (D2 to Di) except the first data line (D1) among the set of data lines (D1 to Di),
wherein, before each of the scan signals is supplied to the a respective one of the scan lines (S1 to Sn), the first data signal corresponding to each horizontal period is supplied to the first data line (D1), and the voltage of the first initialization power source (Vint1) is supplied to the data lines (D2 to Di) except the first data line (D1).

2. The device as claimed in claim 1, wherein the first initialization voltage (Vint1) is set to a voltage lower than that of the data signals.

3. The device as claimed in claim 1 or 2, wherein the first switches (SW1) are progressively turned on, corresponding to control signals (CS1, CS2, CS3).

4. The device as claimed in one of claims 1 to 3, wherein the control signal (CS1) supplied to the first switch (SW1) coupled to the first data line (D1) overlaps with a scan signal during a partial period and/or
the control signal (CS2, CS3) supplied to the first switch (SW1) coupled to the data line (D2 to Di) except the first data line (D1) among the set of data lines (D1 to Di) completely overlaps with the scan signal.

5. The device as claimed in one of claims 1 to 4, further comprising pixels, wherein pixels positioned on a j-th (j is a natural number) horizontal line each includes:

an organic light emitting diode (OLED);
a first transistor (M1) controlling an amount of current supplied to the organic light emitting diode (OLED);
a second transistor (M2) coupled between a first electrode of the first transistor (M1) and a data line (Dm), the second transistor (M2) being turned on when a scan signal is supplied to a j-th scan line;
a third transistor (M3) coupled between a second electrode and a gate electrode of the first transistor (M1), the third transistor (M3) being turned on when the scan signal is supplied to the j-th scan line;
a storage capacitor (Cst) coupled between the gate electrode of the first transistor (M1) and a first power source; and
a sixth transistor (M6) coupled between the gate electrode of the first transistor (M1) and a second initialization power source providing a second initialization voltage (Vint2), the sixth transistor (M6) being turned on when a scan signal is supplied to a (j-1)-th scan line.

6. The device as claimed in claim 5, wherein the second initialization voltage (Vint2) is set to a voltage lower than that of the data signals or a voltage identical to that of the first initialization voltage (Vint1).

7. The device as claimed in claim 5 or 6, wherein each pixel further includes a boosting capacitor (Cb) coupled between the j-th scan line and the gate electrode of the first transistor (M1).

8. The device as claimed in claim 5 or 6, further comprising emission control lines (En) formed for each horizontal line, wherein the scan driver (110) supplies an emission control signal to a j-th emission control line so that the emission control signal overlaps with the scan signal supplied to the [j-1]-th and j-th scan lines.

9. The device as claimed in one of claims 5 to 8, wherein each pixel further includes:

a fourth transistor (M4) coupled between the first electrode of the first transistor (M1) and the first power source, the fourth transistor (M4) being turned off when the emission control signal is supplied to the j-th emission control line and otherwise turned on; and
a fifth transistor (M5) coupled between the second electrode of the first transistor (M1) and the organic light emitting diode (OLED), the fifth transistor (M5) being turned off when the emission control signal is supplied to the j-th emission control line (En) and otherwise turned on.

10. A driving method of an organic light emitting display device which comprises a plurality of scan lines (S1 to Sn) and a plurality of data lines (D1 to Dm), the method comprising:

progressively supplying scan signals to the scan lines (S1 to Sn), each of the scan signals being supplied to a respective one of the scan lines (S1 to Sn) during a horizontal period (1H);
progressively supplying data signals to a plurality of output lines (O1 to Om/i) during the horizontal period (1H); and
supplying the data signals to the data lines (D1 to Dm), wherein a demultiplexer (162) coupled to a respective one of the output lines (O1 to Om/i) supplies the data signals from the respective output line (O1) to a respective set of i data lines (D1 to Di), wherein i is a natural number ≥ 2, wherein during a first period in which a first data signal is initially supplied to a first data line (D1) among said set of i data lines (D1 to Di), a first initialization power source supplies a first initialization voltage (Vint1) to other data lines (D2 to Di) of the set of i data lines (D1 to Di) except the first data line (D1);
wherein the first initialization voltage (Vint1) is supplied only during the first period, and **characterized in that**
the period when the first data signal is supplied to the first data line (D1) of the set of i data lines (D1 to Di) is longer than the period when the data signal is supplied to each of the other data lines (D2 to Di),
wherein, before each of the scan signals is supplied to the respective on e of the scan lines (S1 to Sn), the first data signal corresponding to each horizontal period is supplied to the first data line (D1), and the voltage of the first initialization power source (Vint1) is supplied to the data lines (D2 to Di) except the first data line (D1).

11. The method as claimed in claim 10, wherein the first initialization voltage (Vint1) is set to a voltage lower than that of the data signals.

Patentansprüche

1. Eine organische lichtemittierende Anzeigevorrichtung, aufweisend:

eine Vielzahl von Ansteuerleitungen (S1 bis Sn) und eine Vielzahl von Datenleitungen (D1 bis Dm);
einen Ansteuertreiber (110), der schrittweise Ansteuersignale an die Ansteuerleitungen (S1 bis Sn) anlegt;
einen Datentreiber (120), der eine Vielzahl von Ausgangsleitungen (O1 bis Om/i) aufweist und während einer Periode, in der die Ansteuersignale anliegen, Datensignale an die Ausgangsleitungen (O1 bis Om/i) des Datentreibers (120) anlegt; und
eine Demultiplexereinheit (160), die eine Vielzahl von Demultiplexern (162) aufweist, wobei jeder Demultiplexer (162) mit einer jeweiligen der Ausgangsleitungen (O1 bis Om/i) des Datentreibers (120) gekoppelt ist und die Datensignale an einen jeweiligen Satz von i Datenleitungen (D1 bis Di) anlegt, wobei i eine natürliche Zahl ≥ 2 ist, wobei jeder Demultiplexer (162) aufweist:

i erste Schalter (SW1), wobei jeder erste Schalter (SW1) zwischen die besagte Ausgangsleitung (O1 bis Om/i) des Datentreibers (120) und eine entsprechende Datenleitung aus dem besagten Satz von Datenleitungen (D1 bis Di) gekoppelt ist, und
[i-1] zweite Schalter (SW2), wobei jeder zweite Schalter (SW2) zwischen eine erste Initialisierungsenergiequelle, die eine erste Initialisierungsspannung (Vint1) liefert, und eine Datenleitung (D2 bis Di) außer einer ersten Datenleitung (D1) aus dem besagten Satz von Datenleitungen (D1 bis Di) gekoppelt ist, wobei die erste Datenleitung (D1) die Datenleitung ist, an die ein Datensignal aus dem Satz von Datenleitungen (D1 bis D1) als erstes angelegt wird;

wobei jeder der zweiten Schalter (SW2) vom selben Steuersignal (CS1), das den ersten Schalter (SW1), der mit der ersten Datenleitung (D1) gekoppelt ist, einschaltet, eingeschaltet wird, so dass die Datenleitungen (D2 bis Di) des besagten Satzes von Datenleitungen (D1 bis Di) außer der ersten Datenleitung (D1) mit der Initialisierungsspannung (Vint1) versorgt werden, wenn die erste Datenleitung (D1) mit der Datenspannung versorgt wird, und
dadurch gekennzeichnet, dass
ein Steuersignal (CS1), das am ersten Schalter (SW1), der mit der ersten Datenleitung (D1) gekoppelt ist, anliegt, eine erste Breite (W1) aufweist, die breiter ist als eine zweite Breite (W2) eines Steuersignals (CS2, CS3), das am ersten Schalter (SW1), der mit der Datenleitung (D2 bis Di) außer der ersten Datenleitung (D1) aus dem Satz von Datenleitungen (D1 bis Di) gekoppelt ist, anliegt,
wobei vor dem Anlegen jedes der Ansteuersignale an eine jeweilige der Ansteuerleitungen (S1 bis Sn) das erste Datensignal, das jeder horizontalen Periode entspricht, an die erste Datenleitung (D1) angelegt wird und die Datenleitun-

gen (D2 bis Di) außer der ersten Datenleitung (D1) mit der Spannung der ersten Initialisierungsenergiequelle (Vint1) versorgt werden.

2. Die Vorrichtung nach Anspruch 1, wobei die erste Initialisierungsspannung (Vint1) auf eine Spannung, die niedriger als die der Datensignale ist, eingestellt ist.

3. Die Vorrichtung nach Anspruch 1 oder 2, wobei die ersten Schalter (SW1) entsprechend Steuersignalen (CS1, CS2, CS3) schrittweise eingeschaltet werden.

4. Die Vorrichtung nach einem der Ansprüche 1 bis 3, wobei das Steuersignal (CS1), das am ersten Schalter (SW1), der mit der ersten Datenleitung (D1) gekoppelt ist, anliegt, während einer Teilperiode mit einem Ansteuersignal überlappt, und/oder
das Steuersignal (CS2, CS3), das am ersten Schalter (SW1), der mit der Datenleitung (D2 bis Di) außer der ersten Datenleitung (D1) aus dem Satz von Datenleitungen (D1 bis Di) gekoppelt ist, anliegt, mit dem Ansteuersignal vollständig überlappt.

5. Die Vorrichtung nach einem der Ansprüche 1 bis 4, ferner aufweisend Pixel, wobei Pixel, die auf einer jten (j ist eine natürliche Zahl) horizontalen Linie positioniert sind, jeweils aufweisen:

eine organische lichtemittierende Diode (OLED);
einen ersten Transistor (M1), der eine Menge von Strom, mit dem die organische lichtemittierende Diode (OLED) versorgt wird, steuert;
einen zweiten Transistor (M2), der zwischen eine erste Elektrode des ersten Transistors (M1) und eine Datenleitung (Dm) gekoppelt ist, wobei der zweite Transistor (M2) eingeschaltet wird, wenn ein Ansteuersignal an eine jte Ansteuerleitung angelegt wird;
einen dritten Transistor (M3), der zwischen eine zweite Elektrode und eine Gate-Elektrode des ersten Transistors (M1) gekoppelt ist, wobei der dritte Transistor (M3) eingeschaltet wird, wenn das Ansteuersignal an die jte Ansteuerleitung angelegt wird;
einen Speicherkondensator (Cst), der zwischen die Gate-Elektrode des ersten Transistors (M1) und eine erste Energiequelle gekoppelt ist; und
einen sechsten Transistor (M6), der zwischen die Gate-Elektrode des ersten Transistors (M1) und eine zweite Initialisierungsenergiequelle, die eine zweite Initialisierungsspannung (Vint2) bereitstellt, gekoppelt ist, wobei der sechste Transistor (M6) eingeschaltet wird, wenn ein Ansteuersignal an eine (j-1)te Ansteuerleitung angelegt wird.

6. Die Vorrichtung nach Anspruch 5, wobei die zweite Initialisierungsspannung (Vint2) auf eine Spannung, die niedriger als die der Datensignale oder auf eine Spannung, die gleich der der ersten Initialisierungsspannung (Vint1) ist, eingestellt ist.

7. Die Vorrichtung nach Anspruch 5 oder 6, wobei jeder Pixel ferner einen Boost-Kondensator (Cb), der zwischen die jte Ansteuerleitung und die Gate-Elektrode des ersten Transistors (M1) gekoppelt ist, aufweist.

8. Die Vorrichtung nach Anspruch 5 oder 6, ferner aufweisend Emissionssteuerleitungen (En), die für jede horizontale Linie ausgebildet sind, wobei der Ansteuertreiber (110) ein Emissionssteuersignal an eine jte Emissionssteuerleitung anlegt, so dass das Emissionssteuersignal mit dem an den [j-1]ten und jten Ansteuerleitungen anliegenden Ansteuersignal überlappt.

9. Die Vorrichtung nach einem der Ansprüche 5 bis 8, wobei jeder Pixel ferner aufweist:

einen vierten Transistor (M4), der zwischen die erste Elektrode des ersten Transistors (M1) und die erste Energiequelle gekoppelt ist, wobei der vierte Transistor (M4) ausgeschaltet wird, wenn das Emissionssteuersignal an die jte Emissionssteuerleitung angelegt wird und andernfalls eingeschaltet ist; und
einen fünften Transistor (M5), der zwischen die zweite Elektrode des ersten Transistors (M1) und die organische lichtemittierende Diode (OLED) gekoppelt ist, wobei der fünfte Transistor (M5) ausgeschaltet wird, wenn das Emissionssteuersignal an die jte Emissionssteuerleitung (En) angelegt wird und andernfalls eingeschaltet ist.

10. Ein Verfahren zur Ansteuerung einer organischen lichtemittierenden Anzeigevorrichtung, die eine Vielzahl von Ansteuerleitungen (S1 bis Sn) und eine Vielzahl von Datenleitungen (D1 bis Dm) aufweist, wobei das Verfahren aufweist:

schrittweises Anlegen von Ansteuersignalen an die Ansteuerleitungen (S1 bis Sn), wobei jedes der Ansteuersignale während einer horizontalen Periode (1H) an einer jeweiligen der Ansteuerleitungen (S1 bis Sn) anliegt;
schrittweises Anlegen von Datensignalen an eine Vielzahl von Ausgangsleitungen (O1 bis Om/i) während der horizontalen Periode (1H); und
Anlegen der Datensignale an die Datenleitungen (D1 bis Dm), wobei ein Demultiplexer (162), der mit einer jeweiligen der Ausgangsleitungen

(O1 bis Om/i) des Datentreibers gekoppelt ist, die Datensignale von der jeweiligen Ausgangsleitung (O1) an einen jeweiligen Satz von i Datenleitungen (D1 bis D1) anlegt, wobei i eine natürliche Zahl ≥ 2 ist,
wobei während einer ersten Periode, in der ein erstes Datensignal zuerst an eine erste Datenleitung (D1) aus dem besagten Satz von i Datenleitungen (D1 bis Di) angelegt wird, eine erste Initialisierungsenergiequelle andere Datenleitungen (D2 bis Di) des Satzes von i Datenleitungen (D1 bis Di) außer der ersten Datenleitung (D1) mit einer ersten Initialisierungsspannung (Vint1) versorgt;
wobei die erste Initialisierungsspannung (Vint1) nur während der ersten Periode anliegt,
und **dadurch gekennzeichnet, dass**
die Periode, in der das erste Datensignal an der ersten Datenleitung (D1) des Satzes von i Datenleitungen (D1 bis Di) anliegt, länger ist als die Periode, in der das Datensignal an jeder der anderen Datenleitungen (D2 bis Di) anliegt,
wobei vor dem Anlegen jedes der Ansteuersignale an die jeweilige der Ansteuerleitungen (S1 bis Sn) das erste Datensignal, das jeder horizontalen Periode entspricht, an die erste Datenleitung (D1) angelegt wird und die Datenleitungen (D2 bis Di) außer der ersten Datenleitung (D1) mit der Spannung der ersten Initialisierungsenergiequelle (Vint1) versorgt werden.

11. Das Verfahren nach Anspruch 10, wobei die erste Initialisierungsspannung (Vint1) auf eine Spannung, die niedriger als die der Datensignale ist, eingestellt wird.

Revendications

1. Dispositif d'affichage électroluminescent organique, comprenant :

une pluralité de lignes de balayage (S1 à Sn) et une pluralité de lignes de données (D1 à Dm) ;
un pilote de balayage (110) fournissant progressivement des signaux de balayage aux lignes de balayage (S1 à Sn) ;
un pilote de données (120) ayant une pluralité de lignes de sortie (O1 à Om/i) et fournissant des signaux de données aux lignes de sortie (O1 à Om/i) du pilote de données (120) pendant une période au cours de laquelle les signaux de balayage sont fournis ; et
une unité de démultiplexeur (160) comportant une pluralité de démultiplexeurs (162), chaque démultiplexeur (162) étant couplé à une ligne respective des lignes de sortie (O1 à Om/i) du pilote de données (120), et fournissant les signaux de données à un ensemble respectif de i lignes de données (D1 à Di), où i est un entier naturel ≥ 2, chaque démultiplexeur (162) comportant :

i premiers commutateurs (SW1), chaque premier commutateur (SW1) étant couplé entre ladite ligne de sortie (O1 à Om/i) du pilote de données (120) et une ligne de données correspondante parmi ledit ensemble de lignes de données (D1 à Di), et
[i-1] deuxièmes commutateurs (SW2), chaque deuxième commutateur (SW2) étant couplé entre une première source d'énergie d'initialisation fournissant une première tension d'initialisation (Vint1) et une ligne de données (D2 à Di) à l'exception d'une première ligne de données (D1) parmi ledit ensemble de lignes de données (D1 à Di), où la première ligne de données (D1) est la ligne de données à laquelle est fourni un signal de données en premier parmi l'ensemble des lignes de données (D1 à Di) ;

dans lequel chacun des deuxièmes commutateurs (SW2) est mis à l'état passant par le même signal de commande (CS1) qui met à l'état passant le premier commutateur (SW1) couplé à la première ligne de données (D1), de sorte que la tension d'initialisation (Vint1) soit fournie aux lignes de données (D2 à Di) dudit ensemble de lignes de données (D1 à Di) à l'exception de la première ligne de données (D1) lorsque la tension de données est fournie à la première ligne de données (Dl), et
caractérisé en ce que
un signal de commande (CS1) fourni au premier commutateur (SW1) couplé à la première ligne de données (D1) a une première largeur (W1) plus large qu'une deuxième largeur (W2) d'un signal de commande (CS2, CS3) fourni au premier commutateur (SW1) couplé à la ligne de données (D2 à Di) à l'exception de la première ligne de données (D1) parmi l'ensemble de lignes de données (D1 à Di),
dans lequel, avant que chacun des signaux de balayage ne soit fourni à celle respective des lignes de balayage (S1 à Sn), le premier signal de données correspondant à chaque période horizontale est fourni à la première ligne de données (D1), et la tension de la première source d'énergie d'initialisation (Vint1) est fournie aux lignes de données (D2 à Di) à l'exception de la première ligne de données (D1).

2. Dispositif selon la revendication 1, dans lequel la première tension d'initialisation (Vint1) est réglée sur une tension inférieure à celle des signaux de don-

nées.

3. Dispositif selon la revendication 1 ou 2, dans lequel les premiers commutateurs (SW1) sont mis à l'état passant progressivement, en correspondance avec des signaux de commande (CS1, CS2, CS3).

4. Dispositif selon l'une quelconque des revendications 1 à 3, dans lequel le signal de commande (CS1) fourni au premier commutateur (SW1) couplé à la première ligne de données (D1) chevauche un signal de balayage pendant une période partielle et/ou le signal de commande (CS2, CS3) fourni au premier commutateur (SW1) couplé à la ligne de données (D2 à Di) à l'exception de la première ligne de données (D1) parmi l'ensemble de lignes de données (D1 à Di) chevauche entièrement le signal de balayage.

5. Dispositif selon l'une quelconque des revendications 1 à 4, comprenant en outre des pixels, dans lequel des pixels positionnés sur une j-ème (j est un entier naturel) ligne horizontale comportent chacun :

une diode électroluminescente organique (DELO) ;
un premier transistor (M1) commandant une quantité de courant fournie à la diode électroluminescente organique (DELO) ;
un deuxième transistor (M2) couplé entre une première électrode du premier transistor (M1) et une ligne de données (Dm), le deuxième transistor (M2) étant mis à l'état passant lorsqu'un signal de balayage est fourni à une j-ème ligne de balayage ;
un troisième transistor (M3) couplé entre une deuxième électrode et une électrode de grille du premier transistor (M1), le troisième transistor (M3) étant mis à l'état passant lorsque le signal de balayage est fourni à la j-ème ligne de balayage ;
un condensateur de stockage (Cst) couplé entre l'électrode de grille du premier transistor (M1) et une première source d'énergie ; et
un sixième transistor (M6) couplé entre l'électrode de grille du premier transistor (M1) et une deuxième source d'énergie d'initialisation fournissant une deuxième tension d'initialisation (Vint2), le sixième transistor (M6) étant mis à l'état passant lorsqu'un signal de balayage est fourni à une (j-1)-ème ligne de balayage

6. Dispositif selon la revendication 5, dans lequel la deuxième tension d'initialisation (Vint2) est réglée sur une tension inférieure à celle des signaux de données ou une tension identique à celle de la première tension d'initialisation (Vint1).

7. Dispositif selon la revendication 5 ou 6, dans lequel chaque pixel comporte en outre un condensateur d'amplification (Cb) couplé entre la j-ème ligne de balayage et l'électrode de grille du premier transistor (M1).

8. Dispositif selon la revendication 5 ou 6, comprenant en outre des lignes de commande d'émission (En) formées pour chaque ligne horizontale, dans lequel le pilote de balayage (110) fournit un signal de commande d'émission à une j-ème ligne de commande d'émission de sorte que le signal de commande d'émission chevauche le signal de balayage fourni aux [j-1]-ème et j-ème lignes de balayage.

9. Dispositif selon l'une quelconque des revendications 5 à 8, dans lequel chaque pixel comporte en outre :

un quatrième transistor (M4) couplé entre la première électrode du premier transistor (M1) et la première source d'énergie, le quatrième transistor (M4) étant mis à l'état non passant lorsque le signal de commande d'émission est fourni à la j-ème ligne de commande d'émission et autrement mis à l'état passant ; et
un cinquième transistor (M5) couplé entre la deuxième électrode du premier transistor (M1) et la diode électroluminescente organique (DELO), le cinquième transistor (M5) étant mis à l'état non passant lorsque le signal de commande d'émission est fourni à la j-ème ligne de commande d'émission (En) et autrement mis à l'état passant.

10. Procédé d'attaque d'un dispositif d'affichage électroluminescent organique qui comprend une pluralité de lignes de balayage (S1 à Sn) et une pluralité de lignes de données (D1 à Dm), le procédé comprenant les étapes consistant à :

fournir progressivement des signaux de balayage aux lignes de balayage (S1 à Sn), chacun des signaux de balayage étant fourni à l'une respective des lignes de balayage (S1 à Sn) pendant une période horizontale (1H) ;
fournir progressivement des signaux de données à une pluralité de lignes de sortie (O1 à Om/i) pendant la période horizontale (1H) ; et
fournir les signaux de données aux lignes de données (D1 à Dm), où un démultiplexeur (162) couplé à l'une respective des lignes de sortie (O1 à Om/i) fournit les signaux de données à partir de la ligne de sortie respective (O1) à un ensemble respectif de i lignes de données (D1 à Di), où i est un entier naturel ≥ 2,
dans lequel pendant une première période au cours de laquelle un premier signal de données est initialement fourni à une première ligne de

données (D1) parmi ledit ensemble de i lignes de données (D1 à Di), une première source d'énergie d'initialisation fournit une première tension d'initialisation (Vint1) à d'autres lignes de données (D2 à Di) de l'ensemble de i lignes de données (D1 à Di) à l'exception de la première ligne de données (D1) ;
dans lequel la première tension d'initialisation (Vint1) est fournie uniquement pendant la première période, et
caractérisé en ce que
la période pendant laquelle le premier signal de données est fourni à la première ligne de données (D1) de l'ensemble de i lignes de données (D1 à Di) est plus longue que la période pendant laquelle le signal de données est fourni à chacune des autres lignes de données (D2 à Di),
dans lequel, avant que chacun des signaux de balayage ne soit fourni à celle respective des lignes de balayage (S1 à Sn), le premier signal de données correspondant à chaque période horizontale est fourni à la première ligne de données (D1), et la tension de la première source d'énergie d'initialisation (Vint1) est fournie aux lignes de données (D2 à Di) à l'exception de la première ligne de données (D1) .

11. Procédé selon la revendication 10, dans lequel la première tension d'initialisation (Vint1) est réglée sur une tension inférieure à celle des signaux de données.

FIG. 1

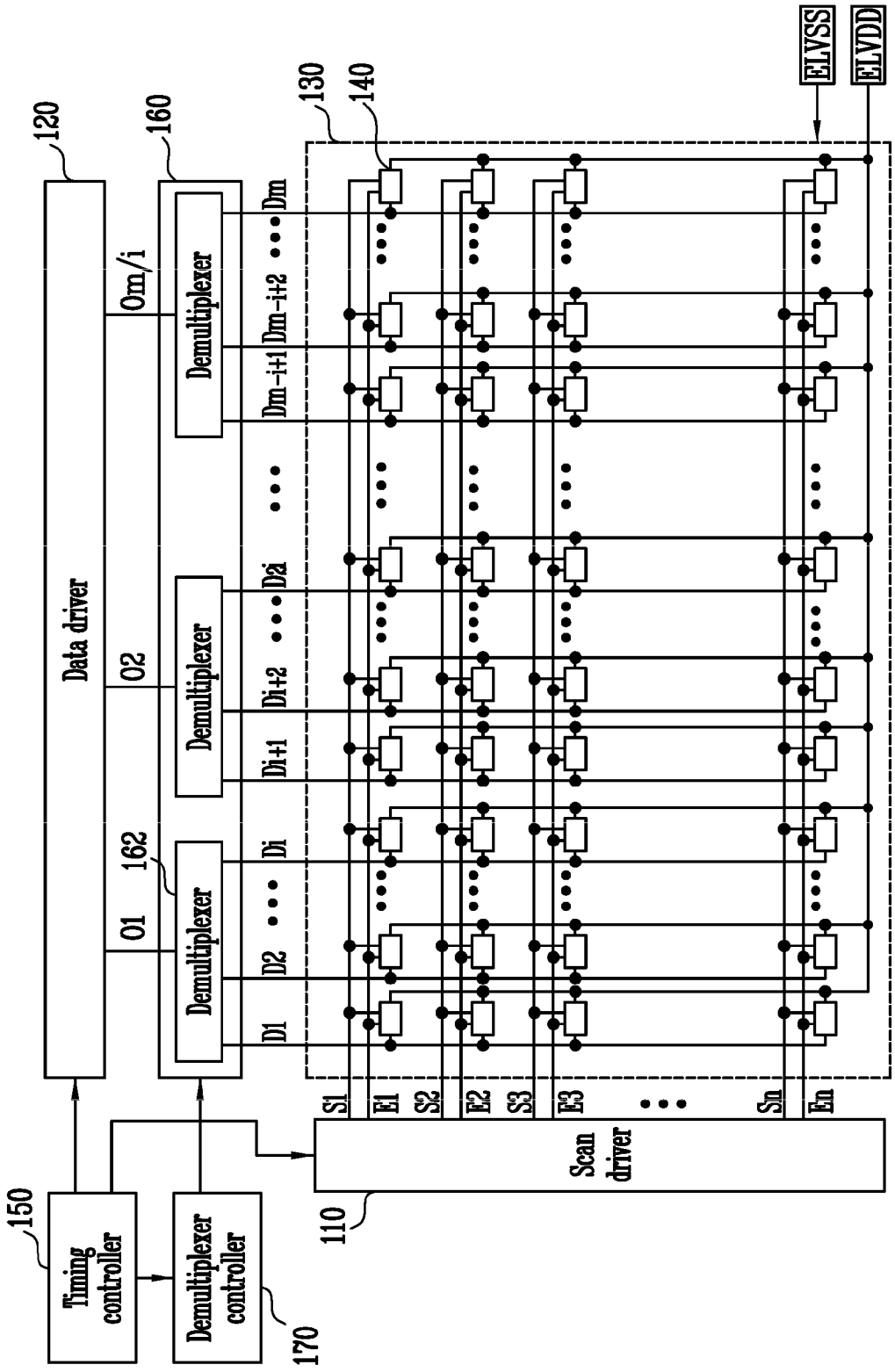

Timing controller
150
Demultiplexer controller
170
Data driver
120
Demultiplexer
160
162
O1
O2
Om/i
D1
D2
Di
Di+1
Di+2
Dai
Dm-i+1
Dm-i+2
Dm
Scan driver
110
S1
E1
S2
E2
S3
E3
Sn
En
130
140
ELVSS
ELVDD

FIG. 2

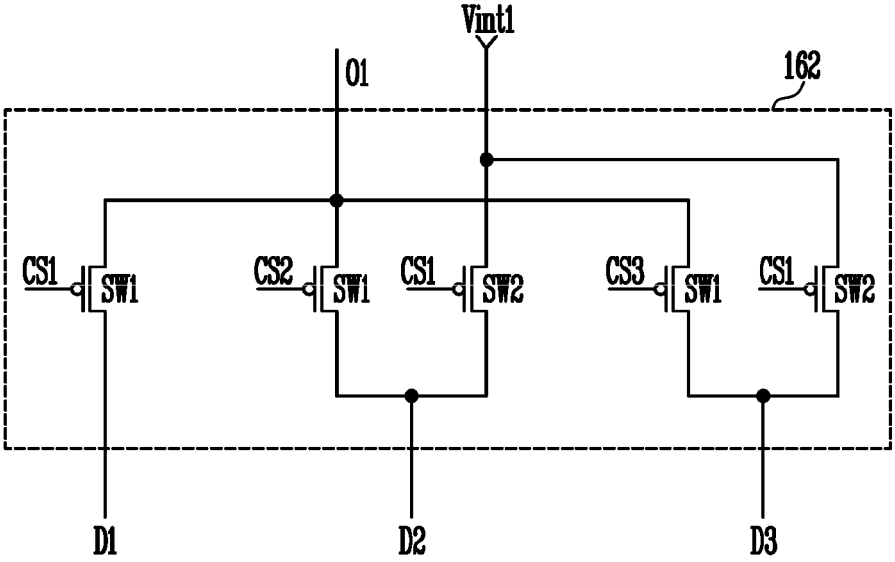

Vint1
O1
162
CS1
SW1
CS2
SW1
CS1
SW2
CS3
SW1
CS1
SW2
D1
D2
D3

FIG. 3

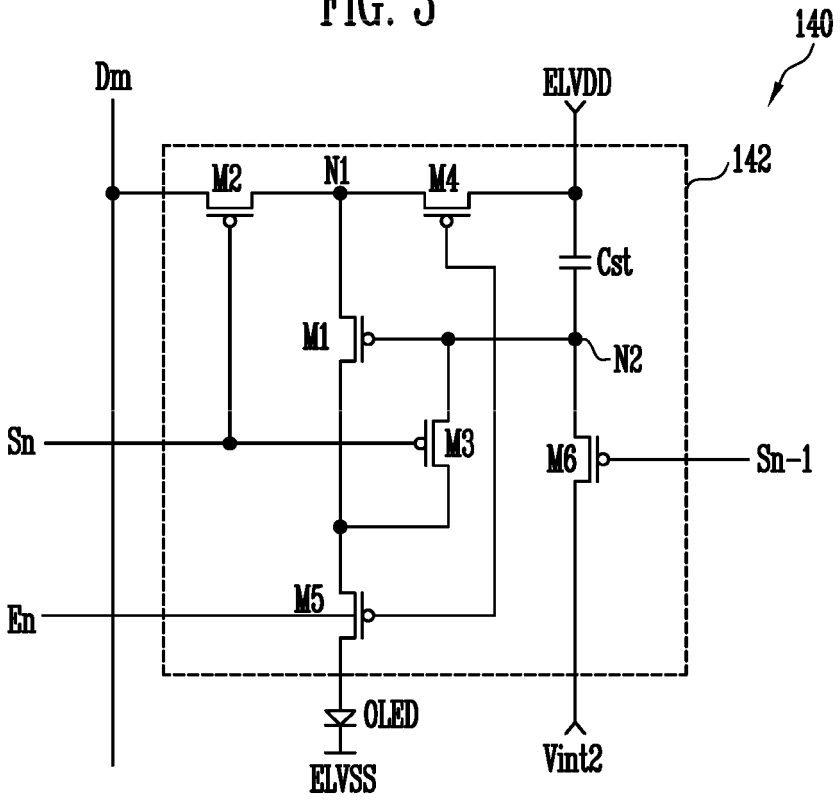

140
Dm
ELVDD
142
M2
N1
M4
Cst
M1
N2
Sn
M3
M6
Sn-1
M5
En
OLED
ELVSS
Vint2

FIG. 4

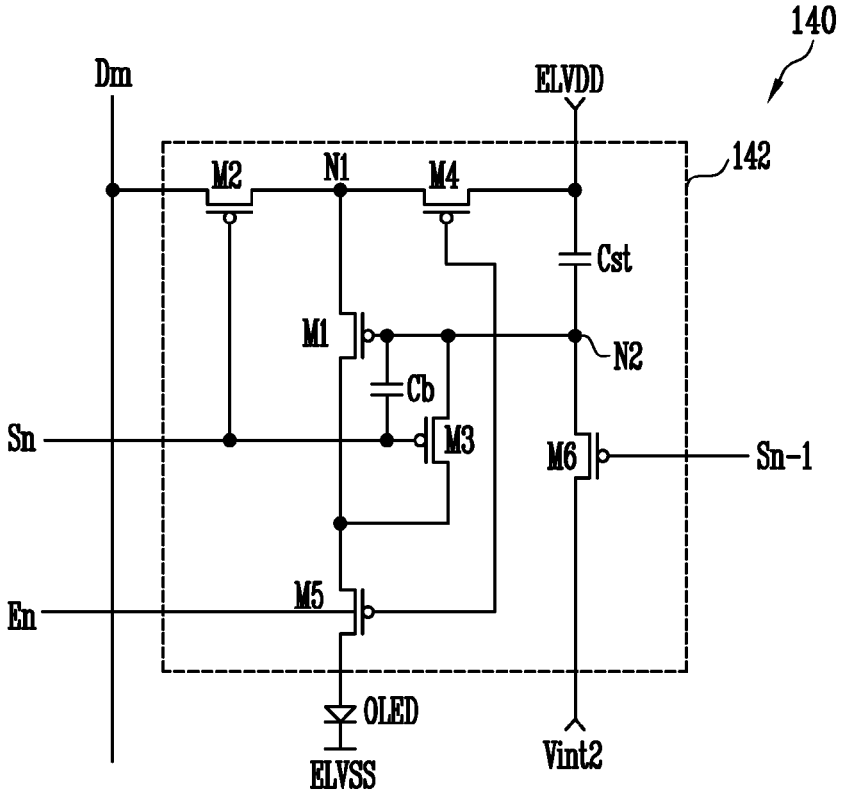

140
Dm
ELVDD
142
M2
N1
M4
Cst
M1
N2
Cb
Sn
M3
M6
Sn-1
M5
En
OLED
ELVSS
Vint2

FIG. 5

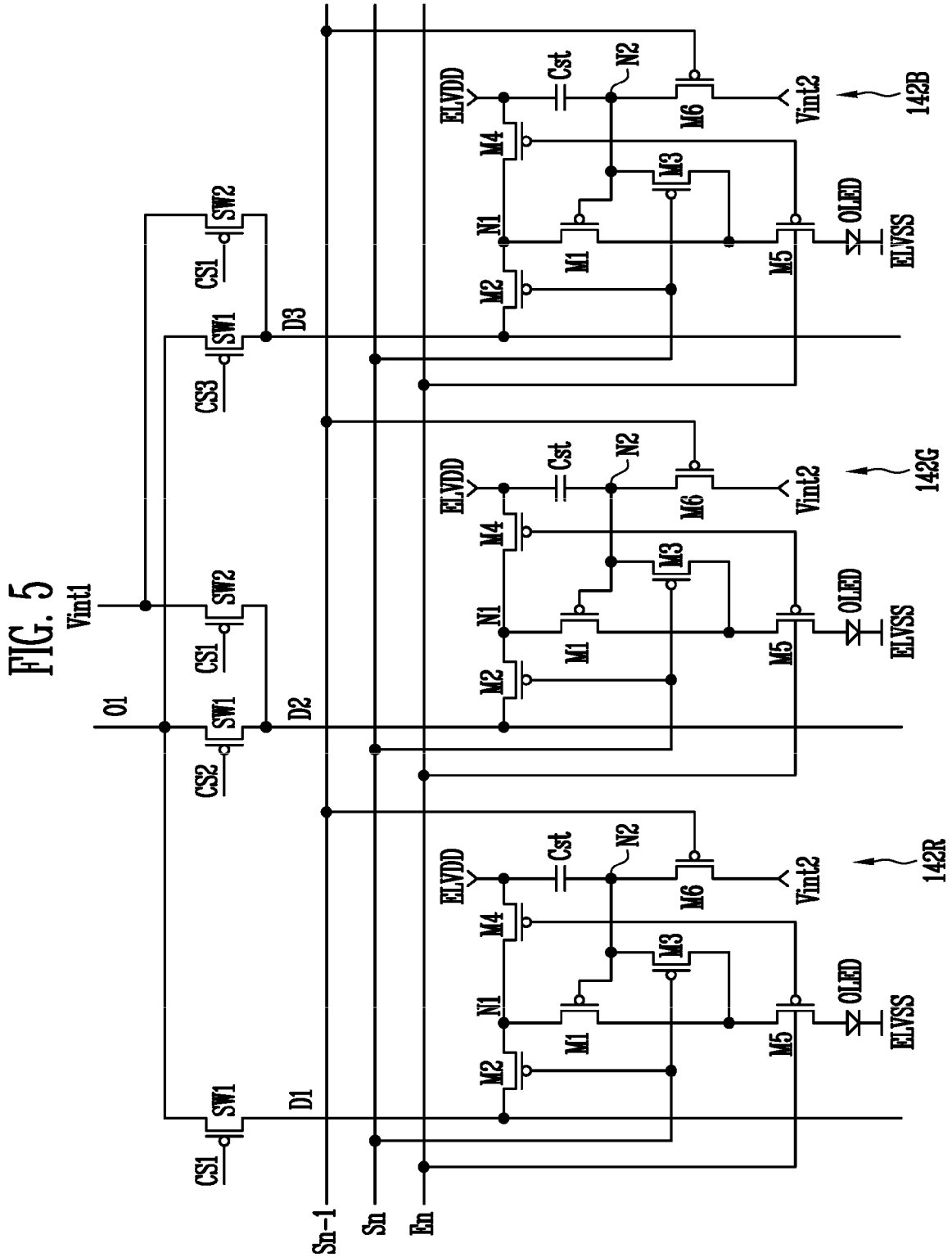

Vint1
O1
CS1
SW2
CS3
SW1
CS2
D3
D2
D1
Sn-1
Sn
En
ELVDD
Cst
N2
M6
Vint2
142B
142G
142R
M4
M3
N1
M1
M2
M5
OLED
ELVSS

FIG. 6

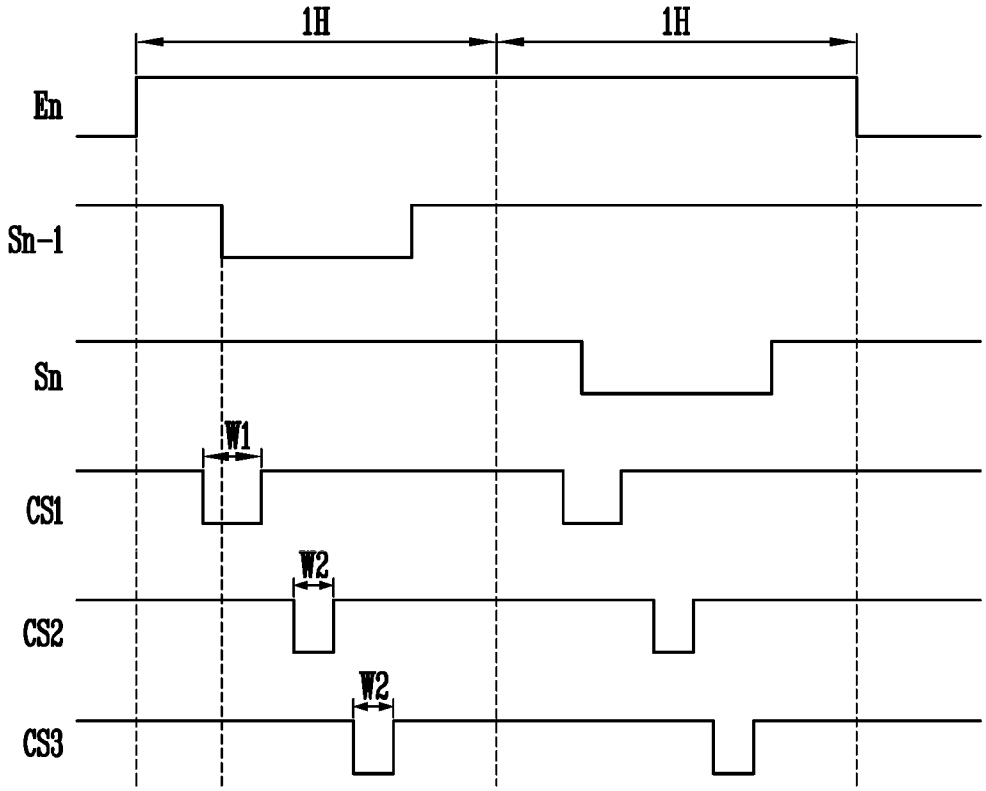
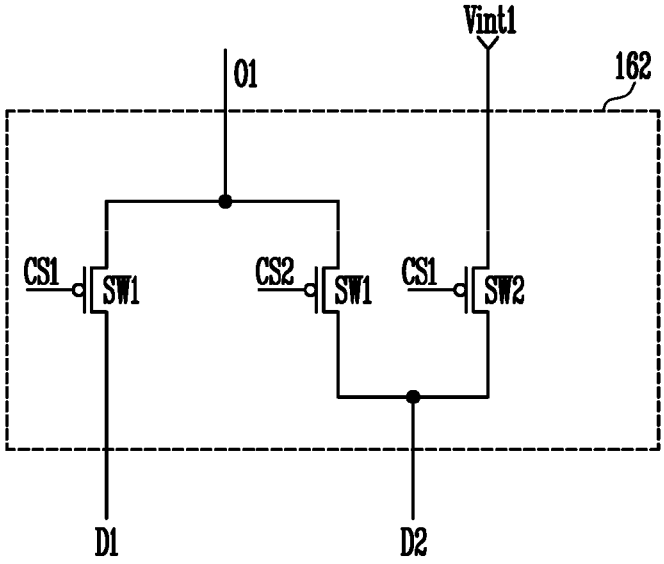

1H
1H
En
Sn-1
Sn
W1
CS1
W2
CS2
W2
CS3

FIG. 7


Vint1
O1
162
CS1
SW1
CS2
SW1
CS1
SW2
D1
D2

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 1347436 A2 **[0004]**
- US 20060151745 A1 **[0005]**

专利名称(译)	有机发光显示装置及其驱动方法		
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摘要(译)

一种有机发光显示装置，包括：扫描驱动器，其向扫描线逐渐提供扫描信号；数据驱动器，在提供扫描信号的时间段内，将数据信号提供给数据驱动器的输出线；以及解复用器，其分别耦合至输出每个多路分解器包括第一开关，每个第一开关耦合在数据驱动器的输出线和第一组数据线中的数据线之间，第二开关将数据信号提供给数据线。在第二组数据线中的第一初始化电源和数据线之间耦合，其中第一组数据线包括第二组数据线和至少一条其他数据线。

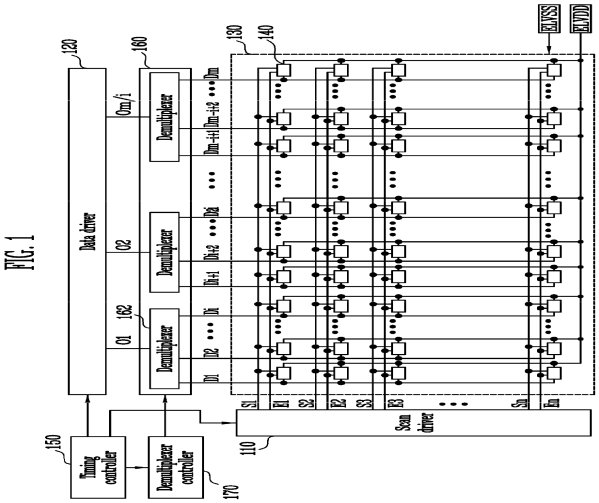

FIG. 1