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(54) **Organic light emitting display and driving method thereof**

Organische lichtemittierende Anzeige und Verfahren zu ihrer Ansteuerung

Affichage électroluminescent organique et son procédé de commande

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Description

[0001] This application claims the priority date of Korean Patent Application NO. 10-2012-0095604 filed on August 30, 2012.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] This document relates to an active matrix type organic light emitting display and a driving method thereof.

Discussion of the Related Art

[0003] US2011/0157143 A1 discloses a pixel and organic light emitting display device using the same. A pixel is provided, which is capable of displaying images with substantially uniform luminance.

[0004] US 2011/0154352 A1 discloses a display apparatus that can compensate for a temporal variation in luminance of a display element.

[0005] KR 2010/0053233 A discloses an organic light emitting display having pixels, a data driving circuit and a gate driving circuit, wherein each pixel comprises an OLED, a driving TFT, a storage capacitor and four switching TFT to control the OLED in order to improve the lowering of uniformity phenomenon caused by deterioration.

[0006] An active matrix type organic light emitting display includes a self-luminous organic light emitting diode (hereinafter, referred to as "OLED"), and is advantageous in that it has high response speed, luminous efficiency, and luminance, and a large viewing angle.

[0007] An OLED, which is a self-luminous element, has the structure as shown in FIG. 1. The OLED includes an anode, a cathode, and an organic compound layer HIL, HTL, EML, ETL, EIL formed between the anode and the cathode. The organic compound layer includes a hole injection layer HIL, a hole transport layer HTL, an emission layer EML, an electron transport layer ETL and an electron injection layer EIL. If drive voltages are applied to the anode electrode and the cathode electrode, holes within the hole injection layer HTL and electrons within the electron transport layer ETL respectively move to the emission layer EML to form excitons. As a result, the emission layer EML emits a visible ray.

[0008] The organic light emitting display includes pixels each including an OLED which area arranged in a matrix form, and controls the luminance of the pixels according to the gray scale of video data. Each pixel includes a driving TFT (thin film transistor) for controlling the driving current flowing through the OLED in accordance with a gate-source voltage, a capacitor for keeping a gate potential of the driving TFT constant during a frame, and a switching TFT for storing a data voltage in the capacitor in response to a gate signal. The luminance of a pixel is proportional to the magnitude of the driving current that flows through the OLED.

[0009] The organic light emitting display is disadvantageous in that the driving TFTs of the pixels have different threshold voltages depending on where they are formed, due to a process deviation or the like, or the electrical properties of the driving TFTs are deteriorated due to a gate-bias stress which occurs with the elapse of driving time. To solve this problem, Korean Laid-Open Patent Publication No. 10-2005-0122699 discloses a pixel circuit of an organic light emitting display which detects, as the threshold voltage of a driving TFT, a gate-source voltage at which a drain-source current becomes sufficiently small by diode-connecting the driving TFT, and compensates a data voltage by the detected threshold voltage. The pixel circuit uses a light emission control TFT serially connected between the driving TFT and an OLED in order to turn off light emission of the OLED upon detecting the threshold voltage of the driving TFT.

[0010] However, the conventional pixel circuit of an organic light emitting display is problematic in that its capability of compensating for the threshold voltage of the driving TFT is low and some TFTs show low reliability due to the following reasons.

[0011] First, when detecting the threshold voltage of a driving TFT of a diode structure, a gate-drain voltage becomes "0V", and thus a minimum threshold voltage (for n-type) or maximum detectable threshold voltage (for p-type) is "0V". Therefore, according to a conventional method for detecting the threshold voltage of a driving TFT by diode connection, a pixel circuit using an n-type TFT can detect the threshold voltage of the driving TFT only when the threshold voltage of the driving TFT has a positive value, and a pixel circuit using a p-type TFT can detect the threshold voltage of the driving TFT only when the threshold voltage of the driving TFT has a negative value. In other words, a conventional method for compensating a threshold voltage cannot be applied if the threshold voltage of the driving TFT in the pixel circuit using a p-type TFT has a negative value, and also cannot be applied if the threshold voltage of the driving TFT in the pixel circuit using an n-type TFT has a positive value.

[0012] Second, a parasitic capacitance exists between a TFT of a pixel circuit and a signal line. The parasitic capacitance causes a kick-back voltage when a gate signal applied to the TFT is turned off. If the kick-back voltage is high, a detected threshold voltage cannot be properly maintained but distorted, thus decreasing the accuracy of compensation. To increase the accuracy of threshold voltage compensation, the gate and source voltages of the driving TFT need to be increased further when detecting a threshold voltage, by taking distortion in subsequent steps into consideration. However, the conventional method for threshold voltage compensation cannot improve the accuracy of compensation because a fixed potential is applied to the gate of the driving TFT.

[0013] Third, the light emission control TFT serially connected between the driving TFT and the OLED is turned off in a period during which threshold voltage sensing and data programming are performed is a first period, and the period during which light emission occurs is a second period, a proportion that the second period occupies in one frame is much larger than that of the first period. Since the light emission control TFT in the pixel circuit is kept turned on during the entire emission period, the reliability of the light emission control TFT is lowered due to a deterioration caused by a gate-bias stress.

SUMMARY

[0014] The invention is defined by the independent claims. Accordingly, it is an object of the present invention to provide an organic light emitting display and a driving method thereof which increase the capability of compensating for the threshold voltage of a driving TFT and improve the reliability of TFTs in the pixel circuit. The objects are solved by the features of the independent claims.

[0015] To accomplish the above aspect, according to an exemplary embodiment of the present invention, there is provided an organic light emitting display comprising: an organic light emitting diode; a driving TFT comprising a gate connected to a node B, a drain connected to an input terminal of high-potential cell driving voltage, and a source connected to the organic light emitting diode through a node C, and for controlling the current applied to the organic light emitting diode; a first switching TFT for switching the current path between a node A and the node B in response to a light emission control signal; a second switching TFT for initializing the node C to an initialization voltage in response to an initialization signal; a third switching TFT for initializing either the node A or the node B to a reference voltage higher than the initialization voltage in response to the initialization signal; a fourth switching TFT for switching the current path between a data line and the node B in response to a scan signal; a compensation capacitor connected between the node B and the node C; and a storage capacitor connected between node A and node C.

[0016] To accomplish the above aspect, a driving method of an organic light emitting display comprising a driving TFT comprising a gate connected to a node B, a drain connected to an input terminal of high-potential cell driving voltage, and a source connected to the organic light emitting diode through a node C, and for controlling the current applied to the organic light emitting diode, the method comprising: initializing the node C to an initialization voltage in response to an initialization signal, and initializing the node B to a reference voltage higher than the initialization voltage in response to the initialization signal and a light emission control signal; stopping the supply of the initialization voltage and allowing the node B to float, and then detecting and storing the threshold voltage of the driving TFT by using a compensation capacitor connected between the node B and the node C; applying a data voltage to a node A connected to a storage capacitor in response to a scan signal; and transmitting the data voltage of the node A to the node B in response to the light emission control signal to compensate for the driving current applied to the organic light emitting diode, regardless of the threshold voltage, and causing the organic light emitting diode to emit light.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0018] In the drawings:

FIG. 1 is a view showing an organic light emitting diode and the principle of light emission thereof;
FIG. 2 shows an organic light emitting display according to an exemplary embodiment of the present invention;
FIG. 3 shows an example of the pixel P of FIG. 2;
FIG. 4 is a waveform diagram showing signals applied to the pixel of FIG. 3, potential changes of nodes A, B, and C responsive to these signals, and changes in the current flowing through the driving TFT and the OLED;
FIG. 5a is an equivalent circuit diagram of the pixel corresponding to an initialization period;
FIG. 5b is an equivalent circuit diagram of the pixel corresponding to a sensing period;
FIG. 5c is an equivalent circuit diagram of the pixel corresponding to a programming period;
FIG. 5d is an equivalent circuit diagram of the pixel corresponding to a first emission period;
FIG. 5e is an equivalent circuit diagram of the pixel corresponding to a second emission period;
FIG. 6 shows a design method of a driving TFT for improving the threshold voltage compensation capability;
FIG. 7 shows another example of the pixel P of FIG. 2; and
FIG. 8 shows a driving waveform of a gate signal suggested in the present invention, as compared to the conventional art;
FIG. 9 shows the progress of threshold voltage degradation in accordance with the on duty of the gate signal; and
FIG. 10 shows the result of simulation of the threshold voltage compensation performance of the pixel suggested in the present invention.

DETAILED DESCRIPTION

[0019] Hereinafter, an exemplary embodiment of the present invention will be described with reference to FIGS. 2 to 10.

[0020] FIG. 2 shows an organic light emitting display according to an exemplary embodiment of the present invention.

[0021] Referring to FIG. 2, the organic light emitting display according to the exemplary embodiment of the present invention comprises a display panel 10 having pixels P arranged in a matrix form, a data driving circuit 12 for driving data lines 14, a gate driving circuit 13 for driving gate line portions 15, and a timing controller for controlling the driving timings of the data and gate driving circuits 12 and 13.

[0022] A plurality of data lines 14 and a plurality of gate line portions 15 cross each other on the display panel 10, and pixels P are disposed in a matrix form at crossing regions of the data lines 14 and the gate line portions 15. Each of the gate line portions 15 comprises a scan line 15a, an emission line 15b, and an initialization line 15c. Each pixel P is connected to a data line 14 and the three signal lines 15a, 15b, and 15c constituting a gate line portion 15. The pixels P are supplied with high-potential and low-potential cell driving voltages EVDD and EVSS, a reference voltage Vref, and an initialization voltage Vinit. The reference voltage Vref and the initialization voltage Vinit may be set lower than the low-potential cell driving voltage EVSS. The reference voltage Vref is set higher than the initialization voltage Vinit; especially, the difference between the reference voltage Vref and the initialization voltage Vinit may be set higher than the threshold voltage of a driving TFT. Each of the pixels P comprises an OLED, a driving TFT, four switching TFTs, and two capacitors.

[0023] The pixel P of the present invention detects the threshold voltage of the driving voltage according to a source-follower method, instead of a conventional diode connection method. In the source-follower method, a compensation capacitor is connected between the gate and source of the driving TFT, and the source voltage of the driving TFT follows the gate voltage upon detecting the threshold voltage. Moreover, since the drain of the driving TFT is separated from the gate and supplied with the high-potential cell driving voltage EVDD, this source-follower method makes it possible to detect a negative threshold voltage value, as well as a positive threshold voltage value. The pixel P of the present invention allows the gate of the driving TFT to float upon sensing the threshold voltage of the driving TFT, and improves the threshold voltage compensation capability by using the compensation capacitor connected between the gate and source of the driving TFT and a parasitic capacitor of the driving TFT. By minimizing the on-duty of a light emission control signal applied to the pixel P of the present invention, any deterioration of the switching TFTs to be switched on in accordance with a light emission control signal can be minimized. A detailed configuration of the pixel P of the present invention will be described later in detail with reference to FIG. 3.

[0024] The TFTs constituting the pixel P may be implemented as oxide TFTs each including an oxide semiconductor layer. When electron mobility, process deviation, etc are all considered, the oxide TFTs are advantageous for a large-sized display panel 10. However, the present invention is not limited thereto, but the semiconductor layers of the TFTS may be formed of amorphous silicon, polysilicon, etc. Although the following detailed description is made with respect to an n-type TFT, the present invention is also applicable to a p-type TFT.

[0025] The timing controller 11 re-aligns digital video data RGB input from an external system board in accordance with the resolution of the display panel 10 to supply to the data driving circuit 12. And, the timing controller 11 generates a data timing control signal DDC for controlling an operating timing of the data driving circuit 12 and a gate timing control signal GDC for controlling an operating timing of the gate driving circuit 13 based on timing signals including a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a dot clock signal DCL, and a data enable signal DE.

[0026] The data driving circuit 12 converts the digital video data RGB input from the timing controller 11 based on the data control signal DDC into an analog data voltage and supplies it to the data lines 14.

[0027] The gate driving circuit 13 generates a scan signal, a light emission signal, and an initialization signal based on the gate control signal GDC. The gate driving circuit 13 supplies scan signals to the scan lines 15a in a line-sequential manner, supplies light emission control signals to the emission lines 15b in a line-sequential manner, and supplies initialization signals to the initialization lines 15c in a line-sequential manner. The gate driving circuit 13 may be formed directly on the display panel 10 in a GIP (Gate-driver In Panel) manner.

[0028] FIG. 3 shows an example of the pixel P of FIG. 2.

[0029] Referring to FIG. 3, the pixel P according to one exemplary embodiment of the present invention comprises an OLED, a driving TFT (DT), first to fourth TFTs (ST1 to ST4), a compensation capacitor Cgss, and a storage capacitor Cst.

[0030] The OLED emits light by the driving current supplied from the driving TFT (DT). As shown in FIG. 1, multiple organic compound layers are formed between the anode and cathode of the OLED. The organic compound layers comprise a hole injection layer HIL, a hole transport layer a hole transport layer HTL, an emission layer EML, an electron transport layer ETL, and an electron injection layer EIL. The anode of the OLED is connected to a source electrode of the driving TFT (DT), and the cathode thereof is connected to an input terminal of low-potential cell driving voltage EVSS.

[0031] The driving TFT (DT) controls the driving current applied to the OLED by its gate-source voltage. The gate electrode of the driving TFT (DT) is connected to node B, the drain electrode thereof is connected to an input terminal of high-potential cell driving voltage EVDD, and the source electrode thereof is connected to node C.

[0032] The first switching TFT (ST1) switches the current path between node A and node B in response to a light emission control signal EM. The first switching TT (ST1) is turned to transmit the data voltage Vdata stored in node A to node B. The gate electrode of the first switching TFT (ST1) is connected to the emission line 15b, its drain electrode is connected to node A, and its source electrode is connected to node B.

[0033] The second switching TFT (ST2) switches the current path between an input terminal of initialization voltage Vinit and node C. The second switching TFT (ST2) is turned on to supply an initialization voltage Vinit to node C. The gate electrode of the second switching TFT (ST2) is connected to the initialization line 15c, its drain electrode is connected to the input terminal of initialization voltage Vinit, and its source electrode is connected to node C.

[0034] The third switching TFT (ST3) switches the current path between an input terminal of reference voltage Vref and node B in response to an initialization signal INIT. The third switching TFT (ST3) is turned on to supply a reference voltage Vref to node B. The gate electrode of the third switching TFT (ST3) is connected to the initialization line 15c, its drain electrode is connected to the input terminal of reference voltage Vref, and its source electrode is connected to node B.

[0035] The fourth switching TFT (ST4) switches the current path between the data line 14 and node A in response to a san signal SCAN. The fourth switching TFT (ST4) is turned on to supply a data voltage Vdata to node A. The gate electrode of the fourth switching TFT is connected to the scan lines 15a, its drain electrode is connected to the data line 14, and its source electrode is connected to node A.

[0036] The compensation capacitor Cgss is connected between node B and node C. The compensation capacitor Cgss enables the source-follower method upon detecting the threshold voltage of the driving TFT (DT).

[0037] The storage capacitor Cst is connected between node A and node B. The storage capacitor Cst functions to store the data voltage Vdata input into node A and then transmit it to node B.

[0038] FIG. 4 is a waveform diagram showing signals EM, SCAN, INIT, and DATA applied to the pixel P of FIG. 3, potential changes of nodes A, B, and C responsive to these signals, and changes in the current flowing through the driving TFT (DT) and the OLED. FIGS. 5a to 5e show equivalent circuits of the pixel P in an initialization period Ti, a sensing period TS, a programming period Tp, and first and second emission periods Te1 and Te2, respectively. In FIGS. 5a to 5e, the activation of the elements is indicated by solid lines, and the deactivation of the elements is indicated by dotted lines.

[0039] Referring to FIG. 4, the operation of the pixel P according to the present invention is divided into an initialization period Ti for initializing nodes A, B, and C to a specific voltage, a sensing period Ts for detecting and storing the threshold voltage of the driving TFT (DT), a programming period Tp for applying a data voltage Vdata, and an emission period Te for compensating the driving current applied to the OLED using the threshold voltage and the data voltage Vdata, regardless of the threshold voltage. The emission period Te is subdivided into first and second emission periods Te1 and Te2.

[0040] Referring to FIG. 4 and FIG. 5a, the second switching TFT (ST2) is turned on in response to an initialization signal INIT of ON level in the initialization period Ti to supply an initialization voltage Vinit to node C, and the third switching TFT (ST3) is turned on in response to the initialization signal INIT of ON level to supply a reference voltage Vref to node B. The first switching TFT (ST1) is turned on in response to a light emission control signal EM of ON level to supply the reference voltage Vref to node A. The fourth switching TFT (ST4) is turned off in response to a scan signal SCAN of OFF level. The reference voltage Vref is set higher than the initialization voltage Vinit to make the driving TFT (DT) conductive. Also, the initialization voltage Vinit is set to an appropriate low value to prevent the light emission of the OLED in the other periods Ti, Ts, and Tp than the emission period Te. For example, if the high-potential cell driving voltage EVDD is set to 20 V, and the low-potential cell driving voltage EVSS is set to 0 V, the reference voltage Vref and the initialization voltage Vinit may be set to -1 V and -5 V, respectively.

[0041] In the initialization period Ti, nodes A and B are charged with the reference voltage Vref, and node C is charged with the initialization voltage Vinit. During the initialization period Ti, the gate-source voltage of the driving TFT (DT) is higher than the threshold voltage. Therefore, the driving TFT (DT) is turned on, and the current Idt flowing through the driving TFT (DT) has an appropriate initialization value.

[0042] Referring to FIG. 4 and FIG. 5b, in the sensing period Ts, the first switching TFT (ST1) is turned off by the light emission control signal EM of OFF level, the second and third switching TFTs (ST2 and ST3) are turned off by the initialization signal INIT of OFF level, and the fourth switching TFT (ST4) is turned off by the scan signal SCAN of OFF level.

[0043] In the sensing period Ts, the voltage of node C rises as the supply of the initialization voltage Vinit is stopped, and a result the current Idt flowing through the driving TFT (DT) gradually decreases. When the gate-source voltage of the driving TFT (DT) reaches the threshold voltage Vth, the driving TFT (DT) is turned off. At this point, the threshold voltage Vth of the driving TFT (DT) is detected in the source-follower method, and reflected on the potential of node C. In the present invention, even an threshold voltage Vth having a positive value, as well as a negative value, can be detected according to the source-follower method, regardless of whether the driving TFT is an n-type TFT or p-type TFT. The potential of node C rises from the initialization voltage Vinit up to "(Vref-Vth)+α" (hereinafter, referred to as an "intermediate source voltage"). In the sensing period Ts, node B is allowed to float. In this case, when the potential of node C rises to the "intermediate source voltage"), the potential of node B also rises to "Vref+α" (hereinafter, referred to as an "intermediate gate voltage") due to a capacitor coupling effect. "α" included in the "intermediate source voltage" and "intermediate gate voltage" is an amplification compensation factor, which increases in proportion to the threshold voltage of the driving TFT (DT). An additional increase in the potentials of both nodes B and C plays an important role in improving the accuracy of compensation of the threshold voltage Vth in a subsequent emission period Te. "α" on which the threshold voltage compensation capability depends on is a design value which is set in consideration of distortion of threshold voltage compensation caused by a kick-back voltage. The value of "α" can be adjusted by a parasitic capacitor of the driving TFT (DT) and the compensation capacitor Cgss. By properly adjusting the value of "α", the threshold voltage Vth can be efficiently compensated for without being affected by the parasitic capacitor of the driving TFT (DT). This will be described later in FIG. 6. The threshold voltage Vth of the driving TFT (DT) detected in the sensing period Ts is stored and maintained in node C by the compensation capacitor Cgss. The threshold voltage Vth of the driving TFT (DT) stored and maintained in node C may have a negative voltage value of "-Vth".

[0044] Referring to FIG. 4 and FIG. 5c, in the programming period Tp, the fourth switching TFT (ST4) is turned on by a scan signal SCAN of ON level to supply a data voltage Vdata to node A. The first switching TFT (ST1) is turned off by the light emission signal EM of OFF level, and the second and third switching TFTs (ST2 and ST3) are turned off by the initialization signal INIT of OFF level. In the programming period Tp, nodes B and C are separated from node A by a TFT or capacitor, and therefore maintains nearly the same potential as that in the sensing period Ts (although the potential is slightly changed due to the capacitor coupling effect, but almost ignorable).

[0045] Referring to FIG. 4 and FIG. 5d, in the first emission period Te1, the first switching TFT (ST1) is turned on by the light emission period of ON level to transmit the data voltage Vdata charged in node A to node B. The second and third switching TFTs (ST2 and ST3) are turned off by the initialization signal INIT of OFF level, and the fourth switching TFT (ST4) is turned off by the scan signal SCAN of OFF level.

[0046] In the first emission period Te1, the driving TFT (DT) is turned on by the data voltage Vdata transmitted to node B. The current Idt flowing through the driving TFT (DT) causes the potential of node C to increase to "Voled" by which the OLED is made conductive, and as a result, the OLED is turned on. When the OLED is turned on, the currents Iddt and Ioled flowing through the OLED and the driving TFT (DT) become equal. When the first driving current IOlde1 flows through the OLED, the potential of node C is boosted to "Voled" (hereinafter, referred to as a "first final source voltage"), and the potentials of nodes A and B are all boosted to a*Vth+b*Vdata+Voled+C" (hereinafter, referred to as a "first final gate voltage"). In the first final gate voltage, "a" multiplied by the threshold voltage Vth is a constant affected by parasitic capacitors (Cgs and Cgd of FIG. 6) of the driving TFT (DT), which is ideally "1", but actually "less than 1" because of the parasitic capacitors. In this case, in the equation of the first driving current Iolde1, the factors of the threshold voltage Vth are not completely compensated for, as shown in β/2 (Vgs-Vth)2 = β/2 (a*Vth+b*Vdata+C-Vth)2, whereby the threshold voltage compensation capability is lowered. To completely compensate for the threshold voltage, "a" multiplied by the threshold voltage Vth has to be 1. In the present invention, "a" multiplied by the threshold voltage Vth becomes 1 by properly selecting the amplification compensation factor "α" included in the intermediate source voltage" and the intermediate gate voltage". By this, the present invention can improve the threshold voltage compensation capability. In the above equation, "β" denotes a constant determined by the mobility of the driving TFT (DT), a parasitic capacitance, and a channel size, "Vgs" denotes the gate-source voltage of the driving TFT (DT), "b" denotes a distribution coefficient caused by the compensation capacitor Cgss, the storage capacitor Cst, and the parasitic capacitor of the driving TFT (DT), and "C" denotes a constant for simplifying the equation of the first final source voltage.

[0047] Referring to FIG. 4 and FIG. 5e, in the second emission period Te2, the first switching TFT (ST1) is turned off by the light emission control signal EM of OFF level, the second and third switching TFTs (ST2 and ST3) are turned off by the initialization signal INIT of OFF level, and the fourth switching TFT (ST4) is turned off by the scan signal SCAN of off level.

[0048] The second emission period Te2 is a period required to prevent deterioration of the first switching TFT (ST1) to which the light emission control signal EM is applied. To this end, the light emission control signal EM is maintained at the OFF level during the second emission period Te2, unlike the conventional art. Since it is maintained at the OFF level in the second emission period Te2, the light emission control signal EM has a first pulse P1 corresponding to the initialization period Ti and a second pulse P2 corresponding to the first emission period Te1. A proportion that the second emission period TE2 occupies in one frame is much larger than those of the other periods Ti, Ts, Tp, and Te1. Since the first switching TFT (ST1) is kept turned off in the second emission period Te2, it is free of any degradation caused by a gate bias stress.

[0049] When the first switching TFT (ST1) is turned off in the second emission period T32, the potentials of nodes B and C (needless to say, the potential of node A also changes) are reduced to a second final gate voltage "X" and a second final source voltage "Y", respectively. At this point, compensation of the driving TFT (DT) is maintained the same as that in the first emission period T31, and the currents Idt and Ioled flowing through the OLED and the driving TFT (DT) become equal, that is, the second driving current Ioled2. The gray scale of the pixel is determined by integral values of the first and second driving currents Ioled1 and Ioled2.

[0050] FIG. 6 shows a design method of a driving TFT (DT) for improving the threshold voltage compensation capability.

[0051] Referring to FIG. 6, a first parasitic capacitor Cgs is formed between the gate and source of the driving TFT (DT), and a second parasitic capacitor Cgs is formed between the gate and drain of the driving TFT (DT). In the present invention, the capacitance of the compensation capacitor Cgss and first parasitic capacitor Cgs connected in parallel and the capacitance of the second parasitic capacitor Cgd connected in series to these capacitors Cgss and Cgs can be adjusted in order to improve the threshold voltage compensation capability. By adjusting the capacitances of the above-mentioned capacitors, the above-described "α" on which the threshold voltage compensation capability depends is determined. In the present invention, the design size of the first and second parasitic capacitors Cgs and Cgd, in addition to the design size of the compensation capacitor Cgss, can be adjusted. Moreover, in the present invention, an adjustment capacitor Cgds may be further formed between the gate and drain of the driving TFT (DT), in order to supplement the capacitance of the second parasitic capacitor Cgd, if required.

[0052] FIG. 7 shows another example of the pixel P of FIG. 2.

[0053] Referring to FIG. 7, the pixel P according to another exemplary embodiment of the present invention comprises an OLED, a driving TFT (DT), first to fourth switching TFTs (ST1 to sT2), a compensation capacitor Cgss, and a storage capacitor Cst.

[0054] The pixel P according to another exemplary embodiment of the present invention is identical to that of FIG. 2, except for a connection structure of the third switching TFT (ST3). Unlike in FIG. 2, the third switching TFT (ST3) of FIG. 7 switches the current path between the input terminal of reference voltage Vref and node A in response to the initialization signal INIT. The third switching TFT (ST3) is turned on to supply the reference voltage to not node B but node A. Even if the reference voltage Vref is supplied to node A in the initialization perid, the first switching TFT (St1) is turned on during the initialization period to transmit the reference voltage Vref of node A to node B. Accordingly, the operation of the pixel P of FIG. 7 is substantially identical to the pixel P of FIG. 2, regarding the sensing period, the programming period, and the emission period.

[0055] FIG. 8 shows a driving waveform of a gate signal suggested in the present invention, as compared to the conventional art. FIG. 9 shows the progress of threshold voltage degradation in accordance with the on duty of the gate signal.

[0056] Referring to (a) of FIG. 8, in a conventional pixel circuit, an EM TFT is connected between a driving TFT (DT) and an OLED to control light emission of the OLED. In the conventional art, SW TFTs are turned on prior to an emission period and turned off in the emission period, whereas the EM TFT is turned only during the emission period. The emission period is relatively much longer than the other periods, and an ON-level light emission control signal is applied to the gate of the EM TFT during the entire emission period. It is inevitable that the EM TFT is further deteriorated than the SW TFTs, due to a positive bias stress applied for a long time.

[0057] Referring to (b) of FIG. 8, in the pixel circuit of the present invention, only the driving TFT (DT) and the OLED are serially connected between input terminals of cell driving voltages EVDD and EVSS, and the conventional EM TFT is not connected between these input terminals EVDD and EVSS. A light emission control signal is applied to the first switching TFT (ST1) for transmitting a data voltage to induce light emission, as explained above, and is in the form of two pulses. The first switching TFT (ST1) is turned on by first and second pulses P1 and P2 having the ON level respectively corresponding to the initialization period and the first emission period. Since the first switching TFT (ST1) is turned off in response to an OFF-level light emission control signal in the second emission period, deterioration of the first switching TFT (ST1) caused by a positive gate bias stress is greatly reduced. Even if the first switching TFT (ST1) is turned off in the second emission period, the condition of light emission of the first emission period is kept nearly the same due to the compensation capacitor connected between the gate and source of the driving TFT. Meanwhile, the OFF period of all the TFTs including the first switching TFT (ST1) in one frame is much longer than the ON period thereof. However, the absolute value of the off voltage level of gate signals is much smaller than the absolute value of the on voltage level thereof. Thus, any problem caused by a negative bias stress is not significant and also ignorable.

[0058] The progress of deterioration of the threshold voltage of a TFT in accordance with the on duty of a gate signal is as shown in FIG. 9. Referring to FIG. 9, if the frame frequency is 120 Hz, 1 frame period is approximately 8.3 msec. According to a test, it was found that the on duty of a gate signal (especially, light emission control signal) within one frame may be set to approximately 5% or less, the effect of preventing threshold voltage deterioration becomes larger as the on duty of the gate signal is set to a lower level within a predetermined range. For example, as shown in FIG. 9, if the on duty of the light emission control signal is set to 2%, the threshold voltage of the TFT operated by the light emission control signal gradually rises and becomes deteriorated with the elapse of driving time. On the other hand, if the on duty of the light emission control signal is set to 0.1 %, the threshold voltage of the TFT is maintained nearly constant in spite of the elapse of driving time. IN the present invention, the ON period of the first pulse of FIG. 4 can be further reduced within the on period of the initialization signal to reduce the on duty of the light emission control signal as much as possible.

[0059] FIG. 10 shows the result of simulation of the threshold voltage compensation performance of the pixel suggested in the present invention.

[0060] Referring to FIG. 10, according to the pixel circuit of the present invention, the threshold voltage compensation performance ranges from -2V to 4V, and the compensation range can be shifted, increased, or decreased according to power settings and how much the TFT and capacitor sizes are optimized. Especially, the threshold voltage compensation technique suggested in the present invention exhibits an excellent compensation performance even in low gray levels (63gray), as shown in FIG. 10.

[0061] As described above, the organic light emitting display and driving method thereof according to the present invention has the following effects to overcome the problems occurring in the conventional art.

[0062] First, while the conventional compensation circuit method is limited to when the threshold voltage of a driving TFT has a positive value (or negative value), the present invention can detect a threshold voltage having a negative value, as well as a threshold voltage having a positive value, regardless of whether the TFT is the n-type or p-type by employing the source-follower method.

[0063] Second, in the conventional compensation circuit method a fixed potential is applied to the gate of the driving TFT upon sensing a threshold voltage; whereas, in the present invention, the gate of the driving TFT is allowed to float upon sensing a threshold voltage, and the threshold voltage compensation capability is improved by using the compensation capacitor connected between the gate and source of the driving TFT and a parasitic capacitor of the driving TFT. The present invention increases the accuracy of threshold voltage compensation by additionally amplifying the gate-source voltage of the driving TFT upon detecting a threshold voltage in consideration of distortion of threshold voltage compensation caused by the parasitic capacitor

[0064] Third, while, in the conventional compensation circuit, the light emission control TFT which is turned on during the entire emission period is easily deteriorated; whereas, in the present invention, deterioration of the switching TFTs to be switched in response to a gate signal can be minimized by minimizing the on duty of gate signals (especially, a light emission control signal). The present invention can enhance the reliability of the switching TFTS by minimizing deterioration caused by a gate bias stress.

[0065] Throughout the description, it should be understood for those skilled in the art that various changes and modifications are possible without departing from the technical principles of the present invention. Therefore, the technical scope of the present invention is not limited to those detailed descriptions in this document but should be defined by the scope of the appended claims.

Claims

1. An organic light emitting display comprising:

a display panel (10) having pixels (P) disposed in a matrix form at crossing regions of data lines (14) and gate line portions (15); a data driving circuit (12) configured to drive the data lines (14); and

a gate driving circuit (13) configured to drive a scan line (15a), an emission line (15b), and an initialization line (15c) of each gate line portion (15), wherein each of the pixels (P) comprises:

an organic light emitting diode (OLED);

a driving TFT (DT) configured to control the current applied to the organic light emitting diode (OLED), said driving TFT comprising a gate connected to a node B, a drain connected to an input terminal of high-potential cell driving voltage (EVDD), and a source connected to the organic light emitting diode through a node C; a first switching TFT (ST1) configured to switch the current path between a node A and the node B in response to a light emission control signal (EM) supplied from the emission line (15b);

a second switching TFT (ST2) configured to initialize the node C to an initialization voltage (Vinit) in response to an initialization signal (INIT) supplied from the initialization line (15c);

a third switching TFT (ST3) configured to initialize either the node A or the node B to a reference voltage (Vref) higher than the initialization voltage (Vinit) in response to the initialization signal (INIT);

a fourth switching TFT (ST4) configured to switch the current path between a data line (14) and the node A in response to a scan signal (SCAN) supplied from the scan line (15a);

a compensation capacitor (Cgss) connected between the node B and the node C; and a storage capacitor (Cst) connected between the node A and the node C,

wherein the gate driving circuit (13) is configured to:

turn on the driving TFT (DT) in an initialization period (Ti) of one frame period to enable an initial current flow through the driving TFT (DT) by:

supplying an ON level of the initialization signal (INIT) to the initialization line (15c) in order to turn on the second switching TFT (ST2) to

thereby charge node C with the initialization voltage (Vinit) in the initialization period (Ti) and in order to turn on the third switching TFT (ST3) to thereby supply the reference voltage (Vref) to the node B in the initialization period (Ti);
supplying an ON level of the light emission control signal (EM) to the emission line (15b) in order to turn on the first switching TFT (ST1) in the initialization period (Ti): and supplying an OFF level of the scan signal (SCAN) to the scan line (15a) to turn off the fourth switching TFT (ST4) in the initialization period (Ti)
and wherein the gate driving circuit is configured to allow the node B to float in a subsequent sensing period (Ts) of the frame period for detecting and storing a threshold voltage (Vth) of the driving TFT (DT) by:

supplying an OFF level of the light emission control signal (EM) to turn off the first switching TFT (ST1) in the subsequent sensing period (Ts);
supplying an OFF level of the initialization signal (INIT) to turn off the second switching TFT (ST2) and the third switching TFT (ST3) in the subsequent sensing period (Ts);
supplying an OFF level of the scan signal (SCAN) to turn off the fourth switching TFT (ST4) in the subsequent sensing period (Ts).

2. The organic light emitting display of claim 1, wherein the one frame period is divided into the initialization period (Ti) for initializing the nodes A, B, and C, the sensing period (Ts), a programming period (Tp) for applying the data voltage, and an emission period (Te) for compensating the driving current applied to the organic light emitting diode using the threshold voltage and the data voltage, regardless of the threshold voltage.

3. The organic light emitting display of claim 2, wherein, in the sensing period (Ts), the potential of the node C rises to an intermediate source voltage, which is obtained by adding a value obtained by subtracting the threshold voltage (Vth) from the reference voltage (Vref) and an amplification compensation factor (α) for preventing distortion of the threshold voltage, and the potential of the node B rises to an intermediate gate voltage (Vref+α), which is obtained by adding the reference voltage (Vref) and the amplification compensation factor (α).

4. The organic light emitting display of claim 3, wherein the value of the amplification compensation factor (α) is adjusted by a parasitic capacitor of the driving TFT.

5. The organic light emitting display of claim 3, wherein an adjustment capacitor (Cgds) for adjusting the value of the amplification compensation factor (α) is further connected between the node B and the input terminal of high-potential cell driving voltage (EVDD).

6. The organic light emitting display of claim 2, the light emission control signal (EM) comprises a first pulse (P1) having the ON level corresponding to the initialization period (Ti) and a second pulse (P2) having the ON level partially corresponding to the emission period (Te).

7. The organic light emitting display of claim 6, wherein the emission period (Te) comprises a first emission period (Te1) for applying a first driving current (Ioled1) to the organic light emitting diode and a second emission period (Te2) for applying a second driving current (Ioled2), which is lower than the first driving current, to the organic light emitting diode, the second emission period (Te2) being longer than the first emission period (Te1).

8. The organic light emitting display of claim 6, wherein the ON period of the first pulse is set shorter than the on period of the initialization period (Ti) within the on period of the initialization signal.

9. The organic light emitting display of claim 1, wherein a gate electrode of the third switching TFT (ST3) is connected to a signal line to which the initialization signal (INIT) is supplied, one electrode of the third switching TFT is connected to an input terminal of the reference voltage, and the other electrode of the third switching TFT is connected to either the node A or the node B.

10. A driving method of an organic light emitting display comprising a data driving circuit (12), a gate driving circuit(13) and a plurality of pixels, each pixel (P) comprising an organic light emitting diode (OLED), a driving TFT (DT) comprising a gate connected to a node B, a drain connected to an input terminal of high-potential cell driving voltage (EVDD), and a source connected to the organic light emitting diode through a node C, and for controlling the current applied to the organic light emitting diode, a first switching TFT (ST1 configured to switch the current path between a node A and the node B in response to a light emission control signal (EM), a second switching TFT (ST2) configured to initialize the node C to an initialization voltage (Vinit) in response to an initialization signal (INIT), a third switching TFT (ST3) configured to initialize either the node A or the node B to a reference voltage (Vref) higher than the initialization voltage (Vinit) in response to the initialization signal (INIT), a fourth switching TFT (ST4) configured to switch the current path between a data line (14) and the node A in response to a scan signal (SCAN), a compensation capacitor (Cgss) connected between the node B and the node C, and a storage capacitor (Cst) connected between the node A and the node C, the method comprising the steps of:

turning on the driving TFT (DT) in an initialization period (Ti) of one frame period to enable an initial current flow through the driving TFT (DT) by:

supplying an ON level of an initialization signal (INIT) generated by the gate driving circuit (13) to charge the node C with the initialization voltage (Vinit) in the initialization period (Ti), and to charge the node B to a reference voltage (Vref) higher than the initialization voltage (Vinit) in response to the initialization signal (INIT) and the light emission control signal (EM) generated by the gate driving circuit (13) in an initialization period (Ti) of one frame period by turning on the second switching TFT (ST2) and the third switching TFT (ST3) to supply the initialization voltage (Vinit) to the node C and the reference voltage (Vref) to the node B in the initialization period (Ti);
supplying an ON level of the light emission control signal (EM) to the emission line (15b) to turn on the first switching TFT (ST1) in the initialization period (Ti);
supplying an OFF level of the scan signal (SCAN) generated by the gate driving circuit (13) to the scan line (15a) to turn off the fourth switching TFT (ST4) in the initialization period (Ti) and in a subsequent sensing period (Ts); supplying an OFF level of the light emission control signal (EM) to turn off the first switching TFT (ST1) in the subsequent sensing period (Ts);
supplying an OFF level of the initialization signal (INIT) to turn off the second switching TFT (ST2) and the third switching TFT (ST3) in the subsequent sensing period (Ts) in order to stop the supply of the initialization voltage (Vinit) and thereby allowing the node B to float in the subsequent sensing period (Ts) of the frame period, and then detecting and storing a threshold voltage (Vth) of the driving TFT by using the compensation capacitor (Cgss); applying after the subsequent sensing period (Ts) a data voltage supplied by the data driving circuit (12) to the node A connected to the storage capacitor in response to the scan signal; and
transmitting the data voltage of the node A to the node B in response to the light emission control signal (EM) to compensate for the driving current applied to the organic light emitting diode, regardless of the threshold voltage, and causing the organic light emitting diode to emit light.

11. The method of claim 10, wherein, in the detecting and storing of the threshold voltage (Vth), the potential of the node C rises to an intermediate source voltage, which is obtained by adding a value obtained by subtracting the threshold voltage (Vth) from the reference voltage (Vref) and an amplification compensation factor (α) for preventing distortion of the threshold voltage, and the potential of the node B rises to an intermediate gate voltage (Vref+α), which is obtained by adding the reference voltage (Vref) and the amplification compensation factor (α).

12. The method of claim 11, wherein the value of the amplification compensation factor (α) is adjusted by a parasitic capacitor of the driving TFT.

13. The method of claim 10, wherein the light emission control signal comprises a first pulse (P1) having the ON level corresponding to the initialization period and a second (P2) pulse having the ON level partially corresponding to the emission period (Te).

14. The method of claim 10, wherein the organic light emitting diode emits light in an emission period (Te); and
wherein the emission period (Te) comprises a first emission period (Te1) in which the organic light emitting diode emits light by a first driving current (Ioled1) and a second emission period (Te2) in which the organic light emitting diode emits light by a second driving current (Ioled2), the second emission period (Te2) being longer than the first emission period (Te1).

Patentansprüche

1. Organische lichtemittierende Anzeige, die Folgendes umfasst:

eine Anzeigetafel (10) mit Pixeln (P), die in einer Matrixform an Kreuzungsbereichen von Datenleitungen (14) und Gate-Leitungsteilen (15) angeordnet sind;
eine Datenansteuerungsschaltung (12), die konfiguriert ist, die Datenleitungen (14) anzusteuern; und
eine Gate-Ansteuerungsschaltung (13) die konfiguriert ist, eine Abtastleitung (15a), eine Emissionsleitung (15b) und eine Initialisierungsleitung (15c) jedes Gate-Leitungsteils (15) anzusteuern,
wobei jedes der Pixel (P) umfasst:

eine organische Leuchtdiode (OLED);
einen Ansteuerungs-TFT (DT), der konfiguriert ist, den an die organische Leuchtdiode (OLED) angelegten Strom zu steuern, wobei der Ansteuerungs-TFT ein Gate, das mit einem Knoten B verbunden ist, einen Drain, der mit einem Eingangsanschluss einer Hochpotenzialzellenansteuerungsspannung (EVDD) verbunden ist, und eine Source, die mit der organischen Leuchtdiode durch einen Knoten C verbunden ist, umfasst;
einen ersten Schalt-TFT (ST1), der konfiguriert ist, den Stromweg zwischen einem Knoten A und dem Knoten B als Reaktion auf ein von der Emissionsleitung (15b) geliefertes Lichtemissionssteuersignal (EM) zu wechseln;
einen zweiten Schalt-TFT (ST2), der konfiguriert ist, den Knoten C als Reaktion auf ein von der Initialisierungsleitung (15c) geliefertes Initialisierungssignal (INIT) auf eine Initialisierungsspannung (Vinit) zu initialisieren;
einen dritten Schalt-TFT (ST3), der konfiguriert ist, entweder den Knoten A oder den Knoten B als Reaktion auf das Initialisierungssignal (INIT) auf eine Referenzspannung (Vref), die größer als die Initialisierungsspannung (Vinit) ist, zu initialisieren;
einen vierten Schalt-TFT (ST4), der konfiguriert ist, den Stromweg zwischen einer Datenleitung (14) und dem Knoten A als Reaktion auf ein von der Abtastleitung (15a) geliefertes Abtastsignal (SCAN) zu wechseln;
einen Kompensationskondensator (Cgss), der zwischen den Knoten B und den Knoten C geschaltet ist; und
einen Speicherkondensator (Cst), der zwischen den Knoten A und den Knoten C geschaltet ist,
wobei die Gate-Ansteuerungsschaltung (13) konfiguriert ist:

den Ansteuerungs-TFT (DT) in einer Initialisierungsperiode (Ti) einer Rahmenperiode einzuschalten, um zu ermöglichen, dass ein Anfangsstrom durch den Ansteuerungs-TFT (DT) fließt, durch:

Liefern eines EIN-Pegels des Initialisierungssignals (INIT) an die Initialisierungsleitung (15c), um den zweiten Schalt-TFT (ST2) einzuschalten, um dadurch den Knoten C mit der Initialisierungsspannung (Vinit) in der Initialisierungsperiode (Ti) zu laden, und um den dritten Schalt-TFT (ST3) einzuschalten, um dadurch die Referenzspannung (Vref) in der Initialisierungsperiode (Ti) an den Knoten B zu liefern;
Liefern eines EIN-Pegels des Lichtemissionssteuersignals (EM) an die Emissionsleitung (15b), um den ersten Schalt-TFT (ST1) in der Initialisierungsperiode (Ti) einzuschalten; und
Liefern eines AUS-Pegels des Abtastsignals (SCAN) an die Abtastleitung (15a), um den vierten Schalt-TFT (ST4) in der Initialisierungsperiode (Ti) auszuschalten,

und wobei die Gate-Ansteuerungsschaltung konfiguriert ist,
dem Knoten B zu erlauben, in einer folgenden Erfassungsperiode (Ts) der Rahmenperiode zum Detektieren und Speichern einer Schwellenspannung (Vth) des Ansteuerung-TFT (DT) zu schweben durch:

Liefern eines AUS-Pegels des Lichtemissionssteuersignals (EM), um den ersten Schalt-TFT (ST1) in der folgenden Erfassungsperiode (Ts) auszuschalten;
Liefern eines AUS-Pegels des Initialisierungssignals (INIT), um den zweiten Schalt-TFT (ST2) und den dritten Schalt-TFT (ST3) in der folgenden Erfassungsperiode (Ts) auszuschalten;
Liefern eines AUS-Pegels des Abtastsignals (SCAN), um den vierten Schalt-TFT (ST4) in der folgenden Erfassungsperiode (Ts) auszuschalten.

2. Organische lichtemittierende Anzeige nach Anspruch 1, wobei die eine Rahmenperiode in die Initialisierungsperiode (Ti) zum Initialisierung der Knoten A, B und C, in die Erfassungsperiode (Ts), in eine Programmierperiode (Tp) zum Anlegen der Datenspannung und in eine Emissionsperiode (Te) zum Kompensieren des an die organische Leuchtdiode angelegten Ansteuerungsstroms unter Verwendung der Schwellenspannung und der Datenspannung ungeachtet der Schwellenspannung unterteilt ist.

3. Organische lichtemittierende Anzeige nach Anspruch 2, wobei in der Erfassungsperiode (Ts) das Potenzial des Knotens C auf eine intermediäre Source-Spannung ansteigt, die durch Addieren eines durch Subtrahieren der Schwellenspannung (Vth) von der Referenzspannung (Vref) erhaltenen Werts und eines Verstärkungskompensationsfaktors (α) zum Verhindern einer Verzerrung der Schwellenspannung erhalten wird, und das Potenzial des Knotens B auf eine intermediäre Gate-Spannung (Vref + α) ansteigt, die durch Addieren der Referenzspannung (Vref) und des Verstärkungskompensationsfaktors (α) erhalten wird.

4. Organische lichtemittierende Anzeige nach Anspruch 3, wobei der Wert des Verstärkungskompensationsfaktors (α) durch einen parasitären Kondensator des Ansteuerungs-TFT angepasst wird.

5. Organische lichtemittierende Anzeige nach Anspruch 3, wobei ferner zwischen den Knoten B und den Eingangsanschluss der Hochpotenzialzellenansteuerungsspannung (EVDD) ein Anpassungskondensator (Cgds) zum Anpassen des Werts des Verstärkungskompensationsfaktors (α) geschaltet ist.

6. Organische lichtemittierende Anzeige nach Anspruch 2, wobei das Lichtemissionssteuersignal (EM) einen ersten Impuls (P1) mit dem EIN-Pegel, der der Initialisierungsperiode (Ti) entspricht, und einen zweiten Impuls (P2) mit dem EIN-Pegel, der teilweise der Emissionsperiode (Te) entspricht, umfasst.

7. Organische lichtemittierende Anzeige nach Anspruch 6, wobei die Emissionsperiode (Te) eine erste Emissionsperiode (Te1) zum Anlegen eines ersten Ansteuerungsstroms (Ioled1) an die organische Leuchtdiode und eine zweite Emissionsperiode (Te2) zum Anlegen eines zweiten Ansteuerungsstroms (Ioled2), der kleiner als der erste Ansteuerungsstrom ist, an die organische Leuchtdiode umfasst, wobei die zweite Emissionsperiode (Te2) länger als die erste Emissionsperiode (Te1) ist.

8. Organische lichtemittierende Anzeige nach Anspruch 6, wobei die EIN-Periode des ersten Impulses kürzer als die EIN-Periode der Initialisierungsperiode (Ti) innerhalb der EIN-Periode des Initialisierungssignals eingestellt ist.

9. Organische lichtemittierende Anzeige nach Anspruch 1, wobei eine Gate-Elektrode des dritten Schalt-TFT (ST3) mit einer Signal-Leitung verbunden ist, an die das Initialisierungssignal (INIT) geliefert wird, eine Elektrode des dritten Schalt-TFT mit einem Eingangsanschluss der Referenzspannung verbunden ist und die andere Elektrode des dritten Schalt-TFT entweder mit dem Knoten A oder dem Knoten B verbunden ist.

10. Ansteuerungsverfahren einer organischen lichtemittierenden Anzeige, die eine Datenansteuerungsschaltung (12), eine Gate-Ansteuerungsschaltung (13) und mehrere Pixel umfasst, wobei jedes Pixel (P) eine organische Leuchtdiode (OLED), einen Ansteuerungs-TFT (DT), der ein Gate, das mit einem Knoten B verbunden ist, einen Drain, der mit einem Eingangsanschluss einer Hochpotenzialzellenansteuerungsspannung (EVDD) verbunden ist, und eine Source, die mit der organischen lichtausendenden Diode durch einen Knoten C verbunden ist, und zum Steuern des an die organische Leuchtdiode angelegten Stroms einen ersten Schalt-TFT (ST1), der konfiguriert ist, den Stromweg zwischen einem Knoten A und dem Knoten B als Reaktion auf ein Lichtemissionssteuersignal (EM) zu wechseln, einen zweiten Schalt-TFT (ST2), der konfiguriert ist, den Knoten C als Reaktion auf ein Initialisierungssignal (INIT) auf eine Initialisierungsspannung (Vinit) zu initialisieren, einen dritten Schalt-TFT (ST3), der konfiguriert ist, entweder den Knoten A oder den Knoten B als Reaktion auf das Initialisierungssignal (INIT) auf eine Referenzspannung (Vref), die höher als die Initialisierungsspannung ist, zu initialisieren, einen vierten Schalt-TFT (ST4), der konfiguriert ist, den Stromweg zwischen einer Datenleitung (14) und dem Knoten A als Reaktion auf ein Abtastsignal (SCAN) zu wechseln, einen Kompensationskondensator (Cgss), der zwischen dem Knoten B und dem Knoten C angeschlossen ist, und einen Speicherkondensator (Cst), der zwischen dem Knoten A und dem Knoten C angeschlossen ist, umfasst, wobei das Verfahren die folgenden Schritte umfasst:

Einschalten des Ansteuerungs-TFT (DT) in einer Initialisierungsperiode (Ti) einer Rahmenperiode, um zu ermöglichen, dass ein Anfangsstrom durch den Ansteuerungs-TFT (DT) fließt durch:

Liefern eines EIN-Pegels eines durch die Gate-Ansteuerungsschaltung (13) gelieferten Initialisierungssignals (INIT), um den Knoten C mit der Initialisierungsspannung

(Vinit) in der Initialisierungsperiode (Ti) zu laden und den Knoten B als Reaktion auf das Initialisierungssignal (INIT) auf eine Referenzspannung (Vref), die größer als die Initialisierungsspannung (Vinit) ist, und das durch die Gate-Ansteuerungsschaltung (13) erzeugte Lichtemissionssteuersignal (EM) in einer Initialisierungsperiode (Ti) einer Rahmenperiode durch Einschalten des zweiten Schalt-TFT (ST2) und des dritten Schalt-TFT (ST3), um die Initialisierungsspannung (Vinit) an den Knoten C und die Referenzspannung (Vref) an den Knoten B in der Initialisierungsperiode (Ti) zu liefern, zu laden;
Liefern eines EIN-Pegels des Lichtemissionssteuersignals (EM) an die Emissionsleitung (15b), um den ersten Schalt-TFT (ST1) in der Initialisierungsperiode (Ti) einzuschalten;
Liefern eines AUS-Pegels des durch die Gate-Ansteuerungsschaltung (13) erzeugten Abtastsignals (SCAN) an die Abtastleitung (15a), um den vierten Schalt-TFT (ST4) in der Initialisierungsperiode (Ti) und in einer folgenden Erfassungsperiode (Ts) auszuschalten;
Liefern eines AUS-Pegels des Lichtemissionssteuersignals (EM), um den ersten Schalt-TFT (ST1) in der folgenden Erfassungsperiode (Ts) auszuschalten;
Liefern eines AUS-Pegels des Initialisierungssignals (INIT), um den zweiten Schalt-TFT (ST2) und den dritten Schalt-TFT (ST3) in der folgenden Erfassungsperiode (Ts) auszuschalten, um die Versorgung mit der Initialisierungsspannung (Vinit) zu stoppen und dadurch dem Knoten B zu erlauben, in der folgenden Erfassungsperiode (Ts) der Rahmenperiode zu schweben, und dann Detektieren und Speichern einer Schwellenspannung (Vth) des Ansteuerungs-TFT durch Verwenden des Kompensationskondensators (Cgss);
Anwenden nach der folgenden Erfassungsperiode (Ts) einer durch die Datenansteuerungsschaltung (12) an den Knoten A, der mit dem Speicherkondensator verbunden ist, gelieferten Datenspannung als Reaktion auf das Abtastsignal; und
Senden der Datenspannung des Knotens A an den Knoten B als Reaktion auf das Lichtemissionssteuersignal (EM), um den an die organische Leuchtdiode angelegten Ansteuerungsstrom ungeachtet der Schwellenspannung zu kompensieren und Bewirken, dass die organische Leuchtdiode Licht aussendet.

11. Verfahren nach Anspruch 10, wobei beim Detektieren und Speichern der Schwellenspannung (Vth) das Potenzial des Knoten C auf eine intermediäre Source-Spannung ansteigt, die durch Addieren eines durch Subtrahieren der Schwellenspannung (Vth) von der Referenzspannung (Vref) erhaltenen Werts und eines Verstärkungskompensationsfaktors (α) zum Verhindern einer Verzerrung der Schwellenspannung erhalten wird, und das Potenzial des Knotens B auf eine intermediäre Gate-Spannung (Vref + α) ansteigt, die durch Addieren der Referenzspannung (Vref) und des Verstärkungskompensationsfaktors (α) erhalten wird.

12. Verfahren nach Anspruch 11, wobei der Wert des Verstärkungskompensationsfaktors (α) durch einen parasitären Kondensator des Ansteuerungs-TFT angepasst wird.

13. Verfahren nach Anspruch 10, wobei das Lichtemissionssteuersignal einen ersten Impuls (P1) mit dem EIN-Pegel, der der Initialisierungsperiode entspricht, und einen zweiten Impuls (P2) mit dem EIN-Pegel, der teilweise der Emissionsperiode (Te) entspricht, umfasst.

14. Verfahren nach Anspruch 10, wobei die organische Leuchtdiode Licht in einer Emissionsperiode (Te) aussendet; und
wobei die Emissionsperiode (Te) eine erste Emissionsperiode (Te1), in der die organische Leuchtdiode Licht durch einen ersten Ansteuerungsstrom (Ioled1) aussendet, und eine zweite Emissionsperiode (Te2), in der die organische Leuchtdiode Licht durch einen zweiten Ansteuerungsstrom (Ioled2) aussendet, umfasst, wobei die zweite Emissionsperiode (Te2) länger als die erste Emissionsperiode (Te1) ist.

Revendications

1. Affichage électroluminescent organique comprenant :

un panneau d'affichage (10) comportant des pixels (P) disposés sous forme de matrice à des régions d'intersection de lignes de données (14) et de portions de ligne de grille (15) ;
un circuit de commande de données (12) configuré pour commander les lignes de données (14) ; et
un circuit de commande de grille (13) configuré pour commander une ligne de balayage (15a), une ligne d'émission (15b), et une ligne d'initialisation (15c) de chaque portion de ligne de grille (15),
dans lequel chacun des pixels (P) comprend :

une diode électroluminescente organique (OLED) ;
un TFT de commande (DT) configuré pour réguler le courant appliqué à la diode électroluminescente organique (OLED), ledit TFT de commande comprenant une grille reliée à un noeud B, un drain relié à une borne d'entrée d'une tension de commande de cellule à haut potentiel (EVDD), et une source reliée à la diode électroluminescente organique par l'intermédiaire d'un noeud C ;
un premier TFT de commutation (ST1) configuré pour commuter la voie de courant entre un noeud A et le noeud B en réponse à un signal de régulation d'émission lumineuse (EM) fourni depuis la ligne d'émission (15b) ;
un deuxième TFT de commutation (ST2) configuré pour initialiser le noeud C à une tension d'initialisation (Vinit) en réponse à un signal d'initialisation (INIT) fourni depuis la ligne d'initialisation (15c) ;
un troisième TFT de commutation (ST3) configuré pour initialiser le noeud A ou le noeud B à une tension de référence (Vref) supérieure à la tension d'initialisation (Vinit) en réponse au signal d'initialisation (INIT) ;
un quatrième TFT de commutation (ST4) configuré pour commuter la voie de courant entre une ligne de données (14) et le noeud A en réponse à un signal de balayage (SCAN) fourni depuis la ligne de balayage (15a) ;
un condensateur de compensation (Cgss) relié entre le noeud B et le noeud C ; et
un condensateur de stockage (Cst) relié entre le noeud A et le noeud C,
dans lequel le circuit de commande de grille (13) est configuré pour :

mettre sous tension le TFT de commande (DT) au cours d'une période d'initialisation (Ti) d'une période de trame pour permettre un flux de courant initial à travers le TFT de commande (DT) par :

la fourniture d'un niveau d'activation du signal d'initialisation (INIT) à la ligne d'initialisation (15c) pour mettre sous tension le deuxième TFT de commutation (ST2) afin de charger de ce fait le noeud C avec la tension d'initialisation (Vinit) au cours de la période d'initialisation (Ti) et pour mettre sous tension le troisième TFT de commutation (ST3) afin de fournir de ce fait la tension de référence (Vref) au noeud B au cours de la période d'initialisation (Ti) ;
la fourniture d'un niveau d'activation du signal de régulation d'émission lumineuse (EM) à la ligne d'émission (15b) pour mettre sous tension le premier TFT de commutation (ST1) au cours de la période d'initialisation (Ti) ; et
la fourniture d'un niveau de désactivation du signal de balayage (SCAN) à la ligne de balayage (15a) pour mettre hors tension le quatrième TFT de commutation (ST4) au cours de la période d'initialisation (Ti) ; et

dans lequel le circuit de commande de grille est configuré pour :

permettre au noeud B de flotter au cours d'une période de détection (Ts) suivante de la période de trame pour détecter et stocker une tension de seuil (Vth) du TFT de commande (DT) par :

la fourniture d'un niveau de désactivation du signal de régulation d'émission lumineuse (EM) pour mettre hors tension le premier TFT de commutation (ST1) au cours de la période de détection (Ts) suivante ;
la fourniture d'un niveau de désactivation du signal d'initialisation (INIT) pour mettre hors tension le deuxième TFT de commutation (ST2) et le troisième TFT de commutation (ST3) au cours de la période de détection (Ts) suivante ;
la fourniture d'un niveau de désactivation du signal de balayage (SCAN) pour mettre hors tension le quatrième TFT de commutation (ST4) au cours de la période de détection (Ts) suivante.

2. Affichage électroluminescent organique selon la revendication 1, dans lequel la période de trame est divisée en la période d'initialisation (Ti) pour initialiser les noeuds A, B et C, la période de détection (Ts), une période de programmation (Tp) pour appliquer la tension de données, et une période d'émission (Te) pour compenser le courant de commande appliqué à la diode électroluminescente organique en utilisant la tension de seuil et la tension de données, indépendamment de la tension de seuil.

3. Affichage électroluminescent organique selon la revendication 2, dans lequel, au cours de la période de détection (Ts), le potentiel du noeud C augmente à une tension de source intermédiaire, qui est obtenue en ajoutant une valeur obtenue par la soustraction de la tension de seuil (Vth) à la tension de référence (Vref) à un facteur de compensation d'amplification (α) pour empêcher toute distorsion de la tension de seuil, et le potentiel du noeud B augmente à une tension de grille intermédiaire (Vref+α), qui est obtenue en ajoutant la tension de référence (Vref) au facteur de compensation d'amplification (α).

4. Affichage électroluminescent organique selon la revendication 3, dans lequel la valeur du facteur de compensation d'amplification (α) est ajustée par un condensateur parasite du TFT de commande.

5. Affichage électroluminescent organique selon la revendication 3, dans lequel un condensateur d'ajustement (Cgds) pour ajuster la valeur du facteur de compensation d'amplification (α) est en outre relié entre le noeud B et la borne d'entrée de la tension de commande de cellule à haut potentiel (EVDD).

6. Affichage électroluminescent organique selon la revendication 2, dans lequel le signal de régulation d'émission lumineuse (EM) comprend une première impulsion (P1) ayant le niveau d'activation correspondant à la période d'initialisation (Ti) et une deuxième impulsion (P2) ayant le niveau d'activation correspondant partiellement à la période d'émission (Te).

7. Affichage électroluminescent organique selon la revendication 6, dans lequel la période d'émission (Te) comprend une première période d'émission (Te1) pour appliquer un premier courant de commande (Ioled1) à la diode électroluminescente organique et une deuxième période d'émission (Te2) pour appliquer un deuxième courant de commande (Ioled2), qui est inférieur au premier courant de commande, à la diode électroluminescente organique, la deuxième période d'émission (Te2) étant plus longue que la première période d'émission (Te1).

8. Affichage électroluminescent organique selon la revendication 6, dans lequel la période d'activation de la première impulsion est réglée pour être plus courte que la période d'activation de la période d'initialisation (Ti) au cours de la période d'activation du signal d'initialisation.

9. Affichage électroluminescent organique selon la revendication 1, dans lequel une électrode de grille du troisième TFT de commutation (ST3) est reliée à une ligne de signal à laquelle le signal d'initialisation (INIT) est fourni, une électrode du troisième TFT de commutation est reliée à une borne d'entrée de la tension de référence, et l'autre électrode du troisième TFT de commutation est reliée au noeud A ou au noeud B.

10. Procédé de commande d'un affichage électroluminescent organique comprenant un circuit de commande de données (12), un circuit de commande de grille (13) et une pluralité de pixels, chaque pixel (P) comprenant une diode électroluminescente organique (OLED), un TFT de commande (DT) comprenant une grille reliée à un noeud B, un drain relié à une borne d'entrée d'une tension de commande de cellule à haut potentiel (EVDD), et une source reliée à la diode électroluminescente organique par l'intermédiaire d'un noeud C, et destiné à réguler le courant appliqué à la diode électroluminescente organique, un premier TFT de commutation (ST1) configuré pour commuter la voie de courant entre un noeud A et le noeud B en réponse à un signal de régulation d'émission lumineuse (EM), un deuxième TFT de commutation (ST2) configuré pour initialiser le noeud C à une tension d'initialisation (Vinit) en réponse à un signal d'initialisation (INIT), un troisième TFT de commutation (ST3) configuré pour initialiser le noeud A ou le noeud B à une tension de référence (Vref) supérieure à la tension d'initialisation (Vinit) en réponse au signal d'initialisation (INIT), un quatrième TFT de commutation (ST4) configuré pour commuter la voie de courant entre une ligne de données (14) et le noeud A en réponse à un signal de balayage (SCAN), un condensateur de compensation (Cgss) relié entre le noeud B et le noeud C, et un condensateur de stockage (Cst) relié entre le noeud A et le noeud C,
le procédé comprenant les étapes de :

> la mise sous tension du TFT de commande (DT) au cours d'une période d'initialisation (Ti) d'une période de trame pour permettre un flux de courant initial à travers le TFT de commande (DT) par :
>
> > la fourniture d'un niveau d'activation d'un signal d'initialisation (INIT) généré par le circuit de commande de grille (13) afin de charger le noeud C avec la tension d'initialisation (Vinit) au cours de la période d'initialisation

(Ti) et afin de charger le noeud B à une tension de référence (Vref) supérieure à la tension d'initialisation (Vinit) en réponse au signal d'initialisation (INIT) et du signal de régulation d'émission lumineuse (EM) généré par le circuit de commande de grille (13) au cours d'une période d'initialisation (Ti) d'une période de trame en mettant sous tension le deuxième TFT de commutation (ST2) et le troisième TFT de commutation (ST3) pour fournir la tension d'initialisation (Vinit) au noeud C et la tension de référence (Vref) au noeud B au cours de la période d'initialisation (Ti) ;
la fourniture d'un niveau d'activation du signal de régulation d'émission lumineuse (EM) à la ligne d'émission (15b) pour mettre sous tension le premier TFT de commutation (ST1) au cours de la période d'initialisation (Ti) ;
la fourniture d'un niveau de désactivation du signal de balayage (SCAN) généré par le circuit de commande de grille (13) à la ligne de balayage (15a) pour mettre hors tension le quatrième TFT de commutation (ST4) au cours de la période d'initialisation (Ti) et au cours d'une période de détection (Ts) suivante ;
la fourniture d'un niveau de désactivation du signal de régulation d'émission lumineuse (EM) pour mettre hors tension le premier TFT de commutation (ST1) au cours de la période de détection (Ts) suivante ;
la fourniture d'un niveau de désactivation du signal d'initialisation (INIT) pour mettre hors tension le deuxième TFT de commutation (ST2) et le troisième TFT de commutation (ST3) au cours de la période de détection (Ts) suivante afin d'arrêter l'alimentation de la tension d'initialisation (Vinit) et permettre de ce fait au noeud B de flotter au cours de la période de détection (Ts) suivante de la période de trame, puis détecter et stocker une tension de seuil (Vth) du TFT de commande par l'utilisation du condensateur de compensation (Cgss) ;
l'application, après la période de détection (Ts) suivante, d'une tension de données fournie par le circuit de commande de données (12) au noeud A relié au condensateur de stockage en réponse au signal de balayage ; et
la transmission de la tension de données du noeud A au noeud B en réponse au signal de régulation d'émission lumineuse (EM) pour compenser le courant de commande appliqué à la diode électroluminescente organique, indépendamment de la tension de seuil, et amener la diode électroluminescente organique à émettre une lumière.

11. Procédé selon la revendication 10, dans lequel, au cours de la détection et du stockage de la tension de seuil (Vth), le potentiel du noeud C augmente à une tension de source intermédiaire, qui est obtenue en ajoutant une valeur obtenue par la soustraction de la tension de seuil (Vth) à la tension de référence (Vref) à un facteur de compensation d'amplification (α) pour empêcher toute distorsion de la tension de seuil, et le potentiel du noeud B augmente à une tension de grille intermédiaire (Vref+α), qui est obtenue en ajoutant la tension de référence (Vref) au facteur de compensation d'amplification (α).

12. Procédé selon la revendication 11, dans lequel la valeur du facteur de compensation d'amplification (α) est ajustée par un condensateur parasite du TFT de commande.

13. Procédé selon la revendication 10, dans lequel le signal de régulation d'émission lumineuse (EM) comprend une première impulsion (P1) ayant le niveau d'activation correspondant à la période d'initialisation et une deuxième impulsion (P2) ayant le niveau d'activation correspondant partiellement à la période d'émission (Te).

14. Procédé selon la revendication 10, dans lequel la diode électroluminescente organique émet une lumière au cours d'une période d'émission (Te) ; et dans lequel la période d'émission (Te) comprend une première période d'émission (Te1) au cours de laquelle la diode électroluminescente organique émet une lumière par un premier courant de commande (Ioled1) et une deuxième période d'émission (Te2) au cours de laquelle la diode électroluminescente organique émet une lumière par un deuxième courant de commande (Ioled2), la deuxième période d'émission (Te2) étant plus longue que la première période d'émission (Te1).

FIG. 1

(REALTED ART)

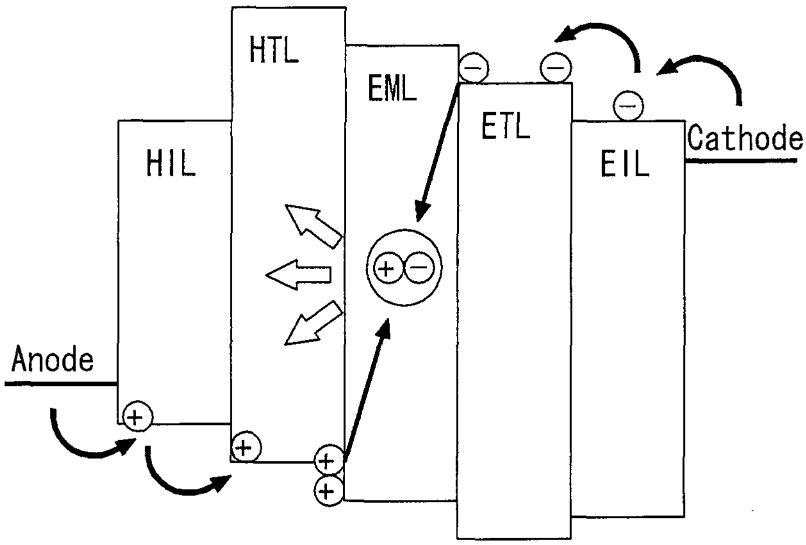


FIG. 2

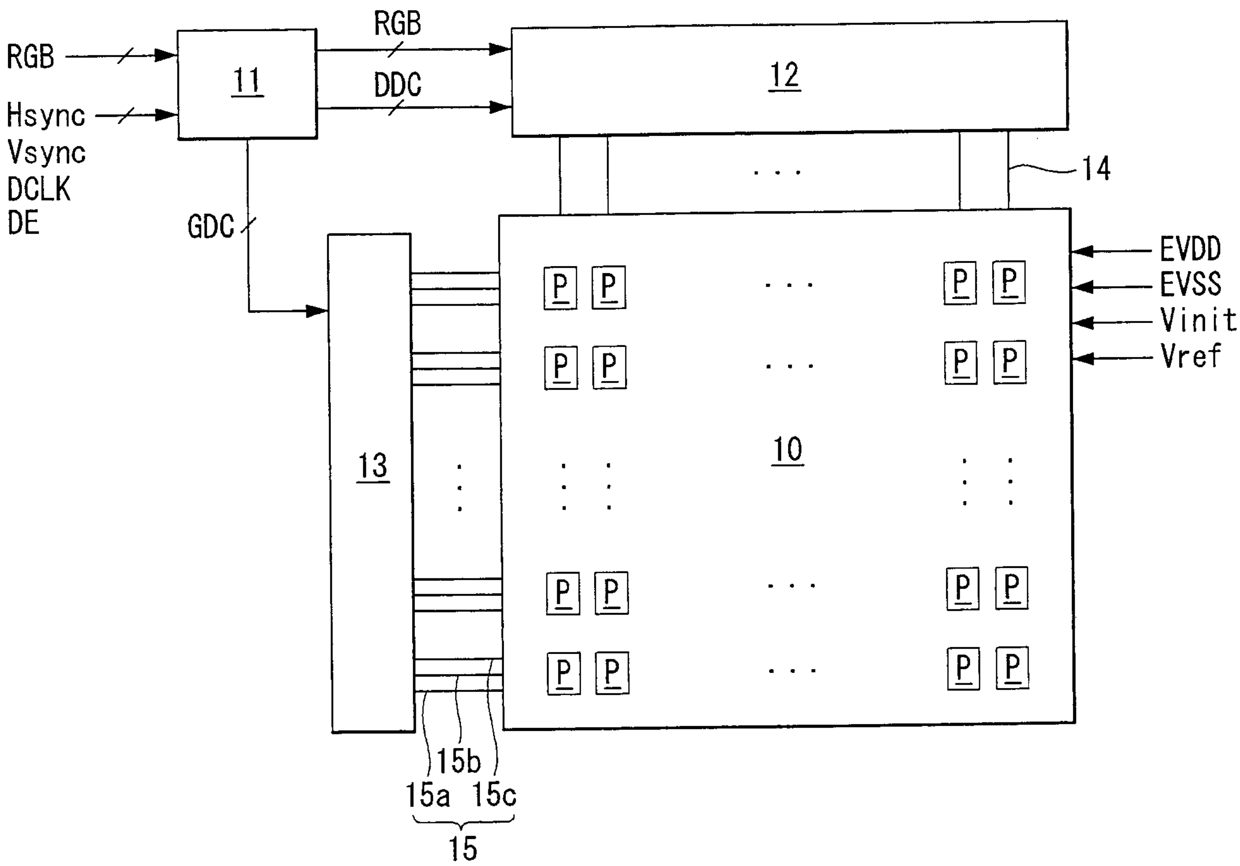

RGB
Hsync
Vsync
DCLK
DE
11
RGB
DDC
12
14
GDC
13
10
P
EVDD
EVSS
Vinit
Vref
15b
15a
15c
15

FIG. 3

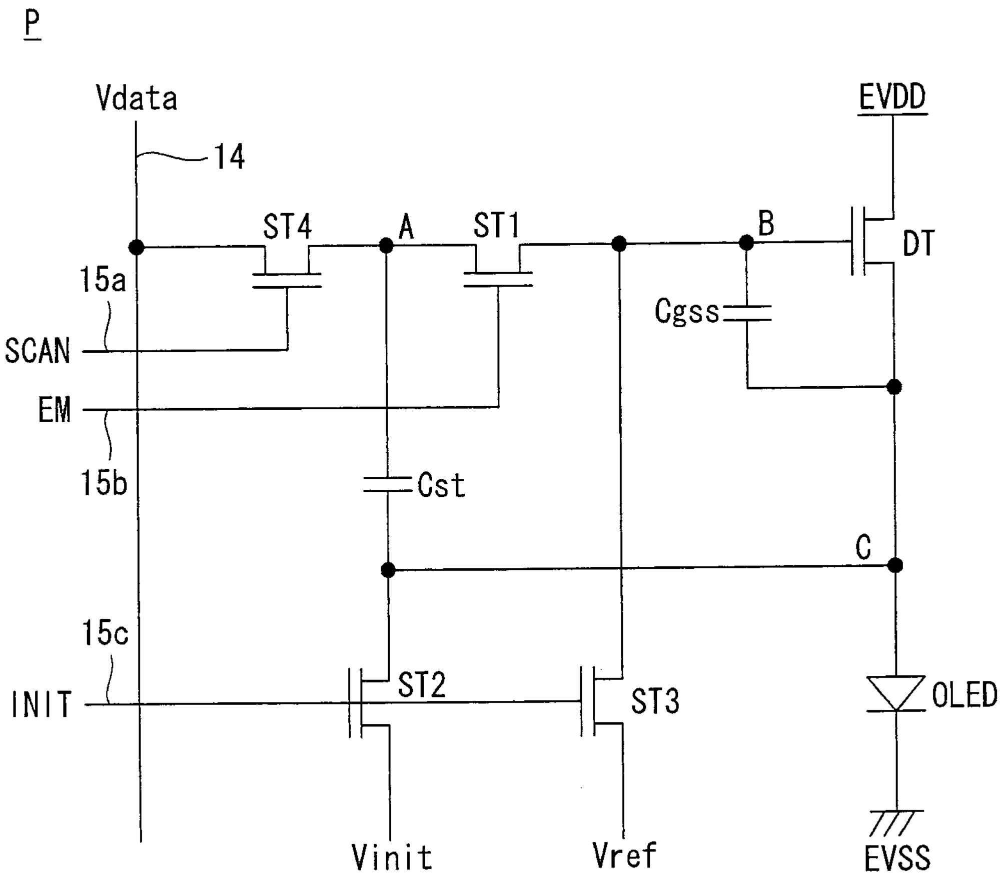

P
Vdata
14
EVDD
ST4
A
ST1
B
DT
15a
Cgss
SCAN
EM
15b
Cst
C
15c
INIT
ST2
ST3
OLED
Vinit
Vref
EVSS

FIG. 4

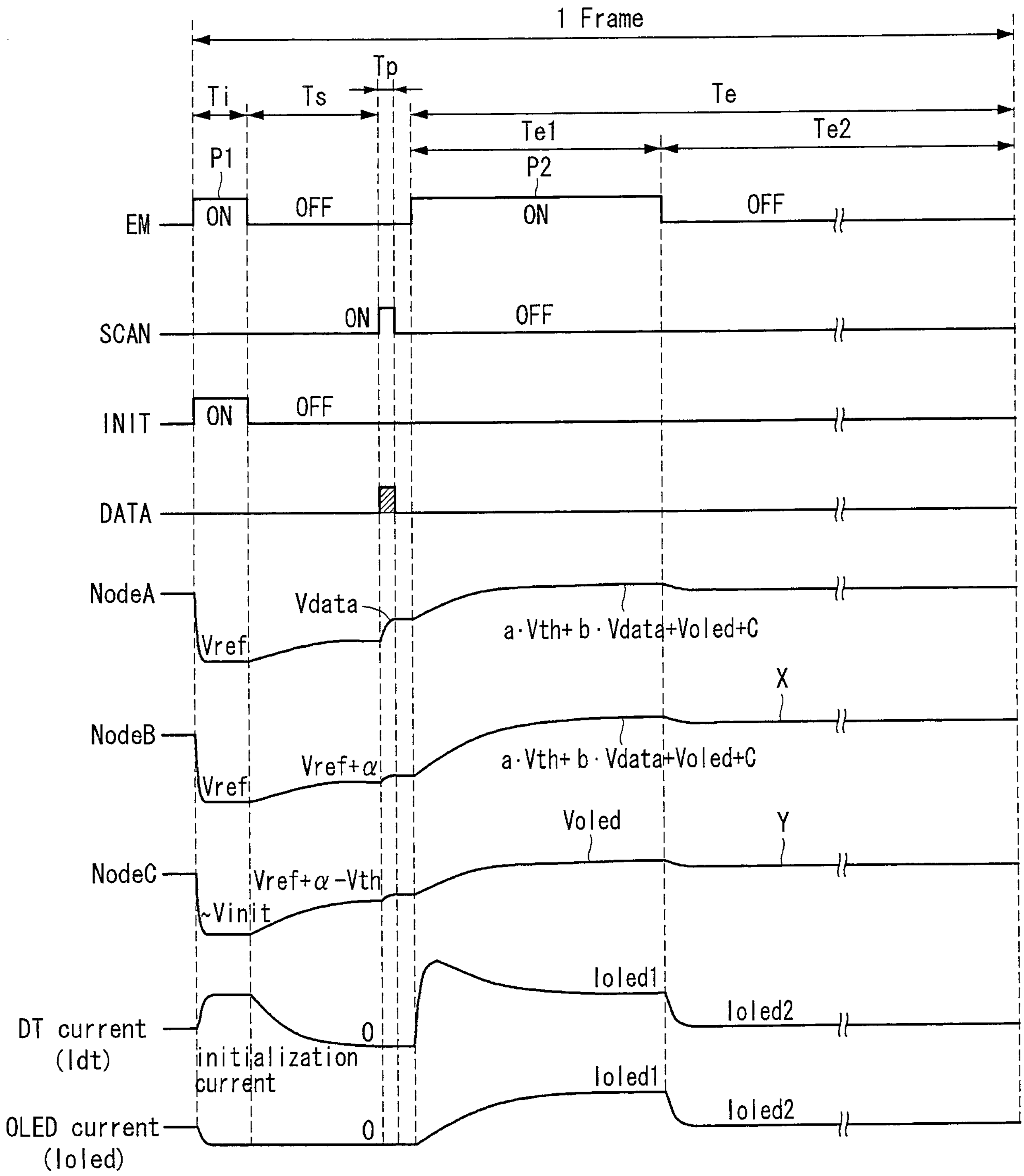
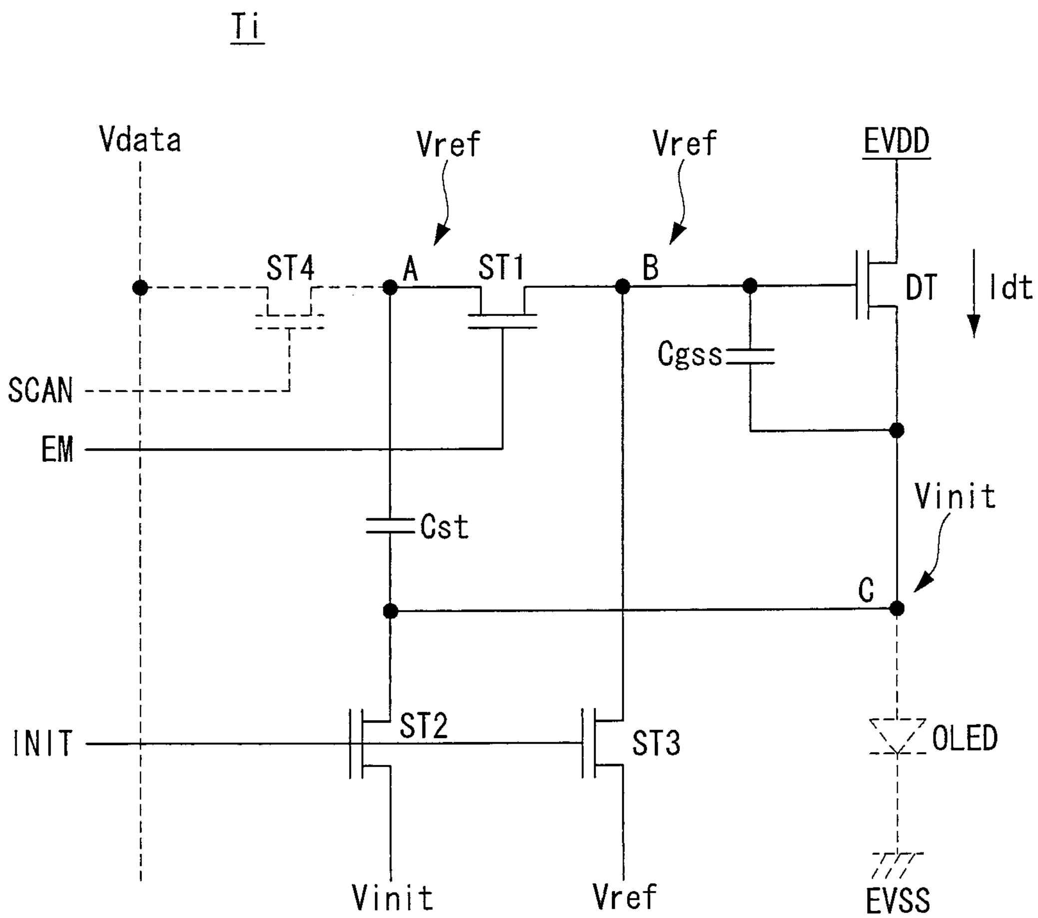

1 Frame
Tp
Ti
Ts
Te
Te1
Te2
P1
P2
EM
ON
OFF
ON
OFF
SCAN
ON
OFF
INIT
ON
OFF
DATA
NodeA
Vref
Vdata
a·Vth+ b · Vdata+Voled+C
NodeB
Vref
Vref+α
a·Vth+ b · Vdata+Voled+C
X
NodeC
~Vinit
Vref+α -Vth
Voled
Y
DT current
(Idt)
initialization
current
0
Ioled1
Ioled2
OLED current
(Ioled)
0
Ioled1
Ioled2

FIG. 5A



Ti
Vdata
Vref
Vref
EVDD
ST4
A
ST1
B
DT
Idt
Cgss
SCAN
EM
Cst
Vinit
C
INIT
ST2
ST3
OLED
Vinit
Vref
EVSS

FIG. 5B

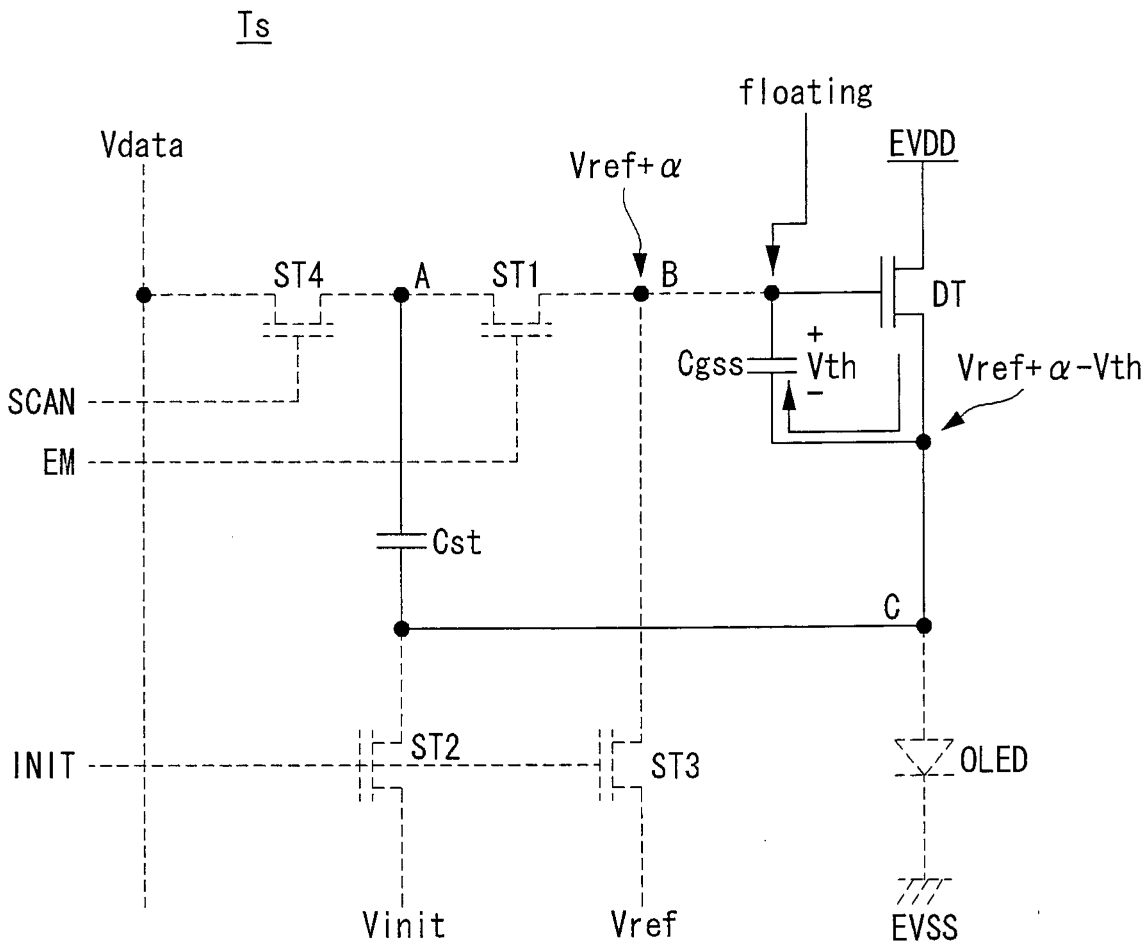

Ts
floating
Vdata
Vref+α
EVDD
ST4
A
ST1
B
DT
Cgss
+
Vth
-
Vref+α-Vth
SCAN
EM
Cst
C
INIT
ST2
ST3
OLED
Vinit
Vref
EVSS

FIG. 5C

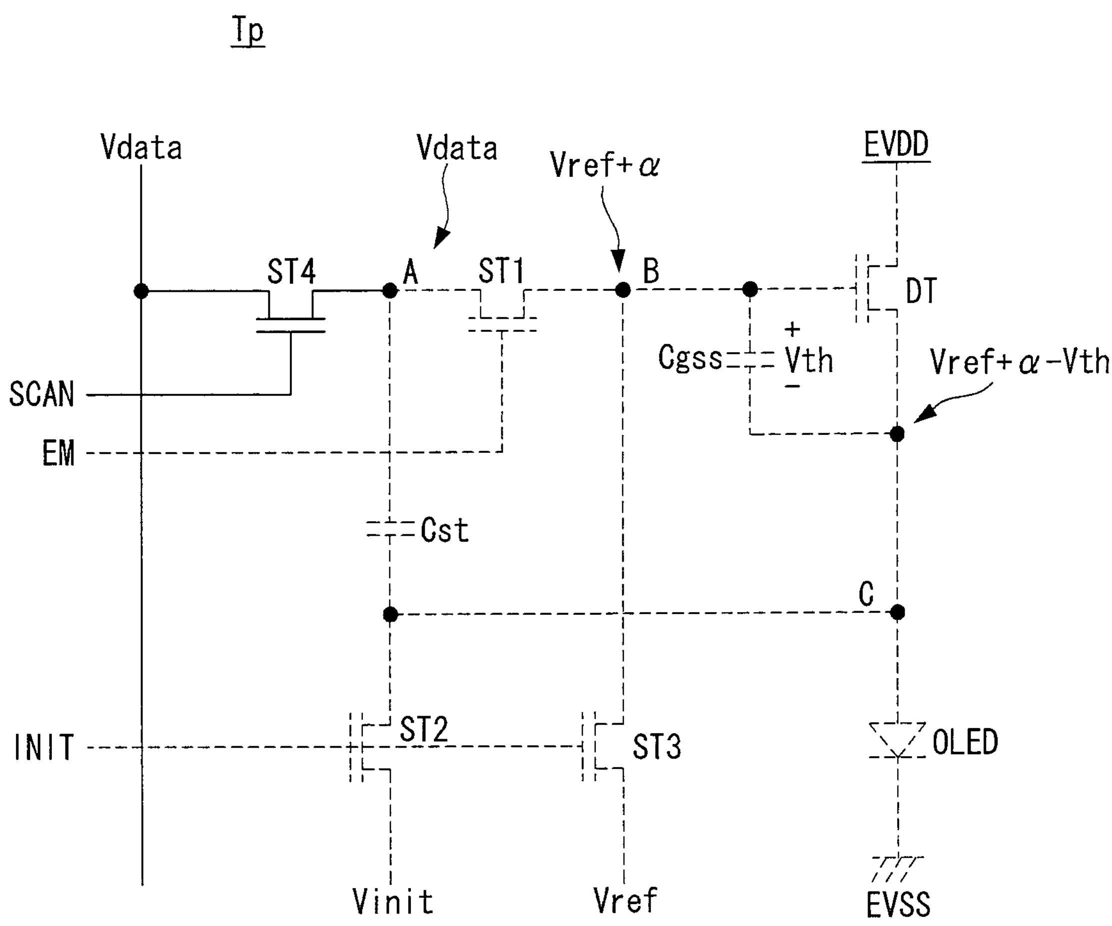

Tp
Vdata
Vdata
Vref+α
EVDD
ST4
A
ST1
B
DT
Cgss
+
Vth
−
Vref+α-Vth
SCAN
EM
Cst
C
INIT
ST2
ST3
OLED
Vinit
Vref
EVSS

FIG. 5D

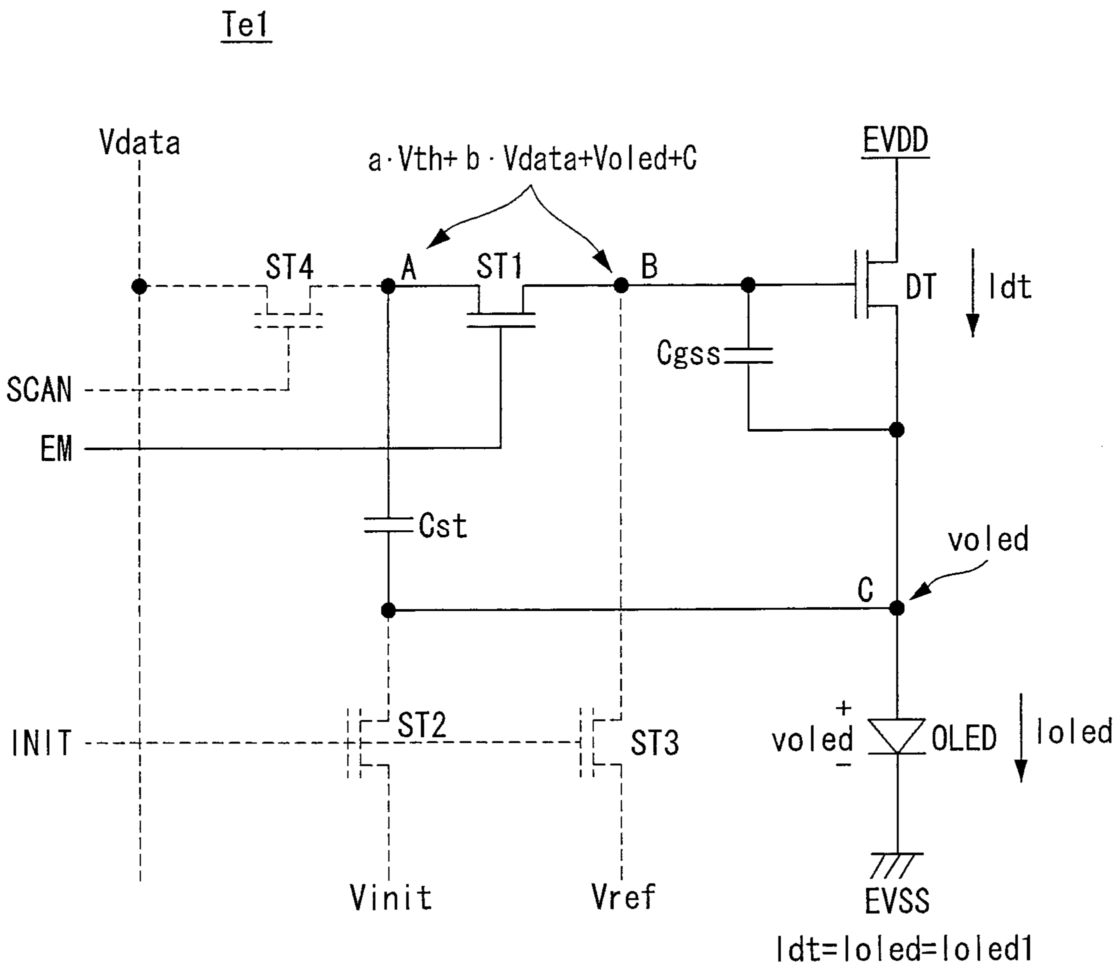

Te1
Vdata
a·Vth+b·Vdata+Voled+C
EVDD
ST4
A
ST1
B
DT
Idt
Cgss
SCAN
EM
Cst
voled
C
INIT
ST2
ST3
+
voled
−
OLED
Ioled
Vinit
Vref
EVSS
Idt=Ioled=Ioled1

FIG. 5E

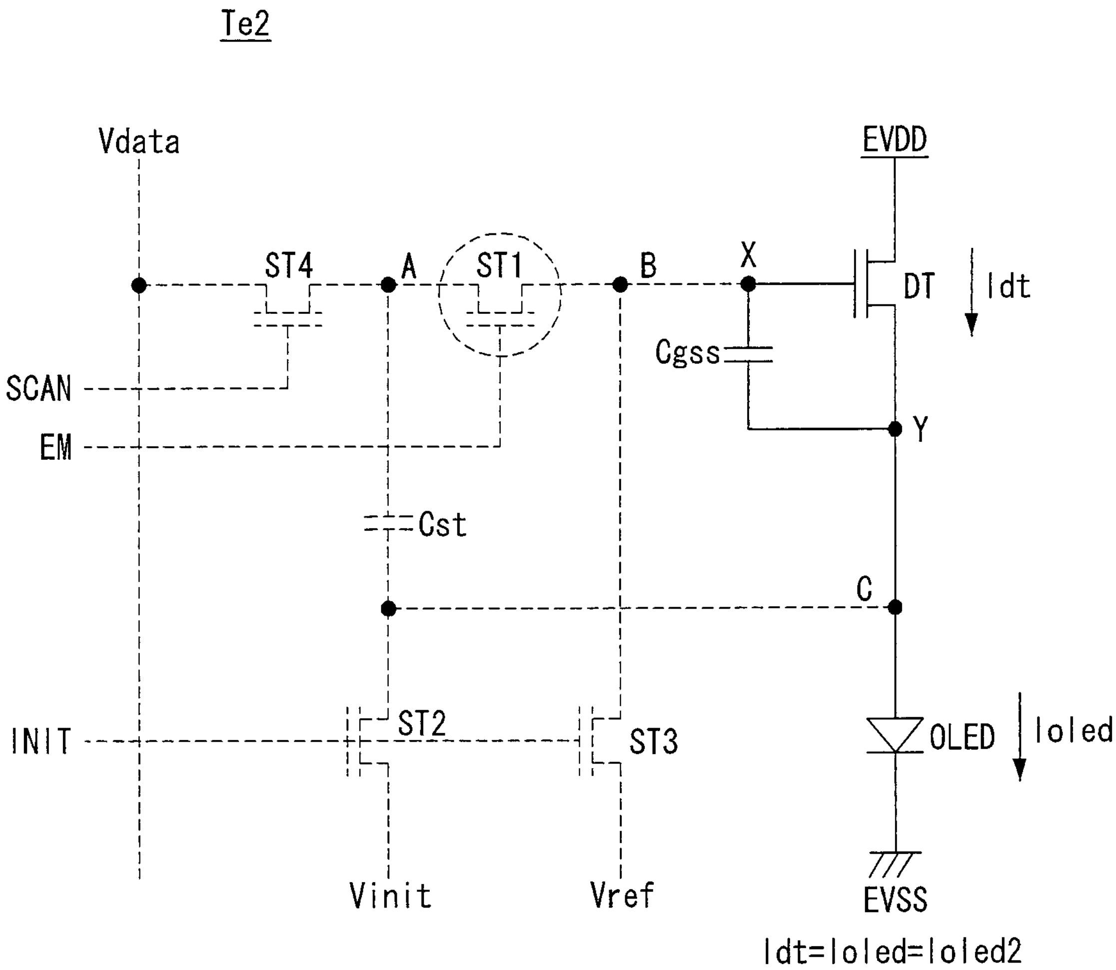

Te2
Vdata
EVDD
ST4
A
ST1
B
X
DT
Idt
Cgss
SCAN
EM
Y
Cst
C
INIT
ST2
ST3
OLED
Ioled
Vinit
Vref
EVSS
Idt=Ioled=Ioled2

FIG. 6

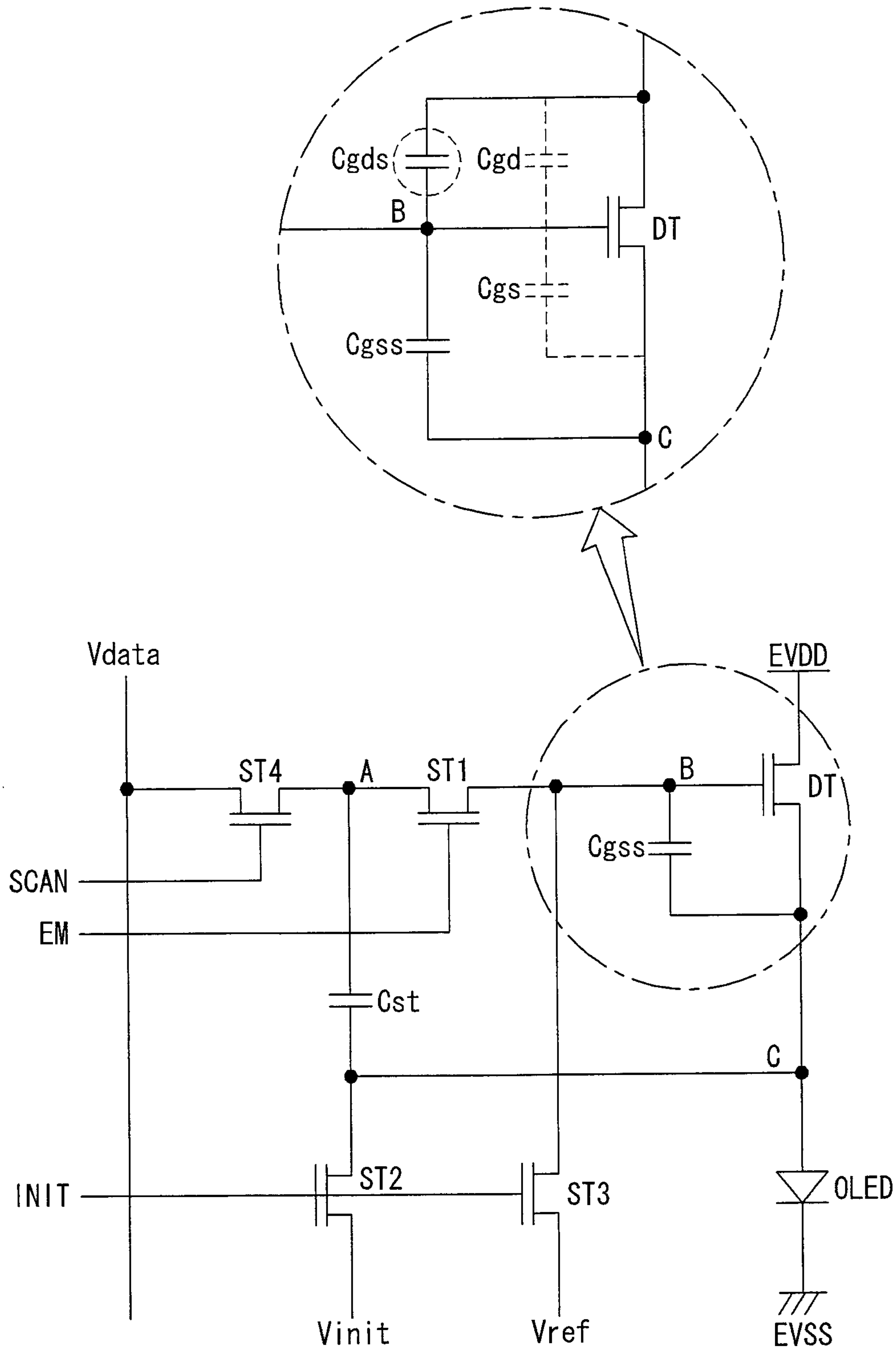

Cgds
Cgd
B
DT
Cgs
Cgss
C
Vdata
EVDD
ST4
A
ST1
B
DT
Cgss
SCAN
EM
Cst
C
INIT
ST2
ST3
OLED
Vinit
Vref
EVSS

FIG. 7

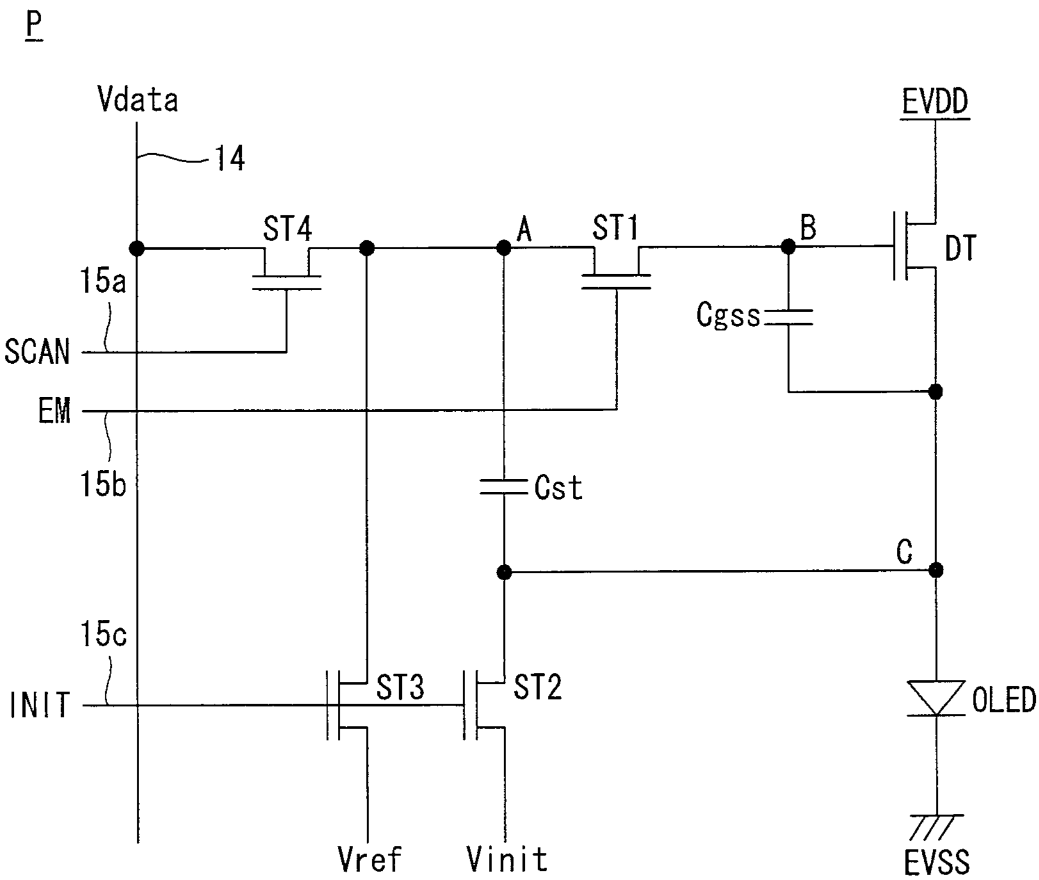

P
Vdata
14
EVDD
ST4
A
ST1
B
DT
15a
SCAN
Cgss
EM
15b
Cst
C
15c
INIT
ST3
ST2
OLED
Vref
Vinit
EVSS

FIG. 8

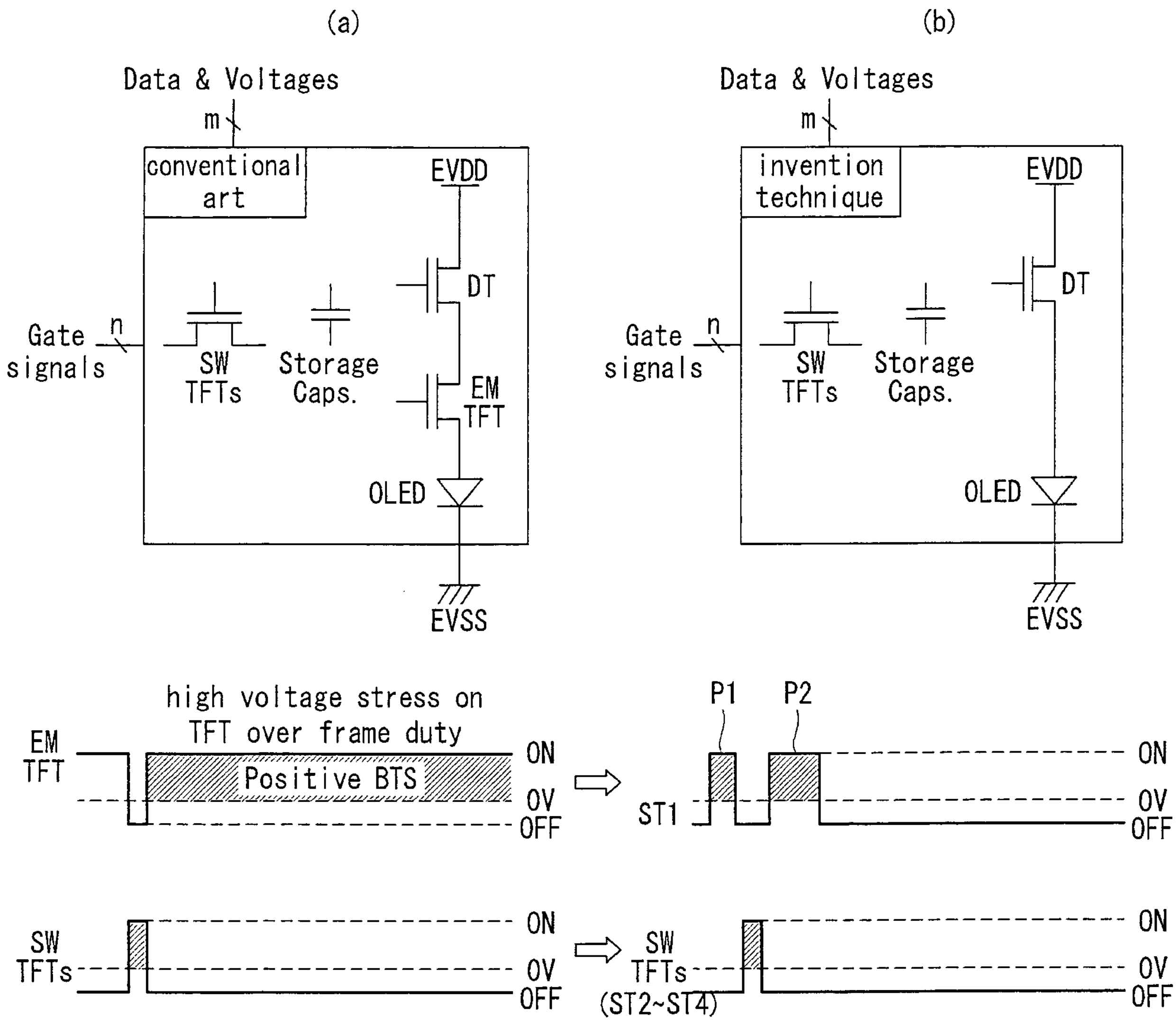

(a)
Data & Voltages
m
conventional art
EVDD
DT
Gate signals
n
SW TFTs
Storage Caps.
EM TFT
OLED
EVSS
(b)
Data & Voltages
m
invention technique
EVDD
DT
Gate signals
n
SW TFTs
Storage Caps.
OLED
EVSS
EM TFT
high voltage stress on TFT over frame duty
Positive BTS
ON
0V
OFF
P1
P2
ST1
ON
0V
OFF
SW TFTs
ON
0V
OFF
SW TFTs (ST2~ST4)
ON
0V
OFF

FIG. 9

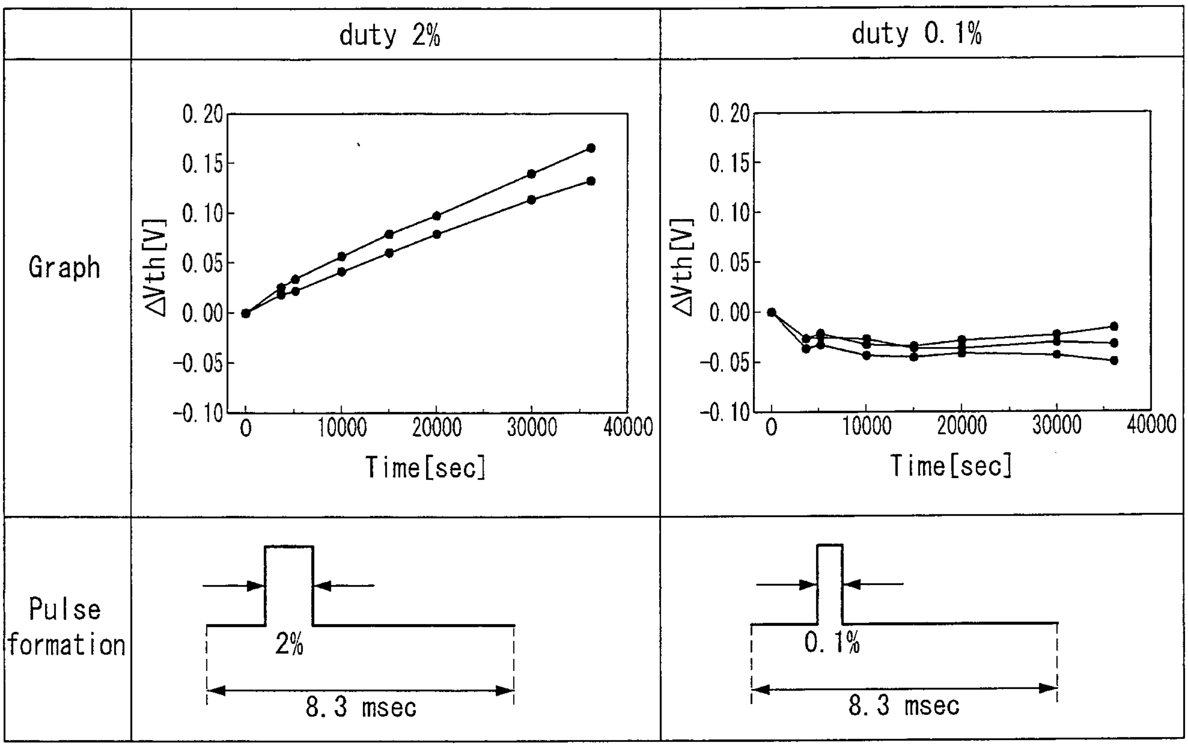
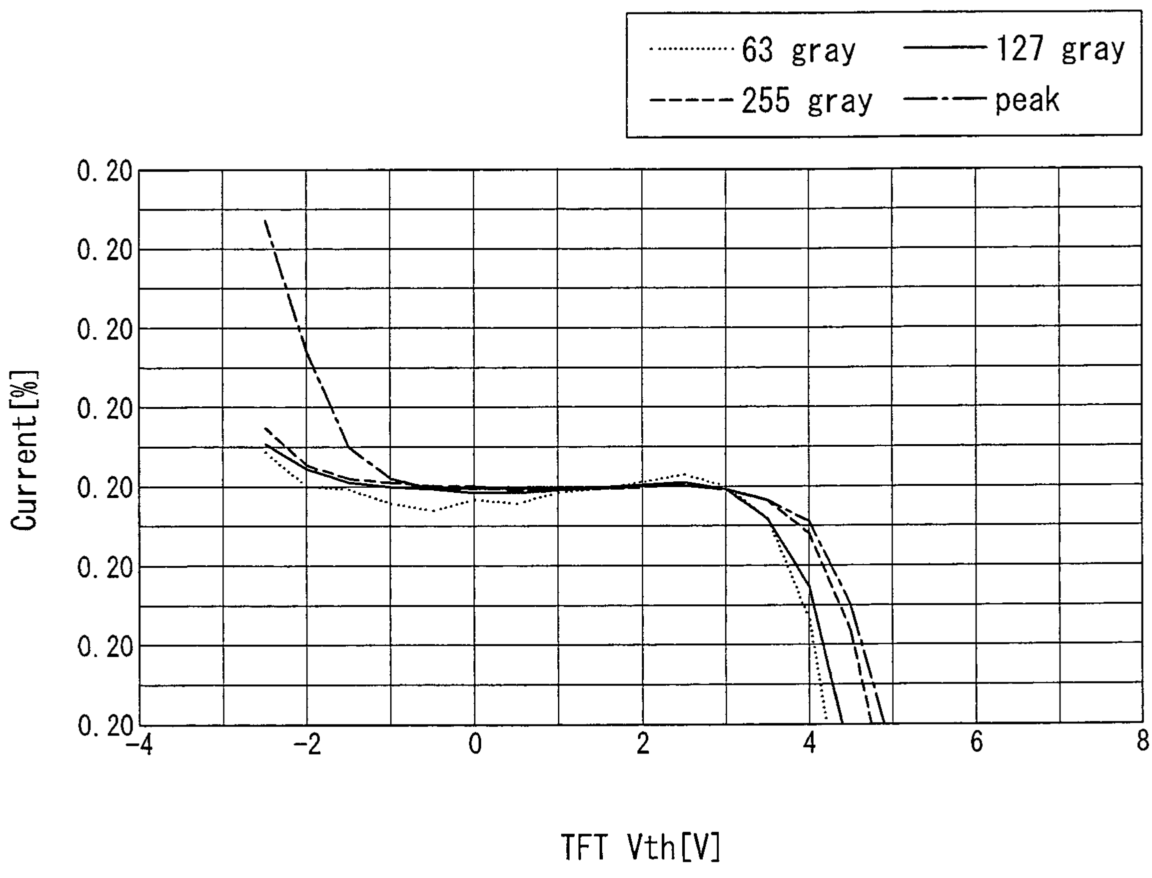

duty 2%
duty 0.1%
Graph
Pulse formation
ΔVth[V]
0.20
0.15
0.10
0.05
0.00
-0.05
-0.10
0
10000
20000
30000
40000
Time[sec]
2%
0.1%
8.3 msec

FIG. 10


63 gray
127 gray
255 gray
peak
0. 20
0. 20
0. 20
0. 20
0. 20
0. 20
0. 20
0. 20
Current[%]
-4
-2
0
2
4
6
8
TFT Vth[V]

REFERENCES CITED IN THE DESCRIPTION

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- US 20110157143 A1 **[0003]**
- US 20110154352 A1 **[0004]**
- KR 20100053233 A **[0005]**
- KR 1020050122699 **[0009]**

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当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	NAM WOOJIN SHIM JONGSIK SHIN HONGJAE CHANG MINKYU		
发明人	NAM, WOOJIN SHIM, JONGSIK SHIN, HONGJAE CHANG, MINKYU		
IPC分类号	G09G3/3233 G09G3/3266		
CPC分类号	G09G3/3233 G09G3/3266 G09G2300/0819 G09G2300/0852 G09G2300/0861 G09G2310/067 G09G2320/0223 G09G2320/043 G09G2320/045		
优先权	1020120095604 2012-08-30 KR		
其他公开文献	EP2704131A1		
外部链接	Espacenet		

摘要(译)

一种有机发光显示器，包括：驱动TFT（DT），包括连接到节点B的栅极，连接到高电位单元驱动电压的输入端子的漏极，以及通过节点连接到有机发光二极管的源极C;第一开关TFT（ST1），用于响应发光控制信号切换节点A和节点B之间的电流路径;第二开关TFT（ST2），用于响应初始化信号初始化节点C;第三开关TFT（ST3），用于响应初始化信号初始化节点A或节点B;第四开关TFT（ST4），用于响应扫描信号切换数据线（14）和节点B之间的电流路径;连接在节点B和节点C之间的补偿电容器（Cgss）。

FIG. 1

(REALTED ART)