



(11) **EP 2 642 476 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention  
of the grant of the patent:  
**14.01.2015 Bulletin 2015/03**

(51) Int Cl.:  
**G09G 3/32** <sup>(2006.01)</sup> **G09G 3/00** <sup>(2006.01)</sup>  
**H04N 13/04** <sup>(2006.01)</sup>

(21) Application number: **12189157.6**

(22) Date of filing: **19.10.2012**

(54) **Pixel circuit, method of driving a pixel circuit, and organic light emitting display device**

Pixelschaltung, Verfahren zum Ansteuern einer Pixelschaltung und organische lichtemittierende Anzeigevorrichtung

Circuit de pixels, procédé de commande d'un circuit de pixels et dispositif d'affichage électroluminescent organique

(84) Designated Contracting States:  
**AL AT BE BG CH CY CZ DE DK EE ES FI FR GB  
GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO  
PL PT RO RS SE SI SK SM TR**

(30) Priority: **23.03.2012 KR 20120029639**

(43) Date of publication of application:  
**25.09.2013 Bulletin 2013/39**

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**WO-A1-2011/077718 US-A1- 2012 007 848**

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**Description**

## BACKGROUND

5     1. Technical Field

**[0001]** Embodiments relate to a pixel circuit, a method of driving the pixel circuit, and an organic light emitting display device.

10     2. Description of the Related Art

**[0002]** In a stereoscopic (3D) image display technique, a stereoscopic image may be implemented using binocular parallax that provides a three-dimensional effect. Generally, a stereoscopic image may be implemented by alternately providing a left image and a right image to a left eye and a right eye, respectively. It may be desirable to use an organic light emitting display device, which may provide fast response speed and low power consumption, as a flat panel display device for displaying a stereoscopic image.

## SUMMARY

20     **[0003]** Embodiments are directed to a pixel circuit, including an organic light emitting diode, a cathode electrode of the organic light emitting diode being coupled to a second power voltage, a first PMOS transistor coupled between a first power voltage and an anode electrode of the organic light emitting diode, a gate terminal of the first PMOS transistor being coupled to a first node, a second PMOS transistor coupled between the first node and the anode electrode of the organic light emitting diode, a gate terminal of the second PMOS transistor receiving a compensation control signal, a  
25     first capacitor coupled between a second node and the first node, a second capacitor coupled between the first power voltage and the second node, a third PMOS transistor coupled between a data line and the second node, a gate terminal of the third PMOS transistor receiving the compensation control signal, a fourth PMOS transistor coupled between a third node and the second node, a gate terminal of the fourth PMOS transistor receiving an emission control signal, a third capacitor coupled between the third node and the gate terminal of the third PMOS transistor, and a fifth PMOS  
30     transistor coupled between the data line and the third node, a gate terminal of the fifth PMOS transistor being coupled to a scan line.

**[0004]** The circuit may be configured to alternately perform a first display operation for displaying a left image and a second display operation for displaying a right image, the first display operation and the second display operation being performed based on a simultaneous emission method.

35     **[0005]** The first display operation may include a first preliminary data writing operation, a first reset operation, a first threshold voltage compensation operation, a first data writing operation, and a first emission operation, and the second display operation may include a second preliminary data writing operation, a second reset operation, a second threshold voltage compensation operation, a second data writing operation, and a second emission operation.

**[0006]** The circuit may be configured to simultaneously perform the first emission operation and the second preliminary data writing operation, and may be configured to simultaneously perform the second emission operation and the first preliminary data writing operation.

**[0007]** While the first preliminary data writing operation is performed, the fourth PMOS transistor may turn off, and a first image data that is applied through the data line may be stored in the third capacitor when the fifth PMOS transistor turns on in response to a scan signal that is applied through the scan line, and, while the second preliminary data writing operation is performed, the fourth PMOS transistor may turn off, and a second image data that is applied through the data line may be stored in the third capacitor when the fifth PMOS transistor turns on in response to the scan signal that is applied through the scan line.

**[0008]** While the first reset operation is performed, the second through fourth PMOS transistors may turn off, the second power voltage may have a high voltage level, and the first power voltage may have a low voltage level, and, while the second reset operation is performed, the second through fourth PMOS transistors may turn off, the second power voltage may have a high voltage level, and the first power voltage may have a low voltage level.

**[0009]** While the first threshold voltage compensation operation is performed, the fourth PMOS transistor may turn off, the second and third PMOS transistors may turn on, the second power voltage may have a high voltage level, and the first power voltage may have a high voltage level, and, while the second threshold voltage compensation operation is performed, the fourth PMOS transistor may turn off, the second and third PMOS transistors may turn on, the second power voltage may have a high voltage level, and the first power voltage may have a high voltage level.

**[0010]** While the first data writing operation is performed, the fourth PMOS transistor may turn on, the second and third PMOS transistors may turn off, the second power voltage may have a high voltage level, and the first power voltage

may have a high voltage level, and, while the second data writing operation is performed, the fourth PMOS transistor may turn on, the second and third PMOS transistors may turn off, the second power voltage may have a high voltage level, and the first power voltage may have a high voltage level.

**[0011]** While the first emission operation is performed, the second through fourth PMOS transistors may turn off, the second power voltage may have a low voltage level, and the first power voltage may have a high voltage level, and, while the second emission operation is performed, the second through fourth PMOS transistors may turn off, the second power voltage may have a low voltage level, and the first power voltage may have a high voltage level.

**[0012]** The first display operation may further include a first off-bias applying operation, and the second display operation may further include a second off-bias applying operation.

**[0013]** While the first off-bias applying operation is performed, the fourth PMOS transistor may turn off, the second and third PMOS transistors may turn on, the second power voltage may have a high voltage level, and the first power voltage may have a low voltage level, and, while the second off-bias applying operation is performed, the fourth PMOS transistor may turn off, the second and third PMOS transistors may turn on, the second power voltage may have a high voltage level, and the first power voltage may have a low voltage level.

**[0014]** The circuit may further include a fourth capacitor coupled between the anode electrode and the cathode electrode of the organic light emitting diode.

**[0015]** Embodiments are also directed to a pixel circuit, including an organic light emitting diode, a cathode electrode of the organic light emitting diode being coupled to a second power voltage, a first PMOS transistor coupled between a first power voltage and an anode electrode of the organic light emitting diode, a gate terminal of the first PMOS transistor being coupled to a first node, a second PMOS transistor coupled between the first node and the anode electrode of the organic light emitting diode, a gate terminal of the second PMOS transistor receiving a compensation control signal, a first capacitor coupled between a second node and the first node, a second capacitor coupled between the first power voltage and the second node, a third PMOS transistor coupled between a data line and the second node, a gate terminal of the third PMOS transistor receiving the compensation control signal, a fourth PMOS transistor coupled between a third node and the second node, a gate terminal of the fourth PMOS transistor receiving an emission control signal, a third capacitor coupled between the third node and a sustain power voltage, and a fifth PMOS transistor coupled between the data line and the third node, a gate terminal of the fifth PMOS transistor being coupled to a scan line.

**[0016]** The circuit may be configured to alternately perform a first display operation for displaying a left image and a second display operation for displaying a right image, the first display operation and the second display operation being performed based on a simultaneous emission method.

**[0017]** The first display operation may include a first preliminary data writing operation, a first reset operation, a first threshold voltage compensation operation, a first data writing operation, and a first emission operation, and the second display operation may include a second preliminary data writing operation, a second reset operation, a second threshold voltage compensation operation, a second data writing operation, and a second emission operation.

**[0018]** The circuit may be configured to simultaneously perform the first emission operation and the second preliminary data writing operation, and may be configured to simultaneously perform the second emission operation and the first preliminary data writing operation.

**[0019]** The first display operation may further include a first off-bias applying operation, and the second display operation may further include a second off-bias applying operation.

**[0020]** The circuit may further include a fourth capacitor coupled between the anode electrode and the cathode electrode of the organic light emitting diode.

**[0021]** Embodiments are also directed to a pixel circuit, including an organic light emitting diode, an anode electrode of the organic light emitting diode being coupled to a first power voltage, a first NMOS transistor coupled between a second power voltage and a cathode electrode of the organic light emitting diode, a gate terminal of the first NMOS transistor being coupled to a first node, a second NMOS transistor coupled between the first node and the cathode electrode of the organic light emitting diode, a gate terminal of the second NMOS transistor receiving a compensation control signal, a first capacitor coupled between a second node and the first node, a second capacitor coupled between the second power voltage and the second node, a third NMOS transistor coupled between a data line and the second node, a gate terminal of the third NMOS transistor receiving the compensation control signal, a fourth NMOS transistor coupled between a third node and the second node, a gate terminal of the fourth NMOS transistor receiving an emission control signal, a third capacitor coupled between the third node and the gate terminal of the third NMOS transistor, and a fifth NMOS transistor coupled between the data line and the third node, a gate terminal of the fifth NMOS transistor being coupled to a scan line.

**[0022]** Embodiments are also directed to a pixel circuit, including an organic light emitting diode, an anode electrode of the organic light emitting diode being coupled to a first power voltage, a first NMOS transistor coupled between a second power voltage and a cathode electrode of the organic light emitting diode, a gate terminal of the first NMOS transistor being coupled to a first node, a second NMOS transistor coupled between the first node and the cathode electrode of the organic light emitting diode, a gate terminal of the second NMOS transistor receiving a compensation

control signal, a first capacitor coupled between a second node and the first node, a second capacitor coupled between the second power voltage and the second node, a third NMOS transistor coupled between a data line and the second node, a gate terminal of the third NMOS transistor receiving the compensation control signal, a fourth NMOS transistor coupled between a third node and the second node, a gate terminal of the fourth NMOS transistor receiving an emission control signal, a third capacitor coupled between the third node and a sustain power voltage, and a fifth NMOS transistor coupled between the data line and the third node, a gate terminal of the fifth NMOS transistor being coupled to a scan line.

**[0023]** Embodiments are also directed to an organic light emitting display device, including a pixel unit having a plurality of pixel circuits, each pixel circuit of the plurality of pixel circuits being the pixel circuit according to an embodiment, a scan driving unit configured to provide a scan signal to the pixel circuits, a data driving unit configured to provide a data signal to the pixel circuits, a control signal generating unit configured to provide the emission control signal and the compensation control signal to the pixel circuits, a power unit configured to provide the first power voltage and the second power voltage to the pixel units, and a timing control unit configured to control the scan driving unit, the data driving unit, the control signal generating unit, and the power unit.

**[0024]** Each pixel circuit of the plurality of pixel circuits may be configured to alternately perform a first display operation for displaying a left image and a second display operation for displaying a right image, the first display operation and the second display operation being performed based on a simultaneous emission method.

**[0025]** The first display operation may include a first preliminary data writing operation, a first reset operation, a first threshold voltage compensation operation, a first data writing operation, and a first emission operation, the second display operation may include a second preliminary data writing operation, a second reset operation, a second threshold voltage compensation operation, a second data writing operation, and a second emission operation, and each pixel circuit of the plurality of pixel circuits may be configured to simultaneously perform the first emission operation and the second preliminary data writing operation, and may be configured to simultaneously perform the second emission operation and the first preliminary data writing operation.

**[0026]** The first display operation may further include a first off-bias applying operation, and the second display operation may further include a second off-bias applying operation.

**[0027]** Embodiments are also directed to an organic light emitting display device, including a pixel unit having a plurality of pixel circuits, each pixel circuit of the plurality of pixel circuits being the pixel circuit according to another embodiment, a scan driving unit configured to provide a scan signal to the pixel circuits, a data driving unit configured to provide a data signal to the pixel circuits, a control signal generating unit configured to provide the emission control signal and the compensation control signal to the pixel circuits, a power unit configured to provide the first power voltage, the second power voltage, and the sustain power voltage to the pixel units, and a timing control unit configured to control the scan driving unit, the data driving unit, the control signal generating unit, and the power unit.

**[0028]** Each pixel circuit of the plurality of pixel circuits may be configured to alternately perform a first display operation for displaying a left image and a second display operation for displaying a right image, the first display operation and the second display operation being performed based on a simultaneous emission method.

**[0029]** The first display operation may include a first preliminary data writing operation, a first reset operation, a first threshold voltage compensation operation, a first data writing operation, and a first emission operation, the second display operation may include a second preliminary data writing operation, a second reset operation, a second threshold voltage compensation operation, a second data writing operation, and a second emission operation, and each pixel circuit of the plurality of pixel circuits may be configured to simultaneously perform the first emission operation and the second preliminary data writing operation, and may be configured to simultaneously perform the second emission operation and the first preliminary data writing operation.

**[0030]** The first display operation may further include a first off-bias applying operation, and the second display operation may further include a second off-bias applying operation.

**[0031]** Embodiments are also directed to a method of driving a pixel circuit, including simultaneously performing a first emission operation of a first display operation for displaying a left image and a second preliminary data writing operation of a second display operation for displaying a right image, sequentially performing a second reset operation, a second threshold voltage compensation operation, and a second data writing operation of the second display operation after the first emission operation is completed, simultaneously performing a second emission operation of the second display operation and a first preliminary data writing operation of the first display operation, and sequentially performing a first reset operation, a first threshold voltage compensation operation, and a first data writing operation of the first display operation after the second emission operation is completed.

**[0032]** The method may further include performing a first off-bias applying operation of the first display operation prior to the first reset operation of the first display operation, and performing a second off-bias applying operation of the second display operation prior to the second reset operation of the second display operation.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0033]** Features will become apparent to those of skill in the art by describing in detail exemplary embodiments with reference to the attached drawings in which;

FIG. 1 illustrates a circuit diagram of a pixel circuit according to an exemplary embodiment.

FIG. 2 illustrates a diagram of an example in which an organic light emitting display device implements a stereoscopic image based on a simultaneous emission method.

FIG. 3 illustrates a diagram of an example in which a stereoscopic image is implemented by an organic light emitting display device having the pixel circuit of FIG. 1.

FIGS. 4A through 4E illustrate timing diagrams of an example operation of the pixel circuit of FIG. 1.

FIG. 5 illustrates a timing diagram of another example operation of the pixel circuit of FIG. 1.

FIG. 6 illustrates a circuit diagram of a pixel circuit according to an exemplary embodiment.

FIG. 7 illustrates a circuit diagram of a pixel circuit according to an exemplary embodiment.

FIGS. 8A through 8E illustrate timing diagrams of an example operation of the pixel circuit of FIG. 7.

FIG. 9 illustrates a circuit diagram of a pixel circuit according to an exemplary embodiment.

FIG. 10 illustrates a flow chart of a method of driving a pixel circuit according to an exemplary embodiment.

FIG. 11 illustrates a flow chart of a method of driving a pixel circuit according to an exemplary embodiment.

FIG. 12 illustrates a block diagram of an organic light emitting display device according to an exemplary embodiment.

FIG. 13 illustrates a diagram of a stereoscopic image display system employing a shutter glasses method, which includes an organic light emitting display device of FIG. 12.

FIG. 14 illustrates a diagram of a stereoscopic image display system employing a parallax barrier method, which includes an organic light emitting display device of FIG. 12.

FIG. 15 illustrates a block diagram of an electric device having an organic light emitting display device of FIG. 12.

## DETAILED DESCRIPTION

**[0034]** Exemplary embodiments will be described hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

**[0035]** In the drawing figures, the dimensions of layers and regions may be exaggerated for clarity of illustration. Like reference numerals refer to like elements throughout.

**[0036]** It will be understood that, although the terms first, second, third, etc., may be used herein to describe various elements, these elements should not be limited by these terms. These terms are used to distinguish one element from another. Thus, a first element discussed below could be termed a second element without departing from the teachings of the present inventive concept. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

**[0037]** It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. Other words used to describe the relationship between elements should be interpreted in a like fashion (e.g., "between" versus "directly between," "adjacent" versus "directly adjacent," etc.).

**[0038]** The terminology used herein is for the purpose of describing particular exemplary embodiments only and is

not intended to be limiting of the present inventive concept. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more

other features, integers, steps, operations, elements, components, and/or groups thereof.

[0039] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this inventive concept belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly

formal sense unless expressly so defined herein.

[0040] FIG. 1 illustrates a circuit diagram of a pixel circuit according to exemplary embodiments.

[0041] Referring to FIG. 1, the pixel circuit 100 may include an organic light emitting diode OLED, first through fifth p-channel metal oxide semiconductor (PMOS) transistors PT1 through PT5, and first through third capacitors C1 through C3. The pixel circuit 100 may have a 5T-3C structure (i.e., a structure having five transistors and three capacitors). In an example embodiment, the pixel circuit 100 may further include a fourth capacitor C4 coupled between an anode electrode and a cathode electrode of the organic light emitting diode OLED. The fourth capacitor C4 may be an auxiliary capacitor.

[0042] The organic light emitting diode OLED may be coupled between a second power voltage ELVSS and the first PMOS transistor PT1. In detail, a cathode electrode of the organic light emitting diode OLED may be coupled to the second power voltage ELVSS, and an anode electrode of the organic light emitting diode OLED may be coupled to a first terminal of the first PMOS transistor PT1. The organic light emitting diode OLED may emit light based on a current that is controlled by the first PMOS transistor PT1. The first PMOS transistor PT1 may be coupled between a first power voltage ELVDD and the anode electrode of the organic light emitting diode OLED. A gate terminal of the first PMOS transistor PT1 may be coupled to a first node N1. The first PMOS transistor PT1 may be a driving transistor that controls a current flowing through the organic light emitting diode OLED. As illustrated in FIG. 1, the first node N1 is a node at which a first terminal of the first capacitor C1, a first terminal of the second PMOS transistor PT2, and the gate terminal of the first PMOS transistor PT1 are coupled to each other. The second PMOS transistor PT2 may be coupled between the first node N1 and the anode electrode of the organic light emitting diode OLED. A gate terminal of the second PMOS transistor PT2 may receive a compensation control signal TCS. In detail, the first terminal of the second PMOS transistor PT2 may be coupled to the first node N1, and a second terminal of the second PMOS transistor PT2 may be coupled to the first terminal of the first PMOS transistor PT1. Thus, when the second PMOS transistor PT2 turns on in response to the compensation control signal TCS, the first PMOS transistor PT1 may be diode-coupled.

[0043] The first capacitor C1 may be coupled between the first node N1 and a second node N2. In detail, the first terminal of the first capacitor C1 may be coupled to the first node N1, and a second terminal of the first capacitor C1 may be coupled to the second node N2. The first capacitor C1 may be a threshold voltage compensation capacitor. As illustrated in FIG. 1, the second node N2 is a node at which a second terminal of the first capacitor C1, a first terminal of the second capacitor C2, a first terminal of the third PMOS transistor PT3, and a first terminal of the fourth PMOS transistor PT4 are coupled to each other. The second capacitor C2 may be coupled between the first power voltage ELVDD and the second node N2. The second capacitor C2 may be a storage capacitor. In detail, the first terminal of the second capacitor C2 may be coupled to the second node N2, and a second terminal of the second capacitor C2 may be coupled to the first power voltage ELVDD. The third PMOS transistor PT3 may be coupled between a data line DL and the second node N2. A gate terminal of the third PMOS transistor PT3 may receive the compensation control signal TCS. In detail, the first terminal of the third PMOS transistor PT3 may be coupled to the second node N2, a second terminal of the third PMOS transistor PT3 may be coupled to the data line DL, and the gate terminal of the third PMOS transistor PT3 may be coupled to the gate terminal of the second PMOS transistor PT2. The fourth PMOS transistor PT4 may be coupled between a third node N3 and the second node N2. A gate terminal of the fourth PMOS transistor PT4 may receive an emission control signal ECS. In detail, the first terminal of the fourth PMOS transistor PT4 may be coupled to the second node N2, and a second terminal of the fourth PMOS transistor PT4 may be coupled to the third node N3. As illustrated in FIG. 1, the third node N3 is a node at which the second terminal of the fourth PMOS transistor PT4, a first terminal of the fifth PMOS transistor PT5, and a first terminal of the third capacitor C3 are coupled to each other.

[0044] The third capacitor C3 may be coupled between the third node N3 and the gate terminal of the third PMOS transistor PT3. In detail, the first terminal of the third capacitor C3 may be coupled to the third node N3, and a second terminal of the third capacitor C3 may be coupled to the gate terminal of the third PMOS transistor PT3. The fifth PMOS transistor PT5 may be coupled between the data line DL and the third node N3. A gate terminal of the fifth PMOS transistor PT5 may be coupled to a scan line SL. In detail, the first terminal of the fifth PMOS transistor PT5 may be coupled to the third node N3, a second terminal of the fifth PMOS transistor PT5 may be coupled to the data line DL, and the gate terminal of the fifth PMOS transistor PT5 may be coupled to the scan line SL. The data line DL may be coupled to a data driving unit of an organic light emitting display device to provide a data signal (e.g., left image data or

right image data). In addition, the scan line SL may be coupled to a scan driving unit of the organic light emitting display device to provide a scan signal. As described above, the pixel circuit 100 may have a 5T-3C structure that includes the organic light emitting diode OLED, the first through fifth PMOS transistors PT1 through PT5, and the first through third capacitors C1 through C3. An organic light emitting display device having the pixel circuit 100 may implement a stereoscopic image by alternately displaying a left image and a right image based on a simultaneous emission method. For example, the right image data may be sequentially written into each pixel circuit 100 of the organic light emitting display device while the left image is simultaneously displayed by each pixel circuit 100 of the organic light emitting display device. Similarly, the left image data may be sequentially written into each pixel circuit 100 of the organic light emitting display device while the right image is simultaneously displayed by each pixel circuit 100 of the organic light emitting display device.

**[0045]** As illustrated in FIG. 1, the pixel circuit 100 may include a first region FA and a second region SA. In the following description, the first region FA includes the third capacitor C3 and the fifth PMOS transistor PT5, and the second region SA includes the first and second capacitors C1 and C2 and the first through fourth PMOS transistors PT1 through PT4. When the fourth PMOS transistor PT4 turns on, the first region FA may be coupled to the second region SA. When the fourth PMOS transistor PT4 turns off, the first region FA may be separated from the second region SA. In detail, when the fourth PMOS transistor PT4 turns on, the first region FA may be coupled to the second region SA in the pixel circuit 100. As a result, a data signal (e.g., the left image data or the right image data) stored in the third capacitor C3 may be transferred to the second region SA. On the other hand, when the fourth PMOS transistor PT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 100. As a result, the first region FA and the second region SA may simultaneously perform respective operations. In detail, an emission operation may be performed in the second region SA while a preliminary data writing operation is performed in the first region FA. Thus, an operation of the first region FA may be independent from an operation of the second region SA. For example, when the fourth PMOS transistor PT4 turns off in response to the emission control signal ECS, the first image (e.g., the left image or the right image) may be displayed by the first and second PMOS transistors PT1 and PT2, the first and second capacitors C1 and C2, and the organic light emitting diode OLED (i.e., an operation of the second region SA). At the same time, the second image data (e.g., the right image data or the left image data) input through the data line DL may be stored in the third capacitor C3 when the fifth PMOS transistor PT5 turns on in response to a scan signal input through the scan line SL (i.e., an operation of the first region FA). Hereinafter, an operation of the pixel circuit 100 will be described in detail.

**[0046]** FIG. 2 illustrates a diagram of an example in which an organic light emitting display device implements a stereoscopic image based on a simultaneous emission method.

**[0047]** FIG. 2 shows how a stereoscopic image is implemented by alternately displaying a left image L\_IMG and a right image R\_IMG based on a simultaneous emission method. In detail, a stereoscopic image may be implemented by providing the left image L\_IMG and the right image R\_IMG to a left eye and a right eye, respectively. For example, in case of a shutter glasses method, a stereoscopic image may be implemented by opening a left shutter of shutter glasses while the left image L\_IMG is displayed, and by opening a right shutter of shutter glasses while the right image R\_IMG is displayed. Here, these operations may be performed (i.e., repeated) very fast to prevent a viewer from noticing a timing difference between the operations. The viewer sees a stereoscopic image by sequentially watching the left image L\_IMG and the right image R\_IMG.

**[0048]** By comparison, for a sequential emission method, a black image B\_IMG is inserted between a left image L\_IMG and a right image R\_IMG when sequentially displaying the left image L\_IMG and the right image R\_IMG. The black image B\_IMG is inserted to separate the right image R\_IMG from the left image L\_IMG. As a result, due to the black image B\_IMG, a luminance may be decreased and power consumption may be increased.

**[0049]** As illustrated in FIG. 2, an organic light emitting display device having the pixel circuit 100 of FIG. 1 according to an embodiment may display the left image L\_IMG and the right image R\_IMG based on a simultaneous emission method. As a result, a time in which the black image B\_IMG is displayed between the left image L\_IMG and the right image R\_IMG may be reduced or eliminated. In addition, the pixel circuit 100 of FIG. 1 has a structure in which the first region FA and the second region SA may be separated from each other by the fourth PMOS transistor PT4. Thus, the organic light emitting display device having the pixel circuit 100 of FIG. 1 may write right image data into the pixel circuit 100 of FIG. 1 while performing an emission operation of the left image L\_IMG, and may write left image data into the pixel circuit of FIG. 1 while performing an emission operation of the right image R\_IMG. As a result, the organic light emitting display device having the pixel circuit 100 of FIG. 1 may operate at a high speed, which may thus allow an operating frequency of the organic light emitting display device having the pixel circuit 100 of FIG. 1 to be reduced.

**[0050]** As described above, embodiments may provide an improvement in luminance by reducing or eliminating a time in which the black image B\_IMG is displayed in the organic light emitting display device having the pixel circuit 100 of FIG. 1. In addition, the right image data may be stored while an emission operation of the left image L\_IMG is performed, and left image data may be stored when an emission operation of the right image R\_IMG is performed, and thus an operating speed may be improved in the organic light emitting display device having the pixel circuit 100 of FIG. 1.

**[0051]** A general organic light emitting display device that sequentially repeats (i.e., displays) the left image L\_IMG of

60Hz, the black image B\_IMG of 60Hz, the right image R\_IMG of 60Hz, and the black image B\_IMG of 60Hz may use an operating speed of 240Hz to implement a stereoscopic image. By comparison, the organic light emitting display device having the pixel circuit 100 of FIG. 1 may sequentially repeat (i.e., displays) the left image L\_IMG of 60Hz and the right image R\_IMG of 60Hz, and thus may use an operating speed of 120Hz to implement a stereoscopic image.

Further, the organic light emitting display device having the pixel circuit 100 of FIG. 1 may obtain a data charging time two times longer than the general organic light emitting display device, may increase a lifetime (e.g., by reducing a peak current by half), and may reduce power consumption by half (e.g., by improving luminance).

**[0052]** The pixel circuit 100 of FIG. 1 may sequentially perform a preliminary data writing operation, a reset operation, a threshold voltage compensation operation, a data writing operation, and an emission operation to display the left image L\_IMG or the right image R\_IMG (i.e., one frame) based on a simultaneous emission method. The preliminary data writing operation may be sequentially performed (by each scan line) for all pixel circuits 100 of the organic light emitting display device, whereas the reset operation, the threshold voltage compensation operation, the data writing operation, and/or the emission operation may be simultaneously performed for all pixel circuits 100 of the organic light emitting display device.

**[0053]** FIG. 3 illustrates a diagram of an example in which a stereoscopic image is implemented by an organic light emitting display device having the pixel circuit of FIG. 1.

**[0054]** FIG. 3 shows how a stereoscopic image is implemented by alternately performing a first display operation for displaying a first image (e.g., a left image L\_IMG) and a second display operation for displaying a second image (e.g., a right image R\_IMG). The first display operation and the second display operation may be performed in the pixel circuit 100 of FIG. 1 based on a simultaneous emission method.

**[0055]** The first display operation for displaying the first image L\_IMG may include a first preliminary data writing operation FPDP, a first reset operation FIP, a first threshold voltage compensation operation FVP, a first data writing operation FWP, and a first emission operation FEP. The second display operation for displaying the second image R\_IMG may include a second preliminary data writing operation SPDP, a second reset operation SIP, a second threshold voltage compensation operation SVP, a second data writing operation SWP, and a second emission operation SEP. The first emission operation FEP of the first display operation and the second preliminary data writing operation SPDP of the second display operation may be simultaneously performed in the pixel circuit 100 of FIG. 1. Similarly, the second emission operation SEP of the second display operation and the first preliminary data writing operation FPDP of the first display operation may be simultaneously performed in the pixel circuit 100 of FIG. 1. Thus, the first emission operation FEP of the first display operation may overlap the second preliminary data writing operation SPDP of the second display operation, and the second emission operation SEP of the second display operation may overlap the first preliminary data writing operation FPDP of the first display operation.

**[0056]** As illustrated in FIG. 3, a viewer may sequentially and repeatedly watch the left image L\_IMG, the black image B\_IMG, the right image R\_IMG, and the black image B\_IMG. Here, since these operations may be performed (i.e., repeated) very fast so that the viewer does not notice a timing difference between these operations. The viewer may see a stereoscopic image by sequentially and repeatedly watching the left image L\_IMG, the black image B\_IMG, the right image R\_IMG, and the black image B\_IMG. For convenience of descriptions, it is illustrated in FIG. 3 that a time in which the black image B\_IMG is displayed is relatively long. However, a time in which the black image B\_IMG is displayed may in practice be much shorter than a time in which the left image L\_IMG is displayed and a time in which the right image R\_IMG is displayed because the first display operation for displaying the left image L\_IMG and the second display operation for displaying the right image R\_IMG may be performed based on a simultaneous emission method. According to certain embodiments, a ratio of the time in which the black image B\_IMG is displayed and the time in which the left image L\_IMG or the right image R\_IMG are displayed is less than 1/2. More preferably, said ratio may be less than 1/3 and even more preferably less than 1/10. As a result, the organic light emitting display device having the pixel circuit 100 of FIG. 1 may improve luminance and may reduce an operating frequency. Hereinafter, an operation of the pixel circuit 100 of FIG. 1 will be described in detail with reference to FIGS. 4A through 4E.

**[0057]** FIGS. 4A through 4E illustrate timing diagrams of an example operation of the pixel circuit of FIG. 1.

**[0058]** A first display operation for displaying a first image (e.g., a left image) may include a first preliminary data writing operation FPDP, a first reset operation FIP, a first threshold voltage compensation operation FVP, a first data writing operation FWP, and a first emission operation FEP. Similarly, a second display operation for displaying a second image (e.g., a right image) may include a second preliminary data writing operation SPDP, a second reset operation SIP, a second threshold voltage compensation operation SVP, a second data writing operation SWP, and a second emission operation SEP.

**[0059]** For convenience of description, FIGS. 4A through 4E, focus on the first display operation for displaying the first image.

**[0060]** Referring to FIGS. 4A-4E, the first preliminary data writing operation FPDP, the first reset operation FIP, the first threshold voltage compensation operation FVP, the first data writing operation FWP, and the first emission operation FEP of the first display operation may respectively correspond to a first preliminary data writing period PA, a first reset

period PB, a first threshold voltage compensation period PC, a first data writing period PD, and a first emission period PE (similarly, the second preliminary data writing operation SPDP, the second reset operation SIP, the second threshold voltage compensation operation SVP, the second data writing operation SWP, and the second emission operation SEP may respectively correspond to a second preliminary data writing period PA, a second reset period PB, a second threshold voltage compensation period PC, a second data writing period PD, and a second emission period PE). Thus, the present inventive concept may be applied to a stereoscopic image display system employing a shutter glasses method, a stereoscopic image display system employing a parallax barrier method, etc.

**[0061]** The preliminary data writing operation (i.e., the first preliminary data writing operation FPDP or the second preliminary data writing operation SPDP) may be sequentially performed for all pixel circuits 100 of the organic light emitting display device by each scan line SL, whereas the reset operation (i.e., the first reset operation FIP or the second reset operation SIP), the threshold voltage compensation operation (i.e., the first threshold voltage compensation operation FVP or the second threshold voltage compensation operation SVP), the data writing operation (i.e., the first data writing operation FWP or the second data writing operation SWP), and/or the emission operation (i.e., the first emission operation FEP or the second emission operation SEP) may be simultaneously performed for all pixel circuits 100 of the organic light emitting display device.

**[0062]** In an example embodiment, a first power voltage ELVDD may have a plurality of voltage levels, and a second power voltage ELVSS may have a fixed voltage level (e.g., 0V). In this case, a structure for providing the second power voltage ELVSS may be simplified because the second power voltage ELVSS has a fixed voltage level. However, a structure for providing the first power voltage ELVDD may be complicated because the first power voltage ELVDD has a plurality of voltage levels (e.g., a negative voltage level may be needed). In another example embodiment, the first power voltage ELVDD may have a plurality of voltage levels, and the second power voltage ELVSS may also have a plurality of voltage levels. In this case, driving signal waveforms may be simplified. However, a structure for providing the first power voltage ELVDD and a structure for providing the second power voltage ELVSS may be complicated. In still another example embodiment, the first power voltage ELVDD may have a fixed voltage level (e.g., 12V), and the second power voltage may have a plurality of voltage levels. In this case, a structure for providing the first power voltage ELVDD may be simplified because the first power voltage ELVDD has a fixed voltage level. However, a structure for providing the second power voltage ELVSS may be complicated because the second power voltage ELVSS has a plurality of voltage levels (e.g., a positive voltage level may be needed). Thus, the first power voltage ELVDD and the second power voltage ELVSS may be determined according to required conditions. For convenience, in the following description, the first power voltage ELVDD and the second power voltage ELVSS have a high voltage level or a low voltage level.

**[0063]** Referring to FIG. 4A, the first preliminary data writing operation FPDP may be performed in the first preliminary data writing period PA. As described above, the first preliminary data writing operation FPDP of the first display operation for displaying the first image and the second emission operation SEP of the second display operation for displaying the second image may be simultaneously performed. Thus, the second image may be displayed based on second image data stored in each pixel circuit 100 while first image data DATA is written into each pixel circuit 100 in the first preliminary data writing period PA. In detail, in the first preliminary data writing period PA, the first power voltage ELVDD may have a high voltage level, and the second power voltage ELVSS may have a logic low level. In addition, the emission control signal ECS may have a high voltage level, and the compensation control signal TCS may also have a high voltage level. Thus, the third and fourth PMOS transistors PT3 and PT4 may turn off in the pixel circuit 100 of FIG. 1. When the fourth PMOS transistor PT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 100 of FIG. 1, and an operation of the first region FA may be independent from an operation of the second region SA. As a result, in the first region FA, when the fifth PMOS transistor PT5 turns on in response to a scan signal that is applied through the scan line SL, the first image data DATA that is applied through the data line DL may be stored in the third capacitor C3. At the same time, in the second region SA, the organic light emitting diode OLED may emit light based on a current flowing from the first power voltage ELVDD having a high voltage level to the second power voltage ELVSS having a low voltage level.

**[0064]** The first power voltage ELVDD, the second power voltage ELVSS, the emission control signal ECS, and the compensation control signal TCS may be simultaneously applied to all pixel circuits 100 of the organic light emitting display device. On the other hand, the first image data DATA may be sequentially applied to all pixel circuits 100 of the organic light emitting display device (i.e., when the fifth PMOS transistor PT5 turns on in response to a scan signal SCAN(n) having a low voltage level (see FIG. 1)). Referring to FIG. 4A, the first power voltage ELVDD, the second power voltage ELVSS, the emission control signal ECS, and the compensation control signal TCS may be simultaneously applied to all pixel circuits 100 in all periods PA, PB, PC, PD, and PE, whereas the first image data DATA may be sequentially applied to all pixel circuits 100 only in the first preliminary data writing period PA. Thus, the first preliminary data writing operation FPDP of the first display operation may be sequentially performed for all pixel circuits 100, and the second emission operation SEP of the second display operation may be simultaneously performed for all pixel circuits 100.

**[0065]** As described above, in the organic light emitting display device having the pixel circuit 100 of FIG. 1, while the second image (i.e., the right image or the left image) is displayed by each pixel circuit 100, the first image data DATA (i.e., the left image data or the right image data) may be stored in the third capacitor C3 of each pixel circuit 100. Similarly, while the first image (i.e., the left image or the right image) is displayed by each pixel circuit 100, the second image data

**[0066]** Referring to FIG. 4B, the first reset operation FIP may be performed in the first reset period PB. In detail, in the first reset period PB, the first power voltage ELVDD may have a low voltage level, and the second power voltage ELVSS may have a high voltage level. In addition, the emission control signal ECS may have a high voltage level, and the compensation control signal TCS may also have a high voltage level. Thus, the third and fourth PMOS transistors PT3 and PT4 may turn off in the pixel circuit 100 of FIG. 1. When the fourth PMOS transistor PT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 100 of FIG. 1 and operation of the first region FA may be independent from an operation of the second region SA. The second power voltage ELVSS is higher than the first power voltage ELVDD. Thus, the first reset operation FIP may be performed in the second region SA, and an anode electrode of the organic light emitting diode OLED may be initialized to have the second power voltage ELVSS, such that the pixel circuit 100 of FIG. 1 may be initialized and reset in the first reset period PB. The first power voltage ELVDD, the second power voltage ELVSS, the emission control signal ECS, and the compensation control signal TCS may be simultaneously applied to all pixel circuits 100 of the organic light emitting display device. Thus, referring to FIG. 4B, the first reset operation FIP of the first display operation may be simultaneously performed for all pixel circuits 100 of the organic light emitting display device.

**[0067]** Referring to FIG. 4C, the first threshold voltage compensation operation FVP may be performed in the first threshold voltage compensation period PC. In detail, in the first threshold voltage compensation period PC, the first power voltage ELVDD may have a high voltage level, and the second power voltage ELVSS may also have a high voltage level. In addition, the emission control signal ECS may have a high voltage level, and the compensation control signal TCS may have a low voltage level. Thus, in the pixel circuit 100 of FIG. 1, the second and third PMOS transistors PT2 and PT3 may turn on, and the fourth and fifth PMOS transistors PT4 and PT5 may turn off. When the fourth PMOS transistor PT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 100 of FIG. 1, and an operation of the first region FA may be independent from an operation of the second region SA. As a result, a gate terminal of the first PMOS transistor PT1 may have a voltage ELVDD-V<sub>th</sub> (generated by subtracting a threshold voltage V<sub>th</sub> of the first PMOS transistor PT1 from the first power voltage ELVDD). In addition, a first voltage V<sub>0</sub> (i.e., a specific high voltage) may be stored in the second capacitor C2. The first power voltage ELVDD, the second power voltage ELVSS, the emission control signal ECS, and the compensation control signal TCS may be simultaneously applied to all pixel circuits 100 of the organic light emitting display device. Thus, the first threshold voltage compensation operation FVP of the first display operation may be simultaneously performed for all pixel circuits 100 of the organic light emitting display device.

**[0068]** Referring to FIG. 4D, the first data writing operation FWP may be performed in the first data writing period PD. In detail, in the first data writing period PD, the first power voltage ELVDD may have a high voltage level, and the second power voltage ELVSS may also have a high voltage level. In addition, the emission control signal ECS may have a low voltage level, and the compensation control signal TCS may have a high voltage level. Thus, in the pixel circuit 100 of FIG. 1, the fourth and fifth PMOS transistors PT4 and PT5 may turn on, and the second and third PMOS transistors PT2 and PT3 may turn off. When the fourth PMOS transistor PT4 turns on, the first region FA may be coupled to the second region SA in the pixel circuit 100 of FIG. 1 and, when the first region FA is coupled to the second region SA, the first image data DATA that is stored in the third capacitor C3 by the first preliminary data writing operation FPDP may be transferred to the second region SA. As a result, a voltage of a gate terminal (i.e., the first node N1) of the first PMOS transistor PT1 may be changed by the first image data DATA. In detail, when the first image data DATA is provided to the second region SA, a voltage of the gate terminal (i.e., the first node N1) of the first PMOS transistor PT1 may be determined according to [Expression 1] and [Expression 2] below.

**[Expression 1]**

$$V_{eff} = \frac{C_{HOLD} \cdot V_{DATA} + (C_{ST} + C_{VTH}) \cdot V_0}{C_{HOLD} + C_{ST} + C_{VTH}}$$

**[0069]** (where, V<sub>eff</sub> denotes a voltage corresponding to an effective data, C<sub>HOLD</sub> denotes a capacitance of the third capacitor C3, V<sub>DATA</sub> denotes a voltage corresponding to the first image data DATA, C<sub>ST</sub> denotes a capacitance of the second capacitor C2, C<sub>VTH</sub> denotes a capacitance of the first capacitor C1, and V<sub>0</sub> denotes the first voltage stored in the second capacitor C2.)

## [Expression 2]

$$V_{GTI} = V_{ELVDD} - V_{TH} + (V_{eff} - V_0)$$

[0070] (where,  $V_{GTI}$  denotes a voltage of the gate terminal of the first PMOS transistor PT1,  $V_{ELVDD}$  denotes a voltage corresponding to the first power voltage ELVDD, and  $V_{TH}$  denotes a threshold voltage of the first PMOS transistor PT1.)

[0071] Referring to FIG. 4E, the first emission operation FEP may be performed in the first emission period PE. In detail, in the first emission period PE, the first power voltage ELVDD may have a high voltage level, and the second power voltage ELVSS may have a low voltage level. In addition, the emission control signal ECS may have a high voltage level, and the compensation control signal TCS may also have a high voltage level. Thus, the third and fourth PMOS transistors PT3 and PT4 may turn off in the pixel circuit 100 of FIG. 1. When the fourth PMOS transistor PT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 100 of FIG. 1, and an operation of the first region FA may be independent from an operation of the second region SA. Similar to FIG. 4A, the second preliminary data writing operation SPDP of the second display operation and the first emission operation FEP of the first display operation may be simultaneously performed. Thus, the second image data may be written into each pixel circuit 100 while the first image is displayed based on the first image data DATA stored in each pixel circuit 100. As a result, in the first region FA, when the fifth PMOS transistor PT5 turns on in response to a scan signal applied through the scan line SL, the second image data applied through the data line DL may be stored in the third capacitor C3. At the same time, in the second region SA, the organic light emitting diode OLED may emit light based on a current flowing from the first power voltage ELVDD having a high voltage level to the second power voltage ELVSS having a low voltage level.

[0072] The first power voltage ELVDD, the second power voltage ELVSS, the emission control signal ECS, and the compensation control signal TCS may be simultaneously applied to all pixel circuits 100 of the organic light emitting display device. On the other hand, the second image data may be sequentially applied to all pixel circuits 100 of the organic light emitting display device (i.e., when the fifth PMOS transistor PT5 turns on in response to a scan signal SCAN[n] having a low voltage level). Thus, the first emission operation FEP of the first display operation may be simultaneously performed for all pixel circuits 100, and the second preliminary data writing operation SPDP of the second display operation may be sequentially performed for all pixel circuits 100.

[0073] A current flowing through the organic light emitting diode OLED may be determined based on a voltage of the gate terminal of the first PMOS transistor PT1. That is, a current flowing through the organic light emitting diode OLED may be substantially determined based on the effective data  $V_{eff}$  and the first voltage  $V_0$  stored in the second capacitor C2. In detail, the organic light emitting display device may operate based on a simultaneous emission method in which all pixel circuits 100 simultaneously emit light. Here, a current flowing through the organic light emitting diode OLED of each pixel circuit 100 may be determined according to [Expression 3] below.

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{eff} - V_0)^2$$

[0074] (where,  $I_D$  denotes a current flowing through the organic light emitting diode OLED,  $\frac{1}{2} \mu C_{ox} \frac{W}{L}$  is a unique constant,  $V_{GS}$  denotes a voltage difference between the gate terminal and the source terminal of the first PMOS transistor PT1,  $V_{TH}$  denotes a threshold voltage of the first PMOS transistor PT1,  $V_{eff}$  denotes a voltage corresponding to the effective data, and  $V_0$  denotes the first voltage stored in the second capacitor C2.)

[0075] Although the first display operation for displaying the first image (i.e., the first preliminary data writing period PA, the first reset period PB, the first threshold voltage compensation period PC, the first data writing period PD, and the first emission period PE) and the second display operation for displaying the second image (i.e., the second preliminary data writing period PA, the second reset period PB, the second threshold voltage compensation period PC, the second data writing period PD, and the second emission period PE) are described with reference to FIGS. 4A through 4E, it should be understood that the driving signal waveforms illustrated in FIGS. 4A through 4E are simplified for convenience of descriptions. Thus, for example, the pixel circuit 100 of FIG. 1 may operate based on more complicated driving signal waveforms.

[0076] FIG. 5 illustrates a timing diagram of another example of operation of the pixel circuit of FIG. 1.

[0077] Referring to FIG. 5, a period of a first display operation for displaying a first image (e.g., a left image) may include a first preliminary data writing period PA, a first off-bias applying period PF, a first reset period PB, a first threshold

voltage compensation period PC, a first data writing period PD, and a first emission period PE. Similarly, a period of a second display operation for displaying a second image (e.g., a right image) may include a second preliminary data writing period PA, a second off-bias applying period PF, a second reset period PB, a second threshold voltage compensation period PC, a second data writing period PD, and a second emission period PE. For convenience, the following description of FIG. 5 will focus on the first display operation for displaying the first image. As described above, the first and second power voltages ELVDD and ELVSS may be determined according to required conditions. For convenience of description, however, it will be described below that each of the first power voltage ELVDD and the second power voltage ELVSS have a high voltage level or a low voltage level. In addition, the first preliminary data writing period PA, the first reset period PB, the first threshold voltage compensation period PC, the first data writing period PD, and the first emission period PE are described above, and details thereof will not be repeated below.

**[0078]** As illustrated in FIG. 5, a period of the first display operation for displaying the first image (e.g., the left image) may include the first off-bias applying period PF prior to the first reset period PB. The first off-bias applying period PF may be used as a period for improving a step response waveform by applying an off-bias to the pixel circuit 100 of FIG. 1. Thus, the first off-bias applying period PF may be set to reduce or prevent crosstalk in the organic light emitting display device. For example, the first off-bias applying period PF may be set to prevent a hysteresis (i.e., shift) of a characteristic curve of the first PMOS transistor PT1 (i.e., a driving transistor). As a result, a position of a characteristic curve of the first PMOS transistor PT1 may be fixed (i.e., may be reset) in the first off-bias applying period PF before a threshold voltage of the first PMOS transistor PT1 is compensated. Thus, a position of a characteristic curve of the first PMOS transistor PT1 may be fixed regardless of a data signal (e.g., the left image data or the right image data) of a previous frame.

**[0079]** In detail, in the first off-bias applying period PF, the emission control signal ECS may have a high voltage level, and the compensation control signal TCS may have a low voltage level. In addition, the second power voltage ELVSS may have a high voltage level, and the first power voltage ELVDD may have a low voltage level. Hence, the fourth PMOS transistor PT4 may turn off, and the second and third PMOS transistors PT2 and PT3 may turn on. When the fourth PMOS transistor PT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 100 of FIG. 1, and an operation of the first region FA may be independent from an operation of the second region SA. At this time, the second region SA may perform the first off-bias applying operation because the second power voltage ELVSS is maintained to be greater than the first power voltage ELVDD for a predetermined time while the second and third PMOS transistors PT2 and PT3 are turned on.

**[0080]** Although not illustrated in FIG. 5, a period in which the second power voltage ELVSS has a high voltage level and the first power voltage ELVDD also has a high voltage level may be inserted between the first off-bias applying period PF and the first reset period PB. In another implementation, a period in which the second power voltage ELVSS has a low voltage level and the first power voltage ELVDD also has a low voltage level may be inserted between the first off-bias applying period PF and the first reset period PB. The period may prevent interference between the first off-bias applying operation and the first reset operation when the first display operation is performed. Although the first display operation for displaying the first image (i.e., the first preliminary data writing period PA, the first off-bias applying period PF, the first reset period PB, the first threshold voltage compensation period PC, the first data writing period PD, and the first emission period PE) and the second display operation for displaying the second image (i.e., the second preliminary data writing period PA, the second off-bias applying period PF, the second reset period PB, the second threshold voltage compensation period PC, the second data writing period PD, and the second emission period PE) are described with reference to FIG. 5, it should be understood that the driving signal waveforms illustrated in FIG. 5 are simplified for convenience of description, and thus other driving signal waveforms may be used for operating the pixel circuit 100 of FIG. 1.

**[0081]** FIG. 6 illustrates a circuit diagram of a pixel circuit 200 according to exemplary embodiments.

**[0082]** Referring to FIG. 6, the pixel circuit 200 may include an organic light emitting diode OLED, first through fifth PMOS transistors PT1 through PT5, and first through third capacitors C1 through C3. The pixel circuit 200 may have a 5T-3C structure (i.e., a structure having five transistors and three capacitors). In an example embodiment, the pixel circuit 200 may further include a fourth capacitor C4 coupled between an anode electrode and a cathode electrode of the organic light emitting diode OLED.

**[0083]** The connections of the first through fifth PMOS transistors PT1 through PT5, and of the first and second capacitors C1 and C2 are the same as described for the embodiment of Fig. 1 and will be here therefore omitted.

**[0084]** The third capacitor C3 may be coupled between the third node N3 and a sustain power voltage VSUS. In detail, the first terminal of the third capacitor C3 may be coupled to the third node N3, and a second terminal of the third capacitor C3 may be coupled to the sustain power voltage VSUS. In FIG. 6, since the sustain power voltage VSUS is applied to the third capacitor C3, a fluctuation of a data signal (e.g., left image data or right image data) stored in the third capacitor C3 may be prevented. That is, the sustain power voltage VSUS may be a predetermined DC voltage to prevent the fluctuation of the data signal stored in the third capacitor C3.

**[0085]** As illustrated in FIG. 6, the pixel circuit 200 may include a first region FA and a second region SA. In the following description, the first region FA includes the third capacitor C3 and the fifth PMOS transistor PT5, and the second region

SA includes the first and second capacitors C1 and C2 and the first through fourth PMOS transistors PT1 through PT4. When the fourth PMOS transistor PT4 turns on, the first region FA may be coupled to the second region SA. When the fourth PMOS transistor PT4 turns off, the first region FA may be separated from the second region SA. In detail, when the fourth PMOS transistor PT4 turns on, the first region FA may be coupled to the second region SA in the pixel circuit 200. As a result, a data signal (e.g., the left image data or the right image data) stored in the third capacitor C3 may be transferred to the second region SA. On the other hand, when the fourth PMOS transistor PT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 200. As a result, the first region FA and the second region SA may simultaneously perform respective operations.

**[0086]** FIG. 7 illustrates a circuit diagram of a pixel circuit 300 according to another exemplary embodiment.

**[0087]** Referring to FIG. 7, the pixel circuit 300 may include an organic light emitting diode OLED, first through fifth n-channel metal oxide semiconductor (NMOS) transistors NT1 through NT5, and first through third capacitors C1 through C3. The pixel circuit 300 may have a 5T-3C structure (i.e., a structure having five transistors and three capacitors). In an example embodiment, the pixel circuit 300 may further include a fourth capacitor C4 coupled between an anode electrode and a cathode electrode of the organic light emitting diode OLED.

**[0088]** The organic light emitting diode OLED may be coupled between a first power voltage ELVDD and the first NMOS transistor NT1. In detail, an anode electrode of the organic light emitting diode OLED may be coupled to the first power voltage ELVDD, and a cathode electrode of the organic light emitting diode OLED may be coupled to a first terminal of the first NMOS transistor NT1. Thus, the organic light emitting diode OLED may emit light based on a current that is controlled by the first NMOS transistor NT1. The first NMOS transistor NT1 may be coupled between a second power voltage ELVSS and the cathode electrode of the organic light emitting diode OLED. A gate terminal of the first NMOS transistor NT1 may be coupled to a first node N1. The first NMOS transistor NT1 may be a driving transistor that controls a current flowing through the organic light emitting diode OLED. As illustrated in FIG. 7, the first node N1 is a node at which a first terminal of the first capacitor C1, a first terminal of the second NMOS transistor NT2, and the gate terminal of the first NMOS transistor NT1 are coupled to each other. The second NMOS transistor NT2 may be coupled between the first node N1 and the cathode electrode of the organic light emitting diode OLED. A gate terminal of the second NMOS transistor NT2 may receive a compensation control signal TCS. In detail, the first terminal of the second NMOS transistor NT2 may be coupled to the first node N1, and a second terminal of the second NMOS transistor NT2 may be coupled to the first terminal of the first NMOS transistor NT1. Thus, when the second NMOS transistor NT2 turns on in response to the compensation control signal TCS, the first NMOS transistor NT1 may be diode-coupled.

**[0089]** The first capacitor C1 may be coupled between the first node N1 and a second node N2. In detail, the first terminal of the first capacitor C1 may be coupled to the first node N1, and a second terminal of the first capacitor C1 may be coupled to the second node N2. The first capacitor C1 may be a threshold voltage compensation capacitor. As illustrated in FIG. 7, the second node N2 is a node at which the second terminal of the first capacitor C1, a first terminal of the second capacitor C2, a first terminal of the third NMOS transistor NT3, and a first terminal of the fourth NMOS transistor NT4 are coupled to each other. The second capacitor C2 may be coupled between the second power voltage ELVSS and the second node N2. The second capacitor C2 may be a storage capacitor. In detail, the first terminal of the second capacitor C2 may be coupled to the second node N2, and a second terminal of the second capacitor C2 may be coupled to the second power voltage ELVSS. The third NMOS transistor NT3 may be coupled between a data line DL and the second node N2. A gate terminal of the third NMOS transistor NT3 may receive the compensation control signal TCS. In detail, the first terminal of the third NMOS transistor NT3 may be coupled to the second node N2, a second terminal of the third NMOS transistor NT3 may be coupled to the data line DL, and the gate terminal of the third NMOS transistor NT3 may be coupled to the gate terminal of the second NMOS transistor NT2. The fourth NMOS transistor NT4 may be coupled between a third node N3 and the second node N2. A gate terminal of the fourth NMOS transistor NT4 may receive an emission control signal ECS. In detail, the first terminal of the fourth NMOS transistor NT4 may be coupled to the second node N2, and a second terminal of the fourth NMOS transistor NT4 may be coupled to the third node N3. As illustrated in FIG. 7, the third node N3 is a node at which the second terminal of the fourth NMOS transistor NT4, a first terminal of the fifth NMOS transistor NT5, and a first terminal of the third capacitor C3 are coupled to each other.

**[0090]** The third capacitor C3 may be coupled between the third node N3 and the gate terminal of the third NMOS transistor NT3. In detail, the first terminal of the third capacitor C3 may be coupled to the third node N3, and a second terminal of the third capacitor C3 may be coupled to the gate terminal of the third NMOS transistor NT3. The fifth NMOS transistor NT5 may be coupled between the data line DL and the third node N3. A gate terminal of the fifth NMOS transistor NT5 may be coupled to a scan line SL. In detail, the first terminal of the fifth NMOS transistor NT5 may be coupled to the third node N3, a second terminal of the fifth NMOS transistor NT5 may be coupled to the data line DL, and the gate terminal of the fifth NMOS transistor NT5 may be coupled to the scan line SL.

**[0091]** As described above, the pixel circuit 300 may have a 5T-3C structure that includes the organic light emitting diode OLED, the first through fifth NMOS transistors NT1 through NT5, and the first through third capacitors C1 through C3. An organic light emitting display device having the pixel circuit 300 may implement a stereoscopic image by alternately displaying a left image and a right image based on a simultaneous emission method such as the method described in

relation to Fig. 1.

**[0092]** As illustrated in FIG. 7, the pixel circuit 300 may include a first region FA and a second region SA. In the following description, the first region FA includes the third capacitor C3 and the fifth NMOS transistor NT5, and the second region SA includes the first and second capacitors C1 and C2 and the first through fourth NMOS transistors NT1 through NT4. When the fourth NMOS transistor NT4 turns on, the first region FA may be coupled to the second region SA. When the fourth NMOS transistor NT4 turns off, the first region FA may be separated from the second region SA. In detail, when the fourth NMOS transistor NT4 turns on, the first region FA may be coupled to the second region SA in the pixel circuit 300. As a result, a data signal (e.g., the left image data or the right image data) stored in the third capacitor C3 may be transferred to the second region SA. On the other hand, when the fourth NMOS transistor NT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 300. As a result, the first region FA and the second region SA may simultaneously perform respective operations.

**[0093]** In detail, an emission operation may be performed in the second region SA while a preliminary data writing operation is performed in the first region FA. Thus, an operation of the first region FA may be independent from an operation of the second region SA. For example, when the fourth NMOS transistor NT4 turns off in response to the emission control signal ECS, the first image (e.g., the left image or the right image) may be displayed by the first and second NMOS transistors NT1 and NT2, the first and second capacitors C1 and C2, and the organic light emitting diode OLED (i.e., an operation of the second region SA). At the same time, the second image data (e.g., the right image data or the left image data) input through the data line DL may be stored in the third capacitor C3 when the fifth NMOS transistor NT5 turns on in response to a scan signal input through the scan line SL (i.e., an operation of the first region FA). Hereinafter, an operation of the pixel circuit 300 will be described in detail.

**[0094]** FIGS. 8A through 8E illustrate timing diagrams of an example operation of the pixel circuit of FIG. 7.

**[0095]** A detailed description of the first display operation for displaying a first image (e.g., a left image) and a second display operation for displaying a second image (e.g., a right image) has already been disclosed in relation to FIGS. 4A through 4E and will be here therefore omitted. For convenience, the following description of FIGS. 8A through 8E will focus on the first display operation for displaying the first image. The first power voltage ELVDD and the second power voltage ELVSS may be determined according to required conditions. For convenience of description, it will be described below the case in which each of the first power voltage ELVDD and the second power voltage ELVSS has a high voltage level or a low voltage level.

**[0096]** Referring to FIG. 8A, the first preliminary data writing operation FPDP may be performed in the first preliminary data writing period PA. As described above, the first preliminary data writing operation FPDP of the first display operation for displaying the first image and the second emission operation SEP of the second display operation for displaying the second image may be simultaneously performed. Thus, the second image may be displayed based on second image data stored in each pixel circuit 300 while first image data DATA is written into each pixel circuit 300 in the first preliminary data writing period PA. In detail, in the first preliminary data writing period PA, the first power voltage ELVDD may have a high voltage level, and the second power voltage ELVSS may have a logic low level. In addition, an emission control signal ECS may have a low voltage level, and a compensation control signal TCS may also have a low voltage level. Thus, the third and fourth NMOS transistors NT3 and NT4 may turn off in the pixel circuit 300 of FIG. 7. When the fourth NMOS transistor NT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 300 of FIG. 7, and an operation of the first region FA may be independent from an operation of the second region SA. As a result, in the first region FA, when the fifth NMOS transistor NT5 turns on in response to a scan signal that is applied through the scan line SL, the first image data DATA that is applied through the data line DL may be stored in the third capacitor C3. At the same time, in the second region SA, the organic light emitting diode OLED may emit light based on a current flowing from the first power voltage ELVDD having a high voltage level to the second power voltage ELVSS having a low voltage level.

**[0097]** As described above, in the organic light emitting display device having the pixel circuit 300 of FIG. 7, while the second image (i.e., the right image or the left image) is displayed by each pixel circuit 300, the first image data DATA (i.e., the left image data or the right image data) may be stored in the third capacitor C3 of each pixel circuit 300. Similarly, while the first image (i.e., the left image or the right image) is displayed by each pixel circuit 300, the second image data DATA (i.e., the right image data or the left image data) may be stored in the third capacitor C3 of each pixel circuit 300.

**[0098]** Referring to FIG. 8B, the first reset operation FIP may be performed in the first reset period PB. In detail, in the first reset period PB, the first power voltage ELVDD may have a low voltage level, and the second power voltage ELVSS may have a high voltage level. In addition, the emission control signal ECS may have a low voltage level, and the compensation control signal TCS may also have a low voltage level. Thus, the third and fourth NMOS transistors NT3 and NT4 may turn off in the pixel circuit 300 of FIG. 7. When the fourth NMOS transistor NT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 300 of FIG. 7, and an operation of the first region FA may be independent from an operation of the second region SA. Since the second power voltage ELVSS is higher than the first power voltage ELVDD, the first reset operation FIP may be performed in the second region SA.

**[0099]** Referring to FIG. 8C, the first threshold voltage compensation operation FVP may be performed in the first

threshold voltage compensation period PC. In detail, in the first threshold voltage compensation period PC, the first power voltage ELVDD may have a high voltage level, and the second power voltage ELVSS may also have a high voltage level. In addition, the emission control signal ECS may have a low voltage level, and the compensation control signal TCS may have a high voltage level. Thus, in the pixel circuit 300 of FIG. 7, the second and third NMOS transistors NT2 and NT3 may turn on, and the fourth and fifth NMOS transistors NT4 and NT5 may turn off. When the fourth NMOS transistor NT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 300 of FIG. 7, and an operation of the first region FA may be independent from an operation of the second region SA. When the second and third NMOS transistors NT2 and NT3 turn on, the first threshold voltage compensation operation FVP may be performed in the second region SA.

**[0100]** Referring to FIG. 8D, the first data writing operation FWP may be performed in the first data writing period PD. In detail, in the first data writing period PD, the first power voltage ELVDD may have a high voltage level, and the second power voltage ELVSS may also have a high voltage level. In addition, the emission control signal ECS may have a high voltage level, and the compensation control signal TCS may have a low voltage level. Thus, in the pixel circuit 300 of FIG. 7, the fourth and fifth NMOS transistors NT4 and NT5 may turn on, and the second and third NMOS transistors NT2 and NT3 may turn off. When the fourth NMOS transistor NT4 turns on, the first region FA may be coupled to the second region SA in the pixel circuit 300 of FIG. 7. When the first region FA is coupled to the second region SA, the first image data DATA that is stored in the third capacitor C3 by the first preliminary data writing operation FPDP may be transferred to the second region SA. As a result, a voltage of a gate terminal (i.e., the first node N1) of the first NMOS transistor NT1 may be changed by the first image data DATA.

**[0101]** Referring to FIG. 8E, the first emission operation FEP may be performed in the first emission period PE. In detail, in the first emission period PE, the first power voltage ELVDD may have a high voltage level, and the second power voltage ELVSS may have a low voltage level. In addition, the emission control signal ECS may have a low voltage level, and the compensation control signal TCS may also have a low voltage level. Thus, the third and fourth NMOS transistors NT3 and NT4 may turn off in the pixel circuit 300 of FIG. 7. When the fourth NMOS transistor NT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 300 of FIG. 7, and an operation of the first region FA may be independent from an operation of the second region SA. Similar to FIG. 8A, the second preliminary data writing operation SPDP of the second display operation and the first emission operation FEP of the first display operation may be simultaneously performed. Thus, the second image data may be written into each pixel circuit 300 while the first image is displayed based on the first image data DATA stored in each pixel circuit 300. As a result, in the first region FA, when the fifth NMOS transistor NT5 turns on in response to a scan signal applied through the scan line SL, the second image data applied through the data line DL may be stored in the third capacitor C3. At the same time, in the second region SA, the organic light emitting diode OLED may emit light based on a current flowing from the first power voltage ELVDD having a high voltage level to the second power voltage ELVSS having a low voltage level.

**[0102]** Although the first display operation for displaying the first image (i.e., the first preliminary data writing period PA, the first reset period PB, the first threshold voltage compensation period PC, the first data writing period PD, and the first emission period PE) and the second display operation for displaying the second image (i.e., the second preliminary data writing period PA, the second reset period PB, the second threshold voltage compensation period PC, the second data writing period PD, and the second emission period PE) are described with reference to FIGS. 8A through 8E, it should be understood that the driving signal waveforms illustrated in FIGS. 8A through 8E are simplified for convenience of description. Thus, the pixel circuit 300 of FIG. 7 may operate based on more complicated driving signal waveforms.

**[0103]** FIG. 9 illustrates a circuit diagram of a pixel circuit 400 according to another exemplary embodiment.

**[0104]** Referring to FIG. 9, the pixel circuit 400 may include an organic light emitting diode OLED, first through fifth NMOS transistors NT1 through NT5, and first through third capacitors C1 through C3. The pixel circuit 400 may have a 5T-3C structure (i.e., a structure having five transistors and three capacitors). In an example embodiment, the pixel circuit 400 may further include a fourth capacitor C4 coupled between an anode electrode and a cathode electrode of the organic light emitting diode OLED.

**[0105]** The connections of the first through fifth NMOS transistors NT1 through NT5, and of the first and second capacitors C1 and C2 are the same as described for the embodiment of Fig. 7 and will be here therefore omitted.

**[0106]** The third capacitor C3 may be coupled between the third node N3 and a sustain power voltage VSUS. In detail, the first terminal of the third capacitor C3 may be coupled to the third node N3, and a second terminal of the third capacitor C3 may be coupled to the sustain power voltage VSUS. In FIG. 9, since the sustain power voltage VSUS is applied to the third capacitor C3, a fluctuation of a data signal (e.g., left image data or right image data) stored in the third capacitor C3 may be prevented. That is, the sustain power voltage VSUS may be a predetermined DC voltage to prevent the fluctuation of the data signal stored in the third capacitor C3.

**[0107]** As described above, the pixel circuit 400 may have a 5T-3C structure that includes the organic light emitting diode OLED, the first through fifth NMOS transistors NT1 through NT5, and the first through third capacitors C1 through C3. An organic light emitting display device having the pixel circuit 400 may implement a stereoscopic image by alternately displaying a left image and a right image based on a simultaneous emission method. For example, the right image data

may be sequentially written into each pixel circuit 400 of the organic light emitting display device while the left image is simultaneously displayed by each pixel circuit 400 of the organic light emitting display device. Similarly, the left image data may be sequentially written into each pixel circuit 400 of the organic light emitting display device while the right image is simultaneously displayed by each pixel circuit 400 of the organic light emitting display device.

**[0108]** As illustrated in FIG. 9, the pixel circuit 400 may include a first region FA and a second region SA. In the following description, the first region FA includes the third capacitor C3 and the fifth NMOS transistor NT5, and the second region SA includes the first and second capacitors C1 and C2 and the first through fourth NMOS transistors NT1 through NT4. When the fourth NMOS transistor NT4 turns on, the first region FA may be coupled to the second region SA. When the fourth NMOS transistor NT4 turns off, the first region FA may be separated from the second region SA. In detail, when the fourth NMOS transistor NT4 turns on, the first region FA may be coupled to the second region SA in the pixel circuit 400. As a result, a data signal (e.g., the left image data or the right image data) stored in the third capacitor C3 may be transferred to the second region SA. On the other hand, when the fourth NMOS transistor NT4 turns off, the first region FA may be separated from the second region SA in the pixel circuit 400. As a result, the first region FA and the second region SA may perform respective operations. In detail, an emission operation may be performed in the second region SA while a preliminary data writing operation is performed in the first region FA. Thus, an operation of the first region FA may be independent from an operation of the second region SA. For example, when the fourth NMOS transistor NT4 turns off in response to the emission control signal ECS, the first image (e.g., the left image or the right image) may be displayed by the first and second NMOS transistors NT1 and NT2, the first and second capacitors C1 and C2, and the organic light emitting diode OLED (i.e., an operation of the second region SA). At the same time, the second image data (e.g., the right image data or the left image data) input through the data line DL may be stored in the third capacitor C3 when the fifth NMOS transistor NT5 turns on in response to a scan signal input through the scan line SL (i.e., an operation of the first region FA).

**[0109]** FIGS. 10 and 11 illustrate flow charts of a method of driving a pixel circuit according to exemplary embodiments.

**[0110]** Referring to FIGS. 10 and 11, the method of FIG. 10 and the method of FIG. 11 may alternatively perform a first display operation for displaying a left image and a second display operation for displaying a right image. The first and second display operations may be performed based on a simultaneous emission method.

**[0111]** According to the method of FIG. 10, a first emission operation of the first display operation and a second preliminary data writing operation of the second display operation may be simultaneously performed (operation S120). After the first emission operation is completed, a second reset operation, a second threshold voltage compensation operation, and a second data writing operation of the second display operation may be sequentially performed (operation S140). Next, a second emission operation of the second display operation and a first preliminary data writing operation of the first display operation may be simultaneously performed (operation S160). After the second emission operation is completed, a first reset operation, a first threshold voltage compensation operation, and a first data writing operation of the first display operation may be sequentially performed (operation S180).

**[0112]** According to the method of FIG. 11, a second off-bias applying operation may be performed (operation S130) prior to the second reset operation of the second display operation, and a first off-bias applying operation may be performed (operation S170) prior to the first reset operation of the first display operation. For these operations, a pixel circuit according to exemplary embodiments may have a 5T-3C structure that includes an organic light emitting diode, first through fifth PMOS transistors, and first through third capacitors. In another implementation, a pixel circuit according to exemplary embodiments may have a 5T-3C structure that includes an organic light emitting diode, first through fifth NMOS transistors, and first through third capacitors. The pixel circuit may be a circuit as described with reference to FIGS. 1, 6, 7, and 9.

**[0113]** FIG. 12 illustrates a block diagram of an organic light emitting display device according to exemplary embodiments.

**[0114]** Referring to FIG. 12, the organic light emitting display device 500 may include a pixel unit 510, a scan driving unit 520, a data driving unit 530, a timing control unit 540, a control signal generating unit 550, and a power unit 560. In some exemplary embodiments, the scan driving unit 520, the data driving unit 530, the timing control unit 540, the control signal generating unit 550, and the power unit 560 may be implemented by one integrated circuit (IC).

**[0115]** The pixel unit 510 may be coupled to the scan driving unit 520 via a plurality of scan lines SL1 through SLn, to the data driving unit 530 via a plurality of data lines DL1 through DLm, and to the control signal generating unit 550 via a plurality of control lines. The pixel unit 510 may receive a first power voltage ELVDD and a second power voltage ELVSS from the power unit 560. In an exemplary embodiment, the pixel unit 510 may further receive a sustain power voltage VSUS from the power unit 560. The pixel unit 510 may include a plurality of pixel circuits. Each pixel circuit may be coupled to one scan line that provides a scan signal, to one data line that provides a data signal (e.g., left image data or right image data), and to the control lines that provide an emission control signal ECS and a compensation control signal TCS. In addition, each pixel circuit may receive the first power voltage ELVDD and the second power voltage ELVSS. In an exemplary embodiment, each pixel circuit may further receive the sustain power voltage VSUS.

**[0116]** The pixel circuits may be located at crossing points of the scan lines SL1 through SLn and the data lines DL1

through DLM. Thus, the pixel unit 510 may include  $n \times m$  pixel circuits (i.e., the number of pixel circuits is  $n \times m$ ). The timing control unit 540 may control the scan driving unit 520, the data driving unit 530, the control signal generating unit 550, and the power unit 560 by generating and providing a plurality of timing control signals CTL1, CTL2, CTL3, and CTL4 to the scan driving unit 520, the data driving unit 530, the control signal generating unit 550, and the power unit 560.

**[0117]** As described above, each pixel circuit may operate based on the first power voltage ELVDD, the second power voltage ELVSS, the scan signal, the data signal, the emission control signal ECS, the compensation control signal TCS, and/or the sustain power voltage VSUS. In an exemplary embodiment, each pixel circuit may include an organic light emitting diode, first through fifth PMOS transistors, and first through third capacitors. In another exemplary embodiment, each pixel circuit may include an organic light emitting diode, first through fifth NMOS transistors, and first through third capacitors. Each pixel circuit may have a 5T-3C structure (i.e., a structure having five transistors and three capacitors).

**[0118]** Each pixel circuit may store the right image data while an emission operation of a left image is performed, and may store the left image data while an emission operation of a right image is performed. The organic light emitting display device 500 may implement a stereoscopic image by alternately performing a first display operation for displaying a first image (e.g., the left image) and a second display operation for displaying a second image (e.g., the right image). The first display operation may include a first preliminary data writing operation, a first reset operation, a first threshold voltage compensation operation, a first data writing operation, and a first emission operation. The second display operation may include a second preliminary data writing operation, a second reset operation, a second threshold voltage compensation operation, a second data writing operation, and a second emission operation. When the first display operation and the second display operation are alternately performed, the first emission operation of the first display operation and the second preliminary data writing operation of the second display operation are simultaneously performed, and the second emission operation of the second display operation and the first preliminary data writing operation of the first display operation are simultaneously performed.

**[0119]** The preliminary data writing operation (i.e., the first preliminary data writing operation or the second preliminary data writing operation) may be sequentially performed for all pixel circuits of the organic light emitting display device 500 by each scan line SL1 through SLn. On the other hand, the reset operation (i.e., the first reset operation or the second reset operation), the threshold voltage compensation operation (i.e., the first threshold voltage compensation operation or the second threshold voltage compensation operation), the data writing operation (i.e., the first data writing operation or the second data writing operation), or the emission operation (i.e., the first emission operation or the second emission operation) may be simultaneously performed for all pixel circuits of the organic light emitting display device 500. As described above, in the organic light emitting display device 500, the first image data (i.e., the left image data or the right image data) may be sequentially written into each pixel circuit of the organic light emitting display device 500 while the second image (i.e., the right image or the left image) is simultaneously displayed by each pixel circuit of the organic light emitting display device 500. Similarly, the second image data (i.e., the right image data or the left image data) may be sequentially written into each pixel circuit of the organic light emitting display device 500 while the first image (i.e., the left image or the right image) is simultaneously displayed by each pixel circuit of the organic light emitting display device 500. As a result, the organic light emitting display device 500 employing a simultaneous emission method may operate at a high speed, may reduce power consumption, and may improve luminance.

**[0120]** FIG. 13 illustrates a diagram of a stereoscopic image display system 600 employing a shutter glasses method, which includes an organic light emitting display device of FIG. 12.

**[0121]** Referring to FIG. 13, the stereoscopic image display system 600 may include an organic light emitting display device 500 and shutter glasses 620.

**[0122]** The organic light emitting display device 500 may implement a stereoscopic image by alternately displaying a left image (i.e., a left image frame) and a right image (i.e., a right image frame). In some exemplary embodiments, the organic light emitting display device 500 may generate a synchronization signal for alternately providing the left image and the right image to a left eye and a right eye, respectively. Thus, the left image and the right image may be synchronized with the synchronization signal. The shutter glasses 620 may open/close a left shutter and a right shutter in synchronization with the left image and the right image, respectively when the organic light emitting display device 500 alternately displays the left image and the right image. For example, the shutter glasses 620 may open the left shutter based on the synchronization signal when the organic light emitting display device 500 displays the left image, and may open the right shutter based on the synchronization signal when the organic light emitting display device 500 displays the right image. In some exemplary embodiments, the organic light emitting display device 500 may provide the shutter glasses 620 with the synchronization signal using various wired/wireless methods.

**[0123]** FIG. 14 illustrates a diagram of a stereoscopic image display system 700 employing a parallax barrier method, which includes an organic light emitting display device of FIG. 12.

**[0124]** Referring to FIG. 14, the stereoscopic image display system 700 may include an organic light emitting display device 500 and a parallax barrier 720.

**[0125]** The organic light emitting display device 500 may implement a stereoscopic image by alternately displaying a left image (i.e., a left image frame) and a right image (i.e., a right image frame). In some exemplary embodiments, the

organic light emitting display device 500 may generate a synchronization signal for alternately providing the left image and the right image to a left eye and a right eye, respectively. Thus, the left image and the right image may be synchronized with the synchronization signal. When the organic light emitting display device 500 alternately displays the left image and the right image, the parallax barrier 720 may allow the left image and the right image to alternatively pass through.

In detail, the parallax barrier 720 may alternately provide the left image and the right image to the left eye and the right eye by changing positions of opening areas and blocking areas of the parallax barrier 720.

**[0126]** FIG. 15 illustrates a block diagram of an electric device 1000 having an organic light emitting display device of FIG. 12.

**[0127]** Referring to FIG. 15, the electric device 1000 may include a processor 1010, a memory device 1020, a storage device 1030, an input/output (I/O) device 1040, a power supply 1050, and an organic light emitting display device 1060. The organic light emitting display device 1060 may correspond to the organic light emitting display device 500 of FIG. 12. In addition, the electric device 1000 may further include a plurality of ports for communicating a video card, a sound card, a memory card, a universal serial bus (USB) device, other electric devices, etc.

**[0128]** The processor 1010 may perform various computing functions. The processor 1010 may be a microprocessor, a central processing unit (CPU), etc. The processor 1010 may be coupled to other components via an address bus, a control bus, a data bus, etc. Further, the processor 1010 may be coupled to an extended bus such as a peripheral component interconnection (PCI) bus. The memory device 1020 may store data for operations of the electric device 1000. For example, the memory device 1020 may include at least one non-volatile memory device such as an erasable programmable read-only memory (EPROM) device, an electrically erasable programmable read-only memory (EEPROM) device, a flash memory device, a phase change random access memory (PRAM) device, a resistance random access memory (RRAM) device, a nano floating gate memory (NFGM) device, a polymer random access memory (PoRAM) device, a magnetic random access memory (MRAM) device, a ferroelectric random access memory (FRAM) device, etc., and/or at least one volatile memory device such as a dynamic random access memory (DRAM) device, a static random access memory (SRAM) device, a mobile dynamic random access memory (mobile DRAM) device, etc.

The storage device 1030 may be a solid state drive device, a hard disk drive device, a CD-ROM device, etc.

**[0129]** The I/O device 1040 may be an input device such as a keyboard, a keypad, a mouse, a touch screen, etc., and/or an output device such as a printer, a speaker, etc. In some exemplary embodiments, the organic light emitting display device 1060 may be included as the output device in the I/O device 1040. The power supply 1050 may provide a power for operations of the electric device 1000. The organic light emitting display device 1060 may communicate with other components via the buses or other communication links.

**[0130]** The organic light emitting display device 1060 may, as described above, implement a stereoscopic image by alternately providing a left image (i.e., a left image frame) and a right image (i.e., a right image frame) to a left eye and a right eye, respectively. Each pixel circuit of the organic light emitting display device 1060 may store the right image data while an emission operation of the left image is performed, and may store the left image data while an emission operation of the right image is performed. Therefore, the organic light emitting display device 1060 may operate at a high speed, may reduce power consumption, and may improve luminance. The organic light emitting display device 1060 may be as described above. The organic light emitting display device 1060 may be applied to a suitable system having a stereoscopic image display device such as a stereoscopic image display system employing a shutter glasses method, a stereoscopic image display system employing a parallax barrier method, etc.

**[0131]** Embodiments may be applied to an electric device having an organic light emitting display device. For example, embodiments may be applied to a television, a computer monitor, a laptop, a digital camera, a cellular phone, a smart phone, a personal digital assistant (PDA), a portable multimedia player (PMP), an MP3 player, a navigation system, a video phone, etc.

**[0132]** By way of summation and review, a method of implementing a stereoscopic image using an organic light emitting display device may include alternately displaying a left image and a right image on the organic light emitting display device. The left image and the right image may be provided to a left eye and a right eye, respectively.

**[0133]** A general organic light emitting display device employing a sequential emission method may exhibit low luminance and high power consumption when implementing a stereoscopic image because of the manner in which the general organic light emitting display device inserts a black image (i.e., a black image frame) between a left image (i.e., a left image frame) and a right image (i.e., a right image frame) when alternately displaying the left image and the right image, so as to separate the right image from the left image. For example, in case that a stereoscopic image of 60Hz is implemented, a left image of 60Hz, a black image of 60Hz, a right image of 60Hz, and a black image of 60Hz may be sequentially displayed, such that a fast operating speed of 240Hz (i.e., 60Hz + 60Hz + 60Hz + 60Hz) is employed for the general organic light emitting display device. In addition, an emission time may be reduced by half, and a luminance may be reduced by half, when the black image is inserted between the left image and the right image in the above manner. Further, high power may be consumed to obtain the same luminance compared to a case without an insertion of the black image.

**[0134]** As described above, exemplary embodiments relate generally to a stereoscopic (3D) image display technique.

Some exemplary embodiments provide a pixel circuit that, when an organic light emitting display device including the pixel circuit implements a stereoscopic image based on a simultaneous emission method, may store right image data while a left image is displayed in an emission period of the left image, and store left image data while a right image is displayed in an emission period of the right image. The pixel circuit according to embodiments may operate at a high speed, and may reduce power consumption and/or improve luminance based on a same power consumption.

**[0135]** Some exemplary embodiments provide a method of driving a pixel circuit so as to write right image data into the pixel circuit while a left image is displayed in an emission period of the left image, and write left image data into the pixel circuit while a right image is displayed in an emission period of the right image when an organic light emitting display device including the pixel circuit implements a stereoscopic image based on a simultaneous emission method.

**[0136]** Some exemplary embodiments provide an organic light emitting display device having the pixel circuit. An organic light emitting display device according to exemplary embodiments may operate at a high speed, and may reduce power consumption when the organic light emitting display device implements a stereoscopic image based on a simultaneous emission method.

**[0137]** Exemplary embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

## Claims

1. A pixel circuit (100, 200), comprising:

an organic light emitting diode (OLED), a cathode electrode of the organic light emitting diode (OLED) being coupled to a second power voltage (ELVSS);

a first PMOS transistor (PT1) coupled between a first power voltage (ELVDD) and an anode electrode of the organic light emitting diode (OLED), a gate terminal of the first PMOS transistor (PT1) being coupled to a first node (N1);

a second PMOS transistor (PT2) coupled between the first node (N1) and the anode electrode of the organic light emitting diode (OLED), a gate terminal of the second PMOS transistor (PT2) receiving a compensation control signal (TCS);

a first capacitor (C1) coupled between a second node (N2) and the first node (N1);

a second capacitor (C2) coupled between the first power voltage (ELVDD) and the second node (N2);

a third PMOS transistor (PT3) coupled between a data line (DL) and the second node (N2), a gate terminal of the third PMOS transistor (PT3) receiving the compensation control signal (TCS);

a fourth PMOS transistor (PT4) coupled between a third node (N3) and the second node (N2), a gate terminal of the fourth PMOS transistor (PT4) receiving an emission control signal (ECS);

a third capacitor (C3) having a first terminal coupled to the third node (N3) and a second terminal coupled to the gate terminal of the third PMOS transistor (PT3) or to a sustain power voltage (VSUS); and

a fifth PMOS transistor (PT5) coupled between the data line (DL) and the third node (N3), a gate terminal of the fifth PMOS transistor (PT5) being coupled to a scan line (SL).

2. A pixel circuit (300, 400), comprising:

an organic light emitting diode (OLED), an anode electrode of the organic light emitting diode (OLED) being coupled to a first power voltage (ELVDD);

a first NMOS transistor (NT1) coupled between a second power voltage (ELVSS) and a cathode electrode of the organic light emitting diode (OLED), a gate terminal of the first NMOS transistor (NT1) being coupled to a first node (N1);

a second NMOS transistor (NT2) coupled between the first node (N1) and the cathode electrode of the organic light emitting diode (OLED), a gate terminal of the second NMOS transistor (NT2) receiving a compensation control signal (TCS);

a first capacitor (C1) coupled between a second node (N2) and the first node (N1);

a second capacitor (C2) coupled between the second power voltage (ELVSS) and the second node (N2);

a third NMOS transistor (NT3) coupled between a data line (DL) and the second node (N2), a gate terminal of

the third NMOS transistor (NT3) receiving the compensation control signal (TCS);  
 a fourth NMOS transistor (NT4) coupled between a third node (N3) and the second node (N2), a gate terminal of the fourth NMOS transistor (NT4) receiving an emission control signal (ECS);  
 a third capacitor (C3) having a first terminal coupled to the third node (N3) and a second first terminal coupled to the gate terminal of the third NMOS transistor (NT3) or to a sustain power voltage (VSUS); and  
 a fifth NMOS transistor (NT5) coupled between the data line (DL) and the third node (N3), a gate terminal of the fifth NMOS transistor (NT5) being coupled to a scan line (SL).

3. The circuit as claimed in one of the preceding claims, wherein the circuit (100, 200, 300, 400) is configured to alternately perform a first display operation for displaying a left image and a second display operation for displaying a right image, the first display operation and the second display operation being performed based on a simultaneous emission method.

4. The circuit as claimed in claim 3, wherein:

the first display operation includes a first preliminary data writing operation, a first reset operation, a first threshold voltage compensation operation, a first data writing operation, and a first emission operation,  
 the second display operation includes a second preliminary data writing operation, a second reset operation, a second threshold voltage compensation operation, a second data writing operation, and a second emission operation, and  
 wherein the circuit is configured to simultaneously perform the first emission operation and the second preliminary data writing operation, and is configured to simultaneously perform the second emission operation and the first preliminary data writing operation.

5. The circuit as claimed in one of the preceding claims, further comprising:

a fourth capacitor (C4) coupled between the anode electrode and the cathode electrode of the organic light emitting diode (OLED).

6. An organic light emitting display device (500), comprising:

a pixel unit (510) having a plurality of pixel circuits, each pixel circuit of the plurality of pixel circuits being the pixel circuit (100, 200, 300, 400) as claimed in one of the preceding claims;  
 a scan driving unit (520) configured to provide a scan signal to the pixel circuits (100, 200, 300, 400);  
 a data driving unit (530) configured to provide a data signal to the pixel circuits (100, 200, 300, 400);  
 a control signal generating unit (550) configured to provide the emission control signal (ECS) and the compensation control signal (TCS) to the pixel circuits (100, 200, 300, 400);  
 a power unit (560) configured to provide the first power voltage (ELVDD) and the second power voltage (ELVSS) to the pixel unit (510); and  
 a timing control unit (540) configured to control the scan driving unit (520), the data driving unit (530), the control signal generating unit (550), and the power unit (560).

7. A method of driving a pixel circuit (100, 200, 300, 400) as claimed in one of claims 1 through 5, the method comprising:

simultaneously performing a first emission operation (FEP) of a first display operation for displaying a left image (L\_IMG) and a second preliminary data writing operation (SPDP) of a second display operation for displaying a right image (R\_IMG);  
 sequentially performing a second reset operation (SIP), a second threshold voltage compensation operation (SVP), and a second data writing operation (SWP) of the second display operation after the first emission operation (FEP) is completed;  
 simultaneously performing a second emission operation (SEP) of the second display operation and a first preliminary data writing operation (FPDP) of the first display operation; and  
 sequentially performing a first reset operation (FIP), a first threshold voltage compensation operation (FVP), and a first data writing operation (FWP) of the first display operation after the second emission operation (SEP) is completed.

8. The method as claimed in claim 7, wherein:

while the first preliminary data writing operation (FPDP) is performed, the fourth transistor (PT4, NT4) is turned off, and a first image data that is applied through the data line (DL) is stored in the third capacitor (C3) when the fifth transistor (PT5, NT5) turns on in response to a scan signal that is applied through the scan line (SL), and while the second preliminary data writing operation (SPDP) is performed, the fourth transistor (PT4, NT4) is turned off, and a second image data that is applied through the data line (DL) is stored in the third capacitor (C3) when the fifth transistor (PT5, NT5) turns on in response to the scan signal that is applied through the scan line (SL).

9. The method as claimed in one of claims 7 and 8, wherein:

while the first reset operation (FIP) is performed, the second through fourth transistors (PT2, PT3, PT4, NT2, NT3, NT4) turn off, the second power voltage (ELVSS) has a high voltage level, and the first power voltage (ELVDD) has a low voltage level, and while the second reset operation (SIP) is performed, the second through fourth transistors (PT2, PT3, PT4, NT2, NT3, NT4) turn off, the second power voltage (ELVSS) has a high voltage level, and the first power voltage (ELVDD) has a low voltage level.

10. The method as claimed in one of claims 7 through 9, wherein:

while the first threshold voltage compensation operation (FVP) is performed, the fourth transistor (PT4, NT4) turns off, the second and third transistors (PT2, PT3, NT2, NT3) turn on, the second power voltage (ELVSS) has a high voltage level, and the first power voltage (ELVDD) has a high voltage level, and while the second threshold voltage compensation operation (SVP) is performed, the fourth transistor (PT4, NT4) turns off, the second and third transistors (PT2, PT3, NT2, NT3) turn on, the second power voltage (ELVSS) has a high voltage level, and the first power voltage (ELVDD) has a high voltage level.

11. The method as claimed in one of claims 7 through 10, wherein:

while the first data writing operation (FWP) is performed, the fourth transistor (PT4, NT4) turns on, the second and third transistors (PT2, PT3, NT2, NT3) turn off, the second power voltage (ELVSS) has a high voltage level, and the first power voltage (ELVDD) has a high voltage level, and while the second data writing operation (SWP) is performed, the fourth transistor (PT4, NT4) turns on, the second and third transistors (PT2, PT3, NT2, NT3) turn off, the second power voltage (ELVSS) has a high voltage level, and the first power voltage (ELVDD) has a high voltage level.

12. The method as claimed in one of claims 7 through 11, wherein:

while the first emission operation (FEP) is performed, the second through fourth transistors (PT2, PT3, PT4, NT2, NT3, NT4) turn off, the second power voltage (ELVSS) has a low voltage level, and the first power voltage (ELVDD) has a high voltage level, and while the second emission operation (SEP) is performed, the second through fourth transistors (PT2, PT3, PT4, NT2, NT3, NT4) turn off, the second power voltage (ELVSS) has a low voltage level, and the first power voltage (ELVDD) has a high voltage level.

13. The method as claimed in one of claims 7 through 12, further comprising:

performing a first off-bias applying operation of the first display operation prior to the first reset operation (FIP) of the first display operation; and performing a second off-bias applying operation of the second display operation prior to the second reset operation (SIP) of the second display operation.

14. The method as claimed in claim 13, wherein:

while the first off-bias applying operation is performed, the fourth transistor (PT4, NT4) turns off, the second and third transistors (PT2, PT3, NT2, NT3) turn on, the second power voltage (ELVSS) has a high voltage level, and the first power voltage (ELVDD) has a low voltage level, and while the second off-bias applying operation is performed, the fourth transistor (PT4, NT4) turns off, the second and third transistors (PT2, PT3, NT2, NT3) turn on, the second power voltage (ELVSS) has a high voltage level,

and the first power voltage (ELVDD) has a low voltage level.

## Patentansprüche

### 1. Pixelschaltung (100, 200), aufweisend:

eine organische lichtemittierende Diode (OLED), wobei eine Kathodenelektrode der organischen lichtemittierenden Diode (OLED) mit einer zweiten Versorgungsspannung (ELVSS) gekoppelt ist;  
 einen ersten PMOS-Transistor (PT1), der zwischen eine erste Versorgungsspannung (ELVDD) und eine Anodenelektrode der organischen lichtemittierenden Diode (OLED) gekoppelt ist, wobei ein Gate-Anschluss des ersten PMOS-Transistors (PT1) mit einem ersten Knoten (N1) gekoppelt ist;  
 einen zweiten PMOS-Transistor (PT2), der zwischen den ersten Knoten (N1) und die Anodenelektrode der organischen lichtemittierenden Diode (OLED) gekoppelt ist, wobei ein Gate-Anschluss des zweiten PMOS-Transistors (PT2) ein Kompensationssteuersignal (TCS) empfängt,  
 einen ersten Kondensator (C1), der zwischen einen zweiten Knoten (N2) und den ersten Knoten (N1) gekoppelt ist;  
 einen zweiten Kondensator (C2), der zwischen die erste Versorgungsspannung (ELVDD) und den zweiten Knoten (N2) gekoppelt ist;  
 einen dritten PMOS-Transistor (PT3), der zwischen eine Datenleitung (DL) und den zweiten Knoten (N2) gekoppelt ist, wobei ein Gate-Anschluss des dritten PMOS-Transistors (PT3) das Kompensationssteuersignal (TCS) empfängt;  
 einen vierten PMOS-Transistor (PT4), der zwischen einen dritten Knoten (N3) und den zweiten Knoten (N2) gekoppelt ist, wobei ein Gate-Anschluss des vierten PMOS-Transistors (PT4) ein Emissionssteuersignal (ECS) empfängt;  
 einen dritten Kondensator (C3), der einen ersten Anschluss, der mit dem dritten Knoten (N3) gekoppelt ist, und einen zweiten Anschluss, der mit dem Gate-Anschluss des dritten PMOS-Transistors (PT3) oder einer Erhaltungsspannung (VSUS) gekoppelt ist, aufweist; und  
 einen fünften PMOS-Transistor (PT5), der zwischen die Datenleitung (DL) und den dritten Knoten (N3) gekoppelt ist, wobei ein Gate-Anschluss des fünften PMOS-Transistors (PT5) mit einer Abtastleitung (SL) gekoppelt ist.

### 2. Pixelschaltung (300, 400), aufweisend:

eine organische lichtemittierende Diode (OLED), wobei eine Anodenelektrode der organischen lichtemittierenden Diode (OLED) mit einer ersten Versorgungsspannung (ELVDD) gekoppelt ist;  
 einen ersten NMOS-Transistor (NT1), der zwischen eine zweite Versorgungsspannung (ELVSS) und eine Kathodenelektrode der organischen lichtemittierenden Diode (OLED) gekoppelt ist, wobei ein Gate-Anschluss des ersten NMOS-Transistors (NT1) mit einem ersten Knoten (N1) gekoppelt ist;  
 einen zweiten NMOS-Transistor (NT2), der zwischen den ersten Knoten (N1) und die Kathodenelektrode der organischen lichtemittierenden Diode (OLED) gekoppelt ist, wobei ein Gate-Anschluss des zweiten NMOS-Transistors (NT2) ein Kompensationssteuersignal (TCS) empfängt;  
 einen ersten Kondensator (C1), der zwischen einen zweiten Knoten (N2) und den ersten Knoten (N1) gekoppelt ist;  
 einen zweiten Kondensator (C2), der zwischen die zweite Versorgungsspannung (ELVSS) und den zweiten Knoten (N2) gekoppelt ist;  
 einen dritten NMOS-Transistor (NT3), der zwischen eine Datenleitung (DL) und den zweiten Knoten (N2) gekoppelt ist, wobei ein Gate-Anschluss des dritten NMOS-Transistors (NT3) das Kompensationssteuersignal (TCS) empfängt;  
 einen vierten NMOS-Transistor (NT4), der zwischen einen dritten Knoten (N3) und den zweiten Knoten (N2) gekoppelt ist, wobei ein Gate-Anschluss des vierten NMOS-Transistors (NT4) ein Emissionssteuersignal (ECS) empfängt;  
 einen dritten Kondensator (C3), der einen ersten Anschluss, der mit dem dritten Knoten (N3) gekoppelt ist, und einen zweiten ersten Anschluss, der mit dem Gate-Anschluss des dritten NMOS-Transistors (NT3) oder einer Erhaltungsspannung (VSUS) gekoppelt ist, aufweist; und  
 einen fünften NMOS-Transistor (NT5), der zwischen die Datenleitung (DL) und den dritten Knoten (N3) gekoppelt ist, wobei ein Gate-Anschluss des fünften NMOS-Transistors (NT5) mit einer Abtastleitung (SL) gekoppelt ist.

### 3. Schaltung nach einem der vorhergehenden Ansprüche, wobei die Schaltung (100, 200, 300, 400) konfiguriert ist,

um alternierend einen ersten Anzeigevorgang zum Anzeigen eines linken Bildes und einen zweiten Anzeigevorgang zum Anzeigen eines rechten Bildes durchzuführen, wobei der erste Anzeigevorgang und der zweite Anzeigevorgang auf der Basis eines simultanen Emissionsverfahrens durchgeführt werden.

4. Schaltung nach Anspruch 3, wobei:

der erste Anzeigevorgang einen ersten vorausgehenden Datenschreibvorgang, einen ersten Reset-Vorgang, einen ersten Schwellenspannungskompensationsvorgang, einen ersten Datenschreibvorgang und einen ersten Emissionsvorgang aufweist,  
 der zweite Anzeigevorgang einen zweiten vorausgehenden Datenschreibvorgang, einen zweiten Reset-Vorgang, einen zweiten Schwellenspannungskompensationsvorgang, einen zweiten Datenschreibvorgang und einen zweiten Emissionsvorgang aufweist, und  
 wobei die Schaltung konfiguriert ist, um den ersten Emissionsvorgang und den zweiten vorausgehenden Datenschreibvorgang simultan durchzuführen, und konfiguriert ist, um den zweiten Emissionsvorgang und den ersten vorausgehenden Datenschreibvorgang simultan durchzuführen.

5. Schaltung nach einem der vorhergehenden Ansprüche, weiterhin aufweisend:

einen vierten Kondensator (C4), der zwischen die Anodenelektrode und die Kathodenelektrode der organischen lichtemittierenden Diode (OLED) gekoppelt ist.

6. Organische lichtemittierende Anzeigevorrichtung (500), aufweisend:

eine Pixeleinheit (510), die eine Vielzahl von Pixelschaltungen aufweist, wobei jede Pixelschaltung aus der Vielzahl der Pixelschaltungen die Pixelschaltung (100, 200, 300, 400) nach einem der vorhergehenden Ansprüche ist;  
 eine Abtaststeuerungseinheit (520), die konfiguriert ist, um die Pixelschaltungen (100, 200, 300, 400) mit einem Abtastsignal zu versorgen;  
 eine Datenansteuereinheit (530), die konfiguriert ist, um die Pixelschaltungen (100, 200, 300, 400) mit einem Datensignal zu versorgen;  
 eine Steuersignalerzeugungseinheit (550), die konfiguriert ist, um die Pixelschaltungen (100, 200, 300, 400) mit dem Emissionssteuersignal (ECS) und dem Kompensationssteuersignal (TCS) zu versorgen;  
 eine Versorgungseinheit (560), die konfiguriert ist, um die Pixeleinheit (510) mit der ersten Versorgungsspannung (ELVDD) und der zweiten Versorgungsspannung (ELVSS) zu versorgen; und  
 eine Zeitsteuereinheit (540), die konfiguriert ist, um die Abtaststeuerungseinheit (520), die Datenansteuereinheit (530), die Steuersignalerzeugungseinheit (550) und die Versorgungseinheit (560) zu steuern.

7. Verfahren zum Ansteuern einer Pixelschaltung (100, 200, 300, 400) nach einem der Ansprüche 1 bis 5, wobei das Verfahren aufweist:

simultanes Durchführen eines ersten Emissionsvorgangs (FEP) eines ersten Anzeigevorgangs zum Anzeigen eines linken Bildes (L\_IMG) und eines zweiten vorausgehenden Datenschreibvorgangs (SPDP) eines zweiten Anzeigevorgangs zum Anzeigen eines rechten Bildes (R\_IMG);  
 aufeinanderfolgendes Durchführen eines zweiten Reset-Vorgangs (SIP), eines zweiten Schwellenspannungskompensationsvorgangs (SVP), und eines zweiten Datenschreibvorgangs (SVP) des zweiten Anzeigevorgangs, nachdem der erste Emissionsvorgang (FEP) abgeschlossen ist;  
 simultanes Durchführen eines zweiten Emissionsvorgangs (SEP) des zweiten Anzeigevorgangs und eines ersten vorausgehenden Datenschreibvorgangs (FPDP) des ersten Anzeigevorgangs; und  
 aufeinanderfolgendes Durchführen eines ersten Reset-Vorgangs (FIP), eines ersten Schwellenspannungskompensationsvorgangs (FVP) und eines ersten Datenschreibvorgangs (FWP) des ersten Anzeigevorgangs, nachdem der zweite Emissionsvorgang (SEP) abgeschlossen ist.

8. Verfahren nach Anspruch 7, wobei:

während der erste vorausgehende Datenschreibvorgang (FPDP) durchgeführt wird, der vierte Transistor (PT4, NT4) ausgeschaltet ist, und erste Bilddaten, die durch die Datenleitung (DL) angelegt werden, im dritten Kondensator (C3) gespeichert werden, wenn der fünfte Transistor (PT5, NT5) in Reaktion auf ein Abtastsignal, das durch die Abtastleitung (SL) angelegt wird, eingeschaltet wird, und

während der zweite vorausgehende Datenschreibvorgang (SPDP) durchgeführt wird, der vierte Transistor (PT4, NT4) ausgeschaltet ist, und zweite Bilddaten, die durch die Datenleitung (DL) angelegt werden, im dritten Kondensator (C3) gespeichert werden, wenn der fünfte Transistor (PT5, NT5) in Reaktion auf das Abtastsignal, das durch die Abtastleitung (SL) angelegt wird, eingeschaltet wird.

5  
9. Verfahren nach einem der Ansprüche 7 und 8, wobei:

10 während der erste Reset-Vorgang (FIP) durchgeführt wird, der zweite bis vierte Transistor (PT2, PT3, PT4, NT2, NT3, NT4) ausgeschaltet werden, die zweite Versorgungsspannung (ELVSS) einen hohen Spannungspegel aufweist und die erste Versorgungsspannung (ELVDD) einen niedrigen Spannungspegel aufweist, und während der zweite Reset-Vorgang (SIP) durchgeführt wird, der zweite bis vierte Transistor (PT2, PT3, PT4, NT2, NT3, NT4) ausgeschaltet werden, die zweite Versorgungsspannung (ELVSS) einen hohen Spannungspegel aufweist und die erste Versorgungsspannung (ELVDD) einen niedrigen Spannungspegel aufweist.

15 10. Verfahren nach einem der Ansprüche 7 bis 9, wobei:

20 während der erste Schwellenspannungskompensationsvorgang (FVP) durchgeführt wird, der vierte Transistor (PT4, NT4) ausgeschaltet wird, der zweite und dritte Transistor (PT2, PT3, NT2, NT3) eingeschaltet werden, die zweite Versorgungsspannung (ELVSS) einen hohen Spannungspegel aufweist und die erste Versorgungsspannung (ELVDD) einen hohen Spannungspegel aufweist, und während der zweite Schwellenspannungskompensationsvorgang (SVP) durchgeführt wird, der vierte Transistor (PT4, NT4) ausgeschaltet wird, der zweite und dritte Transistor (PT2, PT3, NT2, NT3) eingeschaltet werden, die zweite Versorgungsspannung (ELVSS) einen hohen Spannungspegel aufweist und die erste Versorgungsspannung (ELVDD) einen hohen Spannungspegel aufweist.

25 11. Verfahren nach einem der Ansprüche 7 bis 10, wobei:

30 während der erste Datenschreibvorgang (FWP) durchgeführt wird, der vierte Transistor (PT4, NT4) eingeschaltet wird, der zweite und dritte Transistor (PT2, PT3, NT2, NT3) ausgeschaltet werden, die zweite Versorgungsspannung (ELVSS) einen hohen Spannungspegel aufweist, und die erste Versorgungsspannung (ELVDD) einen hohen Spannungspegel aufweist, und während der zweite Datenschreibvorgang (SWP) durchgeführt wird, der vierte Transistor (PT4, NT4) eingeschaltet wird, der zweite und dritte Transistor (PT2, PT3, NT2, NT3) ausgeschaltet werden, die zweite Versorgungsspannung (ELVSS) einen hohen Spannungspegel aufweist und die erste Versorgungsspannung (ELVDD) einen hohen Spannungspegel aufweist.

35 12. Verfahren nach einem der Ansprüche 7 bis 11, wobei:

40 während der erste Emissionsvorgang (FEP) durchgeführt wird, der zweite bis vierte Transistor (PT2, PT3, PT4, NT2, NT3, NT4) ausgeschaltet werden, die zweite Versorgungsspannung (ELVSS) einen niedrigen Spannungspegel aufweist und die erste Versorgungsspannung (ELVDD) einen hohen Spannungspegel aufweist, und während der zweite Emissionsvorgang (SEP) durchgeführt wird, der zweite bis vierte Transistor (PT2, PT3, PT4, NT2, NT3, NT4) ausgeschaltet werden, die zweite Versorgungsspannung (ELVSS) einen niedrigen Spannungspegel aufweist und die erste Versorgungsspannung (ELVDD) einen hohen Spannungspegel aufweist.

45 13. Verfahren nach einem der Ansprüche 7 bis 12, weiterhin aufweisend:

Durchführen eines ersten Ausschalt-Vorspannungsanlegevorgangs des ersten Anzeigevorgangs vor dem ersten Reset-Vorgang (FIP) des ersten Anzeigevorgangs; und  
50 Durchführen eines zweiten Ausschalt-Vorspannungsanlegevorgangs des zweiten Anzeigevorgangs vor dem zweiten Reset-Vorgang (SIP) des zweiten Anzeigevorgangs.

14. Verfahren nach Anspruch 13, wobei:

55 während der erste Ausschalt-Vorspannungsanlegevorgang durchgeführt wird, der vierte Transistor (PT4, NT4) ausgeschaltet wird, der zweite und dritte Transistor (PT2, PT3, NT2, NT3) eingeschaltet werden, die zweite Versorgungsspannung (ELVSS) einen hohen Spannungspegel aufweist und die erste Versorgungsspannung (ELVDD) einen niedrigen Spannungspegel aufweist, und

während der zweite Ausschalt-Vorspannungsanlegevorgang durchgeführt wird, der vierte Transistor (PT4, NT4) ausgeschaltet wird, der zweite und dritte Transistor (PT2, PT3, NT2, NT3) eingeschaltet werden, die zweite Versorgungsspannung (ELVSS) einen hohen Spannungspegel aufweist und die erste Versorgungsspannung (ELVDD) einen niedrigen Spannungspegel aufweist.

## Revendications

### 1. Circuit de pixel (100, 200), comprenant . i

une diode électroluminescente organique (OLED), une électrode de cathode de la diode électroluminescente organique (OLED) étant couplée à une deuxième tension d'alimentation (ELVSS) ;  
 un premier transistor PMOS (PT1) couplé entre une première tension d'alimentation (ELVDD) et une électrode d'anode de la diode électroluminescente organique (OLED), une borne de grille du premier transistor PMOS (PT1) étant couplée à un premier noeud (N1) ;  
 un deuxième transistor PMOS (PT2) couplé entre le premier noeud (N1) et l'électrode d'anode de la diode électroluminescente organique (OLED), une borne de grille du deuxième transistor PMOS (PT2) recevant un signal de commande de compensation (TCS) ;  
 un premier condensateur (C1) couplé entre un deuxième noeud (N2) et le premier noeud (N1) ;  
 un deuxième condensateur (C2) couplé entre la première tension d'alimentation (ELVDD) et le deuxième noeud (N2) ;  
 un troisième transistor PMOS (PT3) couplé entre une ligne de données (DL) et le deuxième noeud (N2), une borne de grille du troisième transistor PMOS (PT3) recevant le signal de commande de compensation (TCS) ;  
 un quatrième transistor PMOS (PT4) couplé entre un troisième noeud (N3) et le deuxième noeud (N2), une borne de grille du quatrième transistor PMOS (PT4) recevant un signal de commande d'émission (ECS) ;  
 un troisième condensateur (C3) ayant une première borne couplée au troisième noeud (N3) et une deuxième borne couplée à la borne de grille du troisième transistor PMOS (PT3) ou à une tension d'alimentation d'entretien (VSUS) ; et  
 un cinquième transistor PMOS (PT5) couplé entre la ligne de données (DL) et le troisième noeud (N3), une borne de grille du cinquième transistor PMOS (PT5) étant couplée à une ligne de balayage (SL).

### 2. Circuit de pixel (300, 400), comprenant :

une diode électroluminescente organique (OLED), une électrode d'anode de la diode électroluminescente organique (OLED) étant couplée à une première tension d'alimentation (ELVDD) ;  
 un premier transistor NMOS (NT1) couplé entre une deuxième tension d'alimentation (ELVSS) et une électrode de cathode de la diode électroluminescente organique (OLED), une borne de grille du premier transistor NMOS (NT1) étant couplée à un premier noeud (N1) ;  
 un deuxième transistor NMOS (NT2) couplé entre le premier noeud (N1) et l'électrode de cathode de la diode électroluminescente organique (OLED), une borne de grille du deuxième transistor NMOS (NT2) recevant un signal de commande de compensation (TCS) ;  
 un premier condensateur (C1) couplé entre un deuxième noeud (N2) et le premier noeud (N1) ;  
 un deuxième condensateur (C2) couplé entre la deuxième tension d'alimentation (ELVSS) et le deuxième noeud (N2) ;  
 un troisième transistor NMOS (NT3) couplé entre une ligne de données (DL) et le deuxième noeud (N2), une borne de grille du troisième transistor NMOS (NT3) recevant le signal de commande de compensation (TCS) ;  
 un quatrième transistor NMOS (NT4) couplé entre un troisième noeud (N3) et le deuxième noeud (N2), une borne de grille du quatrième transistor NMOS (NT4) recevant un signal de commande d'émission (ECS) ;  
 un troisième condensateur (C3) ayant une première borne couplée au troisième noeud (N3) et une deuxième borne couplée à la borne de grille du troisième transistor NMOS (NT3) ou à une tension d'alimentation d'entretien (VSUS) ; et  
 un cinquième transistor NMOS (NT5) couplé entre la ligne de données (DL) et le troisième noeud (N3), une borne de grille du cinquième transistor NMOS (NT5) étant couplée à une ligne de balayage (SL).

### 3. Circuit tel que revendiqué dans l'une des revendications précédentes, dans lequel le circuit (100, 200, 300, 400) est configuré pour exécuter de manière alternée une première opération d'affichage pour afficher une image gauche et une deuxième opération d'affichage pour afficher une image droite, la première opération d'affichage et la deuxième opération d'affichage étant exécutées sur la base d'un procédé d'émission simultanée.

4. Circuit tel que revendiqué dans la revendication 3, dans lequel :

la première opération d'affichage comporte une première opération d'écriture de données préliminaire, une première opération de réinitialisation, une première opération de compensation de tension seuil, une première opération d'écriture de données et une première opération d'émission, la deuxième opération d'affichage comporte une deuxième opération d'écriture de données préliminaire, une deuxième opération de réinitialisation, une deuxième opération de compensation de tension seuil, une deuxième opération d'écriture de données et une deuxième opération d'émission, et dans lequel le circuit est configuré pour exécuter simultanément la première opération d'émission et la deuxième opération d'écriture de données préliminaire et est configuré pour exécuter simultanément la deuxième opération d'émission et la première opération d'écriture de données préliminaire.

5. Circuit tel que revendiqué dans l'une des revendications précédentes, comprenant en outre :

un quatrième condensateur (C4) couplé entre l'électrode d'anode et l'électrode de cathode de la diode électroluminescente organique (OLED).

6. Dispositif d'affichage électroluminescent organique (500), comprenant :

une unité de pixel (510) ayant une pluralité de circuits de pixel, chaque circuit de pixel de la pluralité de circuits de pixel étant le circuit de pixel (100, 200, 300, 400) tel que revendiqué dans l'une des revendications précédentes ;  
une unité de pilotage de balayage (520) configurée pour fournir un signal de balayage aux circuits de pixel (100, 200, 300, 400) ;  
une unité de pilotage de données (530) configurée pour fournir un signal de données aux circuits de pixel (100, 200, 300, 400) ;  
une unité de génération de signal de commande (550) configurée pour fournir le signal de commande d'émission (ECS) et le signal de commande de compensation (TCS) aux circuits de pixel (100, 200, 300, 400) ;  
une unité d'alimentation (560) configurée pour fournir la première tension d'alimentation (ELVDD) et la deuxième tension d'alimentation (ELVSS) à l'unité de pixel (510) ; et  
une unité de commande de synchronisation (540) configurée pour commander l'unité de pilotage de balayage (520), l'unité de pilotage de données (530), l'unité de génération de signal de commande (550) et l'unité d'alimentation (560).

7. Procédé de pilotage d'un circuit de pixel (100, 200, 300, 400) tel que revendiqué dans l'une des revendications 1 à 5, le procédé comprenant le fait :

d'exécuter simultanément une première opération d'émission (FEP) d'une première opération d'affichage pour afficher une image gauche (L\_IMG) et une deuxième opération d'écriture de données préliminaire (SPDP) d'une deuxième opération d'affichage pour afficher une image droite (R\_IMG) ;  
d'exécuter séquentiellement une deuxième opération de réinitialisation (SIP), une deuxième opération de compensation de tension seuil (SVP) et une deuxième opération d'écriture de données (SWP) de la deuxième opération d'affichage après l'achèvement de la première opération d'émission (FEP) ;  
d'exécuter simultanément une deuxième opération d'émission (SEP) de la deuxième opération d'affichage et une première opération d'écriture de données préliminaire (FPDP) de la première opération d'affichage ; et  
d'exécuter séquentiellement une première opération de réinitialisation (FIP), une première opération de compensation de tension seuil (FVP) et une première opération d'écriture de données (FWP) de la première opération d'affichage après l'achèvement de la deuxième opération d'émission (SEP).

8. Procédé tel que revendiqué dans la revendication 7, dans lequel :

tandis que la première opération d'écriture de données préliminaire (FPDP) est exécutée, le quatrième transistor (PT4, NT4) est mis hors tension, et des premières données d'image qui sont appliquées à travers la ligne de données (DL) sont stockées dans le troisième condensateur (C3) lorsque le cinquième transistor (PT5, NT5) est mis sous tension en réponse à un signal de balayage qui est appliqué à travers la ligne de balayage (SL), et tandis que la deuxième opération d'écriture de données préliminaire (SPDP) est exécutée, le quatrième transistor (PT4, NT4) est mis hors tension, et des deuxièmes données d'image qui sont appliquées à travers la ligne de données (DL) sont stockées dans le troisième condensateur (C3) lorsque le cinquième transistor (PT5, NT5)

est mis sous tension en réponse au signal de balayage qui est appliqué à travers la ligne de balayage (SL).

9. Procédé tel que revendiqué dans l'une des revendications 7 et 8, dans lequel :

5 tandis que la première opération de réinitialisation (FIP) est exécutée, les deuxième au quatrième transistors (PT2, PT3, PT4, NT2, NT3, NT4) sont mis hors tension, la deuxième tension d'alimentation (ELVSS) a un niveau de tension élevé et la première tension d'alimentation (ELVDD) a un niveau de tension faible, et  
10 tandis que la deuxième opération de réinitialisation (SIP) est exécutée, les deuxième au quatrième transistors (PT2, PT3, PT4, NT2, NT3, NT4) sont mis hors tension, la deuxième tension d'alimentation (ELVSS) a un niveau de tension élevé et la première tension d'alimentation (ELVDD) a un niveau de tension faible.

10. Procédé tel que revendiqué dans l'une des revendications 7 à 9, dans lequel :

15 tandis que la première opération de compensation de tension seuil (FVP) est exécutée, le quatrième transistor (PT4, NT4) est mis hors tension, les deuxième et troisième transistors (PT2, PT3, NT2, NT3) sont mis sous tension, la deuxième tension d'alimentation (ELVSS) a un niveau de tension élevé et la première tension d'alimentation (ELVDD) a un niveau de tension élevé, et  
20 tandis que la deuxième opération de compensation de tension seuil (SVP) est exécutée, le quatrième transistor (PT4, NT4) est mis hors tension, les deuxième et troisième transistors (PT2, PT3, NT2, NT3) sont mis sous tension, la deuxième tension d'alimentation (ELVSS) a un niveau de tension élevé et la première tension d'alimentation (ELVDD) a un niveau de tension élevé.

11. Procédé tel que revendiqué dans l'une des revendications 7 à 10, dans lequel :

25 tandis que la première opération d'écriture de données (FWP) est exécutée, le quatrième transistor (PT4, NT4) est mis sous tension, les deuxième et troisième transistors (PT2, PT3, NT2, NT3) sont mis hors tension, la deuxième tension d'alimentation (ELVSS) a un niveau de tension élevé et la première tension d'alimentation (ELVDD) a un niveau de tension élevé, et  
30 tandis que la deuxième opération d'écriture de données (SWP) est exécutée, le quatrième transistor (PT4, NT4) est mis sous tension, les deuxième et troisième transistors (PT2, PT3, NT2, NT3) sont mis hors tension, la deuxième tension d'alimentation (ELVSS) a un niveau de tension élevé et la première tension d'alimentation (ELVDD) a un niveau de tension élevé.

12. Procédé tel que revendiqué dans l'une des revendications 7 à 11, dans lequel :

35 tandis que la première opération d'émission (FEP) est exécutée, les deuxième au quatrième transistors (PT2, PT3, PT4, NT2, NT3, NT4) sont mis hors tension, la deuxième tension d'alimentation (ELVSS) a un niveau de tension faible et la première tension d'alimentation (ELVDD) a un niveau de tension élevé, et  
40 tandis que la deuxième opération d'émission (SEP) est exécutée, les deuxième au quatrième transistors (PT2, PT3, PT4, NT2, NT3, NT4) sont mis hors tension, la deuxième tension d'alimentation (ELVSS) a un niveau de tension faible et la première tension d'alimentation (ELVDD) a un niveau de tension élevé.

13. Procédé tel que revendiqué dans l'une des revendications 7 à 12, comprenant en outre le fait :

45 d'exécuter une première opération d'application de polarisation de mise hors tension de la première opération d'affichage avant la première opération de réinitialisation (FIP) de la première opération d'affichage ; et  
d'exécuter une deuxième opération d'application de polarisation de mise hors tension de la deuxième opération d'affichage avant la deuxième opération de réinitialisation (SIP) de la deuxième opération d'affichage.

50 14. Procédé tel que revendiqué dans la revendication 13, dans lequel :

55 tandis que la première opération d'application de polarisation de mise hors tension est exécutée, le quatrième transistor (PT4, NT4) est mis hors tension, les deuxième et troisième transistors (PT2, PT3, NT2, NT3) sont mis sous tension, la deuxième tension d'alimentation (ELVSS) a un niveau de tension élevé et la première tension d'alimentation (ELVDD) a un niveau de tension faible, et  
tandis que la deuxième opération d'application de polarisation de mise hors tension est exécutée, le quatrième transistor (PT4, NT4) est mis hors tension, les deuxième et troisième transistors (PT2, PT3, NT2, NT3) sont mis sous tension, la deuxième tension d'alimentation (ELVSS) a un niveau de tension élevé et la première

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tension d'alimentation (ELVDD) a un niveau de tension faible.

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FIG. 1

100

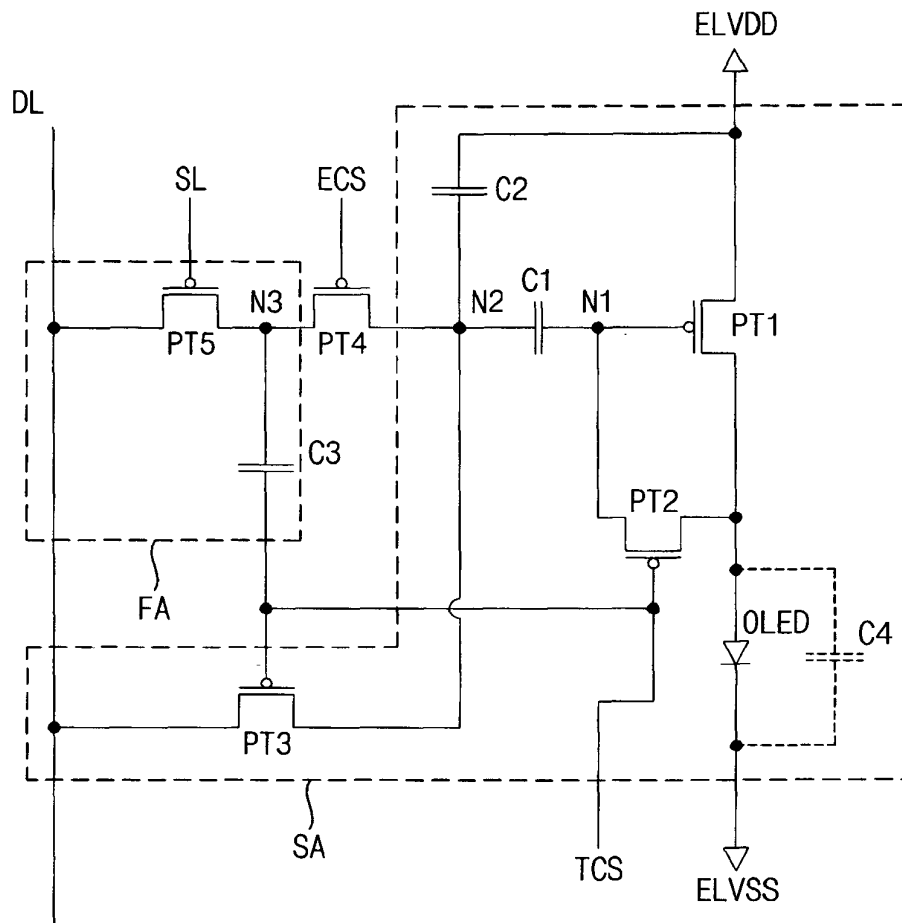


FIG. 2

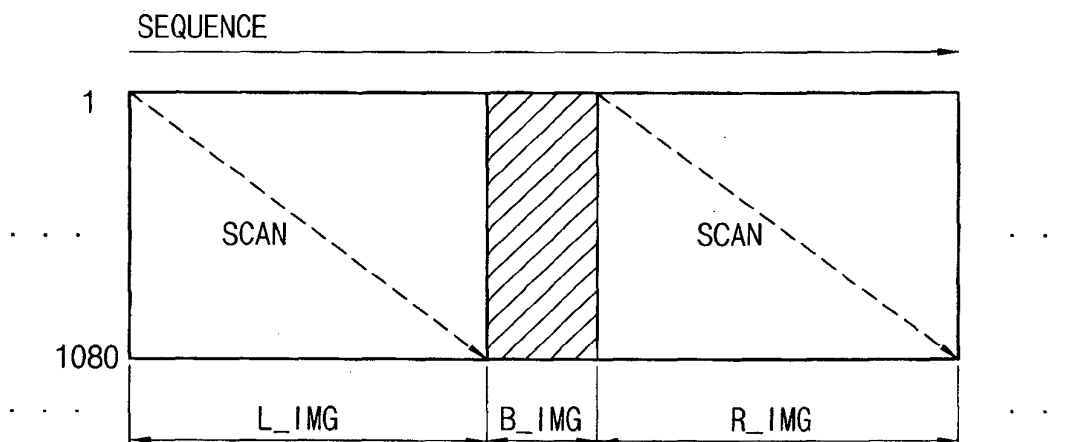


FIG. 3

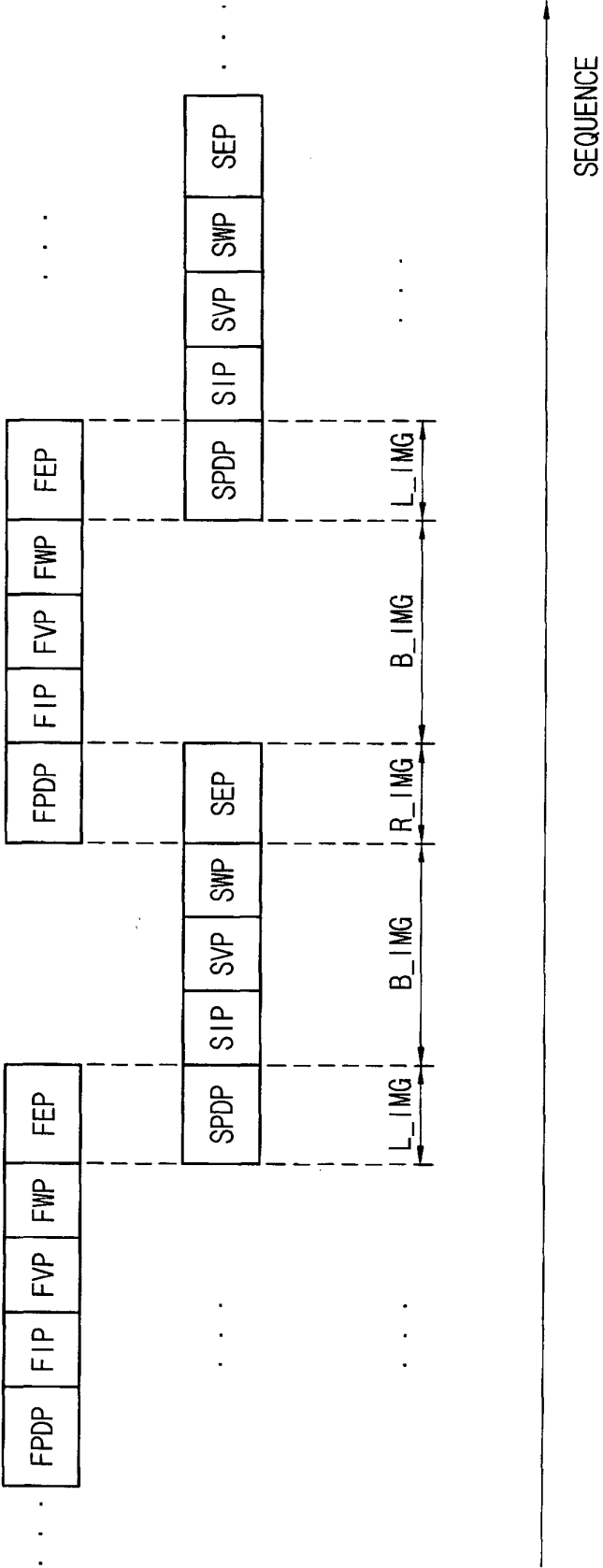


FIG. 4A

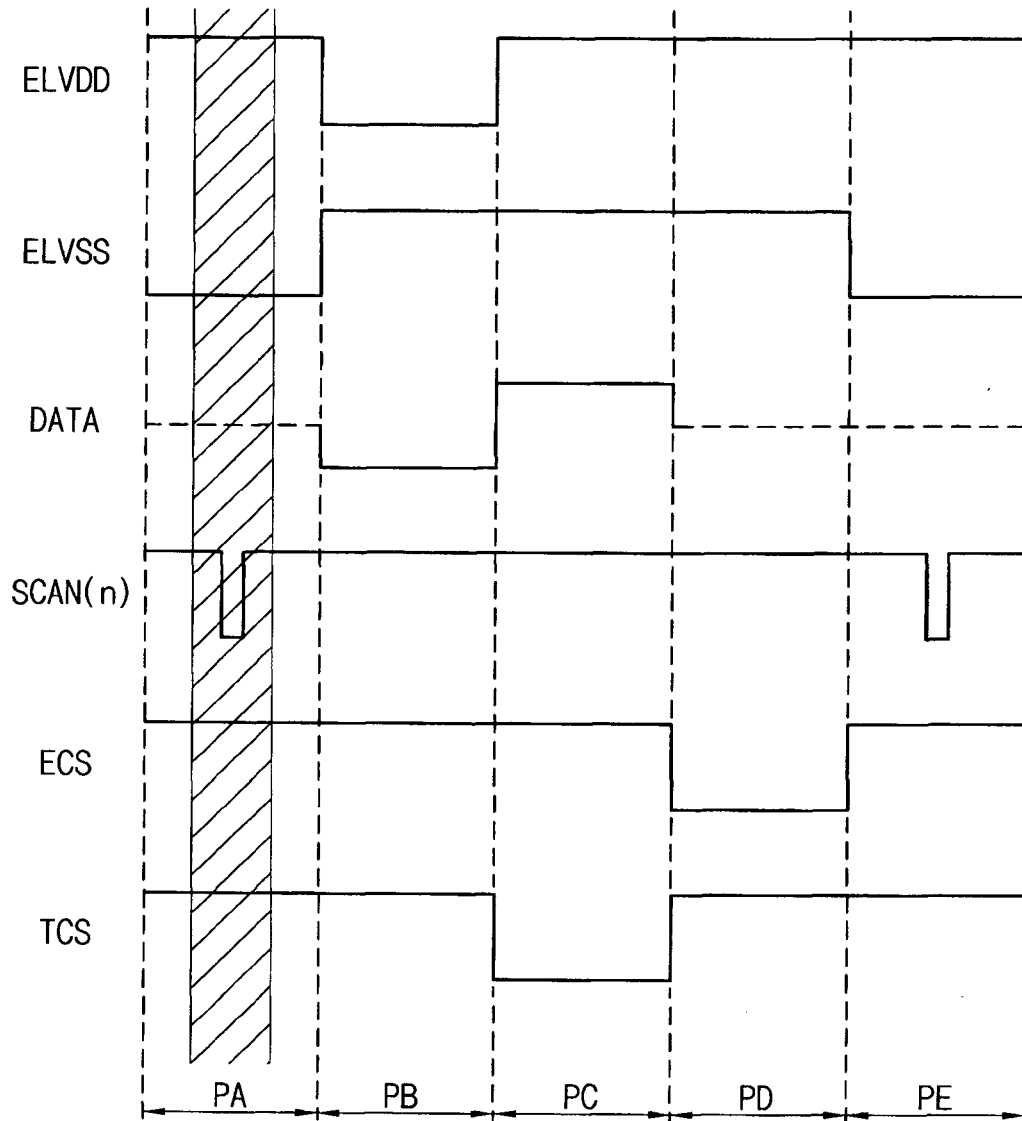


FIG. 4B

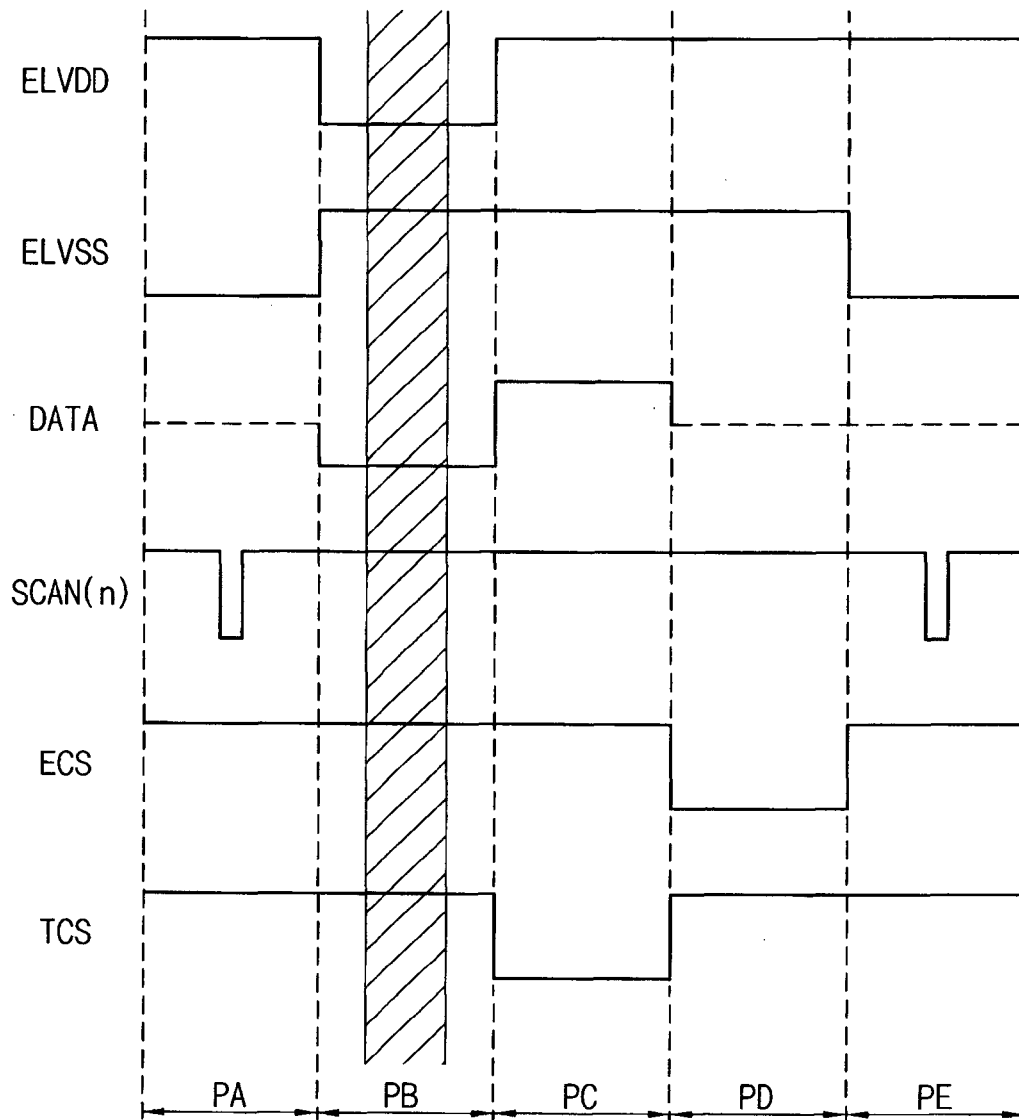


FIG. 4C

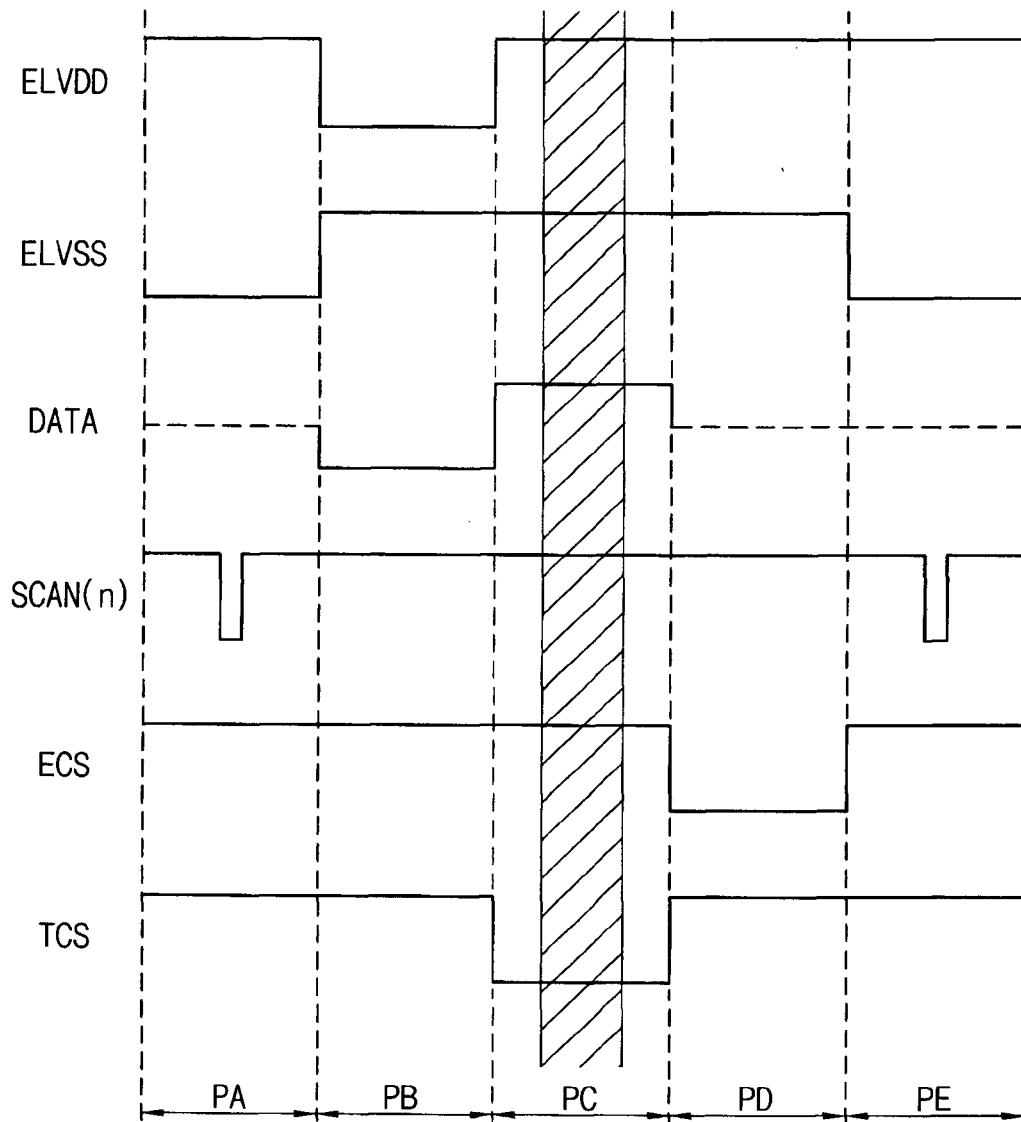


FIG. 4D

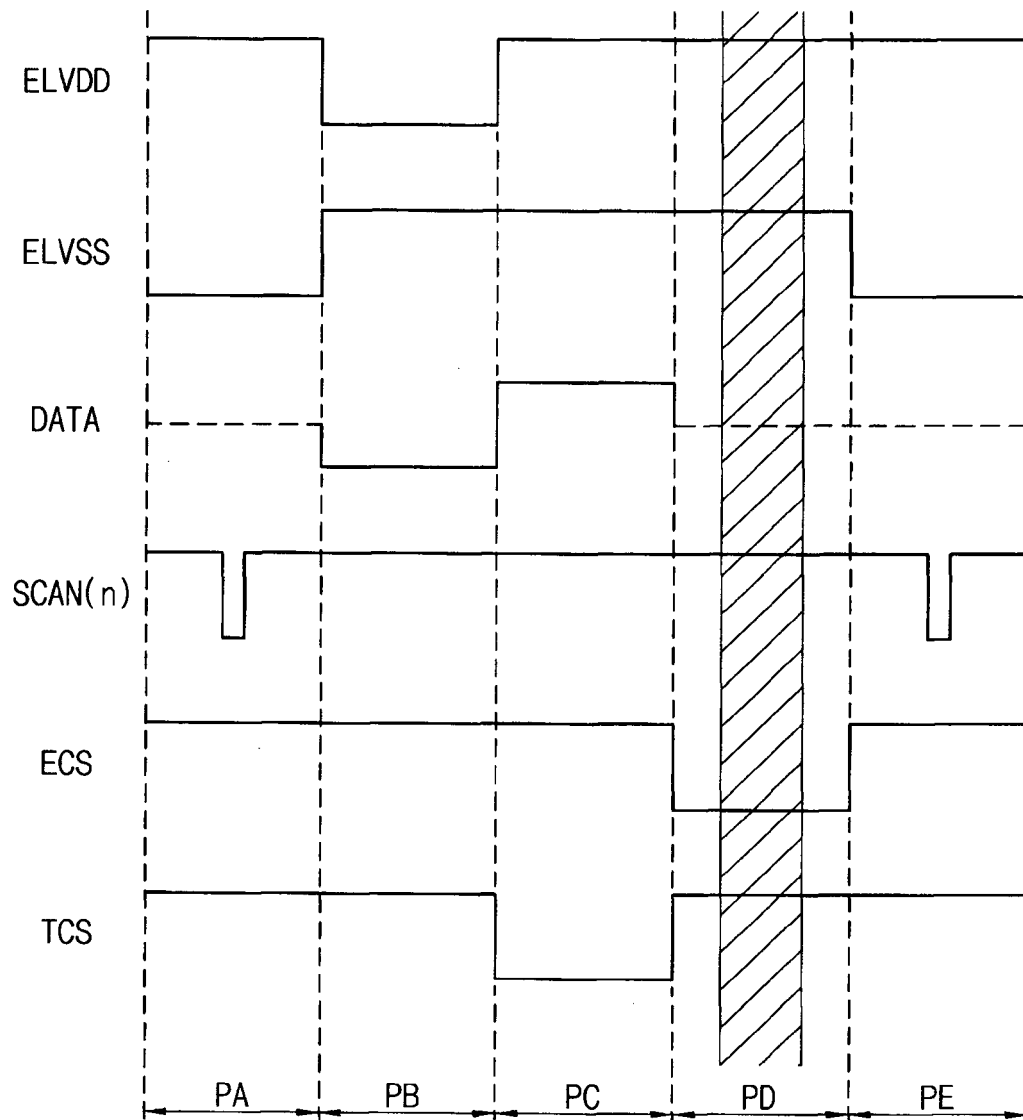


FIG. 4E

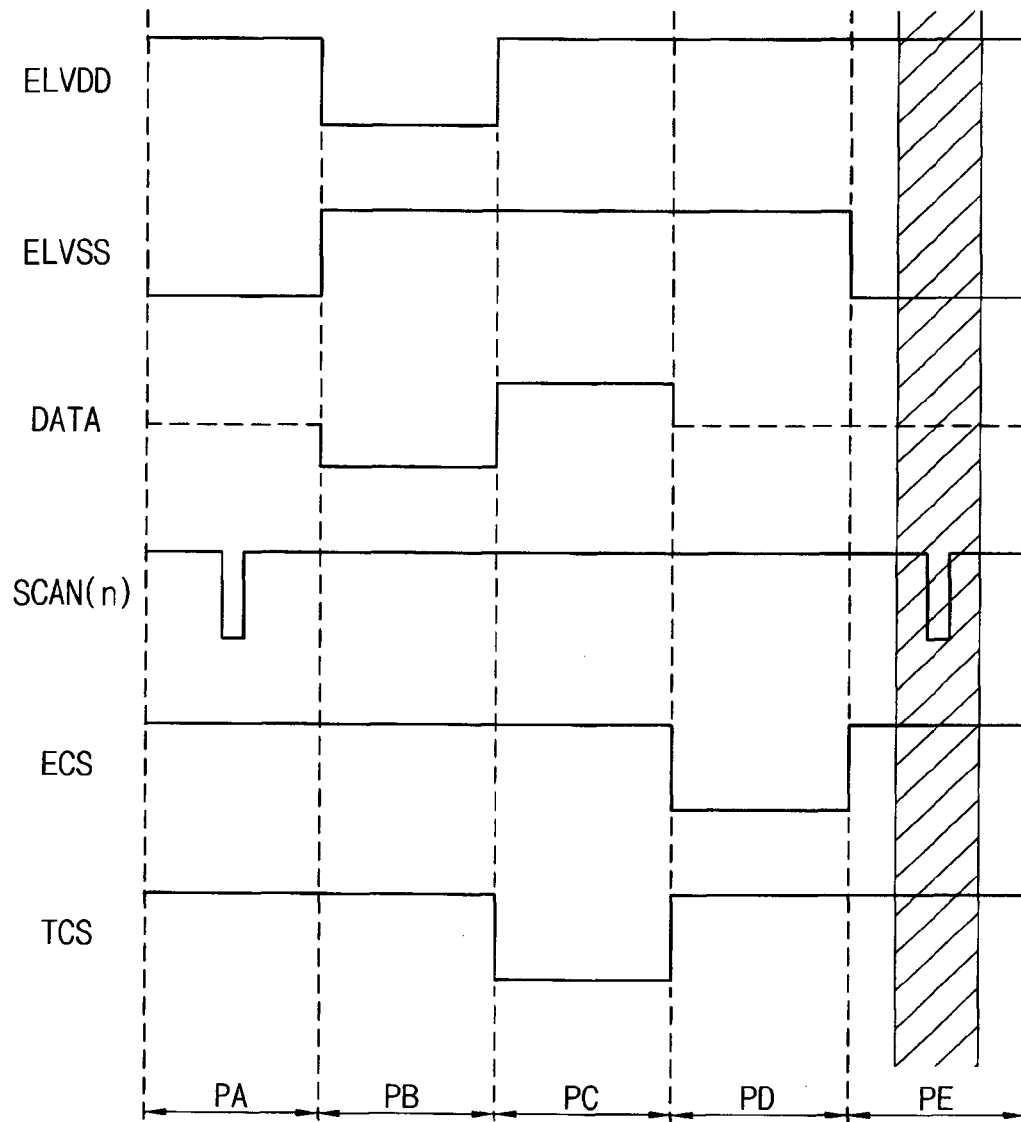


FIG. 5

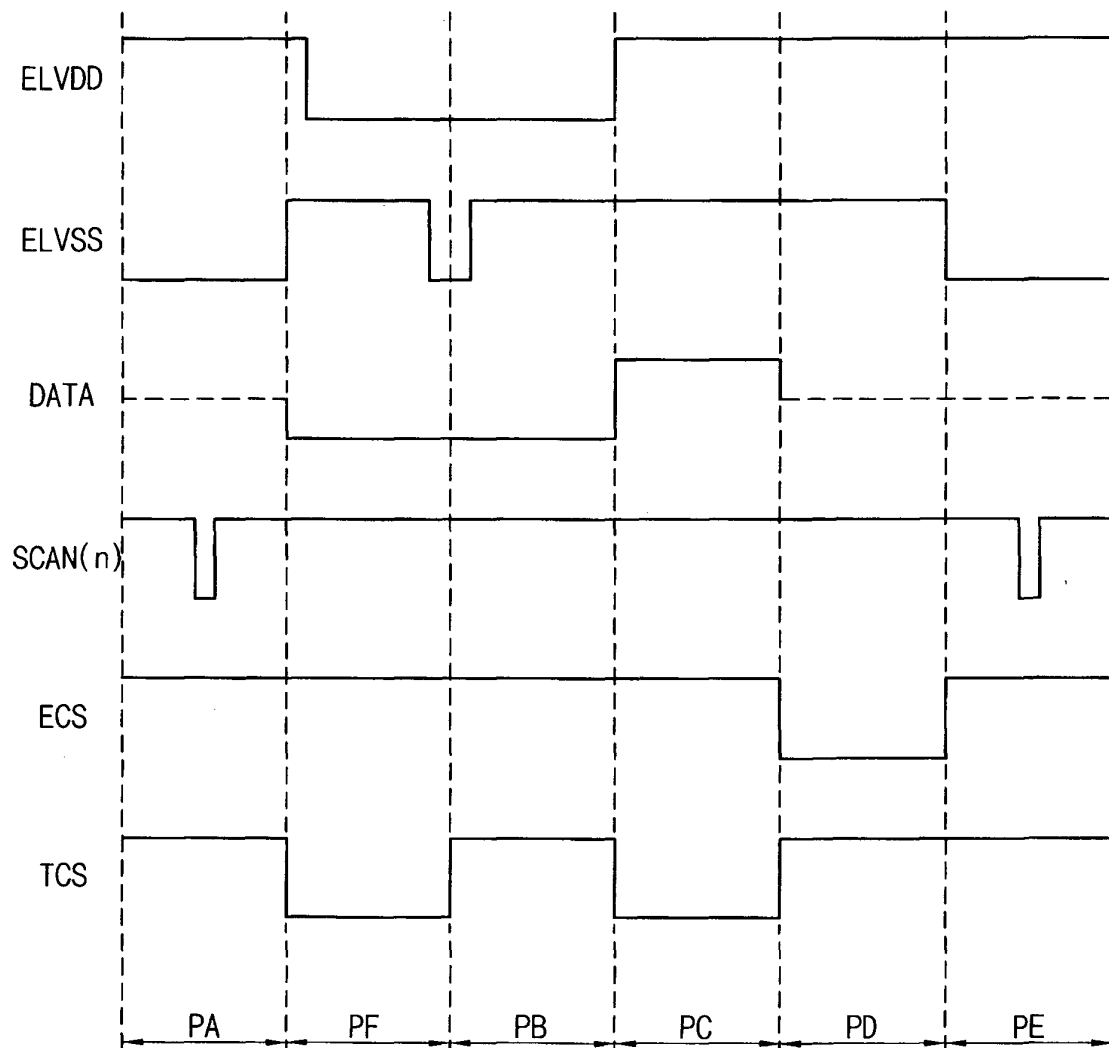


FIG. 6

200

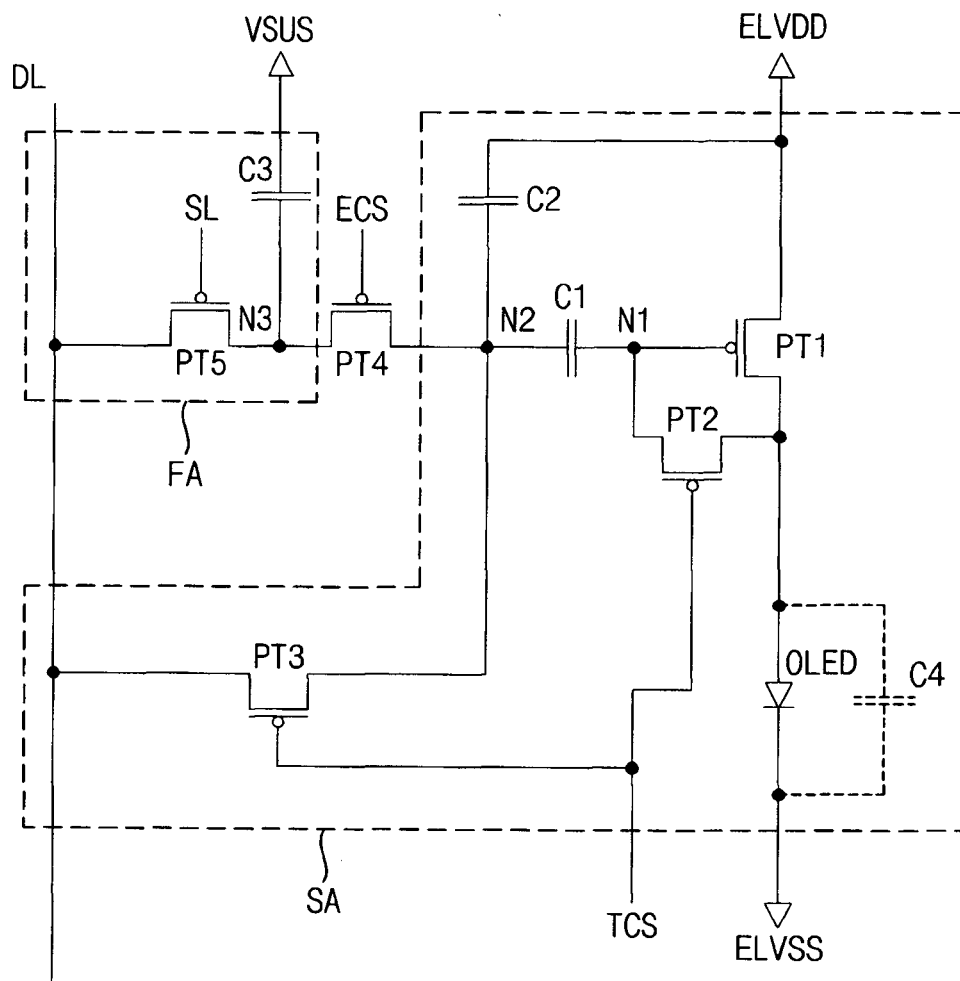


FIG. 7

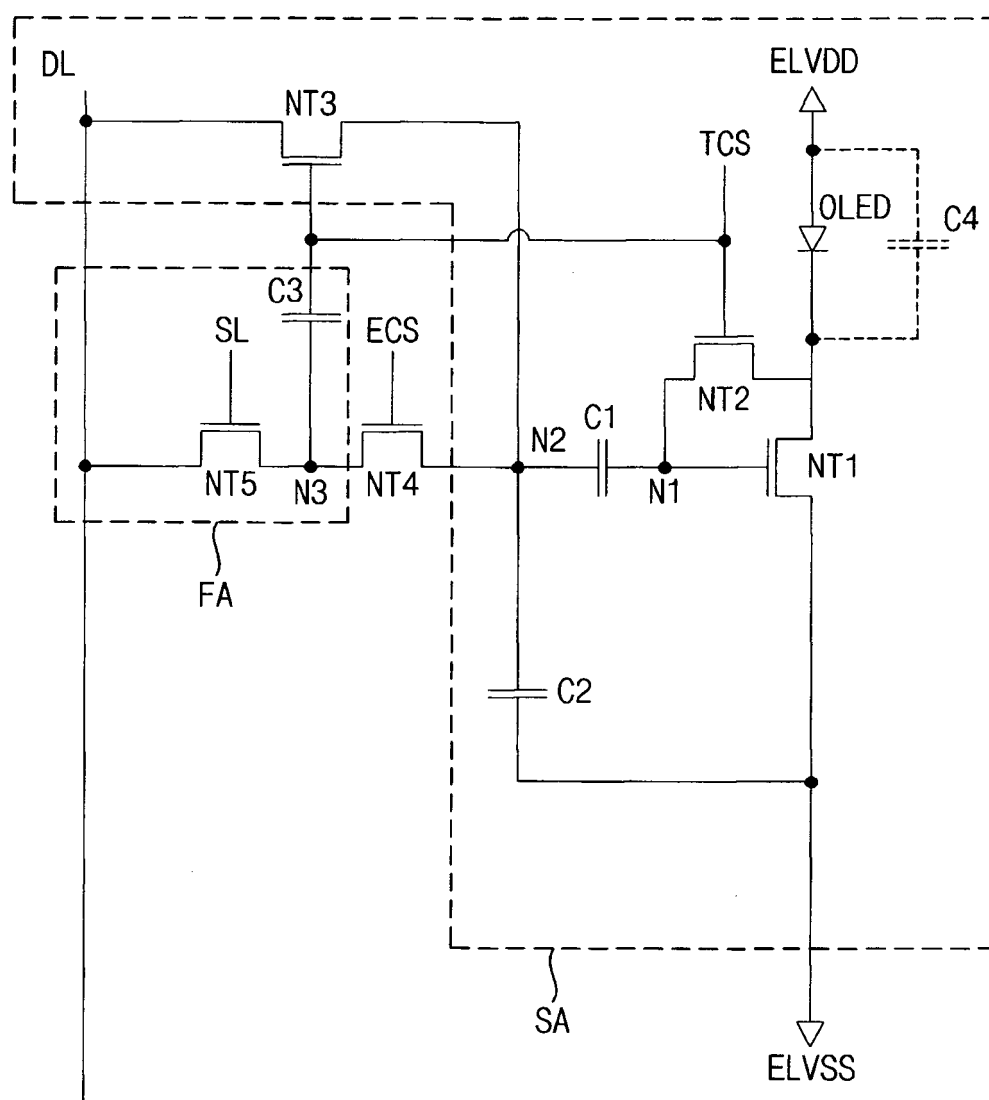
300

FIG. 8A

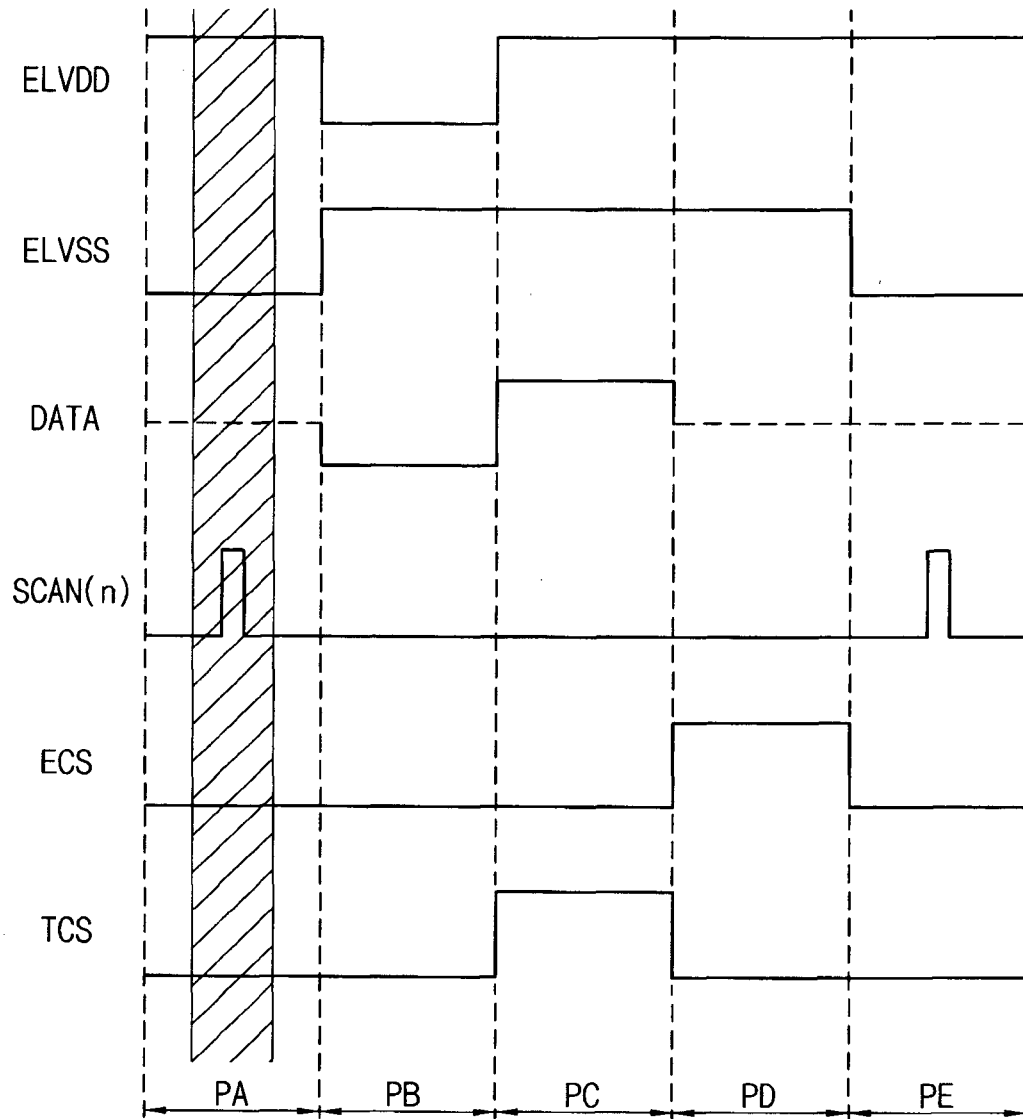


FIG. 8B

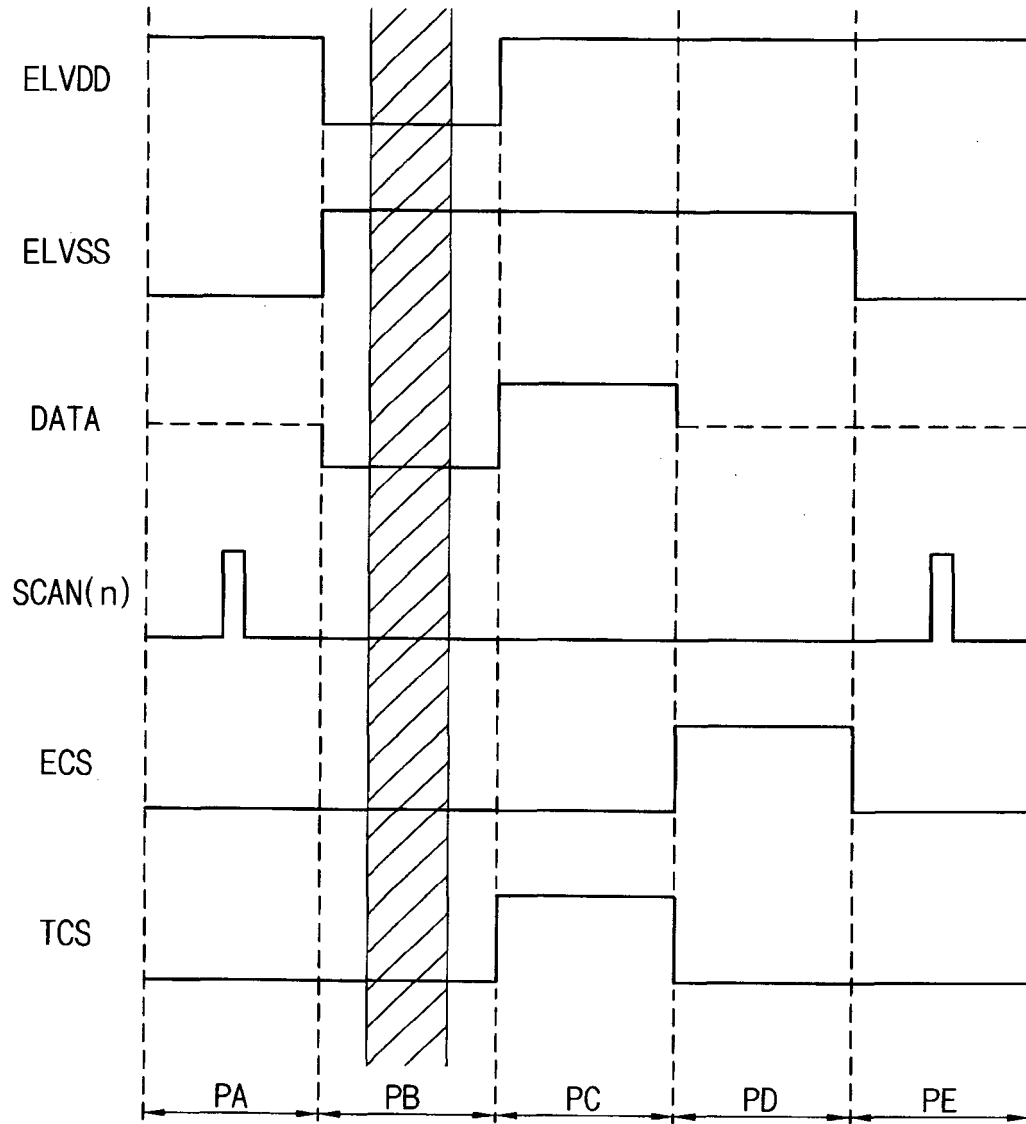


FIG. 8C

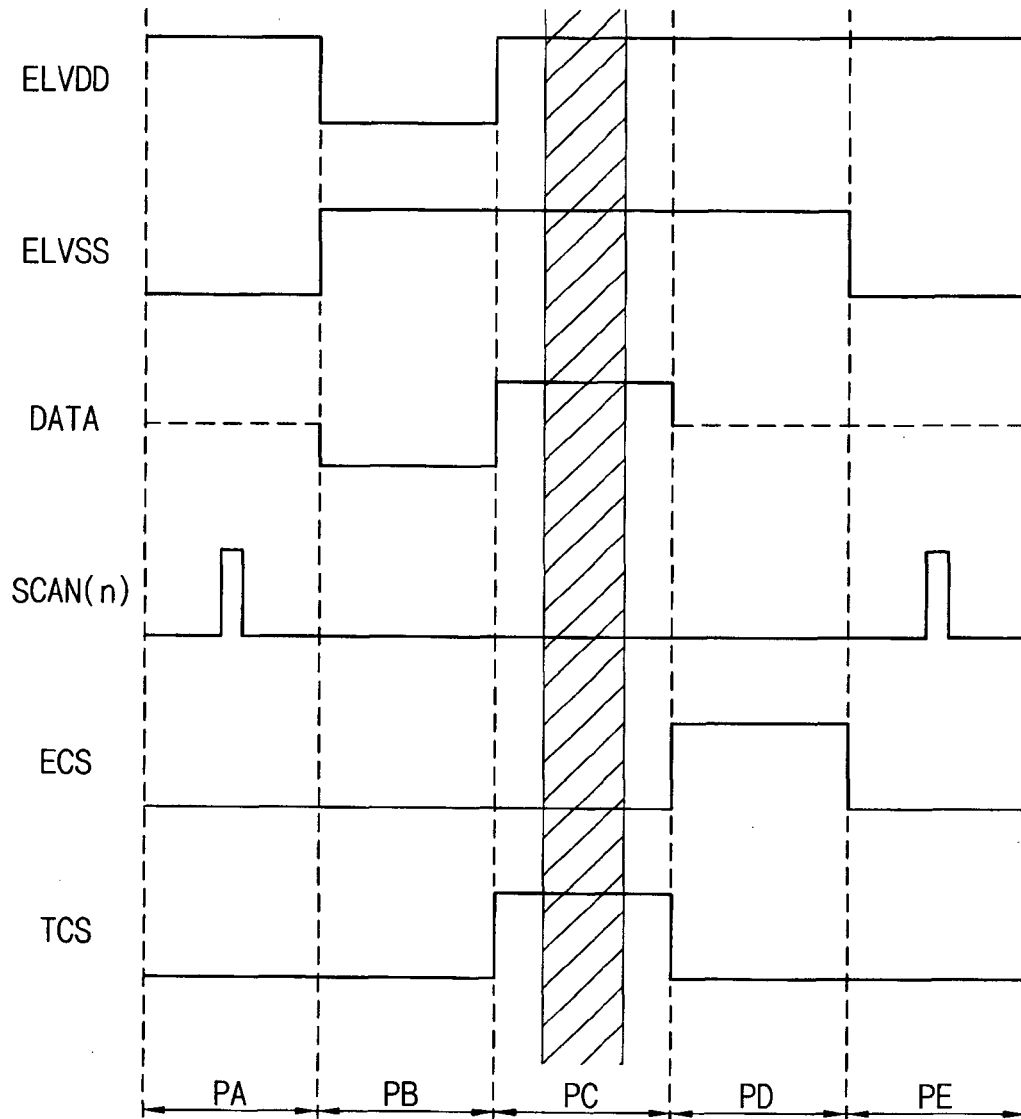


FIG. 8D

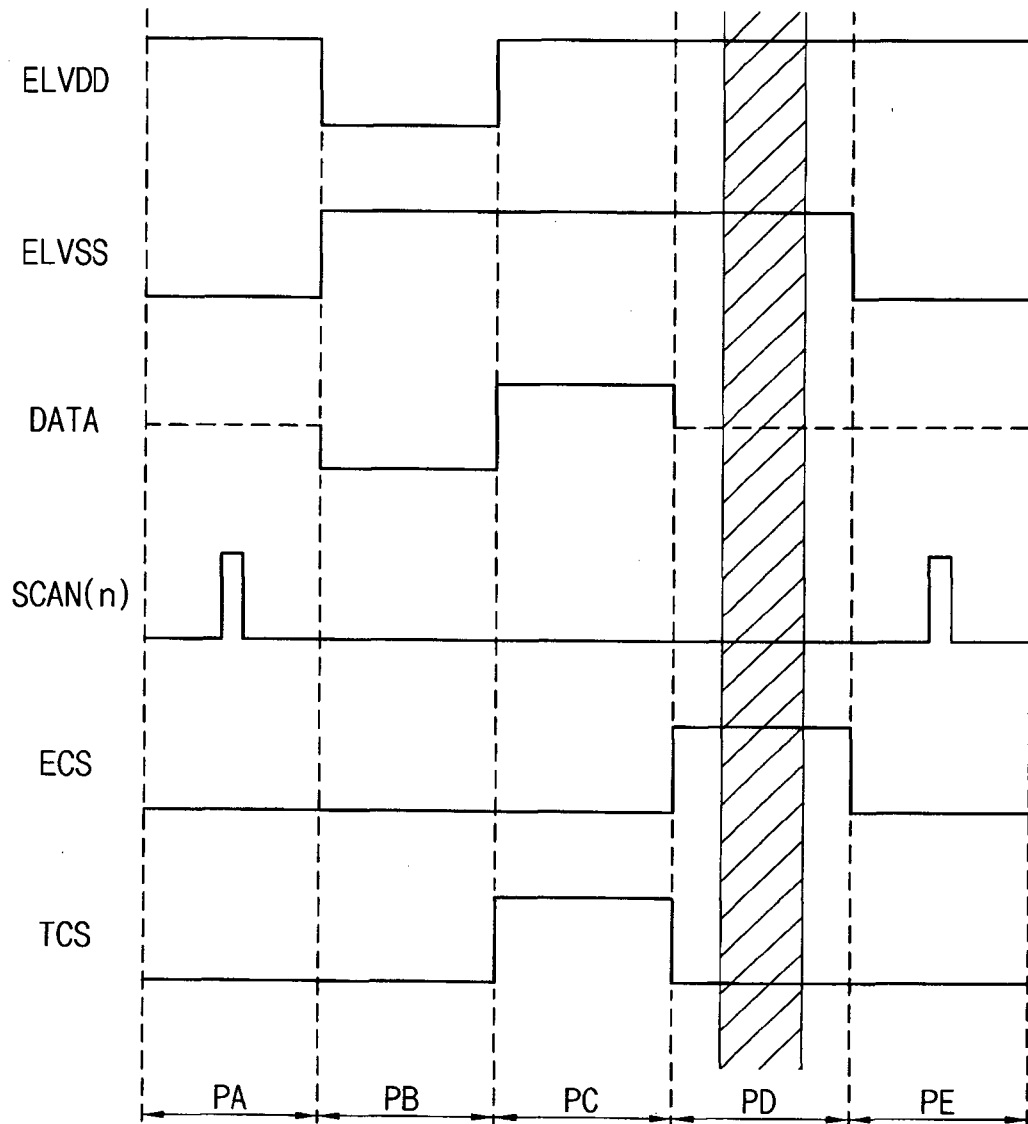


FIG. 8E

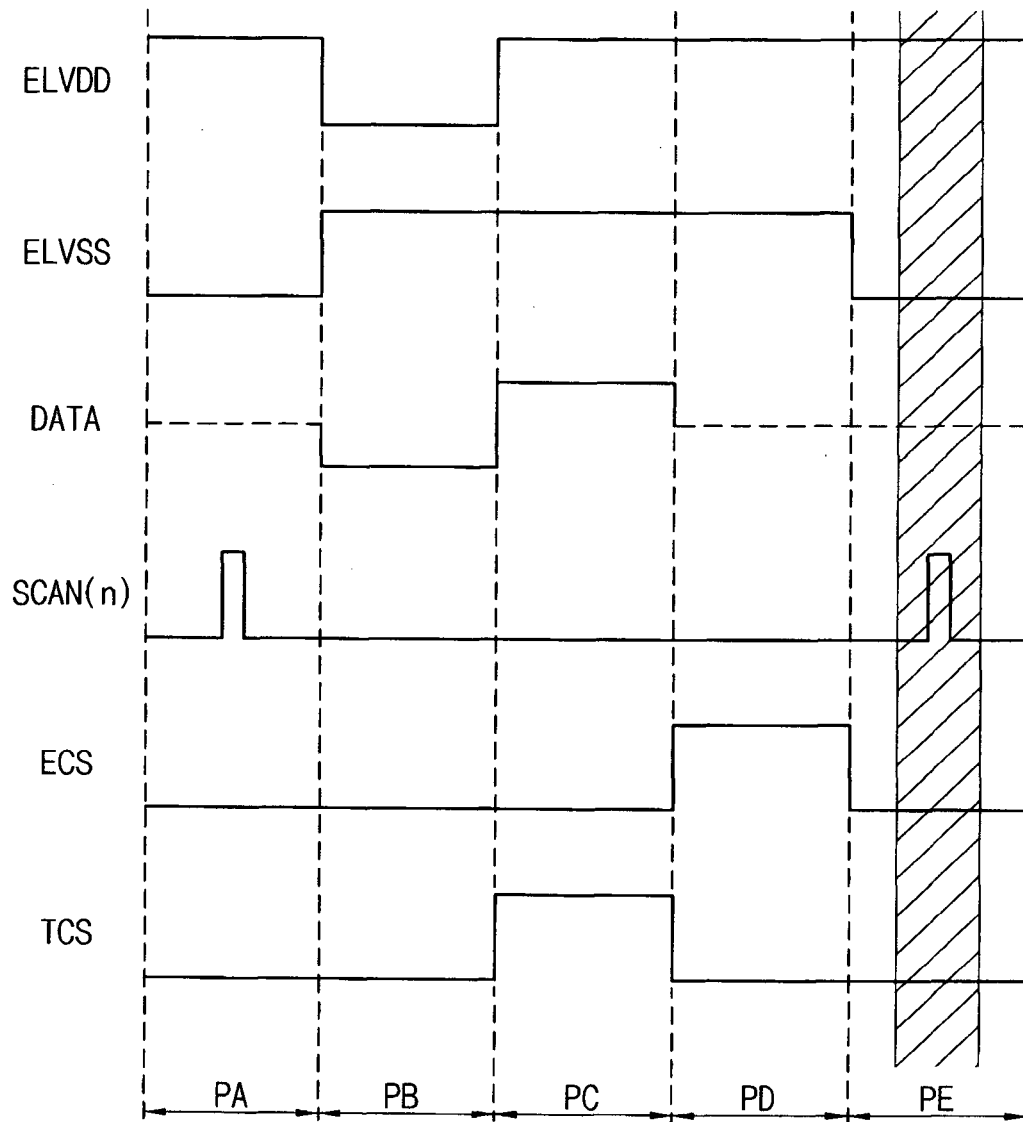


FIG. 9

400

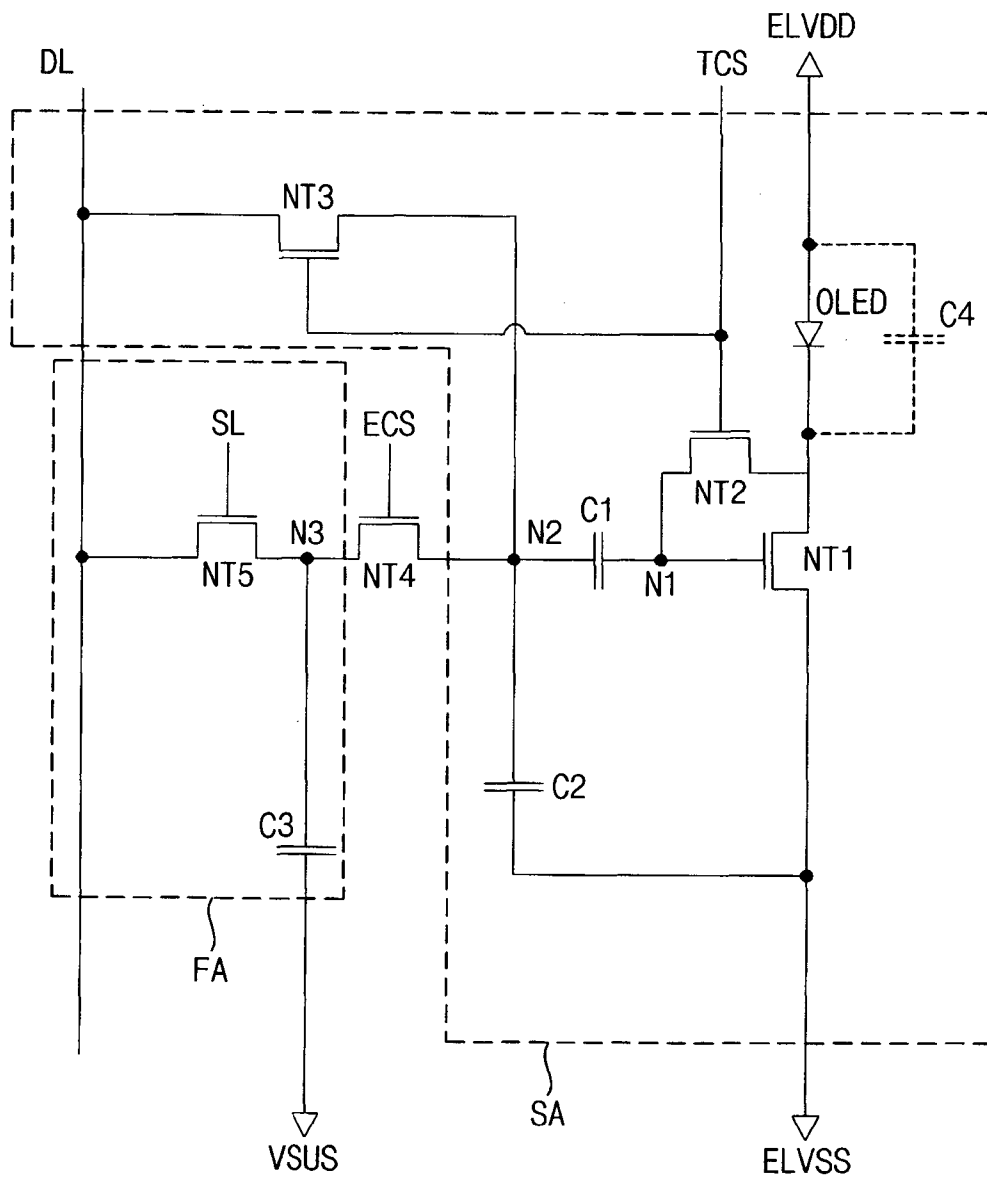


FIG. 10

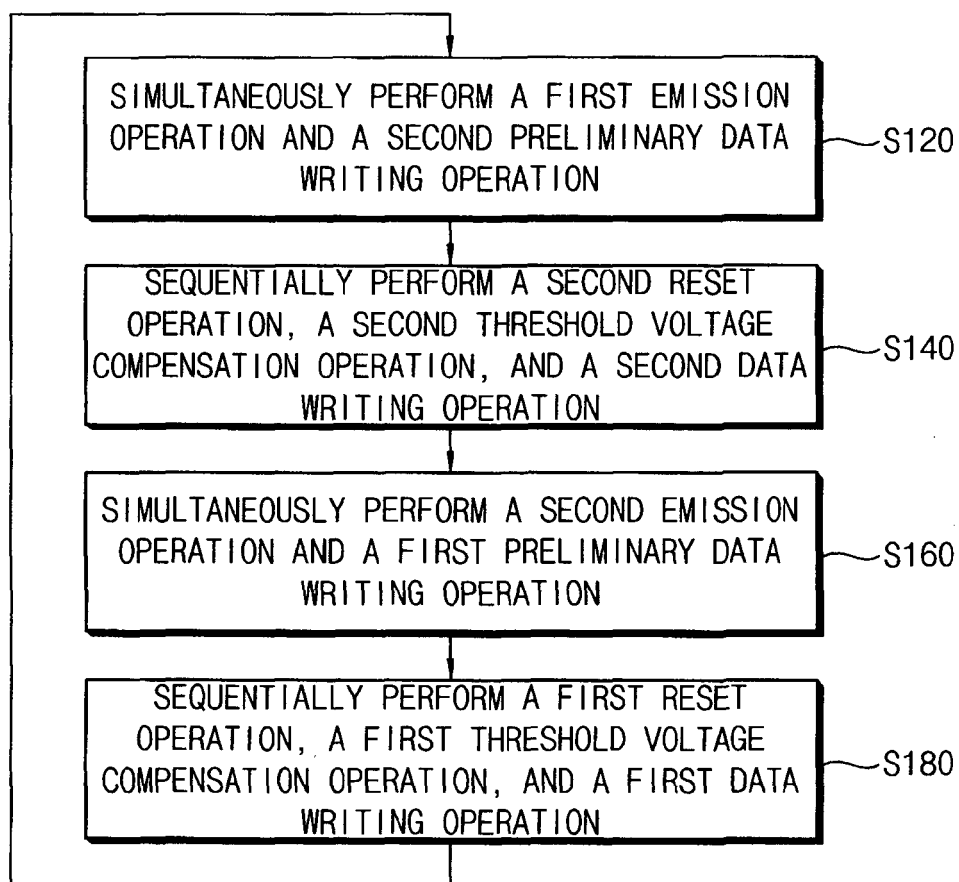


FIG. 11

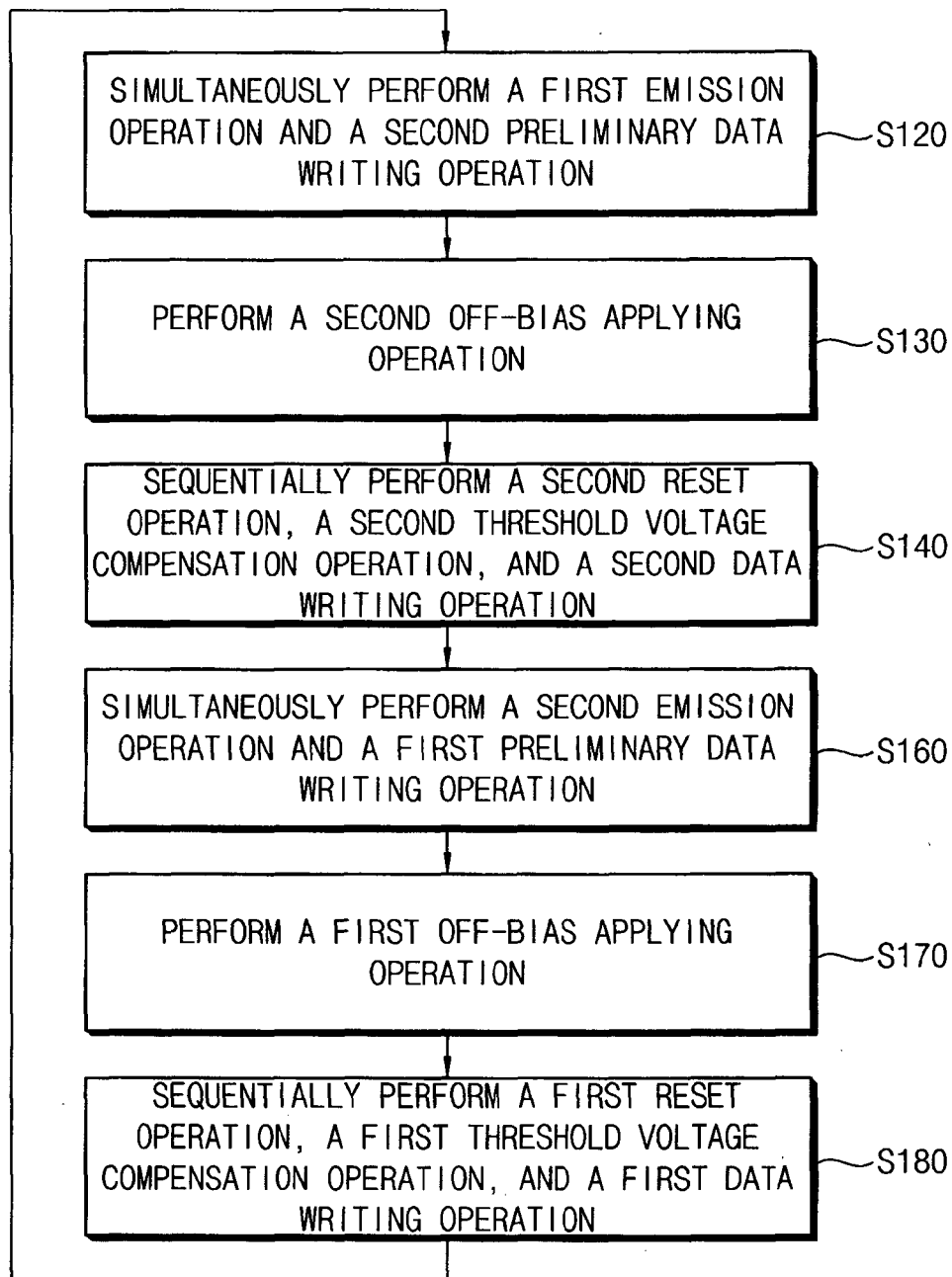


FIG. 12

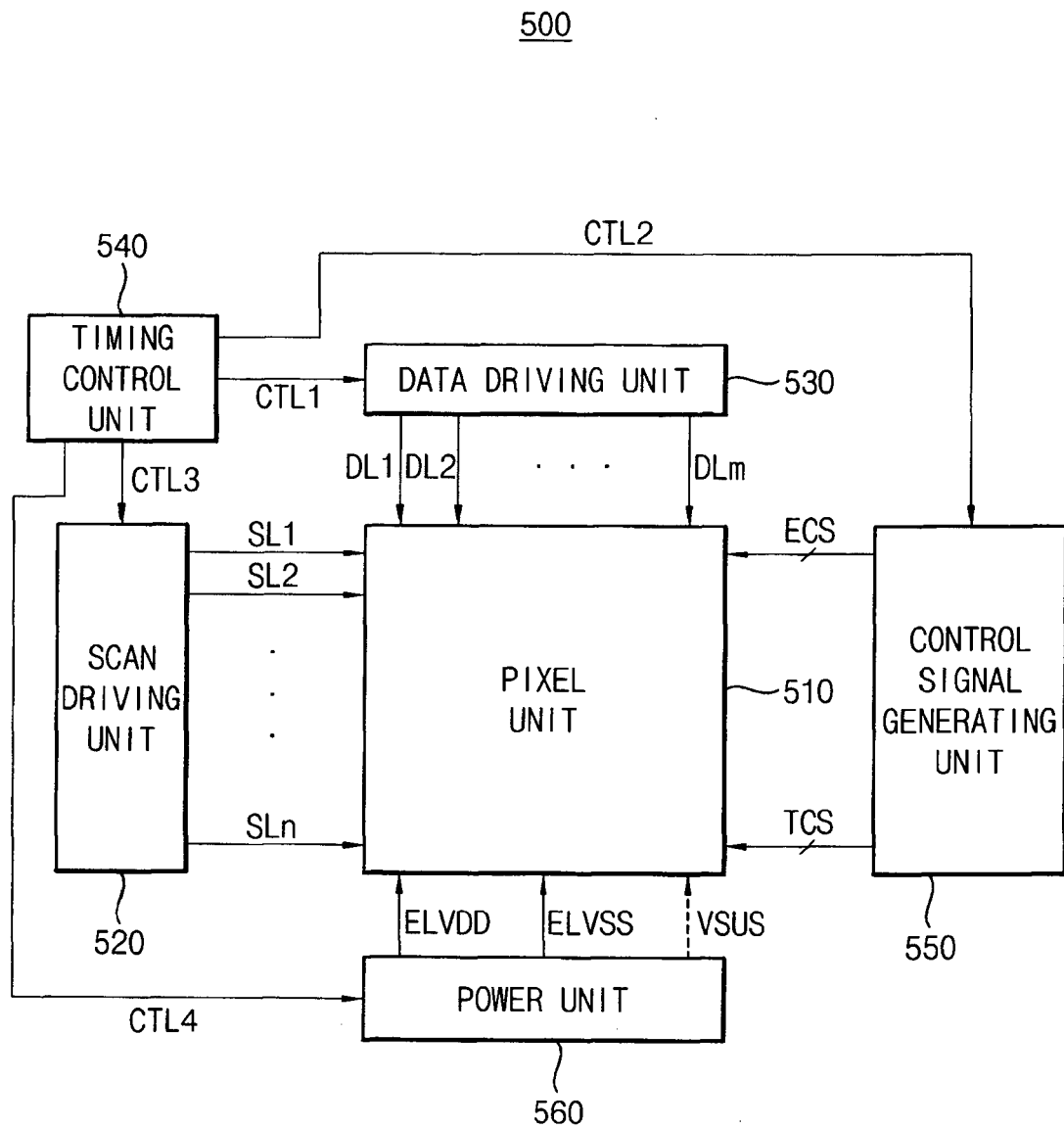


FIG. 13

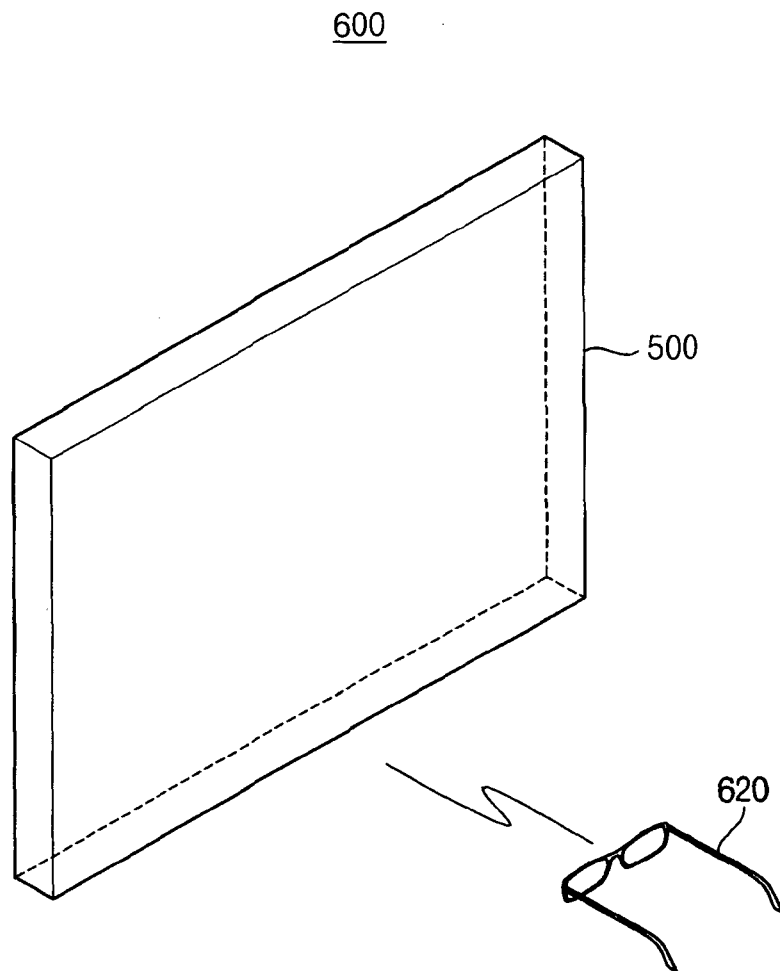


FIG. 14

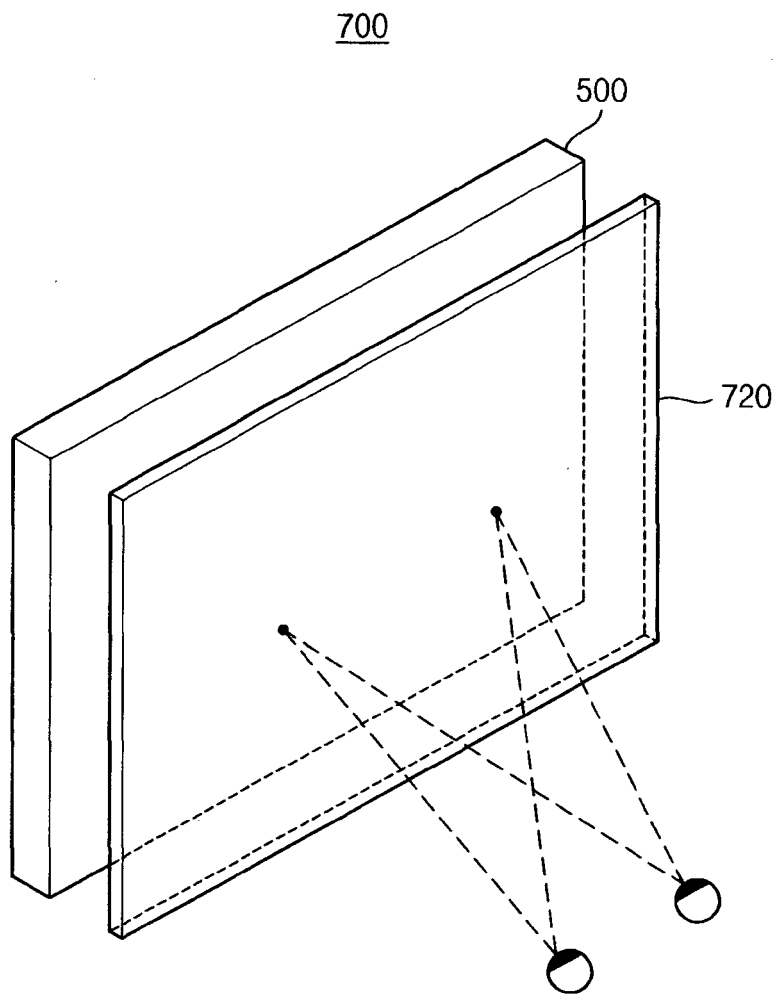
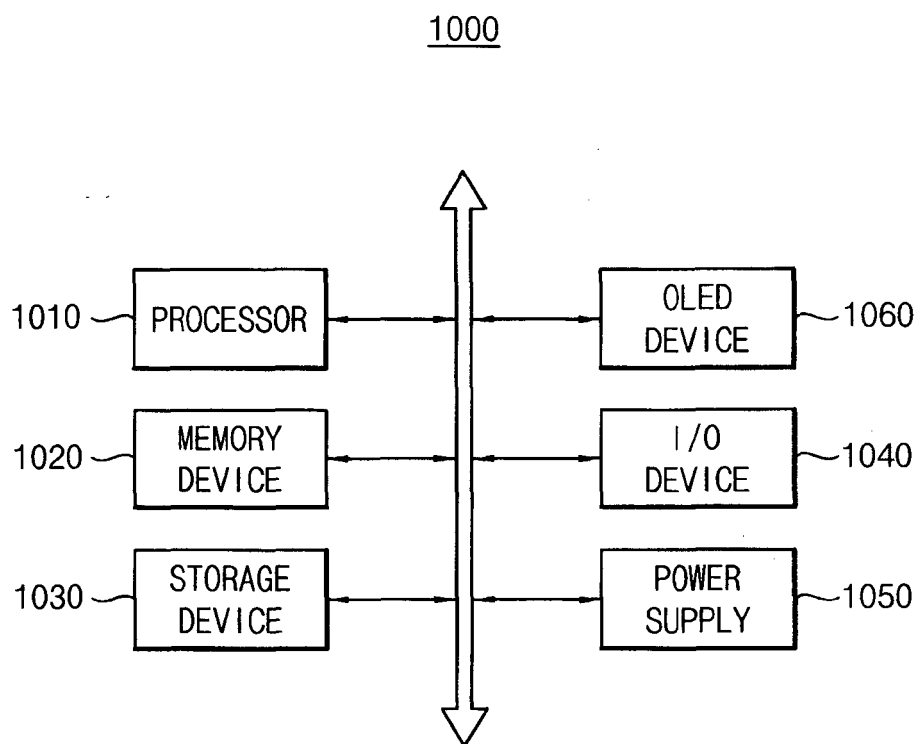


FIG. 15



专利名称(译)	像素电路，驱动像素电路的方法和有机发光显示装置		
公开(公告)号	<a href="#">EP2642476B1</a>	公开(公告)日	2015-01-14
申请号	EP2012189157	申请日	2012-10-19
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	HWANG YOUNG IN		
发明人	HWANG, YOUNG-IN		
IPC分类号	G09G3/32 G09G3/00 H04N13/04		
CPC分类号	G09G3/3258 G09G3/003 G09G3/3233 G09G3/3266 G09G3/3275 G09G2300/0469 G09G2300/0809 G09G2300/0819 G09G2300/0852 G09G2300/0866 G09G2310/0202 G09G2310/0216 G09G2310/0251 G09G2310/0262 G09G2310/063 G09G2310/08 G09G2320/0252 G09G2330/00 H04N13/315 H04N13/341 H04N13/398		
优先权	1020120029639 2012-03-23 KR		
其他公开文献	EP2642476A1		
外部链接	<a href="#">Espacenet</a>		

#### 摘要(译)

像素电路 ( 100,200,300,400 ) 包括有机发光二极管 ( OLED ) , 第一 PMOS 晶体管 ( PT1 ) , 其耦合在第一电源电压 ( ELVDD ) 和有机发光二极管 ( OLED 的阳极电极 ) 之间。 ) , 第二 PMOS 晶体管 ( PT2 ) 耦合在第一节点 ( N1 ) 和有机发光二极管 ( OLED ) 的阳极之间, 第一电容器 ( C1 ) 耦合在第二节点 ( N2 ) 和第一节点之间 ( N1 ) , 耦合在第一电源电压 ( ELVDD ) 和第二节点 ( N2 ) 之间的第二电容器 ( C2 ) , 耦合在数据线 ( DL ) 和第二节点 ( N2 ) 之间的第三 PMOS 晶体管 ( PT3 ) , 第四 PMOS 晶体管 ( PT4 ) 耦合在第三节点 ( N3 ) 和第二节点 ( N2 ) 之间, 第三电容器 ( C3 ) 耦合在第三节点 ( N3 ) 和第三 PMOS 晶体管 ( PT3 ) 的栅极端子之间或者维持电源电压 ( VSUS ) 和耦合在数据线 ( DL ) 和第三节点 ( N3 ) 之间的第五 PMOS 晶体管 ( PT5 ) 。

[Expression 1]

$$V_{eff} = \frac{C_{HOLD} \cdot V_{DATA} + (C_{ST} + C_{VTH}) \cdot V_0}{C_{HOLD} + C_{ST} + C_{VTH}}$$