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# (54) OLED PIXEL STRUCTURE AND DRIVING METHOD

(57) The present invention provides a pixel structure of an organic light emitting display device and driving method thereof. The pixel structure comprises first to fifth thin film transistors, a capacitor and an OLED device, wherein a radio of width to length of the first thin film transistor is set so as to compensate a brightness loss due to the degradation of the organic light emitting display device. Following steps are performed for the pixel structure in a refresh process of each frame of images: during a pre-charging period, the scan line and a first control signal (EM) are at a low level, a second control signal (EMD) is at a high level; during a compensation period, the scan line is at a low level, the first control signal (EM) and the second control signal (EMD) are at a high level; and during a light emitting period, the scan line is at a high level, the first control signal (EM) and the second control signal (EMD) are at a low level.

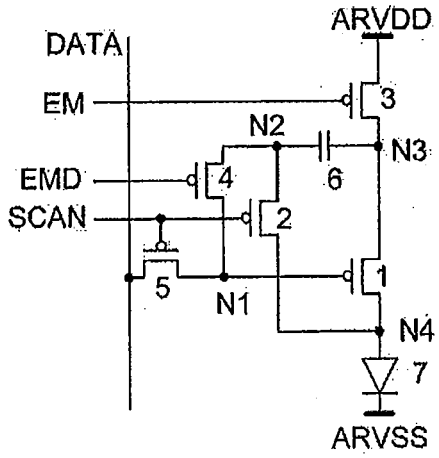


Fig. 1a

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## Description

### FIELD OF THE INVENTION

**[0001]** The present invention relates to a pixel structure of organic light emitting display device and driving method thereof.

### BACKGROUND

**[0002]** An Organic Light Emitting Display Diode (OLED), as a current-type light emitting device, has been applied to displays with high performance more widely. With an increasing in size of the display, the traditional passive matrix OLED requires shorter drive time for single pixel, and thus an instantaneous current has to be increased, which increases power consumption. Further, applying a large current would cause a voltage drop across ITO line too large and an operation voltage of the OLED too high, and in turn the efficiency of the OLED would decrease. Application of an Active Matrix OLED (AMOLED) device may settle such problem well, since it inputs OLED current by scanning line-by-line through switch transistors.

**[0003]** In designs for backboard of the AMOLED, a main problem to be settled is non-uniformity in brightness among pixels.

**[0004]** Firstly, most of the AMOLED constructs a pixel circuit by utilizing Low Temperature polycrystalline silicon Thin Film Transistor (LTPS TFT) so as to provide corresponding currents to the OLED devices. As compared with the general amorphous-Si TFT, the LTPS TFT has a higher mobility and a more steady character, and is more suitable for being applied in the AMOLED displays. However, the LTPS TFT formed on a glass substate with a large area often has non-uniformity on electrical parameters such as threshold voltage, mobility, etc. due to a limitation in the crystallization process, and such non-uniformity will lead to a current difference and brightness difference of the OLED display devices which may be perceptible to human eyes, that is, a mura phenomenon occurs.

**[0005]** Secondly, in an application of displays with large size, power lines on the backboard have certain resistance and the driving currents in all of the pixels are provided by the ARVDD, therefore a voltage of power supply in areas near a power supplying position of the ARVDD is higher than that in areas far away from the power supplying position in the backboard. This phenomenon is called as resistance voltage drop (IR Drop). Because the voltage of the ARVDD is relevant to the current, the IR Drop also causes current differences in different areas, and in turn the mura would occur as display.

**[0006]** Thirdly, uneven thickness in the film, when the OLED device is evaporated, also may cause the non-uniformity in the electrical performances. Further, after operating for a long time, a degradation of its internal electrical performances may result in an increased threshold voltage, such that the efficiency of light emitting is low and brightness drops. As shown in Fig.6(a), the brightness of the OLED device decreases, and its threshold voltage increases gradually, as the usage time increases.

**[0007]** How to compensate the degradation of the OLED device has been an important issue recently, because the degradation of the OLED may cause an occurrence of Image Sticking in areas displaying unchanged pictures for a long time, which affects the display effect.

**[0008]** As shown in Figs.6(b), 6(c), the increasing of the threshold voltage of OLED basically has a linear relationship with the brightness loss, and a relationship between the current of OLED and the brightness is also linear. Therefore, when the degradation of the OLED is compensated, we can increase the driving current linearly as the threshold voltage of OLED increases so as to compensate the brightness loss.

**[0009]** The AMOLED may be divided into three classes based on the driving mode: a digital type, a current type and a voltage type. The driving method of digital type realizes grayscale levels by using TFTs as switches to control a driving time without compensating the non-uniformity, but its operation frequency would increase doubly with an increasing of the display size, which results in a large amount of power consumption and would reach the physical limit of design in a certain range, therefore it is not suitable for applications with large display size. The driving method of current type realizes grayscale levels by providing different currents to the drive transistor directly, and it may compensate the non-uniformity of the TFTs and the IR drop well, however, a overlong written time would occur when a small current charges a large parasitic capacitance on the data line, and such problem is specially serious and difficult to be overcome in the large size display. The driving method of voltage type is similar to the traditional driving method for AMLCD and provides a voltage signal indicating grayscale level by a driving IC, and the voltage signal would be converted into a current signal of the drive transistor inside the pixel circuit, so that the OLED is driven to realize grayscale presenting the brightness. Therefore, the driving method of voltage type is used widely in the industry for its rapid driving speed and simply implementation, and is suitable to drive a large size panel, but the non-uniformity of TFTs and IR drop have to be compensated by other TFTs and capacitors designed additionally.

**[0010]** Fig.7 is a traditional pixel circuit structure of a voltage driving type, comprising 2 TFTs and 1 capacitor (2T1C).

A switching transistor T2 transfers the voltage on the data line to the gate of the driving transistor T1, and the driving transistor T1 converts the data voltage to a corresponding current for supplying for the OLED device. In a normal operation, the driving transistor operates in a saturation area and provides a constant current during a period for scanning one line. As shown in following equation (1), the driving current is expressed as:

**[0011]**

$$I_{OLED} = \frac{1}{2}\mu_P \cdot Cox \cdot \frac{W}{L} \cdot (Vdata - ARVDD - V_{TH})^2 \quad (1)$$

**[0012]** Wherein $\mu_P$ denotes carrier mobility, $C_{OX}$ denotes a gate oxide layer capacitance, W/L denotes a ratio of width to length of the transistor, Vdata denotes a data voltage, ARVDD denotes a backboard power supply of the AMOLED shared by all pixel units, and $V_{th}$ denotes a threshold voltage of the transistor. It can be seen from the above equation, variation occurs in the current if the $V_{th}$ among different pixel units are different. Further, with the degradation of the OLED device, the brightness of the OLED would decrease even if a constant current is provided.

**[0013]** Document [1] discloses a pixel structure which is capable of compensating the non-uniformity of $V_{th}$ and IR drop, and the control timing thereof, as shown in Fig.8. The structure in Fig.8 may compensate effects due to the non-uniformity of $V_{th}$, IR drop and the degradation of OLED, but it is not suitable for the application with a large size panel since it is adopted in a driving method of current type.

**[0014]** It can be seen that, no effectual means for settling the previously-described problems, that is, how to compensate a luminance non-uniformity caused by the degradation of the OLED device, the non-uniformity of the threshold voltage in the TFTs and the voltage drop of the backboard power supply (IR drop), are not proposed in the prior art.

**[0015]** Reference Document

**[0016]** [1] "Current programming pixel circuit and data-driver design for active-matrix organic light-emitting diodes", Journal of the Society for Information Display 12 (2004)227

SUMMARY

**[0017]** Embodiments of the present invention provide an improved pixel structure of an organic light emitting display device (OLED). The pixel structure enables a driving current flowing through the OLED device to be independent of the threshold voltage of a thin film transistor and the power supply of a backboard, and thus the problem of uneven luminance due to non-uniformity in the threshold voltage of the driving TFT and the voltage drop (IR drop) of the power supply of the backboard is eliminate.

**[0018]** According to one embodiment of the present invention, the pixel structure comprises first to fifth thin film transistors, a capacitor and an OLED device, wherein a drain of the first thin film transistor is connected to a negative power supply via the OLED device, a source of the first thin film transistor is connected to a drain of the third thin film transistor, and a source of the third thin film transistor is connected to a positive power supply; one end of the capacitor is connected to a third node N3 between the first and third thin film transistors, and the other end of the capacitor is connected to a second node N2 between a source of the second thin film transistor and a source of the fourth thin film transistor; a drain of the second thin film transistor is connected to a fourth node N4 between the first thin film transistor and the OLED device, a drain of the fourth thin film transistor is connected to a first node N1 between a drain of the fifth thin film transistor and a gate of the first thin film transistor, a source of the fifth thin film transistor is connected to a data line, and a gate of the fifth thin film transistor and a gate of the second thin film transistor are connected to a scan line; and a first control signal (EM) is provided to a gate of the third thin film transistor, and a second control signal (EMD) is provided to a gate of the fourth thin film transistor.

**[0019]** According to one embodiment of the present invention, for example, for the pixel structure, during a pre-charging period, a line scanning voltage on the scan line and the first control signal are at a low level, and the second control signal is at a high level; the fourth thin film transistor is turned off, the first, second, third and fifth thin film transistors are turned on, and a data voltage is transferred to the gate of the first thin film transistor via the fifth thin film transistor.

**[0020]** According to one embodiment of the present invention, for example, for the pixel structure, during a compensation period, a line scanning voltage on the scan line is at a low level, and the first control signal and the second control signal are at a high level; the third and fourth thin film transistors are turned off, the first, second and fifth thin film transistors are turned on, and a data voltage is transferred to the gate of the first thin film transistor via the fifth thin film transistor.

**[0021]** According to one embodiment of the present invention, for example, for the pixel structure, during a light emitting period, a line scanning voltage on the scan line is at a high level, and the first control signal and the second control signal are at the low level; the second and fifth thin film transistors are turned off, and the first, third and fourth thin film transistors

are turned on.

**[0022]** According to one embodiment of the present invention, for example, for the pixel structure, during the pre-charging period and the compensation period, the signal on the data line (DATA) is an actual data voltage.

**[0023]** According to one embodiment of the present invention, for example, the first to fifth thin film transistors in the pixel structure are low temperature polycrystalline silicon thin film transistors.

**[0024]** According to one embodiment of the present invention, for example, a radio of width to length of the first thin film transistor in the pixel structure is set so as to compensate a brightness loss due to the degradation of the OLED device.

**[0025]** According to one embodiment of the present invention, a method for driving the above-described pixel structure is further provided, wherein the method comprises the following steps performed in a refresh process of each frame of an image: during a pre-charging period, the scan line and a first control signal (EM) are at a low level, and a second control signal (EMD) is at a high level, so that a fourth thin film transistor is turned off, and first, second, third and fifth thin film transistors are turned on; during a compensation period, the scan line is at a low level, and the first control signal (EM) and the second control signal (EMD) are at a high level, so that the third and fourth thin film transistors are turned off, and the first, second and fifth thin film transistors are turned on; and during a light emitting period, the scan line is at a high level, the first control signal (EM) and the second control signal (EMD) are at a low level, so that the second and fifth thin film transistors are turned off, and the first, and third and fourth thin film transistors are turned on.

**[0026]** With the above-described improved pixel structure of the AMOLED and driving method thereof, it cab effectively compensate the degradation of the OLED device, the non-uniformity in the threshold voltage of the driving TFT and the voltage drop of the power supply of the backboard, and thus the display effect and power consumption are further improved.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0027]** Below will describe the embodiments of the present invention in details in connection with the accompanying drawings, wherein:

**[0028]** Fig.1a shows the pixel structure of the present invention;

**[0029]** Fig.1b shows a control timing of the pixel structure shown in Fig.1a;

**[0030]** Fig.2a to Fig.2c show circuit states of the pixel structure in Fig.1 during three different periods;

**[0031]** Fig.3 shows a graph which is stimulated for uniformity compensation of the threshold voltage in the TFT driving transistor;

**[0032]** Fig.4 shows a graph which is stimulated for compensation of the voltage drop of the power supply in the backboard;

**[0033]** Fig.5 shows a graph which is stimulated for compensation of the degradation of the OLED device;

**[0034]** Figs.6a-c show a graph indicating the variation in the brightness and threshold voltage of the OLED device as the usage time increases;

**[0035]** Fig. 7 shows a circuit diagram of traditional pixel structure; and

**[0036]** Figs. 8a-b shows pixel compensation circuit diagram and control timing diagram in the reference document 1.

## DETAILED DESCRIPTION

**[0037]** As shown in Fig.1a, the pixel circuit structure comprises P-type TFT transistors 1 to 5, a capacitor 6 and a OLED 7, wherein ARVDD and ARVSS are backboard direct current positive and negative level, respectively, DATA is a data voltage signal, SCAN is a line scanning voltage signal, EM and EMD are control signals. The pixel units in a same row share the SCAN and the EN, END control signals, and the pixel units in a same column share the DATA data voltage signal commonly. In the pixel circuit structure according to the present invention, a drain of the first thin film transistor 1 is connected to the negative level of the backboad via the OLED device, and a source of the first thin film transistor 1 is connected to a drain of the third thin film transistor 3; a source of the third thin film transistor 3 is connected to the positive level of the backboard; one end of the capacitor 6 is connected between the first thin film transistor 1 and the third thin film transistors 3(i.e., the node N3), the other end of the capacitor 6 is connected to a source of the second thin film transistor 2 and a source of the fourth thin film transistor 4 (i.e., the node N2); a drain of the second thin film transistor 2 is connected to the drain of the first thin film transistor 1 and the OLED device 7 (i.e., the node N4); a drain of the fourth thin film transistor 4 is connected to a drain of the fifth thin film transistor 5 and a gate of the first thin film transistor 1 (i.e., the node N1), wherein a source of the fifth thin film transistor 5 is connected to a data line, a gate of the fifth thin film transistor 5 and a gate of the second thin film transistor 2 are connected to a scan line; a first control signal (EM) is provided to a gate of the third thin film transistor, and a second control signal (EMD) is provided to a gate of the fourth thin film transistor.

**[0038]** The operation process of the pixel circuit is divided into three stages, that is, pre-charging, compensation and light emitting, and the control signal timing thereof is as shown in Fig.1b.

**[0039]** As shown in Fig.2a, the first stage is the pre-charging stage. During this stage, the SCAN and EM are at a low level, the EMD is at a high level, and the DATA is at an actual data voltage. At this time, the transistor 4 is turned off, the transistors 1, 2, 3 and 5 are turned on, and a data voltage is transferred to the first node N1 on the gate of the transistor 1 via the transistor 5. The third node N3 is connected to ARVDD via the transistor 3 and its potential is ARVDD. The voltage at the fourth node N4 is ARVSS plus OLED driving voltage. Since the transistor 2 is turned on, here the capacitor 6 is equivalent to being connected between the third node N3 and the fourth node N4. The function of the pre-charging is to make the third node N3 reach a high potential in advance, so that the transistor 1 can establish an appropriate initial voltage during the compensation process in the second stage.

**[0040]** The second stage is the compensation stage, as shown in Fig.2b. In this stage, the SCAN is at a low level, the EM and EMD are at a high level, and the Vdata is the actual data voltage. At this time, the transistors 3, 4 are turned off, and the transistors 1, 2 and 5 are turned on. The data voltage is transferred to the first node N1 via the transistor 5. Because the third node N3 is connected to the ARVDD via the transistor 3 before the EM changes to the high level, the initial voltage of the third node N3 at the moment when being turned off is the high level ARVDD; after the transistor 3 is turned off, the third node N3 is in a floating state and the transistor 1 is turned on, the third node N3 discharges to ARVSS, and therefore the potential at the third node N3 may drop gradually, until the transistor 1 locates in a critical cutoff area. At this time, the voltage at the third node N3 is VDATA-VTH, wherein the VTH is the threshold voltage of the transistor 1. In this course, the potential at the fourth node N4 may reduce with the current flowing through the transistor 1 and OLED decreasing, until the transistor 1 is turned off and the current is zero. At this time, the voltage at the fourth node N4 is $V_{OLED\_0}$, that is, the threshold voltage of the OLED 7. Thus, charges of $(V_{DATA}-V_{TH}-V_{OLED\_0}) \cdot C$ are stored in the capacitor 6.

**[0041]** The third stage is light emitting stage, as shown in Fig.2c. In this stage, the SCAN is at a high level, the EM, EMD are at a low level, and transistors 2, 5 are turned off, the transistors 1, 3, 4 are turned on at this time. The third node N3 is connected with ARVDD via the transistor 3, and its potential changes to ARVDD. Since the transistor 5 is turned off and no direct current path exists for the first node N1, the total amount of the charges at this node remains unchanged as compared with that in the second stage, as indicated by the following equation (2).

**[0042]**

$$(V_{DATA} - V_{TH} - V_{OLED\_0}) \cdot C = (ARVDD - V_{N1}) \cdot C \qquad (2)$$

**[0043]** By calculating, we can get $V_{N1} = ARVDD - V_{DATA} + V_{TH} + V_{OLED\_0}$ (3)

**[0044]** At this time, the current flowing through the transistor 1 is

**[0045]**

$$\begin{aligned} I_{OLED} &= \frac{1}{2} \cdot \mu_p \cdot Cox \cdot \frac{W}{L} \cdot (ARVDD - V_{DATA} + V_{TH} + V_{OLED\_0} - ARVDD - V_{TH})^2 \\ &= \frac{1}{2} \cdot \mu_p \cdot Cox \cdot \frac{W}{L} \cdot [V_{OLED\_0} - V_{DATA}]^2 \end{aligned} \qquad (4)$$

**[0046]** As can be known by the above equation (4), the current is independent of the threshold voltage and ARVDD, therefore the affects of the non-uniformity in the threshold voltages and IR drop are substantially eliminated. Fig.3 shows a simulation result of compensation for the non-uniformity in the threshold voltages. For a traditional structure without any compensation, a maximum drifting of the current may be up to above 1.8 times when the threshold voltage drifts $\pm$0.6V, while in the structure of the present invention, the current fluctuation is smaller than 3%. Fig.4 shows a simulation result of compensation for IR Drop. For a traditional structure without any compensation, a maximum drifting of the current is up to 81% when the voltage drop of ARVDD drifts $\pm$0.5V, while in the structure of the present invention, the current fluctuation is smaller than 3.4%.

**[0047]** Meanwhile, the $I_{oled}$ current is correlated to the threshold voltage $V_{OLED\_0}$ of the OLED, therefore it may compensate the brightness loss due to the degradation of the OLED. When the OLED degrades, the $V_{OLED\_0}$ may increase gradually, and the efficiency of the light emitting may decrease, and it needs the first thin film transistor (drive transistor) 1 to provide larger current so as to maintain the same brightness. However, in an actual application, if Vdata<0 and Vdata<$V_{OLED\_0}$, |Vdata-$V_{OLED\_0}$| may increase as the $V_{OLED\_0}$ increases, which makes an increasing of the $I_{oled}$ so as to compensate the brightness loss of the OLED.

**[0048]** It can be known from an expansion of Taylor series, if the threshold voltage drifts, the drifted threshold voltage may be expressed as $V'_{OLED\_0} = V_{OLED\_0} + \Delta V_{OLED\_0}$, then a 1-order approximate expansion of the $I_{oled}$ with respect to

the $\Delta V_{OLED\_0}$ is as follows:

**[0049]**

$$I_{OLED} = \frac{1}{2} \cdot \mu_p \cdot Cox \cdot \frac{W}{L} \cdot [V_{OLED\_0} - V_{DATA}]^2 + \mu_p \cdot Cox \cdot \frac{W}{L} \cdot [V_{OLED\_0} - V_{DATA}] \cdot \Delta V_{OLED\_0} \quad (5)$$

**[0050]** The $I_{oled}$ is linear with the $\Delta V_{OLED\_0}$, and therefore a slope of the $I_{oled}$ curve may be adjusted by setting a ratio of width to length of the first thin film transistor 1 according to the measurement result of the OLED degradation, so that the Ioled curve complements the brightness-$\Delta V_{OLED\_0}$ curve to compensate the brightness loss due to the OLED degradation. Fig.5 shows a simulation result of compensation for the OLED degradation. For a traditional structure without any compensation, the current tends to reduce tardily when the threshold voltage of the OLED drifts 0~0.8V, which would expedite the drop of the brightness, while in the structure of the present invention, the current may increase linearly synchronously as the threshold voltage of the OLED increases, which may effectively compensate the brightness loss of the OLED. In addition, adjusting the ratio of width to length of the first thin film transistor 1 may control a speed and range for increasing the current.

## Claims

1. A pixel structure of an organic light emitting display device, comprising a first to a fifth thin film transistors, a capacitor and an organic light emitting display device, wherein a drain of the first thin film transistor is connected to a negative supply of a backboard via the organic light emitting display device, a source of the first thin film transistor is connected to a drain of the third thin film transistor, and a source of the third thin film transistor is connected to a positive power supply of the backboard; one end of the capacitor is connected between the first thin film transistor and third thin film transistor, and the other end of the capacitor is connected to a source of the second thin film transistor and a source of the fourth thin film transistor; a drain of the second thin film transistor is connected to a drain of the first thin film transistor and the organic light emitting display device; a drain of the fourth thin film transistor is connected to a drain of the fifth thin film transistor and a gate of the first thin film transistor, a source of the fifth thin film transistor is connected to a data line, and a gate of the fifth thin film transistor and a gate of the second thin film transistor are connected to a scan line; and a first control signal (EM) is provided to a gate of the third thin film transistor, and a second control signal (EMD) is provided to a gate of the fourth thin film transistor.

2. The pixel structure as claimed in claim 1, wherein during a pre-charging period, a line scanning voltage on the scan line and the first control signal are at a low level, and the second control signal is at a high level; the fourth thin film transistor is turned off, the first, second, third and fifth thin film transistors are turned on, and a data voltage is transferred to the gate of the first thin film transistor via the fifth thin film transistor.

3. The pixel structure as claimed in claim 2, wherein during a compensation period, the line scanning voltage on the scan line is at a low level, and the first control signal and the second control signal are at a high level; the third and fourth thin film transistors are turned off, the first, second and fifth thin film transistors are turned on, and a data voltage is transferred to the gate of the first thin film transistor via the fifth thin film transistor.

4. The pixel structure as claimed in claim 3, wherein during a light emitting period, the line scanning voltage on the scan line is at a high level, and the first control signal and the second control signal are at low level; the second and fifth thin film transistors are turned off, and the first, third and fourth thin film transistors are turned on.

5. The pixel structure as claimed in any one of claims 1-4, wherein during the pre-charging period and the compensation period, a signal on the data line (DATA) is an actual data voltage.

6. The pixel structure as claimed in any one of claims 1-5, wherein the first to fifth thin film transistors are low temperature polycrystalline silicon thin film transistors.

7. The pixel structure as claimed in any one of claims 1-6, wherein a ratio of width to length of the first thin film transistor is set so as to compensate a brightness loss due to the degradation of the organic light emitting display device.

8. A method for driving the pixel structure as claimed in claim 1, wherein the method comprises the following steps

performed in a refresh process of each frame of an image:

during a pre-charging period, the scan line and a first control signal (EM) are at a low level, a second control signal (EMD) is at a high level, so that the fourth thin film transistor is turned off, and the first, second, third and fifth thin film transistors are turned on;
during a compensation period, the scan line is at a low level, the first control signal (EM) and the second control signal (EMD) are at a high level, so that the third and fourth thin film transistors are turned off, and the first, second and fifth thin film transistors are turned on; and
during a light emitting period, the scan line is at a high level, the first control signal (EM) and the second control signal (EMD) are at a low level, so that the second and fifth thin film transistors are turned off, and the first, third and fourth thin film transistors are turned on.

**9.** The method as claimed in claim 8, wherein during the pre-charging period and the compensation period, a signal on the data line (DATA) is an actual data voltage.

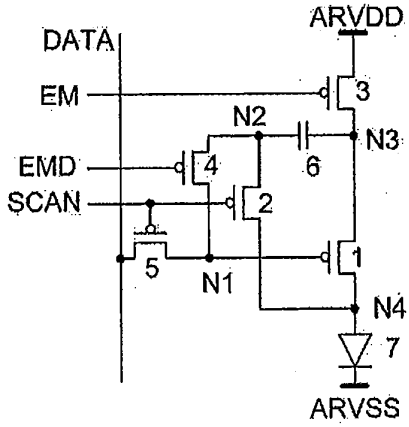
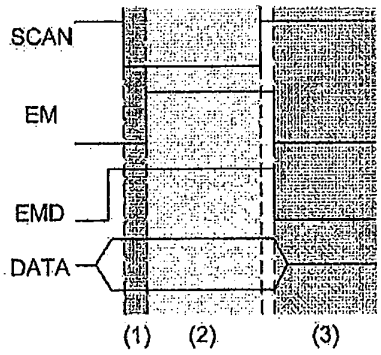



Fig. 1a

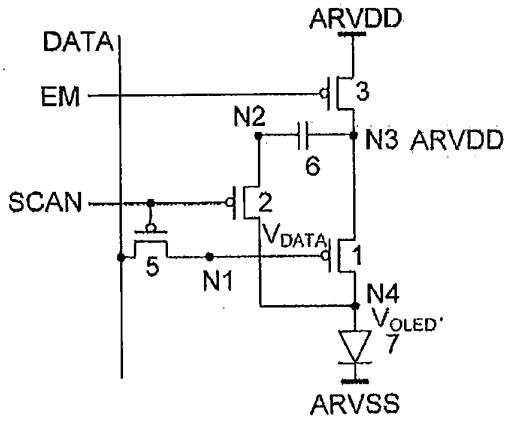



(1) Pre-charging

(2) Compensating

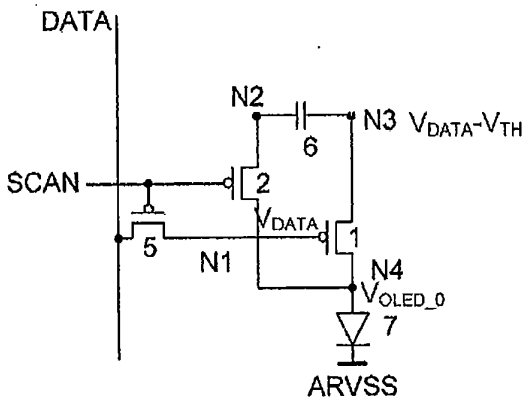
(3) Emitting Light

Fig. 1b



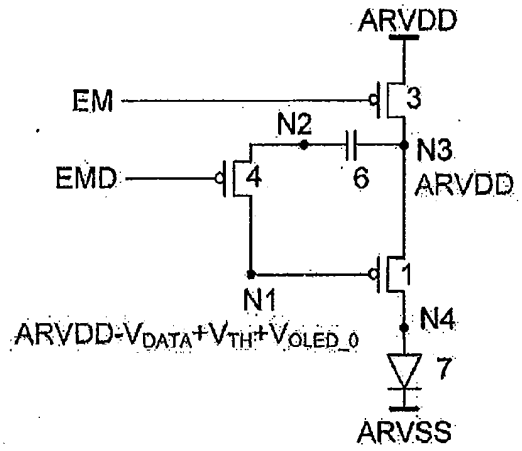

(a) Pre-charging

**Fig. 2a**




(b) Compensating

**Fig. 2b**




(c) EMITTING LIGHT

**Fig. 2c**

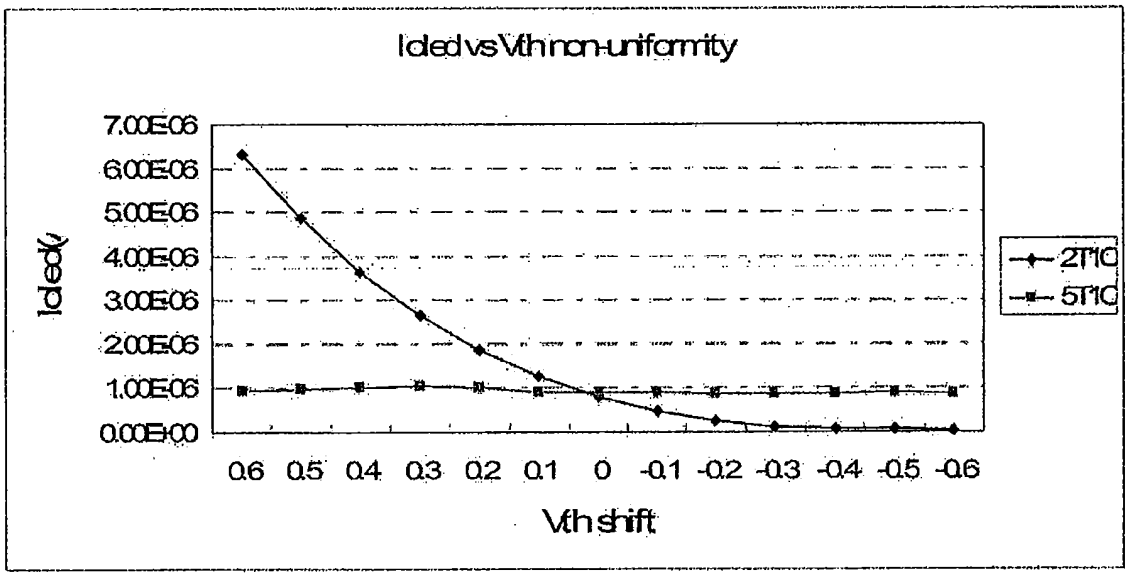



Fig. 3

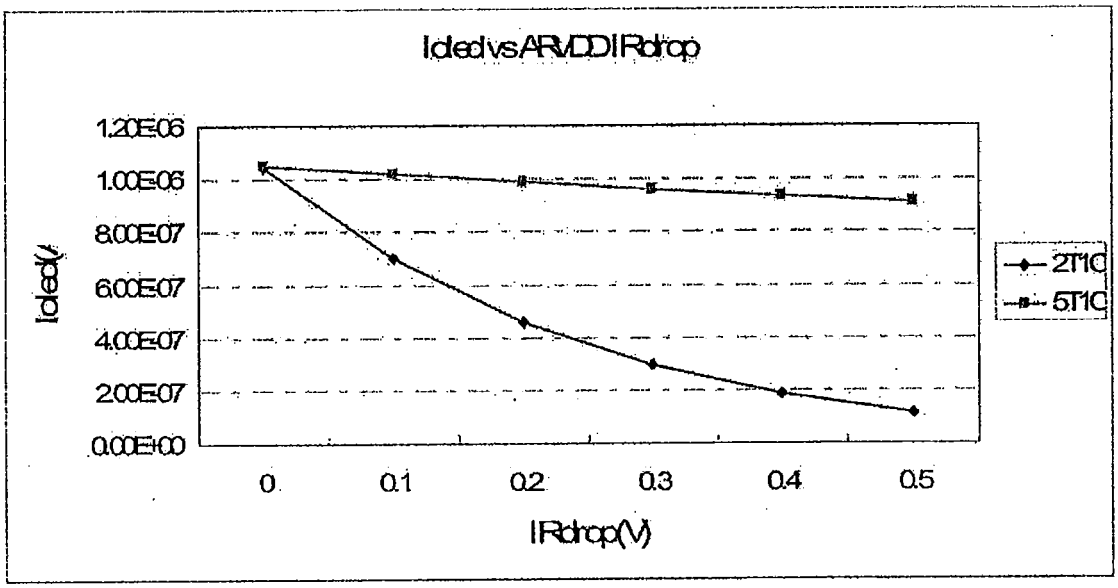

IledvsARVDDIRdrop
1.20E-06
1.00E-06
8.00E-07
6.00E-07
4.00E-07
2.00E-07
0.00E+00
0
0.1
0.2
0.3
0.4
0.5
IRdrop(V)
2T1C
5T1C

Fig. 4

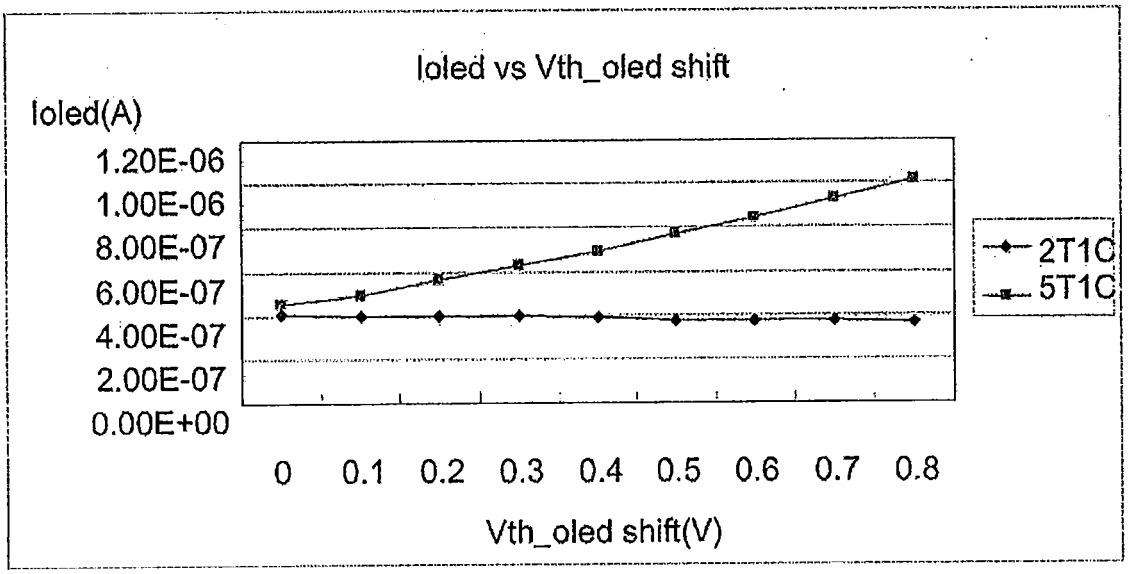

Ioled vs Vth_oled shift
Ioled(A)
1.20E-06
1.00E-06
8.00E-07
6.00E-07
4.00E-07
2.00E-07
0.00E+00
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
Vth_oled shift(V)
2T1C
5T1C

Fig. 5

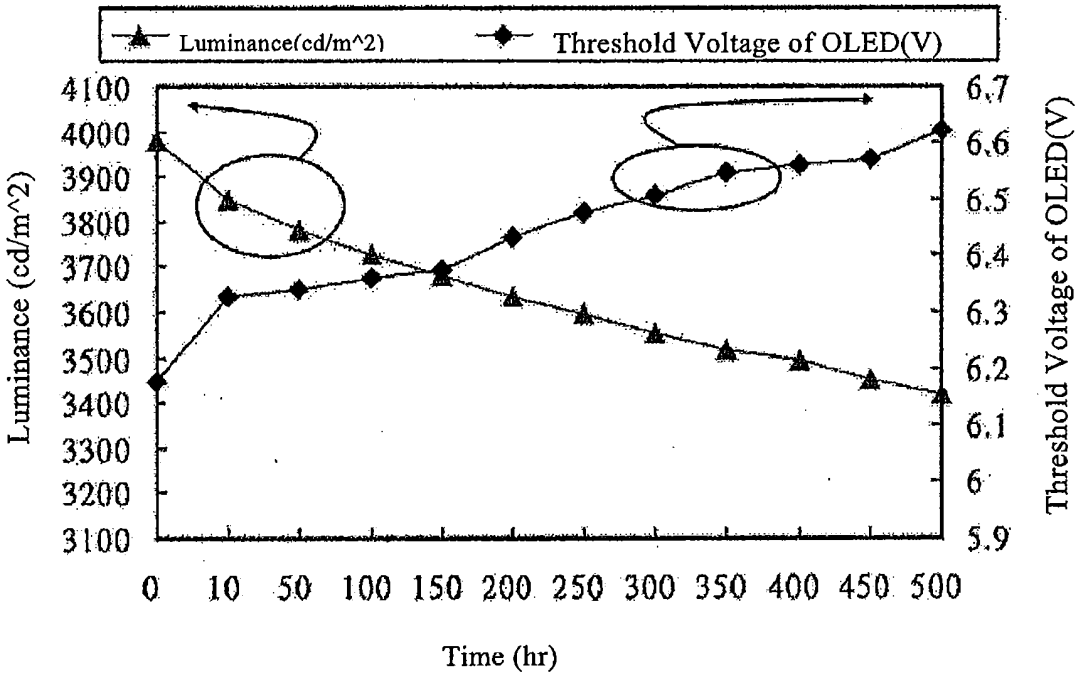



**Fig. 6a**

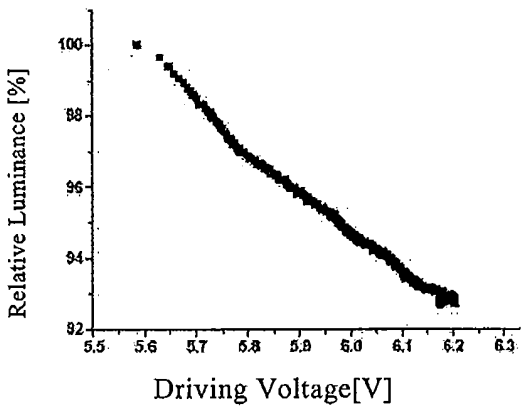



**Fig. 6b**

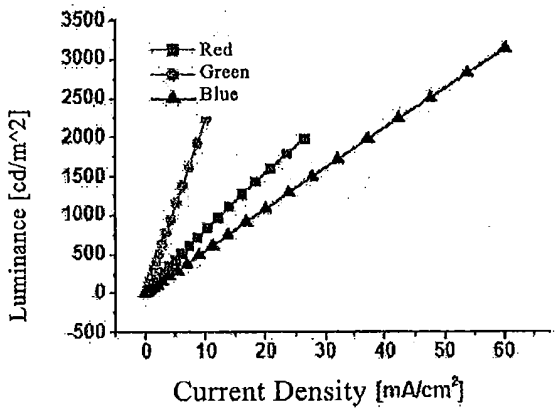



**Fig. 6c**

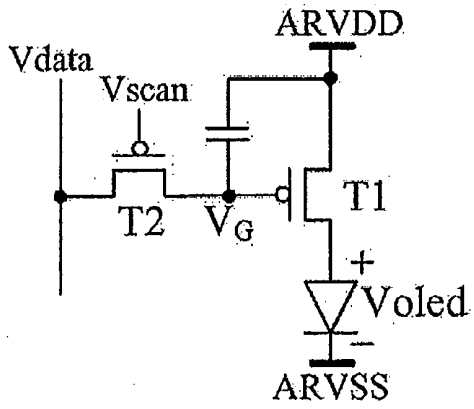



Fig. 7

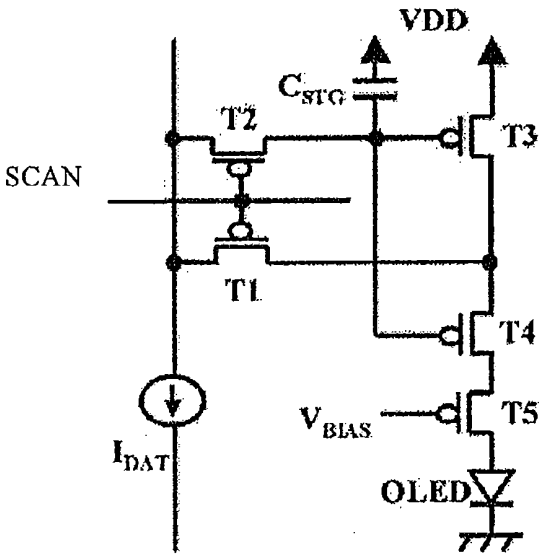



Fig. 8a

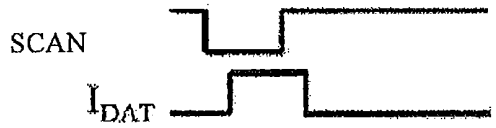



Fig. 8b

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2012/081304

**A. CLASSIFICATION OF SUBJECT MATTER**

G09G3/32 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G09G3/32, G09G3/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS, CNTXT, VEN: OLED, TFT, fifth, transistor, switch, capacitor, age, degrade, threshold, uniform

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| PX | CN102651195A (BOE Technology Group Co., Ltd.) 29 Aug. 2012 (29.08.2012) | |
| | claims 1-8, description, pages 3-5 and figures 1a-8 | 1-9 |
| X | CN1949342A (YOUDA PHOTOELECTRIC CO LTD) 18 Apr. 2007 (18.04.2007) | |
| | description, pages 4-6 and figures 4-8 | 1-9 |
| A | CN101859542A (YOUDA PHOTOELECTRIC CO LTD) 13 Oct. 2010 (13.10.2010) | |
| | the whole document | 1-9 |

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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"&"document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 16 Nov. 2012 (16.11.2012) | 06 Dec. 2012 (06.12.2012) |
| Name and mailing address of the ISA<br>State Intellectual Property Office of the P. R. China<br>No. 6, Xitucheng Road, Jimenqiao<br>Haidian District, Beijing 100088, China<br>Facsimile No. (86-10)62019451 | Authorized officer<br>LIU, Shikui<br>Telephone No. (86-10)62085842 |

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## INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2012/081304

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | CN101996579A (UNIV SOUTH CHINA TECH) 30 Mar. 2011 (30.03.2011) | |
| | the whole document | 1-9 |
| A | CN101996582A (UNIV SOUTH CHINA TECH) 30 Mar. 2011 (30.03.2011) | |
| | the whole document | 1-9 |
| A | US20100127955A1 (SAMSUNG MOBILE DISPLAY CO LTD) 27 May 2010 (27.05.2010) | |
| | the whole document | 1-9 |
| A | KR20110038393A (SAMSUNG MOBILE DISPLAY CO LTD) 14 Apr. 2011 (14.04.2011) | |
| | the whole document | 1-9 |

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**INTERNATIONAL SEARCH REPORT**
Information on patent family members

International application No.
PCT/CN2012/081304

| Patent Documents referred in the Report | Publication Date | Patent Family | Publication Date |
|---|---|---|---|
| CN102651195A | 29.08.2012 | NONE | |
| CN1949342A | 18.04.2007 | CN100435199C | 19.11.2008 |
| CN101859542A | 13.10.2010 | CN101859542B | 23.05.2012 |
| CN101996579A | 30.03.2011 | NONE | |
| CN101996582A | 30.03.2011 | NONE | |
| US20100127955A1 | 27.05.2010 | KR20100059317A | 04.06.2010 |
| | | KR101008438B1 | 14.01.2011 |
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| | | KR101030002B1 | 20.04.2011 |

Form PCT/ISA /210 (patent family annex) (July 2009)

## REFERENCES CITED IN THE DESCRIPTION

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### Non-patent literature cited in the description


- Current programming pixel circuit and data-driver design for active-matrix organic light-emitting diodes. *Journal of the Society for Information Display,* 2004, vol. 12, 227 **[0016]**

| | | | |
|---|---|---|---|
| 专利名称(译) | OLED像素结构和驱动方法 | | |
| 公开(公告)号 | EP2608192A1 | 公开(公告)日 | 2013-06-26 |
| 申请号 | EP2012795318 | 申请日 | 2012-09-12 |
| [标]申请(专利权)人(译) | 京东方科技集团股份有限公司 | | |
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| 当前申请(专利权)人(译) | 京东方科技集团有限公司. | | |
| [标]发明人 | WU ZHONGYUAN | | |
| 发明人 | WU, ZHONGYUAN | | |
| IPC分类号 | G09G3/32 | | |
| CPC分类号 | G09G3/02 G09G3/3233 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2300/0866 G09G2320/0223 G09G2320/043 | | |
| 优先权 | 201110271117.X 2011-09-14 CN | | |
| 其他公开文献 | EP2608192A4 | | |
| 外部链接 | Espacenet | | |


摘要(译)

本发明提供一种有机发光显示装置的像素结构及其驱动方法。像素结构包括第一至第五薄膜晶体管，电容器和OLED器件，其中设置第一薄膜晶体管的宽度与长度的无线电，以补偿由于有机发光显示器的劣化导致的亮度损失。设备。在每帧图像的刷新过程中对像素结构执行以下步骤：在预充电时段期间，扫描线和第一控制信号（EM）处于低电平，第二控制信号（EMD）是在高层;在补偿期间，扫描线处于低电平，第一控制信号（EM）和第二控制信号（EMD）处于高电平;并且在发光时段期间，扫描线处于高电平，第一控制信号（EM）和第二控制信号（EMD）处于低电平。


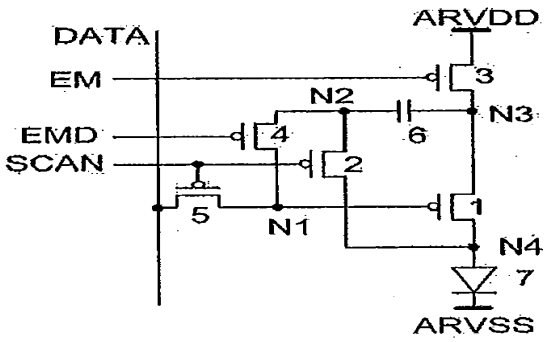


Fig. 1a