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(54) **Thin film transistor array substrate, organic light-emitting display device including the same, and method of manufacturing the organic light-emitting display device**

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Substrat de réseau de transistors à couche mince, dispositif d’affichage électroluminescent organique comprenant celui-ci et procédé de fabrication du dispositif d’affichage électroluminescent organique

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Description

BACKGROUND

1. Field

[0001] The present invention relates to a thin film transistor (TFT) array substrate, an organic light-emitting display device including the same, and a method of manufacturing the organic light-emitting display device.

2. Description of the Related Art

[0002] Flat panel display devices such as organic light-emitting display devices and liquid crystal display (LCD) devices typically include a thin film transistor (TFT), a capacitor, and a wiring for connecting the TFT and the capacitor.

[0003] In the formation of a flat panel display device a TFT, a capacitor, and a wiring are finely patterned on a substrate. In order to form such a fine pattern on the substrate, photolithography is often used to transfer a pattern by using a mask.

[0004] Photolithography involves uniformly applying a photoresist to a substrate on which a pattern is to be formed, exposing the photoresist by using exposure equipment such as a stepper, developing the photoresist if the photoresist is a positive photoresist, etching the pattern formed on the substrate by using a remaining part of the photoresist, and removing an unnecessary remaining part of the photoresist after the pattern is formed.

[0005] A mask including a desired pattern may be prepared in advance when photolithography is used, and the cost for preparing the mask increases the cost for manufacturing a flat panel display device. Also, when complicated steps are performed, the manufacturing process of the flat display device may become complex and the manufacturing time may increase, and thus, the general manufacturing costs of the flat display device may increase.

[0006] The present invention sets out to provide a thin film transistor (TFT) array substrate and an organic light-emitting display device including the TFT array substrate that may be manufactured by a method that uses a simple manufacturing process. The light emitting display device may have excellent signal transmission characteristics.

[0007] US 2002/104995 discloses a thin film transistor array substrate having a TFT disposed on the substrate. A first insulating layer is disposed between the active layer of the TFT and a gate electrode. A second insulating layer is formed between the gate electrode and the source and drain electrodes. A capacitor includes a lower electrode disposed on the second insulating layer, in the same layer as the source and drain electrodes. The capacitor further includes an upper electrode disposed on a third insulating layer which is disposed over the lower electrode and the source and drain electrodes. A pixel electrode is disposed on the third insulating layer, in the same layer as the upper electrode.

[0008] US 2003/0141811 discloses a thin film transistor array substrate having a TFT disposed on the substrate. A first insulating layer is disposed between the active layer of the TFT and a gate electrode. A second insulating layer is formed between the gate electrode and the source and drain electrodes. The gate electrode and a lower electrode of a capacitor are both disposed directly on the first insulating layer. A third insulating layer is disposed on the second insulating layer and an upper electrode of the capacitor is disposed on the third insulating layer. Thus both the second insulating layer and the third insulating layer are disposed between the lower and upper electrodes of the capacitor. A pixel electrode is disposed on the third insulating layer, in the same layer as the upper electrode.

[0009] WO 03/071511 discloses a thin film transistor array substrate having a TFT disposed on the substrate. A first insulating layer is disposed between the active layer of the TFT and a gate electrode. A second insulating layer is formed between the gate electrode and the source and drain electrodes. The gate electrode and a lower electrode of a capacitor are both disposed directly on the first insulating layer. A third insulating layer is disposed over the source and drain electrodes and an upper electrode of the capacitor is disposed on the third insulating layer. A pixel electrode is disposed on the third insulating layer, in the same layer as the upper electrode.

SUMMARY

[0010] According to a first aspect of the invention, there is provided a thin film transistor (TFT) array substrate according to claim 1.

[0011] The first insulating layer may be commonly disposed over the active layer and under the lower electrode.

[0012] A thickness of the third insulating layer may be less than a thickness of the second insulating layer.

[0013] A thickness of the third insulating layer may be equal to or greater than about 500 Å and equal to or less than about 2000 Å.

[0014] A dielectric constant of the third insulating layer may be higher than a dielectric constant of the first insulating layer.

[0015] The third insulating layer may include at least one of SiN_x, SiO_2, ZrO_2, TiO_2, Ta_2O_5, and Al_2O_3.

[0016] The first insulating layer, the second insulating layer, and the third insulating layer may be sequentially disposed between the pixel electrode and the substrate. Refractive indices of adjacent insulating layers of the first through third insulating layers may be different from each other.

[0017] The pixel electrode may include a transparent conductive oxide (TCO).

[0018] The TCO may include at least one of indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO),

indium oxide (In_2O_3), indium gallium oxide (IGO), and aluminum zinc oxide (AZO).

[0019] The pixel electrode may further include a semi-transmissive metal layer.

[0020] The semi-transmissive metal layer may be disposed on a layer including the transparent conductive oxide.

[0021] The semi-transmissive metal layer may include at least one of silver (Ag), an Ag alloy, aluminum (Al), and an Al alloy.

[0022] The TFT array substrate may further include a protective layer disposed on the semi-transmissive metal layer.

[0023] The protective layer may include a TCO.

[0024] A portion of one of the source electrode and the drain electrode that is connected to the pixel electrode may be disposed over the pixel electrode.

[0025] The source electrode and the drain electrode may include a material having an etching rate different from an etching rate of the pixel electrode and the upper electrode.

[0026] The TFT array substrate may further include a pad electrode formed of a same material as the source electrode and the drain electrode.

[0027] The pad electrode may be disposed on a same layer as the source electrode and the drain electrode.

[0028] There is also provided an organic light-emitting display device, including the TFT array substrate, an organic light-emitting layer disposed on the pixel electrode, and a counter electrode disposed on the organic light-emitting layer.

[0029] The counter electrode may be a reflective electrode that reflects light emitted by the organic light-emitting layer.

[0030] According to a second aspect of the invention, there is provided a method of manufacturing a TFT array substrate according to claim 15.

[0031] The method may further include doping the source region and the drain region with ion impurities after forming the gate electrode using the second mask process.

[0032] The fourth mask process may include a first etching process to etch the third insulating layer, and a second etching process to etch the second conductive layer.

[0033] The third conductive layer may include a material having an etching rate different from an etching rate of a material of the second conductive layer.

[0034] The method may further include forming a pad electrode including the same material as the source electrode and the drain electrode using the fifth mask process.

[0035] The second conductive layer may be formed by sequentially stacking a transparent conductive layer and a semi-transmissive conductive layer.

[0036] The method may further include forming a protective layer on the semi-transmissive conductive layer.

[0037] The third insulating layer may be formed to have a thickness less than a thickness of the second insulating layer.

[0038] The third insulating layer may be formed of a material having a dielectric constant higher than a dielectric constant of the first insulating layer.

[0039] At least some of the above and other features of the invention are set out in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0040] The above and other features will become more apparent to those of ordinary skill in the art upon referring to embodiments of the invention that are described below with reference to the attached drawings, in which:

FIG. 1 illustrates a cross-sectional view depicting an organic light-emitting display device according to an embodiment of the invention;

FIGS. 2A and 2B illustrate cross-sectional views depicting a first mask process of a method of manufacturing organic light-emitting display device;

FIGS. 3A and 3B illustrate cross-sectional views depicting a second mask process of the method of manufacturing the organic light-emitting display device;

FIGS. 4A and 4B illustrate cross-sectional views depicting a third mask process of the method of manufacturing the organic light-emitting display device;

FIGS. 5A and 5B illustrate cross-sectional views depicting a fourth mask process of the method of manufacturing the organic light-emitting display device;

FIGS. 6A and 6B illustrate cross-sectional views depicting a fifth mask process of the method of manufacturing the organic light-emitting display device;

FIGS. 7A and 7B illustrate cross-sectional views depicting a sixth mask process of the method of manufacturing the organic light-emitting display device; and

FIG. 8 illustrates a cross-sectional view depicting an organic light-emitting display device according to another embodiment of the invention.

DETAILED DESCRIPTION

[0041] Example embodiments of the invention will now be described more fully hereinafter with reference to the accompanying drawings; however, the invention may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough, and will convey the scope to those skilled in the art.

[0042] In the drawing figures, the dimensions of layers and regions may be exaggerated for clarity of illustration. It will also be understood that when a layer or element is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Further, it will be understood that when a layer is referred to as being "under"

another layer, it can be directly under, and one or more intervening layers may also be present. In addition, it will also be understood that when a layer is referred to as being "between" two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present. Like reference numerals refer to like elements throughout.

[0043] FIG. 1 illustrates a cross-sectional view depicting an organic light-emitting display device 1 according to an embodiment of the invention.

[0044] Referring to FIG. 1, a substrate 10 of the organic light-emitting display device 1 includes a pixel region PXL1 in which at least one organic light-emitting layer 120 is disposed, a thin film transistor (TFT) region TFT1 in which at least one TFT is disposed, a capacitor region CAP1 in which at least one capacitor is disposed, and a pad region PAD1 in which a pad electrode 418 is disposed.

[0045] An active layer 212 of the TFT is disposed on the substrate 10 and a buffer layer 11 is disposed in the transistor region TFT1.

[0046] The substrate 10 may be a transparent substrate such as a glass substrate or a plastic substrate including polyethylene terephthalate (PET), polyethylene naphthalate (PEN), polyimide, or the like.

[0047] In order to planarize the substrate 10 and prevent impurity elements from penetrating into the substrate 10, the buffer layer 11 is disposed on the substrate 10. The buffer layer 11 may have a single-layer structure or a multiple-layer structure including silicon nitride and/or silicon oxide.

[0048] The active layer 212 is disposed on the buffer layer 11. The active layer 212 may be formed of a semiconductor including amorphous silicon or crystalline silicon, and includes a channel region 212c, and a source region 212a and a drain region 212b formed by doping portions around the channel region 212c with ion impurities.

[0049] A gate electrode 214 is disposed on the active layer 212 to correspond to the channel region 212c of the active layer 212. A first insulating layer 13, which may be a gate insulating film, is disposed between the gate electrode 214 and the active layer 212. The gate electrode 214 may have a single-layer structure or a multi-layer structure including at least one metal selected from aluminum (Al), platinum (Pt), palladium (Pd), silver (Ag), magnesium (Mg), gold (Au), nickel (Ni), neodymium (Nd), iridium (Ir), chromium (Cr), lithium (Li), calcium (Ca), molybdenum (Mo), titanium (Ti), tungsten (W), and copper (Cu).

[0050] A source electrode 218a and a drain electrode 218b are disposed on the gate electrode 214 to be respectively connected to the source region 212a and the drain region 212b of the active layer 212. A second insulating layer 15, which may be an interlayer insulating film, is disposed between the source electrode 218a and the drain electrode 218b and the active layer 212. The source electrode 218a and the drain electrode 218b may have a single-layer structure or a multi-layer structure including at least one metal selected from Al, Pt, Pd, Ag, Mg, Au, Ni, Nd, Ir, Cr, Li, Ca, Mo, Ti, W, and Cu.

[0051] A fourth insulating layer 19 is disposed on the second insulating layer 15 to cover the source electrode 218a and the drain electrode 218b.

[0052] The first insulating layer 13 may be used as a gate insulating film. The second insulating layer 15 may be used as an interlayer insulating film in the TFT region TFT1. Each of the first insulating layer 13 and the second insulating layer 15 may be an inorganic insulating film. The inorganic insulating film may include SiO_2, SiN_x, SiON, Al_2O_3, TiO_2, Ta_2O_5, HfO_2, ZrO_2, barium strontium titanate (BST), lead zirconium titanate (PZT), or the like.

[0053] The first insulating layer 13, which may be used as a gate insulating film, is not used as a dielectric film of the capacitor, as will be explained below. Accordingly, the first insulating layer 13 may be designed appropriately according to characteristics of a gate insulating film of the TFT without considering dielectric constant-related characteristics of the capacitor. For example, if silicon nitride (SiN_x), which is often used as a dielectric film of a capacitor in order to increase an electrostatic capacitance, were to be also used as a gate insulating film of the TFT, leakage current may occur in the TFT. However, according to the present embodiment, a dielectric film of the capacitor and a gate insulating film of the TFT may be separately formed, as shown in FIG. 1. The dielectric film and the gate insulating film may be selected in consideration of only the characteristics of the capacitor and the TFT, respectively.

[0054] In the pixel region PXL1, a pixel electrode 117 formed of the same material as an upper electrode 317 of the capacitor, which will be explained below, is disposed on the substrate 10, the buffer layer 11, the first insulating layer 13, and the second insulating layer 15.

[0055] A third insulating layer 116 is disposed between the pixel electrode 117 and the second insulating layer 15. The buffer layer 11, the first insulating layer 13, the second insulating layer 15, and the third insulating layer 116 are sequentially disposed, from the substrate 10 toward the pixel electrode 117, between the pixel electrode 117 and the substrate 10.

[0056] The insulating layers disposed between the substrate 10 and the pixel electrode 117, that is, the buffer layer 11, the first insulating layer 13, the second insulating layer 15, and the third insulating layer 116, are formed to have different refractive indices. Insulating layers having different refractive indices may be alternately disposed to function as a distributed Bragg reflector (DBR). Accordingly, the efficient use of light emitted by a light-emitting layer may be improved.

[0057] Although the buffer layer 11, the first insulating layer 13, the second insulating layer 15, and the third insulating layer 116 may be formed as individual single layers, as shown in FIG. 1, it is also possible for the buffer layer 11, the first insulating layer 13, the second insulating layer 15, and the third insulating layer 116 to have multi-

layer structures.

[0058] The pixel electrode 117 is directly disposed on the third insulating layer 116. The third insulating layer 116 and the pixel electrode 117 are patterned by using the same mask in the same mask process. Accordingly, the third insulating layer 116 and the pixel electrode 117 share the same etched lateral surface. For example, lateral surfaces of the third insulating layer 116 align with lateral surfaces of the pixel electrode 117.

[0059] The pixel electrode 117 may be formed of a transparent conductive material so that light may be emitted toward the pixel electrode 117. The transparent conductive material may include at least one of indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium oxide (In_2O_3), indium gallium oxide (IGO), and aluminum zinc oxide (AZO).

[0060] An organic light-emitting layer 120 is formed on the pixel electrode 117, and light emitted by the organic light-emitting layer 120 may be emitted through the pixel electrode 117 formed of a transparent conductive material toward the substrate 10.

[0061] The fourth insulating layer 19 is formed around the pixel electrode 117. An opening C3 through which the pixel electrode 117 is exposed is formed in the fourth insulating layer 19. The organic light-emitting layer 120 is disposed in the opening C3.

[0062] The organic light-emitting layer 120 may be formed of a low molecular weight organic material or a high molecular weight organic material. If the organic light-emitting layer 120 is formed of a low molecular weight organic material, a hole transport layer (HTL), a hole injection layer (HIL), an electron transport layer (ETL), an electron injection layer (EIL), and so on, may be stacked around the organic light-emitting layer 120. Other various layers may also be stacked. Examples of the low molecular weight organic material may include copper phthalocyanine (CuPc), N,N'-di(naphthalene-1-yl)-N,N'-diphenyl-benzidine (NPB), and tris-8-hydroxyquinoline aluminum (Alq3). If the organic light-emitting layer 120 is formed of a high molecular weight organic material, an HTL may be provided in addition to the organic light-emitting layer 120. The HTL may be formed of poly-(3,4)-ethylene-dihydroxy thiophene (PEDOT), polyaniline (APNI), or the like. Examples of the high molecular weight organic material may include a poly-phenylenevinylene (PPV)-based high molecular weight organic material and a polyfluorene-based high molecular weight organic material. Also, an inorganic material may be further disposed between the organic light-emitting layer 120, the pixel electrode 117, and a counter electrode 121.

[0063] The counter electrode 121 is disposed as a common electrode on the organic light-emitting layer 120. In the organic light-emitting display device 1 of FIG. 1, the pixel electrode 117 may operate as an anode and the counter electrode 121 operate as a cathode. It is also possible for the pixel electrode 117 to operate as a cathode and the counter electrode 121 to operate as an anode.

[0064] The counter electrode 121 may be a reflective electrode including a reflective material. The counter electrode 121 may include at least one of Al, Mg, Li, Ca, LiF/Ca, and LiF/Al. If the counter electrode 121 is a reflective electrode, light emitted by the organic light-emitting layer 120 may be reflected by the counter electrode 121 and may be transmitted through the pixel electrode 117 formed of a transparent conductive material toward the substrate 10.

[0065] The fourth insulating layer 19 covering the portions around the pixel electrode 117 serves to function as a pixel defining film between the pixel electrode 117 and the counter electrode 121.

[0066] The fourth insulating layer 19 may be an organic insulating film. The fourth insulating layer 19 may include a commercial polymer such as polymethyl methacrylate (PMMA) or polystyrene (PS), a polymer derivative having a phenol group, an acryl-based polymer, an imide-based polymer, an acryl ether-based polymer, an amide-based polymer, a fluorine-based polymer, a p-xylene-based polymer, a vinyl alcohol-based polymer, a blend thereof, or the like.

[0067] The fourth insulating layer 19 covers the source electrode 218a and the drain electrode 218b of the TFT. The source electrode 218a is electrically connected to the pixel electrode 117. Although the source electrode 128a is shown as being connected to the pixel electrode 117 in FIG. 1, it is also possible for the pixel electrode 117 to be electrically connected to the drain electrode 218b.

[0068] A portion of one of the source electrode 218a connected to the pixel electrode 117 is disposed over the pixel electrode 117. As described below, the source electrode 218a and the drain electrode 218b are patterned after the pixel electrode 117 has been patterned. Accordingly, the source electrode 218a and the drain electrode 218b may be formed of a material having an etching rate different from that of the pixel electrode 117.

[0069] In the capacitor region CAP1, a lower electrode 314 of the capacitor, which may be formed of the same material as the gate electrode 214 of the TFT, the upper electrode 317 of the capacitor, which may be formed of the same material as the pixel electrode 117, and a third insulating layer 316 directly disposed between the lower electrode 314 and the upper electrode 317 are disposed on the substrate 10 and the buffer layer 11.

[0070] The second insulating layer 15 is disposed between the gate electrode 214 of the TFT and the source electrode 218a and the drain electrode 218b. The second insulating layer 15 is not disposed between the upper electrode 317 and the lower electrode 314 of the capacitor. Accordingly, the second insulating layer 15 does not mainly function as a dielectric film of the capacitor. For example, as shown in FIG. 1, the second insulating layer 15 may slightly overlap with an outer portion of the lower electrode 314. As described below, the overlapped outer portion may be left when an opening C2 (see FIG. 4B),

through which the lower electrode 314 is exposed, is formed by patterning the second insulating layer 15.

[0071] If the lower electrode 314 of the capacitor were to be entirely exposed when the second insulating layer 15 is patterned, a leakage current may occur between the lower electrode 314 and the upper electrode 317 formed on the third insulating layer 316. Accordingly, the second insulating layer 15 may partially cover the outer portion of the lower electrode 314 without entirely exposing the lower electrode 314. A leakage current may be prevented from occurring between the upper electrode 317 and the lower electrode 314.

[0072] The second insulating layer 15, which may function as an interlayer insulating film of the TFT, may be designed to have a thickness equal to or greater than a predetermined thickness in consideration of characteristics of the TFT. Since an electrostatic capacitance of a capacitor typically decreases as a thickness of a dielectric film increases, if the dielectric film were to have the same thickness as that of the interlayer insulating film, the electrostatic capacitance may decrease.

[0073] The second insulating layer 15 shown in FIG. 1 is not used as a dielectric film of the capacitor. The third insulating layer 316, which may be used as a dielectric film, may be thinner than the second insulating layer 15. Accordingly, an electrostatic capacitance may be prevented from being reduced. An appropriate electrostatic capacitance may be maintained when a thickness of the third insulating layer 316 is equal to or greater than about 500 Å and equal to or less than about 2000 Å.

[0074] The third insulating layer 316, which may be used as a dielectric film, may be formed of an insulating material having a high dielectric constant. As described above, the third insulating layer 316 may be separately formed from the first insulating layer 13 which is a gate insulating film. An electrostatic capacitance may increase when the third insulating layer 316 is formed of a material having a dielectric constant higher than that of the first insulating layer 13. An electrostatic capacitance may thereby increase without increasing an area of the capacitor. Accordingly, an area of the pixel electrode 117 may be relatively increased, and thus, an aperture ratio of the organic light-emitting display device 1 may be increased.

[0075] The third insulating layer 316 may be an inorganic insulating film. For example, the third insulating layer 316 may include at least one of SiO_2, SiN_x, SiON, Al_2O_3, TiO_2, Ta_2O_5, HfO_2, ZrO_2, BST, and PZT.

[0076] Also, as described below, the upper electrode 317 and the third insulating layer 316 are patterned in the same mask process. The upper electrode 317 and the third insulating layer 316 have the same etched surface. For example, lateral surfaces of the upper electrode 317 line up with lateral surfaces of the third insulating layer 316.

[0077] The fourth insulating layer 19 is disposed on the upper electrode 317. The fourth insulating layer 19 may be an organic insulating film. The fourth insulating layer 19 may include an organic insulating material having a low dielectric constant and is disposed between the counter electrode 121 and the upper electrode 317. Accordingly, a parasitic capacitance, which may be formed between the counter electrode 121 and the upper electrode 317, may be reduced, and thus, signal interference due to the parasitic capacitance may be prevented.

[0078] The pad region PAD1 in which the pad electrode 418, which is a connection terminal of an external drive, is located is disposed in an outer region of the organic light-emitting display device 1.

[0079] In FIG. 1, the pad electrode 418 may be formed of the same material as the source electrode 218a and the drain electrode 218b. Also, the pad electrode 418 is disposed on the same layer as the source electrode 218a and the drain electrode 218b. The pad electrode 418 is directly disposed on the second insulating layer 15.

[0080] The pad electrode 418 is formed after the gate electrode 214, the pixel electrode 117, and the upper electrode 317 are formed. Accordingly, a material for forming the gate electrode 214, the pixel electrode 117, or the upper electrode 317 is not located over the pad electrode 418. The reliability of the pad electrode 418 may be prevented from being reduced in a process of locating a material for forming the gate electrode 214, the pixel electrode 117, or the upper electrode 317 on the pad electrode 418 or removing such material from the pad electrode 418.

[0081] Although not shown in FIG. 1, the organic light-emitting display device 1 may further include an encapsulation member (not shown) for encapsulating a display region including the pixel region PXL1, the capacitor region CAP1, and the TFT region TFT1. The encapsulation member may be formed as a substrate including a glass material, a metal film, or an encapsulation thin film by alternately disposing an organic insulating film and an inorganic insulating film.

[0082] A method of manufacturing the organic light-emitting display device 1 according to an embodiment of the invention will be explained with reference to FIGS. 2A through 7B.

[0083] FIGS. 2A and 2B illustrate cross-sectional views depicting a first mask process of the method of manufacturing the organic light-emitting display device 1.

[0084] Referring to FIG. 2A, the buffer layer 11 and the semiconductor layer 12 are sequentially formed on the substrate 10.

[0085] The buffer layer 11 and the semiconductor layer 12 may be deposited by using any of various deposition methods such as plasma enhanced chemical vapor deposition (PECVD), atmospheric pressure CVD (APCVD), and low pressure CVD (LPCVD).

[0086] The semiconductor layer 12 may be formed of amorphous silicon or crystalline silicon. The crystalline silicon may be formed by crystallizing the amorphous silicon. Examples of a method of crystallizing amorphous silicon may include rapid thermal annealing (RTA), solid phase crystallization (SPC), excimer laser annealing

(ELA), metal induced crystallization (MIC), metal induced lateral crystallization (MILC), or sequential lateral solidification (SLS).

[0087] A first photoresist PR1 is applied to the semiconductor layer 12, and the first mask process is performed by using a first photomask M1 including a light-blocking portion M11 and a light-transmitting portion M12. Although not shown, after exposure is performed by using an exposure device (not shown), a series of steps such as developing, etching, and stripping or ashing may be performed.

[0088] FIG. 2B illustrates a cross-sectional view depicting a resultant structure of the first mask process.

[0089] Referring to FIG. 2B, a portion of the semiconductor layer 12 corresponding to the light-blocking portion M11 of the first photomask M1 is patterned to form the channel region 212c of the active layer 212 of the TFT.

[0090] FIGS. 3A and 3B illustrate cross-sectional views depicting a second mask process of the method of manufacturing the organic light-emitting display device 1.

[0091] Referring to FIG. 3A, the first insulating layer 13 and the first conductive layer 14 are sequentially formed on the resultant structure of the first mask process of FIG. 2B.

[0092] The first insulating layer 13 may be an inorganic insulating film formed of at least one of SiO_2, SiN_x, SiON, Al_2O_3, TiO_2, Ta_2O_5, HfO_2, ZrO_2, BST, and PZT. The first conductive layer 14 may have a single-layer structure or a multi-layer structure formed of at least one metal selected from Al, Pt, Pd, Ag, Mg, Au, Ni, Nd, Ir, Cr, Li, Ca, Mo, Ti, W, and Cu.

[0093] A second photoresist PR2 is applied to the first conductive layer 14. The second mask process is performed by using a second photomask M2 including light-blocking portions M21T and M21C and a light-transmitting portion M22.

[0094] FIG. 3B illustrates a cross-sectional view depicting a resultant structure of the second mask process.

[0095] Referring to FIG. 3B, a portion of the first conductive layer 14 corresponding to the light-blocking portion M21T of the second mask M2 is patterned to form the gate electrode 214 of the TFT. A portion of the first conductive layer 14 corresponding to the light-blocking portion M21C is patterned to form the lower electrode 314 of the capacitor.

[0096] While the portion of the first insulating layer 13 that is disposed between the gate electrode 214 and the active layer 212 of the TFT may function as a gate insulating film, the portion of the first insulating layer 13 that is disposed under the lower electrode 314 does not function as a dielectric film of the capacitor. Accordingly, a material of the first insulating layer 13 may be selected in consideration of only characteristics of the TFT without considering characteristics of the capacitor.

[0097] The resultant structure of the second mask process is doped with ion impurities. The ion impurities may be B ion impurities or P ion impurities. The resultant structure is doped by using the active layer 212 of the TFT as a target and providing a doping amount of 1×10^{15} atoms/cm^2 or more.

[0098] The active layer 212 includes the source and drain regions 212a and 212b and the channel region 212c disposed between the source and drain regions 212a and 212b. The source and drain regions 212a and 212b are doped with ion impurities by using the gate electrode 214 as a self-aligned mask.

[0099] Meanwhile, although not shown in FIGS. 3A and 3B, a wiring such as a scan line connected to the gate electrode 214 may also be formed by patterning the first conductive layer 14 in the second mask process.

[0100] FIGS. 4A and 4B illustrate cross-sectional views depicting a third mask process of the method of manufacturing the organic light-emitting display device 1.

[0101] Referring to FIG. 4A, the second insulating layer 15 is formed on the resultant structure of the second mask process of FIG. 3B.

[0102] The second insulating layer 15 may be an inorganic insulating film formed of at least one of SiO_2, SiN_x, SiON, Al_2O_3, TiO_2, Ta_2O_5, HfO_2, ZrO_2, BST, and PZT. For example, the second insulating layer 15 may be formed of a material having a refractive index different from that of a material of the first insulating layer 13.

[0103] A third photoresist PR3 is applied to the second insulating layer 15. The third mask process is performed by using a third photomask M3 including a light-blocking portion M31 and light-transmitting portions M32T and M32C.

[0104] FIG. 4B illustrates a cross-sectional view depicting a resultant structure of the third mask process.

[0105] Referring to FIG. 4B, a portion of the second insulating layer 15 corresponding to the light-transmitting portion M32T of the third photomask M3 is formed to include an opening C1 through which the source region 212a and the drain region 212b of the active layer 212 are partially exposed, and a portion of the second insulating layer 15 corresponding to the light-transmitting portion M32C is patterned to form the opening C2 through which the lower electrode 314 of the capacitor is exposed.

[0106] FIGS. 5A and 5B illustrate cross-sectional views depicting a fourth mask process of the method of manufacturing the organic light-emitting display device 1.

[0107] Referring to FIG. 5A, a third insulating layer 16 and a second conductive layer 17 are sequentially formed on the resultant structure of the third mask process of FIG. 4B. The third insulating layer 16 and the second conductive layer 17 are sequentially stacked on the upper electrode 314 of the capacitor and the second insulating layer 15.

[0108] The third insulating layer 16 may be an inorganic insulating film formed of a material selected from the group consisting of SiO_2, SiN_x, SiON, Al_2O_3, TiO_2, Ta_2O_5, HfO_2, ZrO_2, BST, and PZT. The third insulating layer 16 may be formed of a material having a refractive index different from refractive indices of the first insulating layer 13 and the second insulating layer 15.

[0109] The second conductive layer 17 may be formed of a transparent conductive oxide. For example, the second conductive layer 17 may be formed of a material selected from the group consisting of ITO, IZO, ZnO, In_2O_3, IGO, and AZO.

[0110] A fourth photoresist PR4 is applied to the second conductive layer 17. The fourth mask process is performed by using a fourth photomask M4 including light-blocking portions M41X and M41C and a light-transmitting portion M42.

[0111] FIG. 5B illustrates a cross-sectional view depicting a resultant structure of the fourth mask process.

[0112] Referring to FIG. 5B, portions of the third insulating layer 16 and the second conductive layer 17 corresponding to the light-blocking portion M41X of the fourth photomask M4 are patterned to form the pixel electrode 117 and the third insulating layer 116 disposed under the pixel electrode 117. Portions of the third insulating layer 16 and the second conductive layer 17 corresponding to the light-blocking portion M41C are patterned to form the dielectric film 316 and the upper electrode 317 of the capacitor.

[0113] Although the third insulating layer 16 and the second conductive layer 17 are patterned in the same mask process, etching is performed two times. Etching of the third insulating layer 16 and an etching of the second conductive layer 17 is performed separately.

[0114] Etched surfaces of the third insulating layer 116 and the pixel electrode 117 are identical to each other and etched surfaces of the dielectric film 316 and the upper electrode 317 are also identical to each other. The pixel electrode 117 and the upper electrode 317 serve to function as etch masks when the third insulating layer 116 disposed under the pixel electrode 117 and the dielectric film 316 are etched, and thus, etched surfaces thereof are substantially identical to each other. For example, lateral surfaces of the pixel electrode 317 align with lateral surfaces of the third insulating layer 116, and lateral surfaces of the dielectric film 316 align with lateral surfaces of the upper electrode 317.

[0115] The third insulating layer 16 is directly disposed between the upper electrode 317 and the lower electrode 314. Accordingly, the third insulating layer 16 may function as the dielectric film 316 of the capacitor. The third insulating layer 16 is not located in the TFT. Accordingly, the third insulating layer 16 does not function as a gate insulating film. A material or a thickness of the third insulating layer 16 may be selected in consideration of only the characteristics of the capacitor without considering the characteristics of the TFT. Accordingly, the degree of design freedom is increased.

[0116] FIGS. 6A and 6B illustrate cross-sectional views depicting a fifth mask process of the method of manufacturing the organic light-emitting display device 1.

[0117] Referring to FIG. 6A, a third conductive layer 18 is formed on the resultant structure of the fourth mask process of FIG. 5B. The third conductive layer 18 is filled in the opening C1 through which the source region 212a and the drain region 212b are exposed.

[0118] The third conductive layer 18 may have a single-layer structure or a multi-layer structure and may be formed of at least one metal selected from Al, Pt, Pd, Ag, Mg, Au, Ni, Nd, Ir, Cr, Li, Ca, Mo, Ti, W, and Cu.

[0119] A fifth photoresist PR5 is applied to the third conductive layer 18. The fifth mask process is performed by using a fifth photomask M5 including light-blocking portions M51T and M51P and a light-transmitting portion M52.

[0120] FIG. 6B illustrates a cross-sectional view depicting a resultant structure of the fifth mask process.

[0121] Referring to FIG. 6B, portions of the third conductive layer 18 corresponding to the light-blocking portion M51T of the fifth photomask M5 are patterned to form the source electrode 218a and the drain electrode 218b respectively connected to the source region 212a and the drain region 212b of the active layer 212 through the opening C1. A portion of the third conductive layer 18 corresponding to the light-blocking portion M51P is patterned to form the pad electrode 418 of the pad region.

[0122] When the third conductive layer 18 is etched in order to form the source electrode 218a and the drain electrode 218b, the pixel electrode 117 and the upper electrode 317 may also be exposed to an etchant for etching the third conductive layer 18. Accordingly, the third conductive layer 18 may be formed of a material having an etching rate different from the etching rates of the pixel electrode 117 and the upper electrode 317.

[0123] One of the source electrode 218a and the drain electrode 218b is electrically connected to the pixel electrode 117. The source electrode 218a and the drain electrode 218b are patterned after the pixel electrode 117 is formed in FIGS. 6A and 6B. Accordingly, a portion of one of the source electrode 218a or the drain electrode 218b connected to the pixel electrode 117 is formed over the pixel electrode 117.

[0124] Although not shown, a wiring such as a data line connected to the source electrode 218a and/or the drain electrode 218b may be formed by patterning the third conductive layer 18 in the fifth mask process.

[0125] FIGS. 7A and 7B illustrate cross-sectional views depicting a sixth mask process of the method of manufacturing the organic light-emitting display device 1.

[0126] Referring to FIG. 7A, the fourth insulating layer 19 is applied to the resultant structure of the fifth mask process of FIG. 6B. The fourth insulating layer 19 may be an organic insulating film. In particular, if the fourth insulating layer 19 is a photosensitive organic insulating film, use of an additional photoresist may not be necessary.

[0127] The sixth mask process is performed by using a sixth photomask M6 including a light-blocking portion M61 and light-transmitting portions M62X and M62P.

[0128] FIG. 7B illustrates a cross-sectional view depicting a resultant structure of the sixth mask process.

[0129] Referring to FIG. 7B, a portion of the fourth insulating layer 19 corresponding to the light-transmitting

portion M62X is removed to form the opening C3 through which the pixel electrode 117 is partially exposed. A portion of the fourth insulating layer 19 corresponding to the light-transmitting portion M62P is removed to form the opening C4 through which the pad electrode 418 is partially exposed.

[0130] The opening C3 through which the pixel electrode 117 is exposed not only defines a light-emitting region but also serves to increase an interval between the counter electrode 121 (see FIG. 1) and an edge of the pixel electrode 117. Accordingly, an electric field may be prevented from concentrating on the edge of the pixel electrode 117 and a short circuit may be prevented from occurring between the pixel electrode 117 and the counter electrode 120.

[0131] Although not shown, the organic light-emitting device 1 of FIG. 1 may be formed by forming the organic light-emitting layer 120 on the pixel electrode 117 and forming the counter electrode 121 (see FIG. 1), which may be a common electrode, on the organic light-emitting layer 120 after the sixth mask process. Also, an encapsulation member (not shown) may be further formed on the counter electrode 121 (see FIG. 1).

[0132] An organic light-emitting display device 2 according to another embodiment of the invention will be explained with reference to FIG. 8 by focusing on a difference from the organic light-emitting display device 1 of FIG. 1.

[0133] FIG. 8 illustrates a cross-sectional view depicting the organic light-emitting display device 2 according to this embodiment.

[0134] Referring to FIG. 8, the substrate 10 of the organic light-emitting display device 2 includes a pixel region PXL2 in which at least one organic light-emitting layer 120 is disposed, a TFT region TFT2 in which at least one TFT is disposed, a capacitor region CAP2 in which at least one capacitor is disposed, and a pad region PAD2 in which at least one pad electrode 418 is disposed. The TFT region TFT2 and the pad region PAD2 may be the same as the TFT region TFT1 and the pad region PAD1 of the organic light-emitting display device 1.

[0135] In the pixel region PXL2, a pixel electrode 117-1, formed of the same material as the upper electrode 317 of the capacitor, is disposed on the substrate 10, the buffer layer 11, the first insulating layer 13, the second insulating layer 15, and the third insulating layer 116.

[0136] If the organic light-emitting display device 2 is a bottom-emission organic light-emitting display device, the pixel electrode 117-1 may be a transparent electrode and the counter electrode 121 may be a reflective electrode.

[0137] The organic light-emitting layer 120 is formed on the pixel electrode 117-1, and light emitted by the organic light-emitting layer 120 may be emitted through the pixel electrode 117-1 formed of a transparent conductive material toward the substrate 10.

[0138] The pixel electrode 117-1 of the organic light-emitting display device 2 may have a multi-layer structure including a transparent conductive layer 117a and a semi-transmissive metal layer 117b disposed on the transparent conductive layer 117a.

[0139] The counter electrode 121 may function as a reflective mirror and the semi-transmissive metal layer 117b may function as a semi-transmissive mirror. Light emitted by the organic light-emitting layer 119 may resonate between the counter electrode 121 and the semi-transmissive metal layer 117b.

[0140] Accordingly, light use efficiency of the organic light-emitting display device 2 may be further improved by a resonance effect due to a mirror effect as well as a resonance effect due to a DBR effect of the first through third insulating layers 13, 15, and 116, which may be disposed under the pixel electrode 117-1.

[0141] The semi-transmissive metal layer 117b may be formed of at least one material selected from Ag, an Ag alloy, Al, and an Al alloy. In order to act as a resonant mirror with respect to the counter electrode 121, which may be a reflective electrode, the semi-transmissive metal layer 117b may have a thickness equal to or less than about 300 Å.

[0142] In particular, if the semi-transmissive metal layer 117b includes silver (Ag), since the source electrode 218a and the drain electrode 218b may be formed after the semi-transmissive metal layer 117b is formed, the semi-transmissive metal layer 117b including Ag may be damaged when the source electrode 218a and the drain electrode 218b are etched. Accordingly, a protective layer 117c for protecting the Ag is further provided on the semi-transmissive metal layer 117b. The protective layer 117c may be formed of a transparent conductive oxide including ITO or the like.

[0143] The pixel electrode 117-1 including the semi-transmissive metal layer 117b may be patterned in the fourth mask process. The pixel electrode 117-1 may be patterned alone when another conductive layer does not exist over the pixel electrode 117-1.

[0144] If another conductive layer (not shown) is further formed over the pixel electrode 117-1 and the conductive layer and the pixel electrode 117-1 are simultaneously patterned to have the same pattern, it may not be easy to etch the pixel electrode 117-1. In particular, if the semi-transmissive metal layer 117b includes Ag, since the semi-transmissive metal layer 117b may be easily damaged, it may be difficult to form a resonant structure using a mirror effect. However, as shown in FIG. 8, the pixel electrode 117-1 may be patterned alone to function as a semi-transmissive mirror having a resonant structure. Accordingly, it may be easy to form a resonant mirror.

[0145] The pixel electrode 117-1 and the upper electrode 317 of the capacitor of the organic light-emitting display device 2 may be formed of the same material. Although not shown, the upper electrode 317 may include a transparent conductive layer, a semi-transmissive metal layer, and a protective layer which are sequentially disposed from the bottom, like the pixel electrode 117-1.

[0146] From the above it will be appreciated that a TFT array substrate, an organic light-emitting display device including the same, and a method of manufacturing the organic light-emitting display device including the TFT array substrate according to the present invention may provide the following effects.

[0147] A dielectric film of a capacitor and a gate insulating film of a TFT may be formed as separate insulating layers. Accordingly, the insulating layers may be designed appropriately according to characteristics of the capacitor and characteristics of the TFT, respectively.

[0148] A thickness of the dielectric film of the capacitor may be easily controlled. Accordingly, an aperture ratio may be increased.

[0149] A resonant mirror may be patterned from only a pixel electrode, without a conductive layer stacked on the pixel electrode that is used as a semi-transmissive mirror of a resonant structure. Accordingly, a resonant mirror may be easily provided.

[0150] A pad electrode may be formed in a post-process. Accordingly, the reliability of the pad electrode may be prevented from being lowered.

[0151] The TFT array substrate and the organic light-emitting display device may be manufactured by performing only 6 mask processes.

[0152] Embodiments of the invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the scope of the invention as set forth in the following claims.

Claims

1. A thin film transistor (TFT) array substrate, comprising:

   a substrate formation (10, 11);
   a TFT disposed on the substrate formation, the TFT including an active layer (212), a gate electrode (214), a source electrode (218a), a drain electrode (218b), a first insulating layer (13) disposed between the active layer (212) and the gate electrode (214), and a second insulating layer (15) disposed between the gate electrode (214) and the source and drain electrodes (218a, 218b);
   a pixel electrode (117) disposed on the first insulating layer (13) and the second insulating layer (15), the pixel electrode being connected to one of the source electrode and the drain electrode;
   a capacitor including a lower electrode (314) disposed on a same layer as the gate electrode (214), and including an upper electrode (317) including a same material as the pixel electrode (117);
   a third insulating layer (116, 316) directly disposed between the second insulating layer (15) and the pixel electrode (117) and between the lower electrode (314) and the upper electrode (317); and
   a fourth insulating layer (19) that covers the source electrode (218a), the drain electrode (218b), and the upper electrode (317), and exposes the pixel electrode (117);
   characterized in that lateral surfaces of the pixel electrode (117) align with lateral surfaces of the third insulating layer (116) and lateral surfaces of the upper electrode (317) align with lateral surfaces of the third insulating layer (316).

2. A TFT array substrate as claimed in claim 1, wherein the first insulating layer (13) is commonly disposed over the active layer (212) and under the lower electrode (314).

3. A TFT array substrate as claimed in claim 1 or 2, wherein a thickness of the third insulating layer (116, 316) is less than a thickness of the second insulating layer (15).

4. A TFT array substrate as claimed in any preceding claim, wherein a dielectric constant of the third insulating layer (116, 316) is higher than a dielectric constant of the first insulating layer (13).

5. A TFT array substrate as claimed in any preceding claim, wherein the first insulating layer (13), the second insulating layer (15), and the third insulating layer (116) are sequentially disposed between the pixel electrode (117) and the substrate formation (10,11), and refractive indices of adjacent insulating layers of the first through third insulating layers are different from each other.

6. A TFT array substrate as claimed in any preceding claim, wherein the pixel electrode (117) includes a transparent conductive oxide (TCO).

7. A TFT array substrate as claimed in claim 6, wherein the pixel electrode (117-1) further includes a semi-transmissive metal layer (117b) and the semi-transmissive metal layer is disposed on a layer (117a) including the transparent conductive oxide

8. A TFT array substrate as claimed in claim 7 further including a protective layer (117c) disposed on the semi-transmissive metal layer (117b).

9. A TFT array substrate as claimed in any preceding claim, wherein a portion of one of the source electrode (218a) and the drain electrode (218b) that is connected to the pixel electrode (117) is disposed over the pixel electrode.

10. A TFT array substrate as claimed in any preceding claim, wherein the source electrode (218a) and the drain electrode (218b) include a material having an etching rate different from an etching rate of the pixel electrode (117) and the upper electrode (317).

11. A TFT array substrate as claimed in any preceding claim, further comprising a pad electrode (418) formed of a same material as the source electrode (218a) and the drain electrode (218b).

12. A TFT array substrate as claimed in claim 11, wherein the pad electrode (418) is disposed on a same layer as the source electrode (218a) and the drain electrode (218b).

13. An organic light-emitting display device, comprising:

a TFT array substrate according to any preceding claim;
an organic light-emitting layer (120) disposed on the pixel electrode (117); and
a counter electrode (121) disposed on the organic light-emitting layer (120).

14. An organic light-emitting display device as claimed in claim 13, wherein the counter electrode (121) is a reflective electrode that reflects light emitted by the organic light-emitting layer (120).

15. A method of manufacturing a TFT array substrate according to claim 1, the method comprising:

forming a semiconductor layer (12) on a substrate formation (10, 11) and forming an active layer (212) of a TFT by patterning the semiconductor layer (12) using a first mask process;
forming a first insulating layer (13), stacking a first conductive layer (14) on the first insulating layer, and forming a gate electrode (214) of the TFT and a lower electrode (314) of a capacitor by patterning the first conductive layer using a second mask process;
forming a second insulating layer (15), and forming an opening in the second insulating layer using a third mask process to expose a source region (212a) and a drain region (212b) of the active layer and the lower electrode (314) of the capacitor;
sequentially forming a third insulating layer (16) and a second conductive layer (17) on a resultant structure of the third mask process, and forming a pixel electrode (117), an upper electrode (317) of the capacitor, and a dielectric film (316) that is directly disposed on the lower electrode (314) by simultaneously or sequentially patterning the third insulating layer (16) and the second conductive layer (17) using a fourth mask process;
forming a third conductive layer (18) on a resultant structure of the fourth mask process, and forming a source electrode (218a) and a drain electrode (218b) by patterning the third conductive layer using a fifth mask process; and
forming a fourth insulating layer (19) and removing a portion of the fourth insulating layer to expose the pixel electrode (117) using a sixth mask process.

16. A method as claimed in claim 15, wherein the method further includes doping the source region and the drain region with ion impurities after forming the gate electrode (214) using the second mask process.

17. A method as claimed in claim 15 or 16, wherein the fourth mask process includes a first etching process to etch the third insulating layer (16), and a second etching process to etch the second conductive layer (17).

18. A method as claimed in one of claims 15, 16 or 17, further including forming a pad electrode (418) including the same material as the source electrode (218a) and the drain electrode (218b) using the fifth mask process.

19. A method as claimed in one of claims 15 to 18, wherein the second conductive layer (17) is formed by sequentially stacking a transparent conductive layer and a semi-transmissive conductive layer.

20. A method as claimed in claim 19, further including forming a protective layer on the semi-transmissive conductive layer.

Patentansprüche

1. Dünnschichttransistor-(TFT-)Arraysubstrat, umfassend:

eine Substratformation (10, 11);
einen auf der Substratformation angeordneten TFT, wobei der TFT eine aktive Schicht (212), eine Gate-Elektrode (214), eine Source-Elektrode (218a), eine Drain-Elektrode (218b), eine

zwischen der aktiven Schicht (212) und der Gate-Elektrode (214) angeordnete erste isolierende Schicht (13) und eine zwischen der Gate-Elektrode (214) und den Source- und Drain-Elektroden (218a, 218b) angeordnete zweite isolierende Schicht (15) aufweist;
eine Pixelelektrode (117), die auf der ersten isolierenden Schicht (13) und der zweiten isolierenden Schicht (15) angeordnet ist, wobei die Pixelelektrode mit einer der Source-Elektrode und der Drain-Elektrode verbunden ist;
einen Kondensator, der eine untere Elektrode (314) aufweist, die auf einer gleichen Schicht wie die Gate-Elektrode (214) angeordnet ist, und eine obere Elektrode (317) aufweist, die ein gleiches Material wie die Pixelelektrode (117) aufweist;
eine dritte isolierende Schicht (116, 316), die direkt zwischen der zweiten isolierenden Schicht (15) und der Pixelelektrode (117) und zwischen der unteren Elektrode (314) und der oberen Elektrode (317) angeordnet ist; und
eine vierte isolierende Schicht (19), welche die Source-Elektrode (218a), die Drain-Elektrode (218b) und die obere Elektrode (317) bedeckt und die Pixelelektrode (117) frei lässt;
dadurch gekennzeichnet, dass Seitenflächen der Pixelelektrode (117) mit Seitenflächen der dritten isolierenden Schicht (116) fluchten und Seitenflächen der oberen Elektrode (317) mit Seitenflächen der dritten isolierenden Schicht (316) fluchten.

2. TFT-Arraysubstrat nach Anspruch 1, worin die erste isolierende Schicht (13) im Allgemeinen über der aktiven Schicht (212) und unter der unteren Elektrode (314) angeordnet ist.

3. TFT-Arraysubstrat nach Anspruch 1 oder 2, worin eine Dicke der dritten isolierenden Schicht (116, 316) geringer als eine Dicke der zweiten isolierenden Schicht (15) ist.

4. TFT-Arraysubstrat nach einem der vorhergehenden Ansprüche, worin eine Dielektrizitätskonstante der dritten isolierenden Schicht (116, 316) höher als eine Dielektrizitätskonstante der ersten isolierenden Schicht (13) ist.

5. TFT-Arraysubstrat nach einem der vorhergehenden Ansprüche, worin die erste isolierende Schicht (13), die zweite isolierende Schicht (15) und die dritte isolierende Schicht (16) der Reihe nach zwischen der Pixelelektrode (117) und der Substratformation (10, 11) angeordnet werden, und die Brechungsindizes benachbarter isolierender Schichten der ersten bis dritten isolierenden Schicht sich voneinander unterscheiden.

6. TFT-Arraysubstrat nach einem der vorhergehenden Ansprüche, worin die Pixelelektrode (117) ein transparentes leitfähiges Oxid (TCO) aufweist.

7. TFT-Arraysubstrat nach Anspruch 6, worin die Pixelelektrode (117-1) ferner eine halbdurchlässige Metallschicht (117b) aufweist und die halbdurchlässige Metallschicht auf einer Schicht (117a) angeordnet ist, die das transparente leitfähige Oxid aufweist.

8. TFT-Arraysubstrat nach Anspruch 7, ferner eine Schutzschicht (117c) aufweisend, die auf der halbdurchlässigen Metallschicht (117b) angeordnet ist.

9. TFT-Arraysubstrat nach einem der vorhergehenden Ansprüche, worin ein Abschnitt von einer der Source-Elektrode (218a) und der Drain-Elektrode (218b), der mit der Pixelelektrode (117) verbunden ist, über der Pixelelektrode angeordnet ist.

10. TFT-Arraysubstrat nach einem der vorhergehenden Ansprüche, worin die Source-Elektrode (218a) und die Drain-Elektrode (218b) ein Material mit einer Ätzrate aufweist, die sich von einer Ätzrate der Pixelelektrode (117) und der oberen Elektrode (317) unterscheidet.

11. TFT-Arraysubstrat nach einem der vorhergehenden Ansprüche, ferner eine Anschlusselektrode (418) umfassend, die aus dem gleichen Material wie die Source-Elektrode (218a) und die Drain-Elektrode (218b) gebildet ist.

12. TFT-Arraysubstrat nach Anspruch 11, worin die Anschlusselektrode (418) auf einer gleichen Schicht wie die Source-Elektrode (218a) und die Drain-Elektrode (218b) angeordnet ist.

13. Organische Leuchtanzeigenvorrichtung, umfassend:

ein TFT-Arraysubstrat nach einem der vorhergehenden Ansprüche;
eine organische Leuchtschicht (120), die auf der Pixelelektrode (117) angeordnet ist; und
eine Gegenelektrode (121), die auf der organischen Leuchtschicht (120) angeordnet ist.

14. Organische Leuchtanzeigenvorrichtung nach Anspruch 13, worin die Gegenelektrode (121) eine reflektierende Elektrode ist, die durch die organische Leuchtschicht (120) emittiertes Licht reflektiert.

15. Verfahren zum Herstellen eines TFT-Arraysubstrats nach Anspruch 1, wobei das Verfahren umfasst:

Ausbilden einer Halbleiterschicht (12) auf einer Substratformation (10, 11) und Ausbilden einer

aktiven Schicht (212) eines TFT durch Strukturieren der Halbleiterschicht (12) unter Verwendung eines ersten Maskenprozesses;
Ausbilden einer ersten isolierenden Schicht (13), Überschichten einer ersten leitfähigen Schicht (14) auf die erste isolierende Schicht und Ausbilden einer Gate-Elektrode (214) des TFT und einer unteren Elektrode (314) eines Kondensators durch Strukturieren der ersten leitfähigen Schicht unter Verwendung eines zweiten Maskenprozesses;
Ausbilden einer zweiten isolierenden Schicht (15) und Ausbilden einer Öffnung in der zweiten isolierenden Schicht unter Verwendung eines dritten Maskenprozesses, um einen Source-Bereich (212a) und einen Drain-Bereich (212b) der aktiven Schicht und die untere Elektrode (314) des Kondensators freizulegen;
der Reihe nach erfolgendes Ausbilden einer dritten isolierenden Schicht (16) und einer zweiten leitfähigen Schicht (17) auf einer resultierenden Struktur des dritten Maskenprozesses und Ausbilden einer Pixelelektrode (117), einer oberen Elektrode (317) des Kondensators und einer dielektrischen Schicht (316), die direkt über der unteren Elektrode (314) angeordnet ist, durch gleichzeitig oder der Reihe nach erfolgendes Strukturieren der dritten isolierenden Schicht (16) und der zweiten leitfähigen Schicht (17) unter Verwendung eines vierten Maskenprozesses;
Ausbilden einer dritten leitfähigen Schicht (18) auf einer resultierenden Struktur des vierten Maskenprozesses und Ausbilden einer Source-Elektrode (218a) und einer Drain-Elektrode (218b) durch Strukturieren der dritten leitfähigen Schicht unter Verwendung eines fünften Maskenprozesses; und
Ausbilden einer vierten isolierenden Schicht (19) und Entfernen eines Abschnitts der vierten isolierenden Schicht, um die Pixelelektrode (117) freizulegen, unter Verwendung eines sechsten Maskenprozesses.

16. Verfahren nach Anspruch 15, worin das Verfahren ferner aufweist: Dotieren des Source-Bereichs und des Drain-Bereichs mit Ionenstörstellen nach dem Ausbilden der Gate-Elektrode (214) unter Verwendung des zweiten Maskenprozesses.

17. Verfahren nach Anspruch 15 oder 16, worin der vierte Maskenprozess einen ersten Ätzprozess, um die dritte isolierende Schicht (16) zu ätzen, und einen zweiten Ätzprozess, um die zweite leitfähige Schicht (17) zu ätzen, aufweist.

18. Verfahren nach einem der Ansprüche 15, 16 oder 17, ferner aufweisend: Ausbilden einer Anschlusselektrode (418), die das gleiche Material wie die Source-Elektrode (218a) und die Drain-Elektrode (218b) aufweist, unter Verwendung des fünften Maskenprozesses.

19. Verfahren nach einem der Ansprüche 15 bis 18, worin die zweite leitfähige Schicht (17) durch der Reihe nach erfolgendes Überschichten einer transparenten leitfähigen Schicht und einer halbdurchlässigen leitfähigen Schicht ausgebildet wird.

20. Verfahren nach Anspruch 19, ferner aufweisend: Ausbilden einer Schutzschicht auf der halbdurchlässigen leitfähigen Schicht.

Revendications

1. Substrat de matrice de transistor à couches minces (TFT) comprenant :

une formation de substrat (10, 11) ;
un TFT disposé sur la formation de substrat, le TFT comprenant une couche active (212), une électrode de grille (214), une électrode de source (218a), une électrode de drain (218b), une première couche isolante (13) disposée entre la couche active (212) et l'électrode de grille (214) et une deuxième couche isolante (15) disposée entre l'électrode de grille (214) et les électrodes de source et de drain (218a, 218b) ;
une électrode de pixel (117) disposée sur la première couche isolante (13) et la deuxième couche isolante (15), l'électrode de pixel étant connectée à l'une parmi l'électrode de source et l'électrode de drain ;
un condensateur comprenant une électrode inférieure (314) disposée sur une même couche que l'électrode de grille (214) et comprenant une électrode supérieure (317) comprenant le même matériau que l'électrode de pixel (117) ;
une troisième couche isolante (116, 316) disposée directement entre la deuxième couche isolante (15) et l'électrode de pixel (117) et entre l'électrode inférieure (314) et l'électrode supérieure (317) ; et
une quatrième couche isolante (19) qui recouvre l'électrode de source (218a), l'électrode de drain (218b) et l'électrode supérieure (317) et expose l'électrode de pixel (117) ;
caractérisé en ce que des surfaces latérales de l'électrode de pixel (117) s'alignent avec des surfaces latérales de la troisième couche isolante (116) et des surfaces latérales de l'électrode supérieure (317) s'alignent avec des surfaces latérales de la troisième couche isolante (316).

2. Substrat de matrice TFT selon la revendication 1, dans lequel la première couche isolante (13) est communément disposée au-dessus de la couche active (212) et sous l'électrode inférieure (314).

3. Substrat de matrice TFT selon la revendication 1 ou 2, dans lequel une épaisseur de la troisième couche isolante (116, 316) est inférieure à une épaisseur de la deuxième couche isolante (15).

4. Substrat de matrice TFT selon l'une quelconque des revendications précédentes, dans lequel une constante diélectrique de la troisième couche isolante (116, 316) est supérieure à une constante diélectrique de la première couche isolante (13).

5. Substrat de matrice TFT selon l'une quelconque des revendications précédentes, dans lequel la première couche isolante (13), la deuxième couche isolante (15) et la troisième couche isolante (116) sont disposées séquentiellement entre l'électrode de pixel (117) et la formation de substrat (10, 11) et les indices de réfraction de couches isolantes adjacentes et de la première à la troisième couche isolante sont différents les uns des autres.

6. Substrat de matrice TFT selon l'une quelconque des revendications précédentes, dans lequel l'électrode de pixel (117) comprend un oxyde conducteur transparent (TCO).

7. Substrat de matrice TFT selon la revendication 6, dans lequel l'électrode de pixel (117-1) comprend en outre une couche métallique semi-transmissive (117b) et la couche métallique semi-transmissive est disposée sur une couche (117a) comprenant l'oxyde conducteur transparent.

8. Substrat de matrice TFT selon la revendication 7, comprenant en outre une couche protectrice (117c) disposée sur la couche métallique semi-transmissive (117b).

9. Substrat de matrice TFT selon l'une quelconque des revendications précédentes, dans lequel une portion de l'électrode de source (218a) ou de l'électrode de drain (218b), qui est connectée à l'électrode de pixel (117), est disposée au-dessus de l'électrode de pixel.

10. Substrat de matrice TFT selon l'une quelconque des revendications précédentes, dans lequel l'électrode de source (218a) et l'électrode de drain (218b) comprennent un matériau ayant un taux de gravure différent d'un taux de gravure de l'électrode de pixel (117) et de l'électrode supérieure (317).

11. Substrat de matrice TFT selon l'une quelconque des revendications précédentes, comprenant en outre une électrode de contact (418) constituée du même matériau que l'électrode de source (218a) et l'électrode de drain (218b).

12. Substrat de matrice TFT selon la revendication 11, dans lequel l'électrode de contact (418) est disposée sur une même couche que l'électrode de source (218a) et l'électrode de drain (218b).

13. Dispositif d'affichage électroluminescent organique comprenant :

un substrat de matrice TFT selon l'une quelconque des revendications précédentes ;
une couche électroluminescente organique (120) disposée sur l'électrode de pixel (117) ; et
une contre-électrode (121) disposée sur la couche électroluminescente organique (120).

14. Dispositif d'affichage électroluminescent organique selon la revendication 13, dans lequel la contre-électrode (121) est une électrode réfléchissante qui réfléchit la lumière émise par la couche électroluminescente organique (120).

15. Procédé de fabrication d'un substrat de matrice TFT selon la revendication 1, ce procédé comprenant :

la formation d'une couche de semi-conducteur (12) sur une formation de substrat (10, 11) et formation d'une couche active (212) d'un TFT en structurant la couche de semi-conducteur (12) à l'aide d'un premier processus de masquage ;
la formation d'une première couche isolante (13), l'empilement d'une première couche conductrice (14) sur la première couche isolante et la formation d'une électrode de grille (214) du TFT et d'une électrode inférieure (314) d'un condensateur en structurant la première couche conductrice à l'aide d'un deuxième processus de masquage ;
la formation d'une deuxième couche isolante (15) et la formation d'une ouverture dans la deuxième couche isolante à l'aide d'un troisième processus de masquage afin d'exposer une région de source (212a) et une région de drain (212b) de la couche active et l'électrode inférieure (314) du condensateur ;
la formation séquentielle d'une troisième couche isolante (16) et d'une deuxième couche conductrice (17) sur la structure résultant du troisième processus de masquage et la formation d'une électrode de pixel (117), d'une électrode supérieure (317) du condensateur et d'une couche diélectrique (316) qui est directement disposée sur l'électrode inférieure (314) en struc-

turant simultanément ou séquentiellement la troisième couche isolante (16) et la deuxième couche conductrice (17) à l'aide quatrième processus de masquage ;
la formation d'une troisième couche conductrice (18) sur une structure résultant du quatrième processus de masquage, et la formation d'une électrode de source (218a) et d'une électrode de drain (218b) en structurant la troisième couche conductrice à l'aide d'un cinquième processus de masquage ; et
la formation d'une quatrième couche isolante (19) et l'élimination d'une portion de la quatrième couche isolante afin d'exposer l'électrode de pixel (117) à l'aide d'un sixième processus de masquage.

16. Procédé selon la revendication 15, dans lequel ledit procédé comprend en outre le dopage de la région de source et de la région de drain avec des impuretés ioniques après la formation de l'électrode de grille (214) à l'aide du deuxième processus de masquage.

17. Procédé selon la revendication 15 ou 16, dans lequel le quatrième processus de masquage comprend un premier processus de gravure afin de graver la troisième couche isolante (16), et un deuxième processus de gravure afin de graver la deuxième couche conductrice (17).

18. Procédé selon l'une quelconque des revendications 15, 16 ou 17, comprenant en outre la formation d'une électrode de contact (418) comprenant le même matériau que l'électrode de source (218a) et que l'électrode de drain (218b) à l'aide du cinquième processus de masquage.

19. Procédé selon l'une quelconque des revendications 15 à 18, dans lequel la deuxième couche conductrice (17) est formée de manière séquentielle en empilant une couche conductrice transparente et une couche conductrice semi-transmissive.

20. Procédé selon la revendication 19, comprenant en outre la formation d'une couche protectrice sur la couche conductrice semi-transmissive.

FIG. 1

FIG. 2A

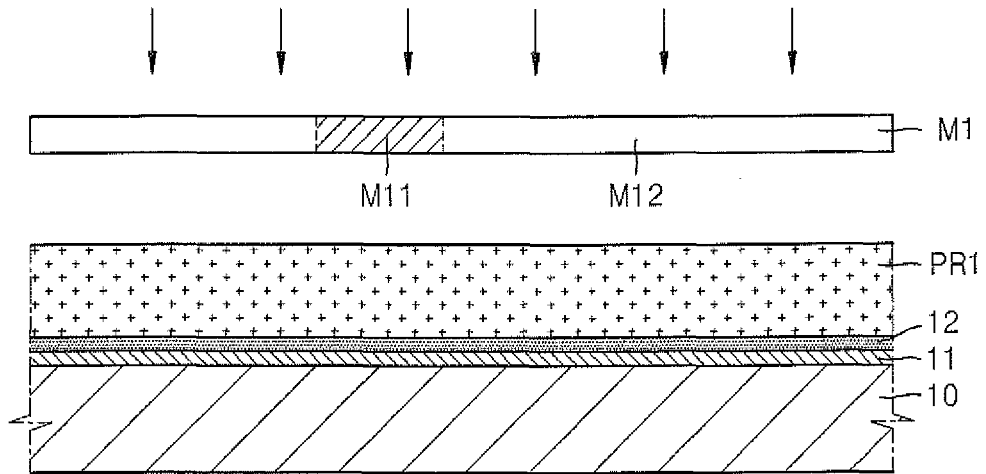


FIG. 2B

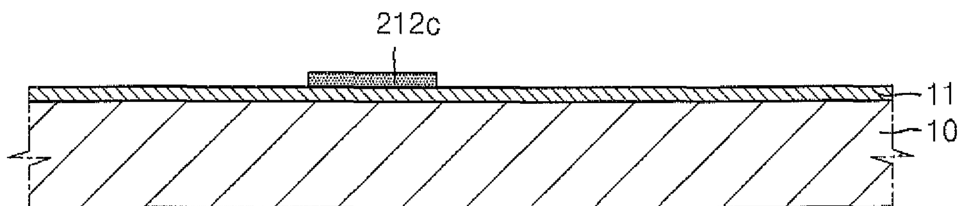


FIG. 3A

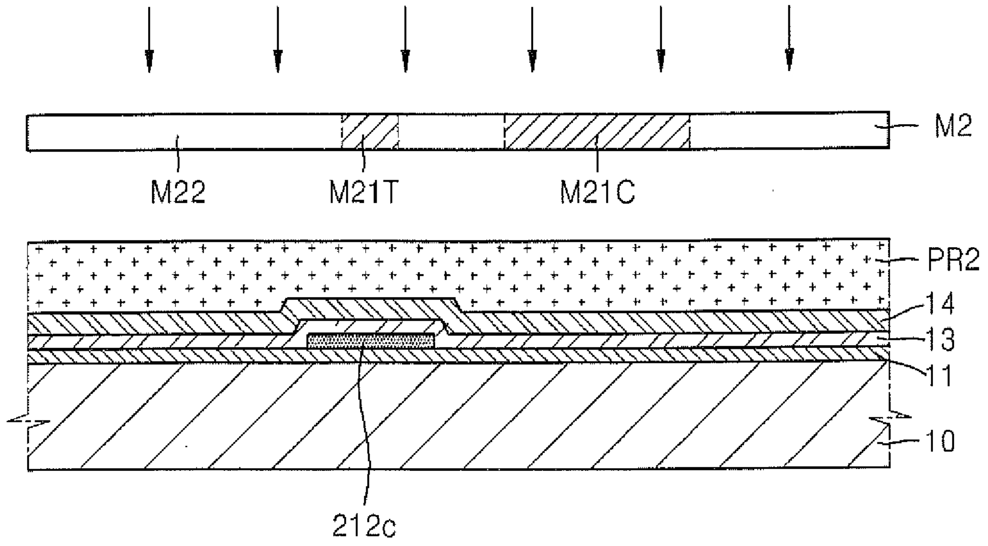


FIG. 3B

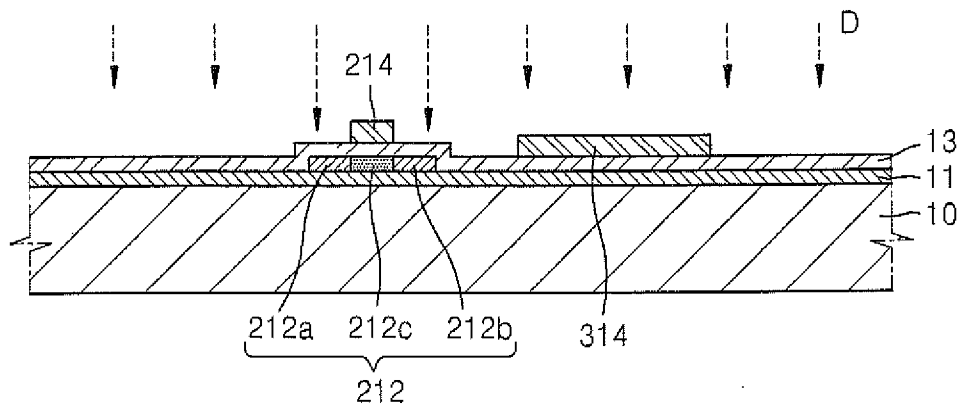


FIG. 4A

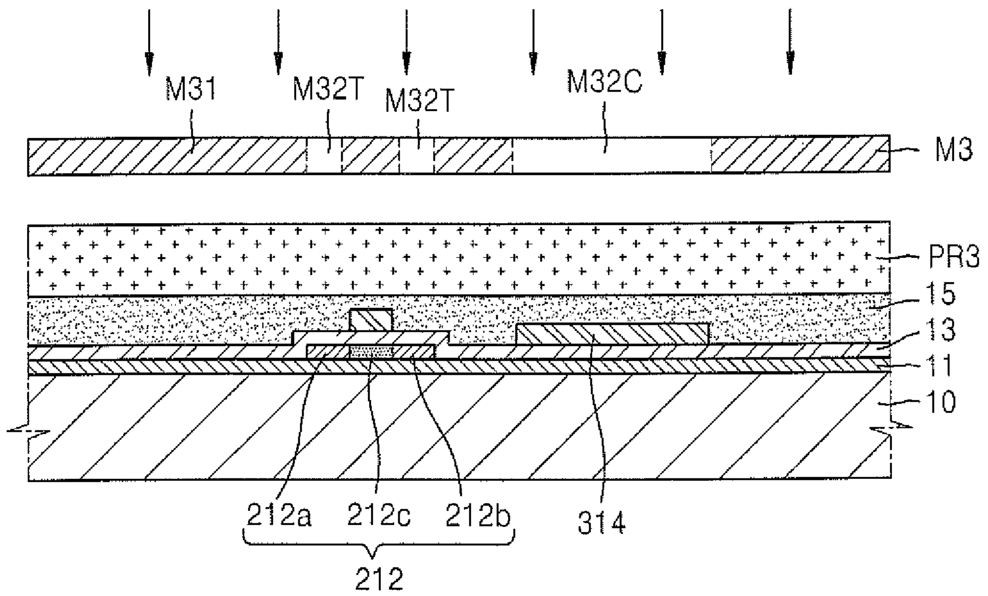


FIG. 4B

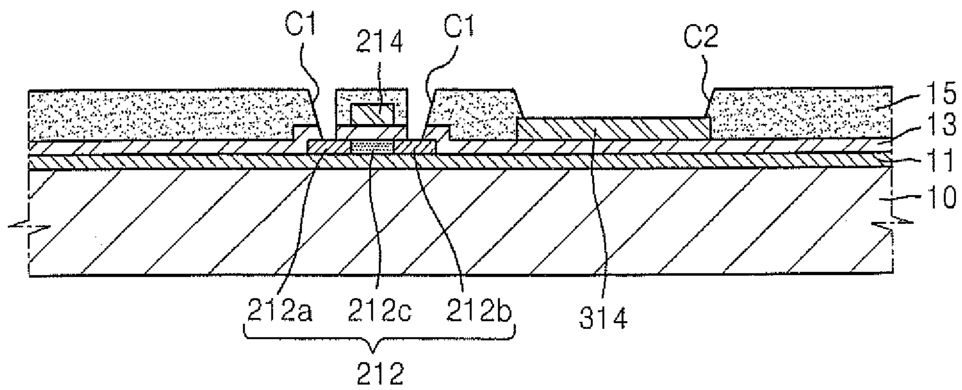


FIG. 5A

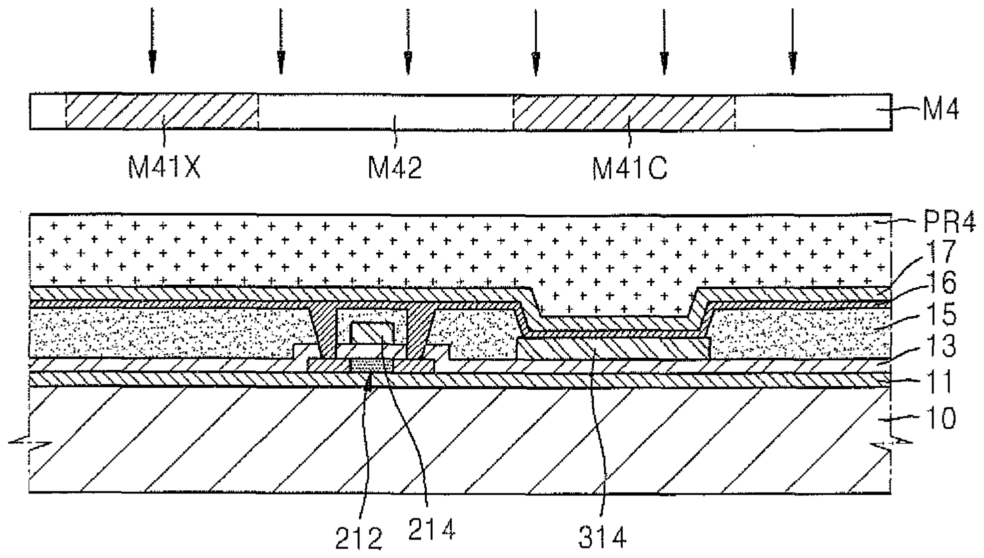


FIG. 5B

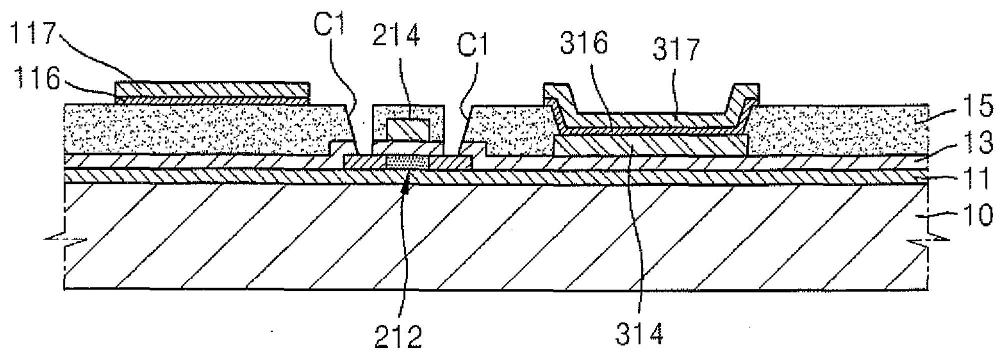


FIG. 6A

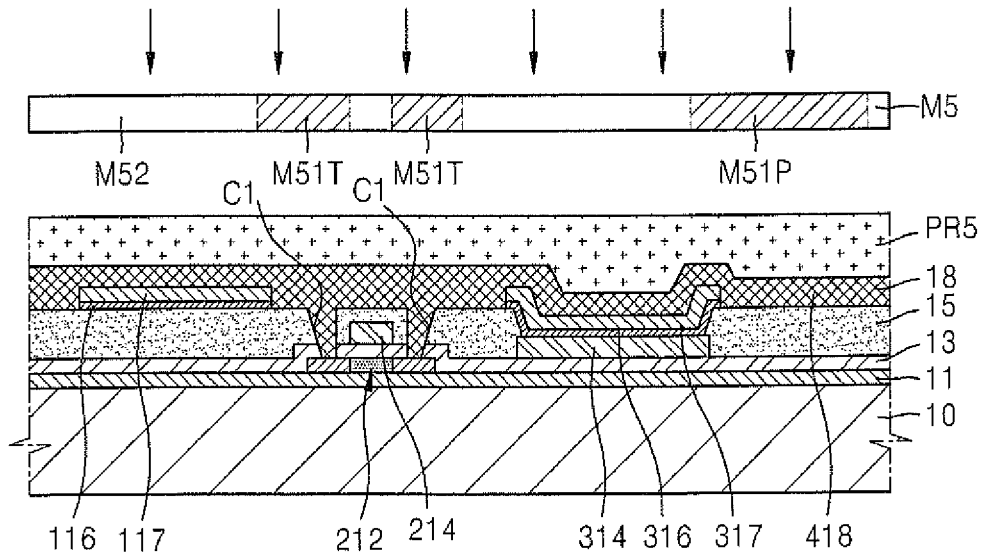


FIG. 6B

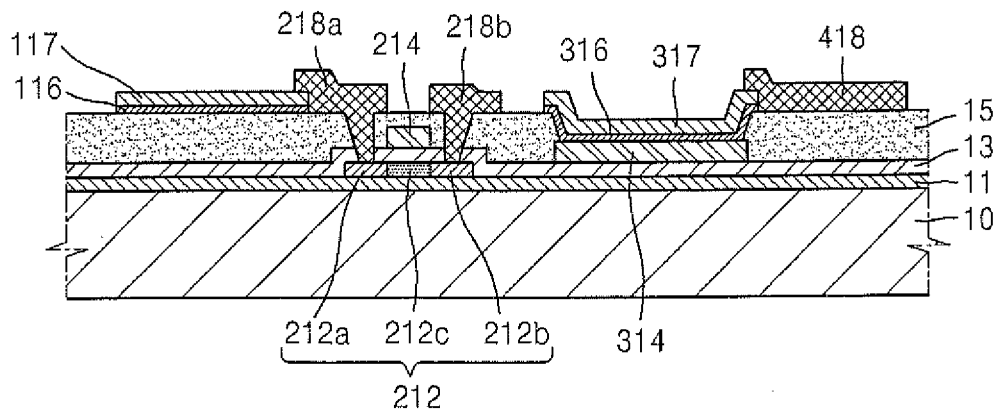


FIG. 7A

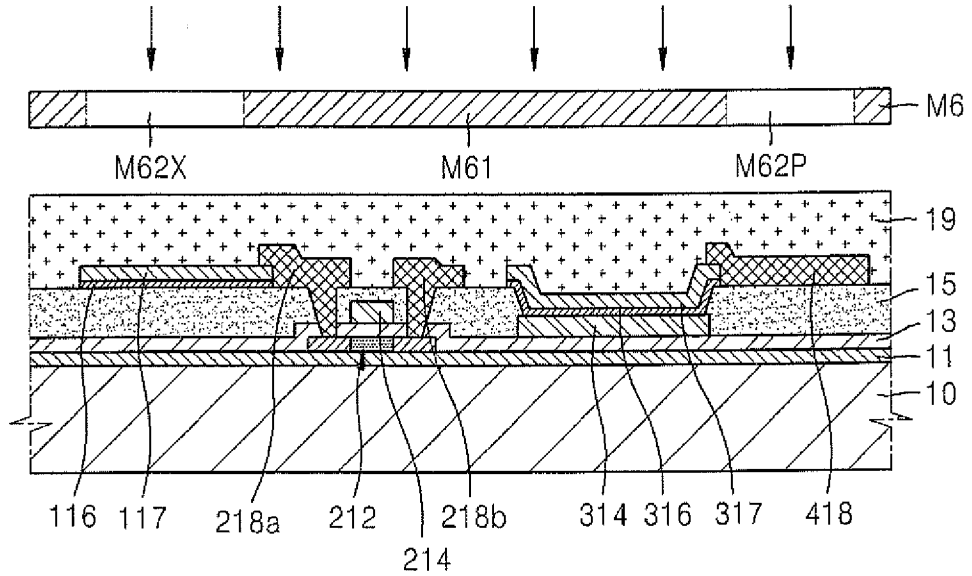


FIG. 7B

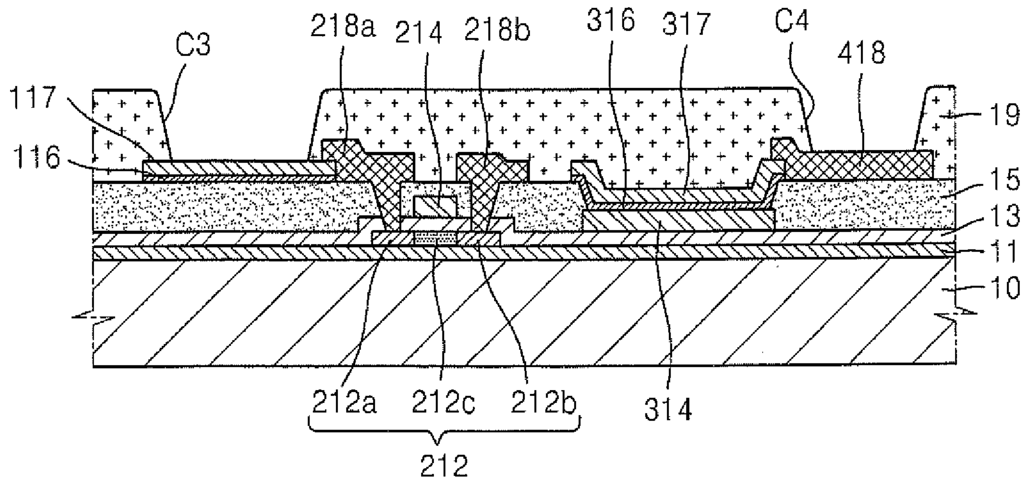
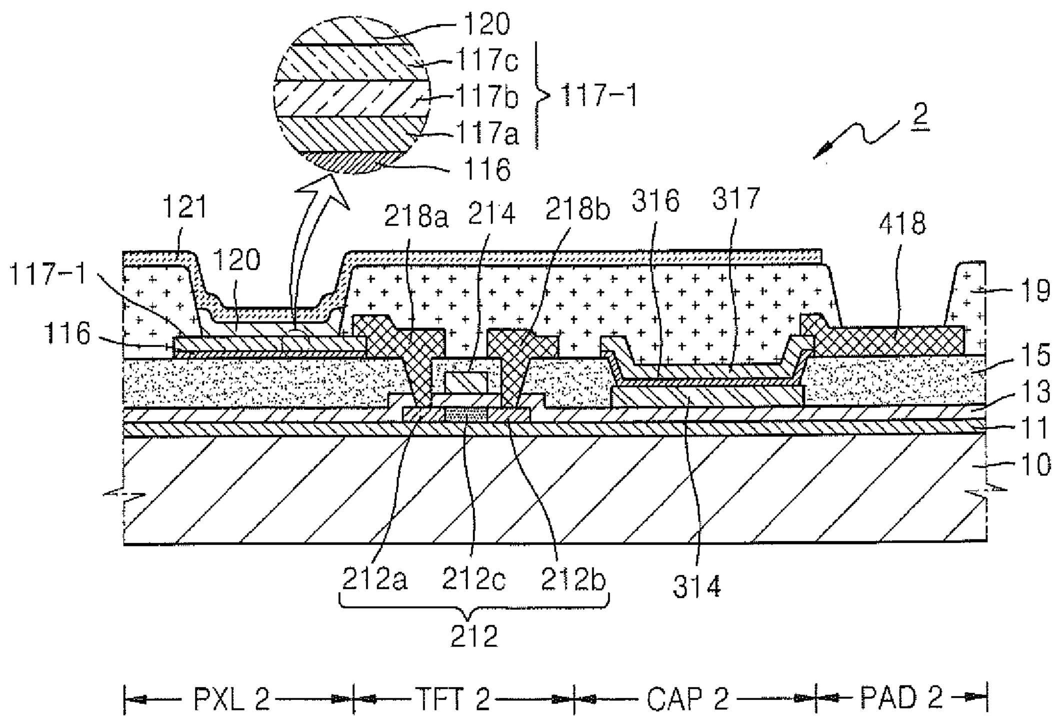


FIG. 8



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2002104995 A **[0007]**
- US 20030141811 A **[0008]**
- WO 03071511 A **[0009]**

patsnap

专利名称(译)	薄膜晶体管阵列基板，包括该薄膜晶体管阵列基板的有机发光显示装置，以及制造该有机发光显示装置的方法		
公开(公告)号	EP2546903B1	公开(公告)日	2017-11-29
申请号	EP2012160792	申请日	2012-03-22
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	LEE JUNE WOO CHOI JAE BEOM JUNG KWAN WOOK OH JAE HWAN JIN SEONG HYUN KIM KWANG HAE CHOI JONG HYUN		
发明人	LEE, JUNE-WOO CHOI, JAE-BEOM JUNG, KWAN-WOOK OH, JAE-HWAN JIN, SEONG-HYUN KIM, KWANG-HAE CHOI, JONG-HYUN		
IPC分类号	H01L27/12 H01L27/32 H01L51/52		
CPC分类号	H01L27/1255 H01L27/1288 H01L27/3265 H01L27/3276 H01L51/5215 H01L51/5265 H01L2227/323 H01L27/3248 H01L27/1237 H01L27/127 H01L29/66742		
优先权	1020110070027 2011-07-14 KR		
其他公开文献	EP2546903A3 EP2546903A2		
外部链接	Espacenet		

摘要(译)

薄膜晶体管（TFT）阵列基板包括基板上的TFT，TFT包括有源层（212），栅电极（214），源电极（218a），漏电极（218b），第一绝缘层（13）在有源层和栅电极之间，以及在栅电极和源电极和漏电极之间的第二绝缘层（15）;第一绝缘层和第二绝缘层上的像素电极（117），像素电极连接到源电极和漏电极中的一个;电容器包括位于与栅电极相同的层上的下电极（314）和包括与像素电极相同的材料的上电极（317）;第三绝缘层（116,316）直接位于第二绝缘层和像素电极之间以及下电极和上电极之间;第四绝缘层（19）覆盖源电极，漏电极和上电极，并暴露像素电极。