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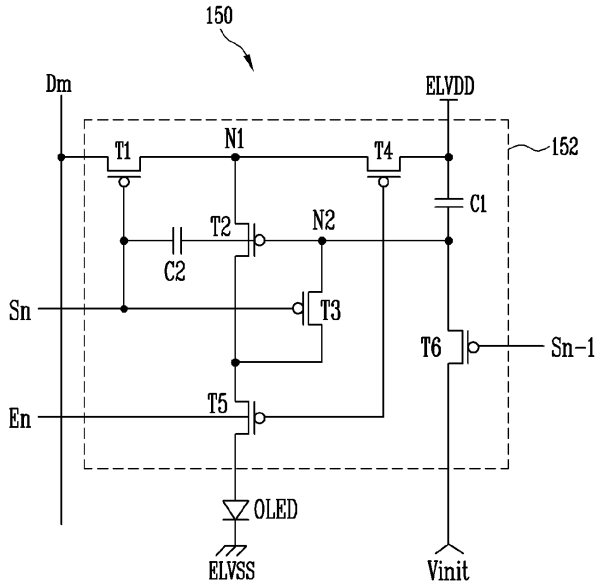
(54) Pixel and organic light emitting display including the same

(57) A pixel includes an organic light emitting diode (OLED) coupled between first and second power sources (ELVDD,ELVSS), and a pixel circuit coupled between the first power source and the OLED to control driving current supplied to the OLED. The pixel circuit includes a first transistor (T1) with a first electrode coupled to a data line (Dm), a second electrode coupled to a first node (N1), and a gate electrode coupled to a current scan line (Sn), a second transistor (T2) with a first electrode coupled to the first power source via the first node, a second electrode coupled to the OLED, and a gate electrode coupled to a second node (N2), a first capacitor (C1) coupled between the first power source and the second node, and a second capacitor (C2) coupled between the second node and the current scan line. An aperture is formed in at least one electrode of the two electrodes of the first capacitor.

FIG. 2



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Description

[0001] The present invention relates to a pixel and an organic light emitting display including the same, and more particularly, to a pixel capable of displaying an image with uniform picture quality and an organic light emitting display including the same.

[0002] An organic light emitting display displays an image using organic light emitting diodes (OLED) as self-emission elements. The organic light emitting display may be made thin and has high brightness and color purity. Thus, the organic light emitting display has attracted attention as a next generation display.

[0003] A pixel of the organic light emitting display includes an OLED and a pixel circuit. The pixel circuit supplies a driving current corresponding to a data signal to the OLED. The pixel circuit includes a switching transistor, a storage capacitor, and a driving transistor. The switching transistor transmits a data signal from a data line to the inside of a pixel to correspond to a scan signal supplied from a scan line. The storage capacitor stores the data signal. The driving transistor supplies a driving current corresponding to the data signal to the OLED.

[0004] The above-described pixel may not sufficiently display desired brightness due to voltage drop caused by a load on a panel. For example, when a black gray scale is to be displayed, the gate voltage of the driving transistor may not sufficiently increase so that contrast ratio may be reduced. Therefore, in order to prevent the contrast ratio from being reduced, a pixel structure that additionally adopts a boosting capacitor is provided.

[0005] In the pixel that adopts the boosting capacitor, charge sharing is generated between the storage capacitor and the boosting capacitor. Thus, the brightness of the pixel varies with the capacitance ratios of the storage capacitor and the boosting capacitor. Therefore, in order to prevent a brightness deviation between pixels and to display an image with uniform picture quality, it is important to maintain uniform capacitance ratios of the storage capacitor and the boosting capacitor.

[0006] However, the capacitance ratios of the storage capacitor and the boosting capacitor may change due to process deviation generated in manufacturing processes. Since the capacitances of the storage capacitor and the boosting capacitor are set to be different, the degrees of change are different. Thus, the capacitance ratios of the storage capacitor and the boosting capacitor are easily changed. Therefore, picture quality may become non-uniform.

[0007] Accordingly, aspects of the present invention provide a pixel capable of displaying an image with uniform picture quality regardless of the process deviation of the capacitors included in pixels and an organic light emitting display including the same.

[0008] According to an aspect of the present invention, there is provided a pixel includes an organic light emitting diode (OLED) coupled between a first power source and a second power source and a pixel circuit coupled between the first power source and the OLED to control driving current supplied to the OLED. The pixel circuit includes a first transistor whose first electrode is coupled to a data line, whose second electrode is coupled to a first node, and whose gate electrode is coupled to a current scan line, a second transistor whose first electrode is coupled to the first power source via the first node, whose second electrode is coupled to the OLED, and whose gate electrode is coupled to a second node, a first capacitor coupled between the first power source and the second node, and a second capacitor coupled between the second node and the current scan line. In a region where two electrodes of the first capacitor overlap each other, an aperture is formed in at least one electrode of the two electrodes of the first capacitor.

[0009] According to an aspect of the invention, the capacitance of the first capacitor is set to be larger than the capacitance of the second capacitor.

[0010] According to an aspect of the invention, the first capacitor includes a first electrode including a first conductive layer coupled to the first power source and positioned in the same layer as a gate electrode of the first and second transistors and a second electrode including a semiconductor layer coupled to the second node and positioned in the same layer as an activation layer of the first and second transistors.

[0011] According to an aspect of the invention, the semiconductor layer that constitutes the second electrode of the first capacitor includes the aperture formed in a region overlapping the first conductive layer.

[0012] According to an aspect of the invention, a plurality of the apertures are formed in at least one electrode of the two electrodes of the first capacitor.

[0013] According to an aspect of the invention, the pixel circuit includes a third transistor whose first electrode is coupled to a second electrode of the second transistor, whose second electrode is coupled to the second node, and whose gate electrode is coupled to the current scan line, a fourth transistor whose first electrode is coupled to the first power source, whose second electrode is coupled to the first node, and whose gate electrode is coupled to an emission control line, a fifth transistor whose first electrode is coupled to the second electrode of the second transistor, whose second electrode is coupled to the OLED, and whose gate electrode is coupled to the emission control line, and a sixth transistor whose first electrode is coupled to the second node, whose second electrode is coupled to an initialize power source, and whose gate electrode is coupled to a previous scan line.

[0014] According to an aspect of the present invention, an organic light emitting display includes a plurality of pixels positioned at intersections between scan lines and data lines so that each of the pixels includes an OLED coupled between a first power source and a second power source and a pixel circuit coupled between the first power source and the OLED to control driving current supplied to the OLED. The pixel circuit includes a first transistor whose first electrode is coupled to a data line,

whose second electrode is coupled to a first node, and whose gate electrode is coupled to a current scan line, a second transistor whose first electrode is coupled to the first power source via the first node, whose second electrode is coupled to the OLED, and whose gate electrode is coupled to a second node, a first capacitor coupled between the first power source and the second node, and a second capacitor coupled between the second node and the current scan line. In a region where two electrodes of the first capacitor overlap each other, an aperture is formed in at least one electrode of the two electrodes of the first capacitor.

[0015] According to an aspect of the present invention, the capacitance ratios of the first capacitor and the second capacitor in each of the pixels are set to be uniform.

[0016] According to an aspect of the present invention, the capacitance of the first capacitor is set to be larger than capacitance of the second capacitor.

[0017] In the pixel according to aspects of the present invention and the organic light emitting display including the same, an aperture is formed in a storage capacitor having larger capacitance than a boosting capacitor so that the capacitance change degrees of the boosting capacitor and the storage capacitor caused by a process deviation are controlled to be similar.

[0018] Aspects of the present invention have the capacitance ratios of the storage capacitor and the boosting capacitor maintained to be uniform so that an image with uniform picture quality may be displayed regardless of the process deviation between the capacitors included in the pixels.

[0019] According to another aspect of the invention, there is provided a pixel circuit to control a driving current supplied to an organic light emitting diode (OLED) coupled to a power source, the pixel circuit comprising a first node to be coupled to the power source, a first transistor having a first electrode to be coupled to a data line, a second electrode coupled to the first node, and a gate electrode to be coupled to a scan line, a second node, a second transistor having a first electrode coupled to the first node, a second electrode to be coupled to the OLED, and a gate electrode coupled to the second node, a first capacitor coupled to the second node and to be coupled to the power source using first and second capacitor electrodes having a shaping element at a region where the first capacitor electrode overlaps the second capacitor electrode and a second capacitor coupled to the second node and to be coupled to the scan line, wherein the shaping element shapes the first and/or second capacitor electrodes to control a capacitance ratio of the first and second capacitors to be a predetermined value.

[0020] The shaping element may comprise an opening extending through one of the first and second capacitor electrodes.

[0021] The shaping element comprises a plurality of openings extending through one of the first and second capacitor electrodes.

[0022] Additional aspects and/or advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

[0023] These and/or other aspects and advantages of the invention will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompanying drawings of which:

FIG. 1 is a block diagram schematically illustrating the structure of an organic light emitting display according to an embodiment of the present invention;
FIG. 2 is a circuit diagram illustrating an example of the pixel of FIG. 1;
FIG. 3 is a waveform chart illustrating the driving signals of the pixel of FIG. 2; and
FIG. 4 is a plan view illustrating an example of the layout of the pixel circuit of FIG. 2.

[0024] Reference will now be made in detail to the present embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below in order to explain the present invention by referring to the figures.

[0025] FIG. 1 is a block diagram schematically illustrating the structure of an organic light emitting display according to an embodiment of the present invention. Referring to FIG. 1, the organic light emitting display includes a scan driver 110, an emission control driver 120, a data driver 130, and a pixel unit 140.

[0026] The scan driver 110 sequentially supplies scan signals to scan lines S1 to Sn to correspond to control signals supplied from an external control circuit (not shown) (for example, a timing controller). Then, pixels 150 are selected by the scan signals to sequentially receive data signals from data lines D1 through Dm.

[0027] The emission control driver 120 sequentially supplies emission control signals to emission control lines E1 to En to correspond to the control signals supplied from the external control unit. The emission of the pixels 150 is controlled by the emission control signals. That is, the emission control signals control the emission time of the pixels 150. The emission control driver 120 may be omitted in accordance with the internal structure of the pixels 150.

[0028] The data driver 130 supplies the data signals to the data lines D1 to Dm to correspond to the control signals supplied from the external control circuit. The data signals supplied to the data lines D1 to Dm are supplied to the selected pixels 150 by the scan signals whenever the scan signals are supplied. Then, the pixels 150 charge voltages corresponding to the data signals and emit light with brightness components corresponding to the voltages.

[0029] The pixel unit 140 includes the plurality of pixels 150 positioned at the intersections of the emission control

lines E1 to En and the data lines D1 to Dm. Here, each of the pixels 150 includes an organic light emitting diode (not shown) that emits light with brightness corresponding to driving current corresponding to the data signal and a pixel circuit (not shown) for controlling driving current that flows through the OLED.

[0030] The pixel unit 140 receives a first power source (for example, a high potential pixel power source, ELVDD) and a second power source (for example, a low potential pixel power source, ELVSS) from the outside. The first power source ELVDD and the second power source ELVSS are transmitted to each of the pixels 150. Then, the pixels 150 emit light with the brightness components corresponding to the driving currents that flow from the first power source ELVDD to the second power source ELVSS via the OLED to correspond to the data signals.

[0031] FIG. 2 is a circuit diagram illustrating an example of the pixel 150 of FIG. 1. FIG. 3 is a waveform chart illustrating the driving signals of the pixel of FIG. 2. First, referring to FIG. 2, the pixel 150 includes an OLED coupled between the first power source ELVDD and the second power source ELVSS. A pixel circuit 152 is coupled between the first power source ELVDD and the OLED to control the driving current supplied to the OLED.

[0032] In detail, the anode electrode of the OLED is coupled to the first power source ELVDD that is a high potential pixel power source via the pixel circuit 152 and the cathode electrode of the OLED is coupled to the second power source ELVDD that is a low potential pixel power source. The OLED emits light with brightness corresponding to the driving current when the driving current is supplied from the pixel circuit 152.

[0033] The pixel circuit 152 includes first to sixth transistors T1 to T6 and first and second capacitors C1 and C2. The first transistor T1 transmits the data signal supplied from the data line Dm to the inside of the pixel 150 when the current scan signal is supplied from the current scan line Sn. That is, the first transistor T1 functions as the switching transistor of the pixel 150. The first electrode of the first transistor T1 is coupled to the data line Dm and the second electrode of the first transistor T1 is coupled to a first node N1 in the pixel 150. Here, the first electrode and the second electrode are different electrodes. For example, when the first electrode is set as a source electrode, the second electrode is set as a drain electrode. The gate electrode of the first transistor T1 is coupled to the current scan line Sn.

[0034] The second transistor T2 supplies the driving current corresponding to the data signal from the first power source ELVDD to the OLED in the emission period of the pixel 150. That is, the second transistor T2 functions as the driving transistor of the pixel 150. The first electrode of the second transistor T2 is coupled to the first power source ELVDD via the first node N1 and the fourth transistor T4. The second electrode of the second transistor T2 is coupled to the OLED via the fifth transistor T5. The gate electrode of the second transistor T2 is coupled to a second node N2 to which one electrode of the first capacitor C1 for storing the data signal is coupled.

[0035] The third transistor T3 compensates the threshold voltage of the second transistor T2 and couples the second transistor T2 in the form of a diode when the data signal is supplied to the inside of the pixel 150. Therefore, the first electrode of the third transistor T3 is coupled to the second electrode of the second transistor T2 and the second electrode of the third transistor T3 is coupled to the second node N2 to which the gate electrode of the second transistor T2 is coupled. The gate electrode of the third transistor T3 is coupled to the current scan line Sn.

[0036] The fourth transistor T4 blocks coupling between the first power source ELVDD and the second transistor T2 in the non-emission period of the pixel 150 and couples the first power source ELVDD and the second transistor T2 to each other in the emission period of the pixel 150 to form a current path through which the driving current flows. Therefore, the first electrode of the fourth transistor T4 is coupled to the first power source ELVDD and the second electrode of the fourth transistor T4 is coupled to the first node N1 to which the first electrode of the second transistor T2 is coupled. The gate electrode of the fourth transistor T4 is coupled to the emission control line En to which an emission control signal for controlling the emission period of the pixel 150 is input.

[0037] The fifth transistor T5 blocks coupling between the second transistor T2 and the OLED in the non-emission period of the pixel 150 and couples the second transistor T2 to the OLED in the emission period of the pixel 150 to form a current path through which the driving current flows. Therefore, the first electrode of the fifth transistor T5 is coupled to the second electrode of the second transistor T2 and the second electrode of the fifth transistor T5 is coupled to the anode electrode of the OLED. The gate electrode of the fifth transistor T5 is coupled to the emission control line En.

[0038] The sixth transistor T6 initializes the second node N2 in an initialize period before a data programming period so that the data signal may be smoothly supplied to the inside of the pixel 150 in the data programming period where the data signal is input to the pixel 150. Therefore, the first electrode of the sixth transistor T6 is coupled to the second node N2 and the second electrode of the sixth transistor T6 is coupled to an initialize power source Vinit. The gate electrode of the sixth transistor T6 is coupled to a previous scan line Sn-1 to which a previous scan signal was supplied.

[0039] The first capacitor C1 stores the data signal supplied to the inside of the pixel 150 in the data programming period and maintains the data signal in one frame. The first capacitor C1 is coupled between the first power source ELVDD and the second node N2. That is, the first capacitor C1 functions as the storage capacitor. The first electrode of the first capacitor C1 is coupled to the first power source ELVDD and the second electrode of the first capacitor C1 is coupled to the second node N2.

[0040] The second capacitor C2 compensates for a voltage drop caused by a load in a panel to improve a contrast ratio. The second capacitor C2 is coupled between the current scan line Sn and the second node N2. That is, the second capacitor C2 increases the voltage of the second node N2 by a coupling operation when the voltage level of the current scan signal changes, in particular, at the point of time where supply of the current scan signal is stopped to function as a boosting capacitor for compensating for the voltage drop caused by the load in the panel. Therefore, the first electrode of the second capacitor C2 is coupled to the current scan line Sn and the second electrode of the second capacitor C2 is coupled to the second node N2.

[0041] Hereinafter, the operation of the above-described pixel 150 will be described in detail with reference to the driving waveform illustrated in FIG. 3 in connection with FIG. 2. Referring to FIG. 3, in a first period t1 set as the initialize period, a previous scan signal SSn-1 in a low level is supplied through the previous scan line Sn-1. Then, the sixth transistor T6 is turned on to correspond to the previous scan signal SSn-1 in the low level. Therefore, the voltage of the initialize power source Vinit is transmitted to the second node N2. Here, the voltage of the initialize power source Vinit may be set to have a value that may initialize the pixel 150, for example, a value no more than the value of the lowermost voltage of the data signal Vdata.

[0042] Then, in a second period t2 set as the data programming period, a current scan signal SSn in a low level is supplied through the current scan line Sn. Then, the first and third transistors T1 and T3 are turned on to correspond to the current scan signal SSn in the low level. The second transistor T2 is turned on to be coupled in the form of a diode by the third transistor T3. In particular, since the second node N2 is initialized in the previous first period t1, the second transistor T2 is coupled in the form of a diode in a forward direction.

[0043] Therefore, the data signal Vdata supplied to the data line Dm is supplied to the second node N2 via the first to third transistors T1 to T3. At this time, since the second transistor T2 is coupled in the form of a diode, a voltage corresponding to a difference between the data signal Vdata and the second transistor T2 is supplied to the second node N2. The voltage supplied to the second node N2 is stored in the first capacitor C1.

[0044] Then, when supply of the current scan signal SSn is stopped and the voltage level of the current scan signal SSn is transited to a high level, the voltage of the second node N2 changes to correspond to the voltage change width of the current scan signal SSn due to the coupling operation of the second capacitor C2. At this time, since the voltage of the second node N2 changes due to charge sharing between the first capacitor C1 and the second capacitor C2, the voltage change amount of the second node N2 changes in proportion to a charge sharing value between the first and second capacitors C1 and C2 with the voltage change width of the current scan signal SSn.

[0045] Then, the emission control signal EMI supplied from the emission control line En in a third period t3 set as an emission period is transited from a high level to a low level. Then, in the third period t3, the fourth and fifth transistors T4 and T5 are turned on by the emission control signal EMI in the low level. Therefore, the driving current flows from the first power source ELVDD to the second power source ELVSS via the fourth transistor T4, the second transistor t2, the fifth transistor T5, and the OLED.

[0046] The driving current is controlled by the second transistor T2. The second transistor T2 generates the voltage supplied to the gate electrode thereof, that is, the driving current of the magnitude corresponding to the voltage of the second node N2.

[0047] At this time, since a voltage to which the threshold voltage of the second transistor T2 is reflected is stored in the first capacitor C1 in the second period t2, the threshold voltage of the second transistor T2 is compensated for in the third period t3.

[0048] Furthermore, since the voltage of the second node N2 changes in accordance with the charge sharing value between the first and second capacitors C1 and C2 together with the voltage change width of the current scan signal SSn when the supply of the current scan signal SSn stops, in order to prevent a brightness deviation among the pixels 150 and to display an image with uniform picture quality, it is important to maintain the capacitance ratios of the first capacitor C1 and the second capacitor C2 to be uniform.

[0049] As such, according to an aspect of the present invention, the first capacitor C1 is designed to have enough capacitance to stably store the data signal in the data programming period. Further, the second capacitor C2 is set to have enough capacitance to provide a voltage boosting effect. The second capacitor C2 is designed to have a smaller capacitance than a capacitance of the first capacitor C1. For example, the first capacitor C1 may be designed to have a capacitance of no less than five times the second capacitor C2. However, the relative capacitances are not specifically so limited.

[0050] Therefore, the areas and positions of the first capacitor C1 and the second capacitor C2 are changed due to the process deviation generated in manufacturing processes so that the sensitivity and degree of change of generated capacitance vary. Specifically, in the case of the second capacitor C2 designed to have the small capacitance, the capacitance change ratio caused by the process deviation is larger than the capacitance change ratio of the first capacitor C1. Therefore, the capacitance ratios of the first capacitor C1 and the second capacitor C2 are changed.

[0051] As described above, when the capacitance ratios of the first capacitor C1 and the second capacitor C2 are changed, the brightness deviation is generated among pixels 150 so that picture quality may be non-uniform. Therefore, aspects of the present invention are

designed to improve the above-described picture quality nonuniformity. There is provided a pixel 150 capable of displaying an image with uniform picture quality by forming an aperture in the first capacitor C1 whose capacitance change ratio was caused by the process deviation is smaller so that the capacitance change degree caused by the process deviation of the first capacitor C1 is controlled to be similar to or the same as the capacitance change degree of the second capacitor C2 to maintain the capacitance ratios of the first capacitor C1 and the second capacitor C2 regardless of the process deviation and an organic light emitting display including the same.

[0052] Therefore, the first capacitor C1 according to an aspect of the present invention includes the aperture formed in at least one electrode in a region where two electrodes of the first capacitor C1 overlap each other. Detailed description thereof will be described with reference to FIG. 4.

[0053] The pixel 150 described above with reference to FIGs. 2 and 3 is a pixel formed in one embodiment and the present invention is not limited to the structure of the above described pixel 150. For example, at least one of the third transistor T3 for compensating for the threshold voltage of the second transistor T2, the fourth and fifth transistors T4 and T5 for controlling the emission period, and the sixth transistor T6 for initialization may be omitted or the coupling relationships and driving waveforms of the third to sixth transistors T3 to T6 may be changed.

[0054] That is, the present invention may be applied to various kinds of pixel structures that are currently made public. In particular, the present invention may be usefully applied when the capacitance ratios of the capacitors are to be uniformly maintained in a structure where at least two capacitors (that is, the first and second capacitors C1 and C2) that affect the gate voltage of the driving transistor (that is, the second transistor T2) are provided.

[0055] FIG. 4 is a plan view illustrating an example of the layout of the pixel circuit 152 of FIG. 2. FIG. 4 illustrates a characteristic of an aspect of the present invention: the aperture 40 formed in the first capacitor C1. Illustration of partial components (for example, the OLED formed on the pixel circuit) that are not essential to describing the characteristic of the present invention will be omitted.

[0056] Referring to FIG. 4, the first to sixth transistors T1 to T6 include a semiconductor layer 10 including an activation layer, a gate electrode 20 arranged to overlap at least one region of the semiconductor layer 10 and formed of a gate metal, and source and drain electrodes 30 coupled to the activation layer and formed of source and drain metals.

[0057] The first and second capacitors C1 and C2 include a semiconductor layer 10' positioned in the same layer as the activation layer of the first to sixth transistors T1 to T6, a first conductive layer 20' positioned in the same layer as the gate electrode 20 of the first to sixth transistor T1 to T6, and a second conductive layer 30' positioned in the same layer as the source and drain electrodes 30 of the first to sixth transistors T1 to T6. Here, CH denotes a contact hole.

[0058] The above is only an example. The structures of the first to sixth transistors T1 to T6 and the first and second capacitors C1 and C2 may be changed. For example, in partial transistors among the first to sixth transistors T1 to T6, the source and/or drain electrodes are formed of the semiconductor layer 10 integrated with the active layer instead of the source and drain metals and may be integrated with the active layer of the transistor coupled thereto.

[0059] Since the active layer of the first to sixth transistors T1 to T6 is formed in the semiconductor layer 10 in the region that overlaps the gate electrode 20, for convenience sake, in FIG. 4, the positions of the first to sixth transistors T1 to T6 are remarked based on the region where the activation layer is formed.

[0060] Also, the first and second capacitors C1 and C2 are formed by overlapping at least two of the semiconductor layers 10' positioned in the same layer as the activation layer of the first to sixth transistors T1 to T6, the first conductive layer 20' positioned in the same layer as the gate electrode 20 of the first to sixth transistors T1 to T6, and the second conductive layer 30' positioned in the same layer as the source and drain electrodes 30 of the first to sixth transistors T1 to T6.

[0061] In particular, FIG. 4 illustrates an example in which most of the capacitance of the first and second capacitors C1 and C2 is formed by the semiconductor layer 10' and the first conductive layer 20'. The first capacitor C1 includes the semiconductor layer 10' and the first conductive layer 20' that almost entirely overlap each other, and the second conductive layer 30' that partially overlaps the semiconductor layer 10' and the first conductive layer 20' in the overlapping region. The second capacitor C2 includes the semiconductor layer 10' and the second conductive layer 30' that almost entirely overlap.

[0062] However, the present invention is not limited to the example described in FIG. 4. For example, in other aspects, the first and second capacitors C1 and C2 may be realized by entirely overlapping the first conductive layer 20' and the second conductive layer 30'.

[0063] While not required in all aspects, the first and second capacitors C1 and C2 may be simultaneously formed while forming the first to sixth transistors T1 to T6 as an example for improving the efficiency of manufacturing processes. Therefore, the semiconductor layer 10' of the first and second capacitors C1 and C2 may be formed in forming the activation layer of the first to sixth transistors T1 to T6 using the same material in the same layer. The first conductive layer 20' of the first and second capacitors C1 and C2 can be formed while forming the gate electrode 20 of the first to sixth transistors T1 to T6 using the same material (that is, the gate metal) in the same layer. The second conductive layer 30' of the first and second capacitors C1 and C2 is formed in forming

the source and drain electrodes 30 of the first to sixth transistors T1 to T6 using the same material (that is, the source and drain metals) in the same layer. However, aspects of the invention are not limited to the above formation methods.

[0064] According to an aspect of the present invention, the first capacitor C1 includes the aperture 40 formed in at least one electrode of two electrodes in the region where the two electrodes overlap each other. For example, when the first capacitor C1 includes a first electrode having the first conductive layer 20' coupled to the first power source ELVDD and positioned in the same layer as the gate electrode of the first to sixth transistors T1 to T6 and a second electrode having the semiconductor layer 10' coupled to the second node N2 of FIG. 2 and positioned in the same layer as the activation layer of the first to sixth transistors T1 to T6, at least one aperture 40 may be formed in at least one of the semiconductor layer 10' and the first conductive layer 20' of the first capacitor C1.

[0065] When the aperture 40 is formed in the semiconductor layer 10' having smaller process deviation than the first conductive layer 20', the position or size of the aperture 40 may be easily controlled. That is, according to an aspect of the present embodiment, the aperture 40 is formed in the region that overlaps the first conductor layer 20' of the semiconductor layer 10' that constitutes the second electrode of the first capacitor C1.

[0066] However, the present invention is not limited to the above. The aperture 40 may be formed in at least one of the semiconductor layer 10', the first conductive layer 20', and the second conductive layer 30'.

[0067] The aperture 40 controls the capacitance change ratio of the first capacitor C1 caused by the process deviation to be sensitive to a degree similar to or the same as the capacitance change ratio of the second capacitor C2 to maintain the capacitance ratios of the first capacitor C1 and the second capacitor C2 to be uniform regardless of the process deviation and to display an image with uniform picture quality. While not required in all aspects, the capacitance reduction amount of the first capacitor C1 caused by the aperture 40 may be compensated for by expanding the outline of the first capacitor C1.

[0068] Therefore, the process deviation between the first capacitor C1 and the second capacitor C2 that is previously grasped through test deposition or simulation is reflected to control the area and position of the aperture 40 and the number of apertures 40 so that the capacitance ratios of the first capacitor C1 and the second capacitor C2 of each of the pixels become uniform (that is, become the same in a predetermined error range).

[0069] In addition, while not required in all aspects, in the shown example, a plurality of apertures 40 are formed in at least one electrode of the two electrodes of the first capacitor C1 so that the capacitance change degree of the first capacitor C1 may be easily controlled. While depicted as round, it is understood that the invention is not limited to a particular shape of the aperture 40. Further, while shown as being in a central area of the electrode, it is understood that the aperture 40 can also extend to an edge of the electrode so as to form a notch in the electrode in addition to or instead of being entirely surrounded by the electrode.

[0070] As described above, according to an aspect of the present invention, the aperture 40 is formed in the storage capacitor (such as the first capacitor C1) having a larger capacitance than the boosting capacitor (such as the second capacitor C2) so that the capacitance change degrees of the boosting capacitor and the storage capacitor caused by the process deviation may be controlled to be similar to each other. Therefore, the capacitance ratios of the storage capacitor and the boosting capacitor are maintained to be uniform so that an image with uniform picture quality may be displayed regardless of the process deviation between the capacitors included in the pixels according to aspects of the invention.

[0071] Although a few embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes may be made in this embodiment without departing from the principles of the invention, the scope of which is defined in the claims.

Claims

1. A pixel comprising:

an organic light emitting diode (OLED) coupled between a first power source and a second power source; and

a pixel circuit coupled between the first power source and the OLED to control a driving current supplied to the OLED, the pixel circuit comprising:

a first transistor having a first electrode coupled to a data line, a second electrode coupled to a first node, and a gate electrode coupled to a current scan line;

a second transistor having a first electrode coupled to the first power source via the first node, a second electrode coupled to the OLED, and a gate electrode coupled to a second node;

a first capacitor coupled between the first power source and the second node using first and second capacitor electrodes; and

a second capacitor coupled between the second node and the current scan line,

wherein an aperture is formed in at least one of the first and second capacitor electrodes in a region where the first and second capacitor electrodes overlap.

2. The pixel as claimed in claim 1, wherein a capacitance of the first capacitor is larger than a capacitance of the second capacitor.

3. The pixel as claimed in claim 1 or 2, wherein:

the first capacitor electrode includes a first conductive layer coupled to the first power source and positioned on the same layer as the gate electrodes of the first and second transistors; and
the second capacitor electrode includes a semiconductor layer coupled to the second node and positioned on the same layer as an activation layer of the first and second transistors.

4. The pixel as claimed in claim 3, wherein the semiconductor layer of the second capacitor electrode comprises the aperture.

5. The pixel as claimed in any one of the preceding claims, wherein the aperture is one of a plurality of apertures formed on the at least one of the first and second capacitor electrodes.

6. The pixel as claimed in any one of the preceding claims, wherein the pixel circuit further comprises:

a third transistor having a first electrode coupled to the second electrode of the second transistor, a second electrode coupled to the second node, and a gate electrode coupled to the current scan line;
a fourth transistor having a first electrode coupled to the first power source, a second electrode coupled to the first node, and a gate electrode coupled to an emission control line;
a fifth transistor having a first electrode coupled to the second electrode of the second transistor, a second electrode coupled to the OLED, and a gate electrode coupled to the emission control line; and
a sixth transistor having a first electrode coupled to the second node, a second electrode coupled to an initialize power source, and a gate electrode coupled to a previous scan line.

7. An organic light emitting display comprising:

scan lines extending in a first direction;
data lines extending in a second direction crossing the first direction; and a plurality of pixels positioned at intersections between the scan lines and the data lines, each of the pixels comprising a pixel according to any one of the preceding claims.

8. The organic light emitting display device as claimed in claim 7, wherein capacitance ratios of the first capacitor and the second capacitor in each of the pixels are set to be uniform.

9. The organic light emitting display device as claimed in claim 8, wherein the size and/or position of the aperture in at least one of the first and second capacitor electrodes is set to control the capacitance ratios of the first and second capacitors to be a predetermined value.

10. The organic light emitting display device as claimed in any one of claims 7 to 9, wherein the outline of the first capacitor is arranged to be expanded to compensate for a capacitance reduction due to the presence of the aperture.

FIG. 1

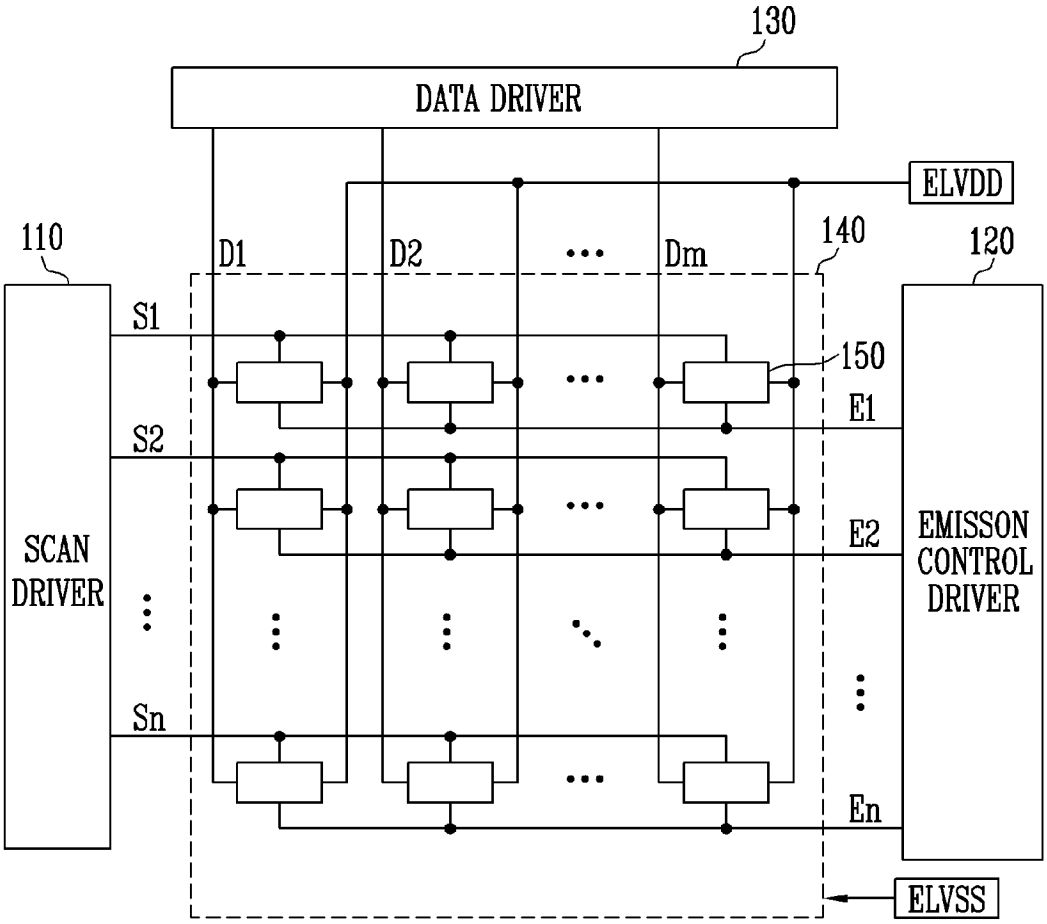

130
DATA DRIVER
ELVDD
110
D1
D2
Dm
140
120
S1
150
E1
S2
E2
SCAN DRIVER
EMISSON CONTROL DRIVER
Sn
En
ELVSS

FIG. 2

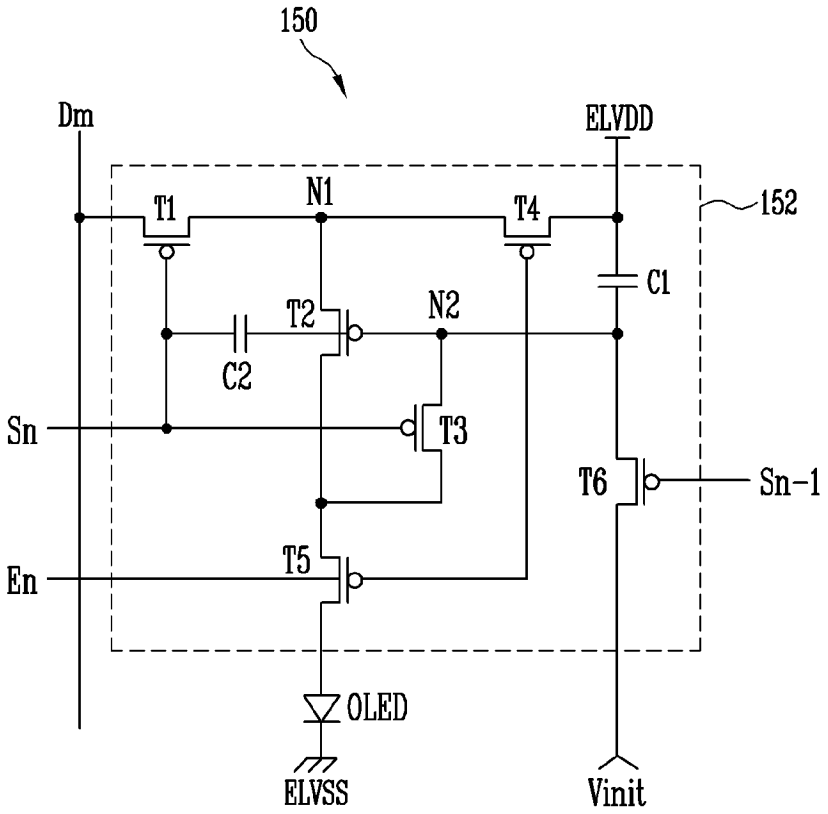

150
Dm
ELVDD
T1
N1
T4
152
C1
T2
N2
C2
Sn
T3
T6
Sn-1
T5
En
OLED
ELVSS
Vinit

FIG. 3

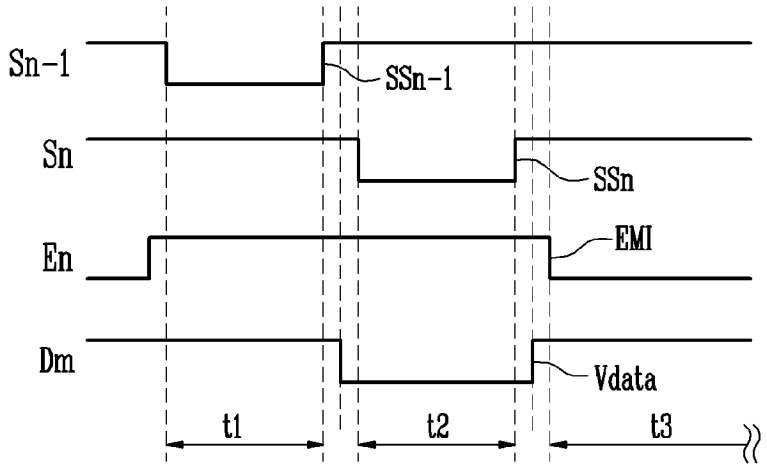
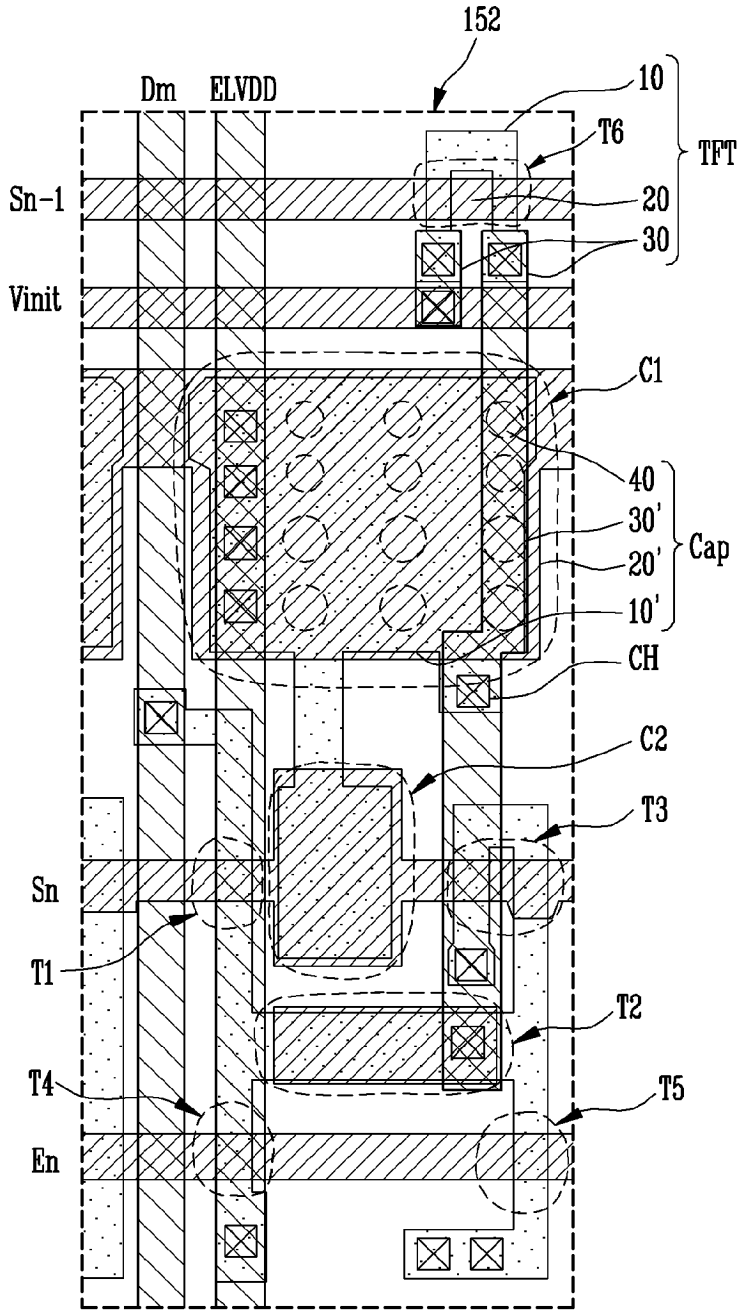

Sn-1
SSn-1
Sn
SSn
En
EMI
Dm
Vdata
t1
t2
t3

FIG. 4


152
Dm
ELVDD
10
T6
TFT
Sn-1
20
30
Vinit
C1
40
30'
Cap
20'
10'
CH
C2
T3
Sn
T1
T2
T4
T5
En

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EUROPEAN SEARCH REPORT

Application Number
EP 10 19 6578

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	US 2008/203931 A1 (KIM YANG-WAN [KR]) 28 August 2008 (2008-08-28) * paragraph [0033] - paragraph [0037] * * paragraph [0054] - paragraph [0066] * * paragraph [0073] - paragraph [0097]; figures 1,4,6-9 *	1-10	INV. G09G3/32
Y	US 3 596 039 A (EDMOND MICHAEL) 27 July 1971 (1971-07-27) * column 1, line 8 - column 1, line 46 * * column 2, line 34 - column 2, line 49; figure 1 *	1-10	
Y	US 3 597 579 A (LUMLEY ROBERT MILLER) 3 August 1971 (1971-08-03) * column 1, line 5 - column 1, line 16 * * column 2, line 30 - column 3, line 15 * * column 4, line 28 - column 4, line 39; figures 1-3,5 *	1-10	
Y	US 6 461 929 B1 (LOEBL HANS-PETER H [DE] ET AL) 8 October 2002 (2002-10-08) * column 1, line 6 - column 1, line 44 * * column 4, line 37 - column 4, line 49; figure 2 *	1-10	TECHNICAL FIELDS SEARCHED (IPC) G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	16 May 2011	Harke, Michael

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 10 19 6578

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16-05-2011

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	包括其的像素和有机发光显示器		
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申请号	EP2010196578	申请日	2010-12-22
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星移动显示器有限公司.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	BAE HAN SUNG BAEK JI WON KWAK WON KYU		
发明人	BAE, HAN-SUNG BAEK, JI-WON KWAK, WON-KYU		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G2300/0814 G09G2300/0819 G09G2300/0852 G09G2310/0251 G09G2320/043 H01L27/3265		
优先权	1020100023343 2010-03-16 KR		
外部链接	Espacenet		

摘要(译)

像素包括耦合在第一和第二电源（ELVDD，ELVSS）之间的有机发光二极管（OLED），以及耦合在第一电源和OLED之间的像素电路，以控制提供给OLED的驱动电流。像素电路包括第一晶体管（T1），其具有耦合到数据线（Dm）的第一电极，耦合到第一节点（N1）的第二电极，以及耦合到电流扫描线（Sn）的栅电极，第二晶体管（T2），其中第一电极经由第一节点耦合到第一电源，第二电极耦合到OLED，栅电极耦合到第二节点（N2），第一电容器（C1）耦合到第二节点之间第一电源和第二节点，以及耦合在第二节点和当前扫描线之间的第二电容器（C2）。孔形成在第一电容器的两个电极的至少一个电极中。

FIG. 2