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(54) **Pixel and organic light emitting display device using the same**

(57) A pixel for compensating for the threshold voltage of a drive transistor and the voltage drop of a first power source is provided. The pixel includes an organic light emitting diode; a driving transistor coupled between a first power source and the organic light emitting diode for controlling the current supplied to the organic light emitting diode; an emission control transistor coupled between a first electrode of the driving transistor and the first power source and configured to be turned off when

a high light emission control signal is applied; a switching transistor coupled between a gate electrode of the driving transistor and a data line and configured to be turned on when a low scan signal is applied; a first capacitor coupled between the gate electrode of the driving transistor and the first electrode of the driving transistor; and a second capacitor coupled between the first electrode of the driving transistor and the first power source.

EP 2 136 353 A1

Description

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a pixel and an organic light emitting display device using the same.

2. Discussion of Related Art

[0002] In recent years, various flat panel display devices have been developed with reduced weight and volume as compared to cathode ray tubes. Types of flat panel display devices include liquid crystal display devices, field emission display devices, plasma display devices, and organic light emitting display devices, among others.

[0003] Of these flat panel display devices, the organic light emitting display device displays an image by using organic light emitting diodes, which generate light by recombining electrons and holes. Organic light emitting display devices are advantageous in that they have rapid response times and may be driven with relatively low power consumption.

[0004] FIG. 1 is a circuit diagram illustrating a pixel of a conventional organic light emitting display device.

[0005] Referring to FIG. 1, the pixel 4 of the conventional organic light emitting display device includes an organic light emitting diode (OLED), and a pixel circuit 2 coupled to a data line (Dm) and a scan line (Sn) to control the organic light emitting diode (OLED).

[0006] An anode electrode of the organic light emitting diode (OLED) is coupled to the pixel circuit 2, and a cathode electrode of the organic light emitting diode (OLED) is coupled to a second power source (ELVSS). The organic light emitting diode (OLED) generates light with a luminance corresponding to an electric current supplied from the pixel circuit 2.

[0007] The pixel circuit 2 controls an amount of current supplied to the organic light emitting diode (OLED) in accordance with a data signal supplied to the data line (Dm) when a scan signal is supplied to the scan line (Sn). For this purpose, the pixel circuit 2 includes a second transistor (M2') (e.g., a driving transistor) coupled between a first power source (ELVDD) and the organic light emitting diode (OLED); a first transistor (M1') (e.g., a switching transistor) coupled between a gate electrode of the second transistor (M2') and the data line (Dm), and having a gate electrode coupled to the scan line (Sn); and a storage capacitor (Cst) coupled between the gate electrode and a first electrode of the second transistor (M2').

[0008] The gate electrode of the first transistor (M1') is coupled to the scan line (Sn), and a first electrode of the first transistor (M1') is coupled to the data line (Dm). A second electrode of the first transistor (M1') is coupled to one terminal of the storage capacitor (Cst). Here, the

first electrode of the first transistor (M1') is either a source electrode or a drain electrode, and the second electrode of the first transistor (M1') is the other of the source electrode and the drain electrode. For example, when the first electrode is the source electrode, the second electrode is the drain electrode. The first transistor (M1') is turned on when a scan signal is supplied from the scan line (Sn), and supplies a data signal from the data line (Dm) to the storage capacitor (Cst). In this case, the storage capacitor (Cst) is charged with a voltage corresponding to the data signal.

[0009] The gate electrode of the second transistor (M2') is coupled to one terminal of the storage capacitor (Cst), and the first electrode of the second transistor (M2') is coupled to the other terminal of the storage capacitor (Cst) and the first power source (ELVDD). A second electrode of the second transistor (M2') is coupled to the anode electrode of the organic light emitting diode (OLED). The second transistor (M2') controls the amount of current in accordance with a voltage value stored in the storage capacitor (Cst), the current flowing from the first power source (ELVDD) to the second power source (ELVSS) via the organic light emitting diode (OLED). In this case, the organic light emitting diode (OLED) generates light in accordance with the amount of current supplied from the second transistor (M2').

[0010] However, the pixel 4 of the conventional organic light emitting display device has difficulties displaying images with uniform luminance. More particularly, a threshold voltage of the second transistor (M2') in each of the plurality of the pixels 4 may have different threshold voltage levels due to manufacturing process variances. When the threshold voltages of the drive transistors have different threshold voltage levels as described above, different luminances may be generated in the organic light emitting diodes (OLEDs), even though data signals corresponding to a same gray level are supplied to the plurality of the pixels 4.

[0011] Also, in a conventional organic light emitting display device, a voltage from the first power source (ELVDD) may be inconsistently applied due to voltage drops of the voltage from the first power source (ELVDD), depending on the positions of the pixels 4 in the display device. When the voltage from the first power source (ELVDD) varies according to the positions of the pixels 4 as described above, it is very difficult to display an image with a uniform or desired luminance.

SUMMARY OF THE INVENTION

[0012] Accordingly, an aspect of an embodiment according to the present invention is to provide a pixel capable of compensating for the threshold voltage of a driving transistor and the voltage drop of a first power source, and an organic light emitting display device using the same.

[0013] One aspect of an embodiment according to the present invention provides a pixel including: an organic

light emitting diode; a second transistor coupled between a first power source and the organic light emitting diode, the second transistor for controlling an amount of current supplied from the first power source to the organic light emitting diode; a third transistor coupled between a first electrode of the second transistor and the first power source, the third transistor configured to turn off when a light emission control signal is applied to a light emission control line coupled to a gate electrode of the third transistor; a first transistor coupled between a gate electrode of the second transistor and a data line, the first transistor configured to turn on when a scan signal is applied to a scan line coupled to a gate electrode of the first transistor; a first capacitor coupled between the gate electrode of the second transistor and the first electrode of the second transistor; and a second capacitor coupled between the first electrode of the second transistor and the first power source.

[0014] In this case, the second capacitor may have a greater capacitance than the first capacitor. Also, the second capacitor may have a capacitance 2 to 10 times a capacitance of the first capacitor.

[0015] Another aspect of an embodiment according to the present invention provides an organic light emitting display device including: a scan driver for applying scan signals to a plurality of scan lines and for applying light emission control signals to a plurality of light emission control lines; a data driver for supplying a reset power voltage and for applying data signals to a plurality of data lines; and a plurality of pixels arranged at crossing regions of the plurality of data lines and the plurality of scan lines, wherein each of the plurality of pixels includes: an organic light emitting diode; a second transistor coupled between a first power source and the organic light emitting diode, the second transistor for controlling an amount of current supplied from the first power source to the organic light emitting diode; a third transistor coupled between a first electrode of the second transistor and the first power source, the third transistor configured to turn off when a light emission control signal is applied to a light emission control line coupled to a gate electrode of the third transistor; a first transistor coupled between a gate electrode of the second transistor and a data line, the first transistor configured to turn on when a scan signal is applied to a scan line coupled to a gate electrode of the first transistor; a first capacitor coupled between the gate electrode of the second transistor and the first electrode of the second transistor; and a second capacitor coupled between the first electrode of the second transistor and the first power source.

[0016] In this case, the scan driver may be configured to apply a light emission control signal to an i^{th} light emission control line during a second portion and a third portion of a period in which a scan signal is being applied to a corresponding i^{th} scan line. Here, the scan driver may be configured to stop the application of the light emission control signal after the application of the scan signal is stopped. Also, the data driver may be configured to sup-

ply the reset power voltage to the data lines during a first portion and the second portion of the period, and may be configured to apply the data signal during the third portion of the period. In addition, the reset power voltage may be higher than the data signal. Furthermore, the reset power voltage may be lower than a voltage of the first power source.

[0017] Yet another aspect of an embodiment according to the present invention provides a method of driving an organic light emitting display, the method comprising the steps of: applying a light emission control signal to an i^{th} light emission control line during a second portion and a third portion of a period in which a scan signal is being applied to a corresponding i^{th} scan line pixel; stopping the application of the light emission control signal after the application of the scan signal is stopped; supplying the reset power voltage to the data lines during a first portion and the second portion of the period; and applying the data signal to the data lines during the third portion of the period.

[0018] As described above, a pixel according to aspects of embodiments of the present invention and an organic light emitting display device using the same may be useful to display an image with uniform luminance by compensating for the threshold voltage of the driving transistor and the voltage drop of the first power source.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The accompanying drawings, together with the specification, illustrate exemplary embodiments of the present invention, and, together with the description, serve to explain the principles of the present invention.

[0020] FIG. 1 is a circuit diagram illustrating a conventional pixel.

[0021] FIG. 2 is a schematic block diagram illustrating an organic light emitting display device according to one exemplary embodiment of the present invention.

[0022] FIG. 3 is a waveform diagram illustrating a driving waveform supplied from a scan driver and a data driver as shown in FIG. 2.

[0023] FIG. 4 is a circuit diagram illustrating a pixel according to one exemplary embodiment of the present invention as shown in FIG. 2.

[0024] FIG. 5 is a waveform diagram illustrating a driving waveform of the pixel as shown in FIG. 4.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0025] Hereinafter, certain exemplary embodiments according to the present invention will be described with reference to the accompanying drawings. Here, when a first element is described as being coupled to a second element, the first element may be directly coupled to the second element or may be indirectly coupled to the second element via one or more additional elements. Further, some of the elements that are not essential to the

complete understanding of the invention are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0026] FIG. 2 is a schematic block diagram illustrating an organic light emitting display device according to one exemplary embodiment of the present invention.

[0027] Referring to FIG. 2, the organic light emitting display device according to one exemplary embodiment of the present invention includes a display unit 130 including pixels 140 arranged at crossing regions of scan lines (S1 to Sn) and data lines (D1 to Dm); a scan driver 110 driving the scan lines (S1 to Sn) and light emission control lines (E1 to En); a data driver 120 driving the data lines (D1 to Dm); and a timing controller 150 controlling the scan driver 110 and the data driver 120.

[0028] The scan driver 110 receives a scan drive control signal (SCS) from the timing controller 150, and sequentially supplies a scan signal to the scan lines (S1 to Sn), as shown in FIG. 3. Also, the scan driver 110 sequentially supplies a light emission control signal to the light emission control lines (E1 to En). Here, the light emission control signal supplied to an i^{th} light emission control line (Ei) is turned on after a corresponding scan signal to the i^{th} scan line (Si) is turned on, and turned off after the corresponding scan signal to the i^{th} scan line (Si) is turned off. In this embodiment, a scan signal has a LOW level voltage when it is applied, and a light emission control signal has a HIGH level voltage when it is applied. In other embodiments, the scan signal and the emission control signal may be at either high or low levels when they are applied, depending on the particular embodiment, without being limited to any particular embodiment.

[0029] The data driver 120 receives a data drive control signal (DCS) and, in some embodiments, additional data (Data) from the timing controller 150. The data driver 120 generates a data signal (DS), and supplies the generated data signal (DS) to the data lines (D1 to Dm). Here, the data driver 120 supplies a reset power source (Vint) (e.g., the reset power source (Vint) described with respect to FIG. 3) to the data lines (D1 to Dm) during a portion of a period when the scan signal is on. The data driver 120 supplies a data signal (DS) to the data lines (D1 to Dm) during a remaining portion of the period when the scan signal is on. A voltage of the reset power source (Vint) is set to a higher voltage level than that of the data signal (DS), and set to a lower voltage level than that of the first power source (ELVDD).

[0030] The timing controller 150 generates a data drive control signal (DCS) and a scan drive control signal (SCS) in accordance with external synchronization signals. The data drive control signal (DCS) generated in the timing controller 150 is supplied to the data driver 120, and the scan drive control signal (SCS) is supplied to the scan driver 110. The timing controller 150 may also supply external data (Data) to the data driver 120.

[0031] The display unit 130 receives a first power source (ELVDD) and a second power source (ELVSS)

from the outside, and supplies the first power source (ELVDD) and second power source (ELVSS) to each of the pixels 140. Each of the pixels 140 generates light corresponding to the data signal (DS).

[0032] FIG. 4 is a diagram illustrating a pixel according to one exemplary embodiment of the present invention, for example, the embodiment illustrated in FIG. 2. For convenience, FIG. 4 shows a pixel coupled to an n^{th} scan line (Sn) and an m^{th} data line (Dm).

[0033] Referring to FIG. 4, the pixel 140 according to one exemplary embodiment of the present invention includes an organic light emitting diode (OLED); and a pixel circuit 142 coupled to the data line (Dm) and the scan line (Sn) to control the current supplied to the organic light emitting diode (OLED).

[0034] An anode electrode of the organic light emitting diode (OLED) is coupled to the pixel circuit 142, and a cathode electrode of the organic light emitting diode (OLED) is coupled to a second power source (ELVSS). The organic light emitting diode (OLED) generates light with a luminance in accordance with the amount of current supplied from the pixel circuit 142. Here, a voltage of the second power source (ELVSS) is set to a lower voltage level than that of the first power source (ELVDD).

[0035] The pixel circuit 142 controls the amount of current supplied to the organic light emitting diode (OLED) by utilizing the data signal supplied to the data line (Dm) in accordance with a scan signal supplied to the scan line (Sn). For this purpose, the pixel circuit 142 includes first, second, and third transistors (M1, M2, and M3), a first capacitor (C1) and a second capacitor (C2).

[0036] A first electrode of the first transistor (M1) (e.g., a switching transistor) is coupled to the data line (Dm), and a second electrode of the first transistor (M1) is coupled to a first node (N1), which is also coupled to a gate electrode of the second transistor (M2) (e.g., a driving transistor). A gate electrode of the first transistor (M1) is coupled to the scan line (Sn). The first transistor (M1) is turned on in accordance with a scan signal supplied to the scan line (Sn), and supplies a reset power source or a data signal from the data line (Dm) to the first node (N1).

[0037] A first electrode of the second transistor (M2) is coupled to a second node (N2), which is also coupled to a second electrode of the third transistor (M3) (e.g., an emission control transistor), and a second electrode of the second transistor (M2) is coupled to an anode electrode of the organic light emitting diode (OLED). The gate electrode of the second transistor (M2) is coupled to the first node (N1). The second transistor (M2) applies an electric current to the organic light emitting diode (OLED), the electric current corresponding to the voltage applied to the first node (N1).

[0038] A first electrode of the third transistor (M3) is coupled to the first power source (ELVDD), and the second electrode of the third transistor (M3) is coupled to the second node (N2). A gate electrode of the third transistor (M3) is coupled to the light emission control line (En). The third transistor (M3) is turned off when a high

light emission control signal is supplied to the light emission control line (En), and turned on when a low light emission control signal is supplied to the light emission control line (En).

[0039] The first capacitor (C1) is coupled between the first node (N1) and the second node (N2). The first capacitor (C1) stores a voltage corresponding to the data signal and the threshold voltage of the second transistor (M2).

[0040] The second capacitor (C2) is arranged between the first power source (ELVDD) and the second node (N2). The second capacitor (C2) stably maintains a voltage of the second node (N2). For this purpose, the second capacitor (C2) has a greater capacitance than the first capacitor (C1). For example, the second capacitor (C2) may have a capacitance 2 to 10 times the capacitance of the first capacitor (C1), or more.

[0041] An operation of the pixel 140 will be described in detail in connection with a waveform as shown in FIG. 5. First, when a low scan signal is supplied to the scan line (Sn), the first transistor (M1) is turned on. A reset power source (Vint) is supplied to the data line (Dm) during a first portion (T1) of a period when the low scan signal is supplied to the scan line (Sn).

[0042] During the first portion (T1), the reset power source (Vint) is supplied to the first node (N1) via the first transistor (M1). Since the third transistor (M3) is turned on during the first portion (T1), the second node (N2) maintains a voltage of the first power source (ELVDD). The second transistor (M2) is turned on since the reset power source (Vint) is set to a lower voltage level than the first power source (ELVDD).

[0043] During a second portion (T2) of the period when the low scan signal is supplied to the scan line (Sn), the third transistor (M3) is turned off since a high light emission control signal is supplied to the light emission control line (En). When the third transistor (M3) is turned off, the second transistor (M2) is consequently turned off. When the second transistor (M2) is turned off, a voltage corresponding to the threshold voltage of the second transistor (M2) (e.g., a voltage difference between the second node (N2) and the first node (N1)) is charged in the first capacitor (C1) during the second portion (T2) of the period.

[0044] During a third portion (T3) of the period when the scan signal is supplied to the scan line (Sn), a data signal (DS) is supplied to the data line (Dm). During the third portion (T3), the data signal (DS) supplied to the data line (Dm) is supplied to the first node (N1) via the first transistor (M1). When the data signal (DS) is supplied to the first node (N1), the voltage of the first node (N1) drops from the reset power source (Vint) to the voltage of the data signal (DS). In this case, the second node (N2) maintains an applied voltage during the third portion (T3) of the period. More particularly, the second capacitor (C2) has a greater capacitance than the first capacitor (C1). Therefore, the voltage at the second node (N2) may be maintained during the third portion (T3), even though the voltage at the first node (N1) is changed. Thus, a

voltage corresponding to the data signal adjusted by the threshold voltage of the second transistor (M2) is charged in the first capacitor (C1).

[0045] Then, the first transistor (M1) is turned off when the scan signal supplied to the scan line (Sn) is turned high. When the first transistor (M1) is turned off, the first node (N1) is floated. Then, when the supply of the light emission control signal to the light emission control line (En) is turned low, the third transistor (M3) is turned on. When the third transistor (M3) is turned on, the second transistor (M2) supplies an electric current to the organic light emitting diode (OLED) in accordance with the voltage applied to the first node (N1).

[0046] When the third transistor (M3) is turned on, the voltage of the first power source (ELVDD) is supplied to the second node (N2). In this case, the voltage of the floating first node (N1) is also increased to correspond with the increase in the voltage of the second node (N2). In other words, the voltage charged in the first capacitor (C1) is maintained when the third transistor (M3) is turned on.

[0047] Also, since the first node (N1) is floating when the voltage from the first power source (ELVDD) is supplied to the second node (N2), voltage variances of the voltage from the first power source (ELVDD) due to the position at which the pixels 140 are located may be compensated for. In other words, the voltage of the first node (N1) is increased corresponding to the increase in the voltage of the second node (N2), and therefore it is possible to display an image with a desired luminance regardless of the voltage drop of the voltage from the first power source (ELVDD).

Claims

1. A pixel (140), comprising:

- an organic light emitting diode (OLED);
- a second transistor (M2) coupled between a first power source (ELVDD) and the organic light emitting diode (OLED), the second transistor (M2) for controlling an amount of current supplied from the first power source (ELVDD) to the organic light emitting diode (OLED);
- a third transistor (M3) coupled between a first electrode of the second transistor (M2) and the first power source (ELVDD), the third transistor (M3) configured to turn off when a light emission control signal is applied to a light emission control line (E1, ..., En) coupled to a gate electrode of the third transistor (M3);
- a first transistor (M1) coupled between a gate electrode of the second transistor (M2) and a data line (D1, ..., Dm), the first transistor (M1) configured to turn on when a scan signal is applied to a scan line (S1, ..., Sn) coupled to a gate electrode of the first transistor (M1);

- a first capacitor (C1) coupled between the gate electrode of the second transistor (M2) and the first electrode of the second transistor (M2); and a second capacitor (C2) coupled between the first electrode of the second transistor (M2) and the first power source (ELVDD).
2. The pixel (140) according to claim 1, wherein the second capacitor (C2) has a greater capacitance than the first capacitor (C1).
 3. The pixel (140) according to claim 2, wherein the second capacitor (C2) has a capacitance 2 to 10 times a capacitance of the first capacitor (C1).
 4. An organic light emitting display device, comprising:
 - a scan driver (110) for applying scan signals to a plurality of scan lines (S1, ..., Sn) and for applying light emission control signals to a plurality of light emission control lines (E1, ..., En);
 - a data driver (120) for supplying a reset power voltage and for applying data signals (DS) to a plurality of data lines (D1, ..., Dm); and
 - a plurality of pixels (140) according to any one of claims 1 to 3 arranged at crossing regions of the plurality of data lines (D1, ..., Dm) and the plurality of scan lines (S1, ..., Sn).
 5. The organic light emitting display device according to claim 4, wherein the scan driver (110) is configured to apply a light emission control signal to an i^{th} light emission control line (Ei) during a second portion (T2) and a third portion (T3) of a period in which a scan signal is being applied to a corresponding i^{th} scan line (Si).
 6. The organic light emitting display device according to claim 5, wherein the scan driver (110) is configured to stop the application of the light emission control signal after the application of the scan signal is stopped.
 7. The organic light emitting display device according to claim 5 or 6, wherein the data driver (120) is configured to supply the reset power voltage to the data lines (D1, ..., Dm) during a first portion (T1) and the second portion (T2) of the period, and wherein the data driver (120) is configured to apply the data signal (DS) during the third portion (T3) of the period.
 8. The organic light emitting display device according to any one of claims 4 to 7, wherein the reset power voltage is higher than the data signal (DS).
 9. The organic light emitting display device according to any one of claims 4 to 8, wherein the reset power voltage is lower than a voltage of the first power source (ELVDD).
 10. A method of driving an organic light emitting display device according to any one of claims 4 to 9, the method comprising the steps of:
 - applying a light emission control signal to an i^{th} light emission control line (Ei) during a second portion (T2) and a third portion (T3) of a period in which a scan signal is being applied to a corresponding i^{th} scan line (Si);
 - stopping the application of the light emission control signal after the application of the scan signal is stopped;
 - supplying the reset power voltage to the data lines (D1, ..., Dm) during a first portion (T1) and the second portion (T2) of the period; and
 - applying the data signal (DS) to the data lines (D1, ..., Dm) during the third portion (T3) of the period.

FIG. 1
(PRIOR ART)

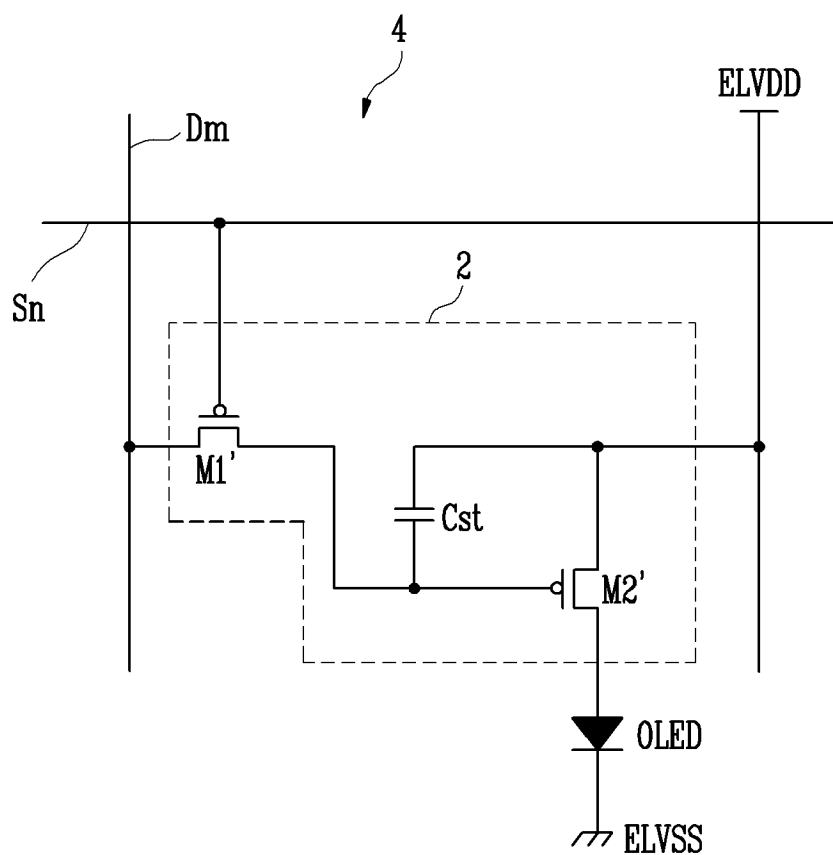


FIG. 2

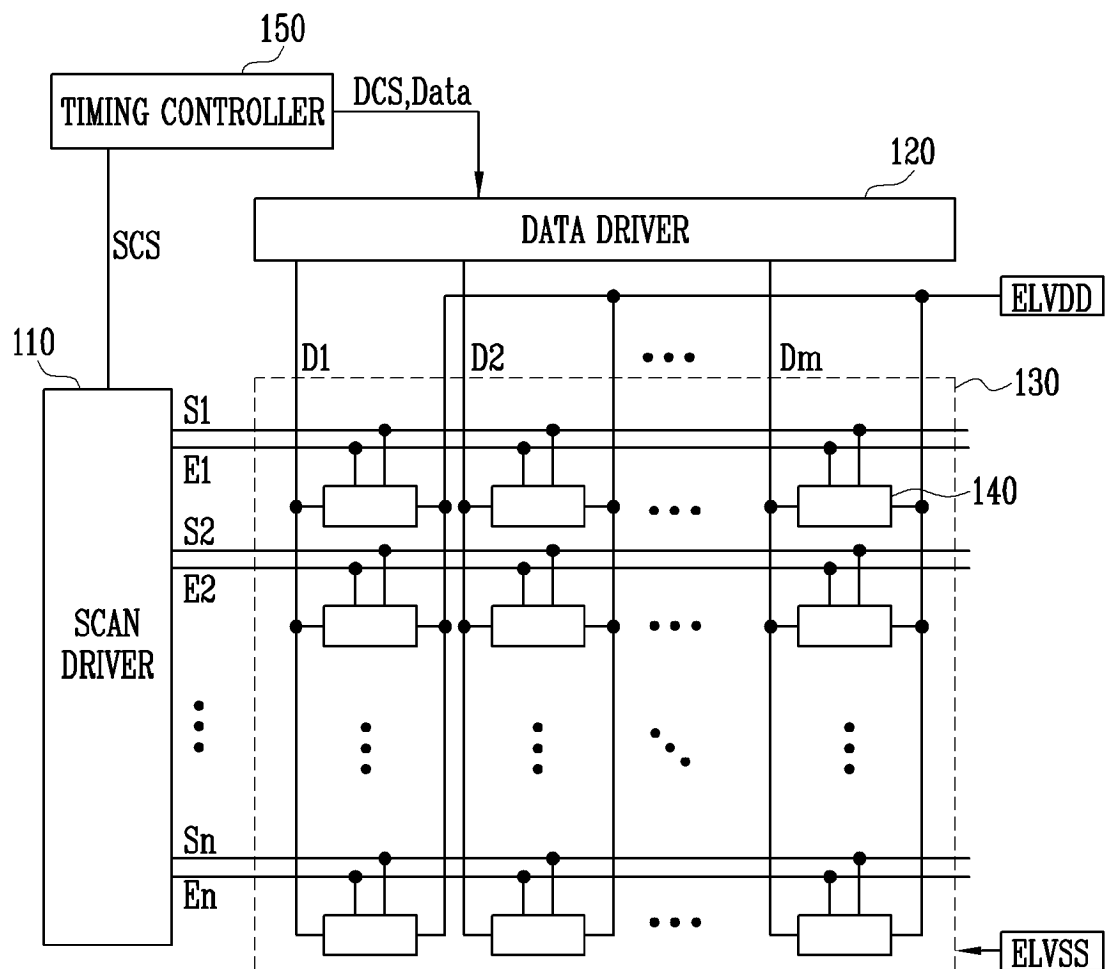


FIG. 3

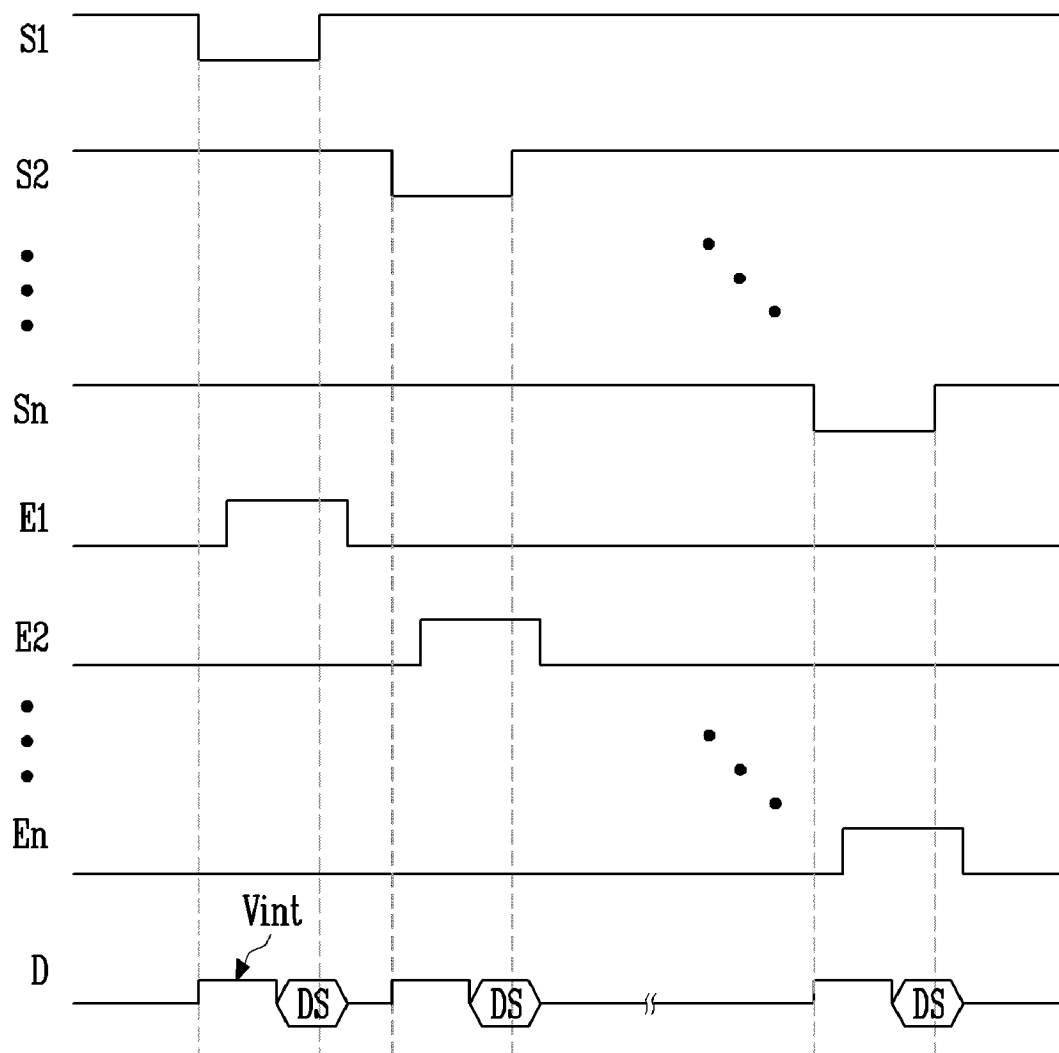


FIG. 4

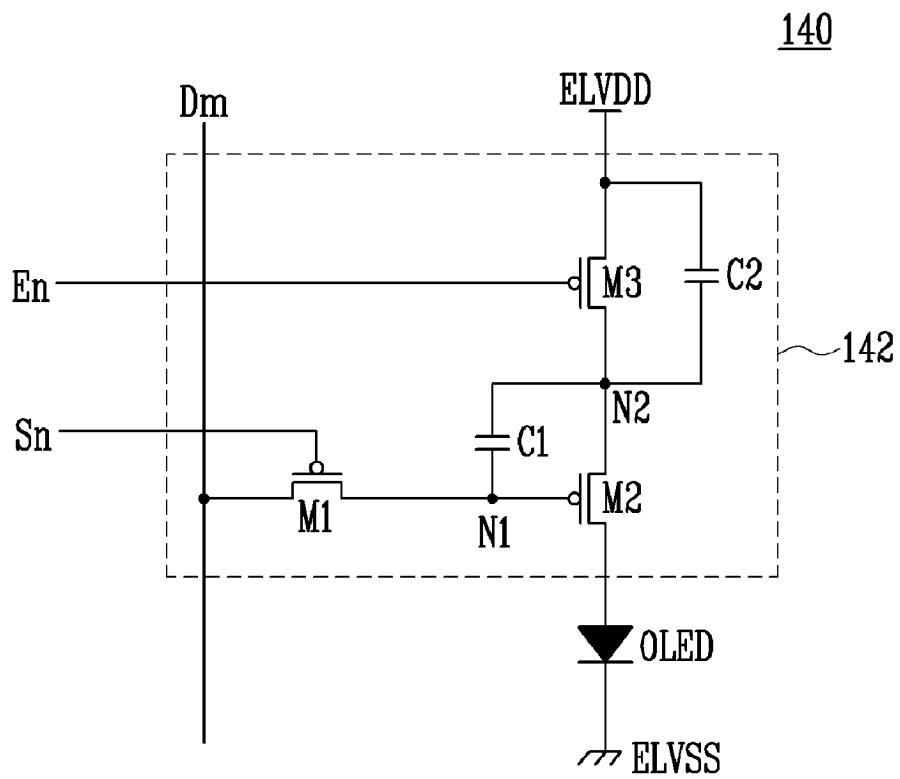
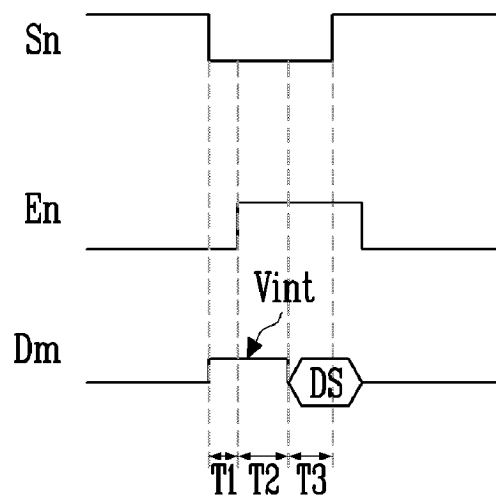


FIG. 5





EUROPEAN SEARCH REPORT

Application Number
EP 09 16 2891

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2005/105031 A1 (SHIH PO-SHENG [TW] ET AL) 19 May 2005 (2005-05-19) * paragraphs [0045] - [0049]; figures 3a-b *	1-10	INV. G09G3/32
A	US 2007/115225 A1 (UCHINO KATSUhide [JP] ET AL) 24 May 2007 (2007-05-24) * paragraphs [0133], [0134]; figures 12a-b *	1-10	
A	US 2005/206590 A1 (SASAKI ISAO [JP] ET AL) 22 September 2005 (2005-09-22) * paragraphs [0089] - [0099], [0128] - [0133]; figures 7,8,25 *	1-10	
P,A	EP 1 947 633 A (SAMSUNG SDI CO LTD [KR]) 23 July 2008 (2008-07-23) * paragraphs [0083] - [0126]; figures 8-12 *	1-10	
			TECHNICAL FIELDS SEARCHED (IPC)
			G09G
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
The Hague		11 August 2009	Pichon, Jean-Michel
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>			

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**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 09 16 2891

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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11-08-2009

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005105031 A1	19-05-2005	JP 2005148704 A TW 286654 B	09-06-2005 11-09-2007
US 2007115225 A1	24-05-2007	EP 1785979 A2 KR 20070051748 A	16-05-2007 18-05-2007
US 2005206590 A1	22-09-2005	WO 03075256 A1	12-09-2003
EP 1947633 A	23-07-2008	CN 101226719 A JP 2008176272 A KR 100833760 B1 US 2008170010 A1	23-07-2008 31-07-2008 29-05-2008 17-07-2008

专利名称(译)	使用其的像素和有机发光显示装置		
公开(公告)号	EP2136353A1	公开(公告)日	2009-12-23
申请号	EP2009162891	申请日	2009-06-17
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星移动显示器有限公司.		
当前申请(专利权)人(译)	三星移动显示器有限公司.		
[标]发明人	KIM YANG WAN		
发明人	KIM, YANG-WAN		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G2300/0819 G09G2300/0852 G09G2300/0861 G09G2320/043		
优先权	1020080056812 2008-06-17 KR		
外部链接	Espacenet		

摘要(译)

提供用于补偿驱动晶体管的阈值电压和第一电源的电压降的像素。像素包括有机发光二极管;驱动晶体管,耦合在第一电源和有机发光二极管之间,用于控制提供给有机发光二极管的电流;发光控制晶体管,其耦合在驱动晶体管的第一电极和第一电源之间,并且被配置为当施加高发光控制信号时关断;开关晶体管,其耦合在驱动晶体管的栅极和数据线之间,并且被配置为在施加低扫描信号时导通;第一电容器,耦合在驱动晶体管的栅极和驱动晶体管的第一电极之间;第二电容器耦合在驱动晶体管的第一电极和第一电源之间。

FIG. 1
(PRIOR ART)

