(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 040 248 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
25.03.2009 Bulletin 2009/13

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(21) Application number: **07124161.6**

(22) Date of filing: **28.12.2007**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC MT NL PL PT RO SE SI SK TR
Designated Extension States:
AL BA HR MK RS

(30) Priority: **20.09.2007 KR 20070096141**

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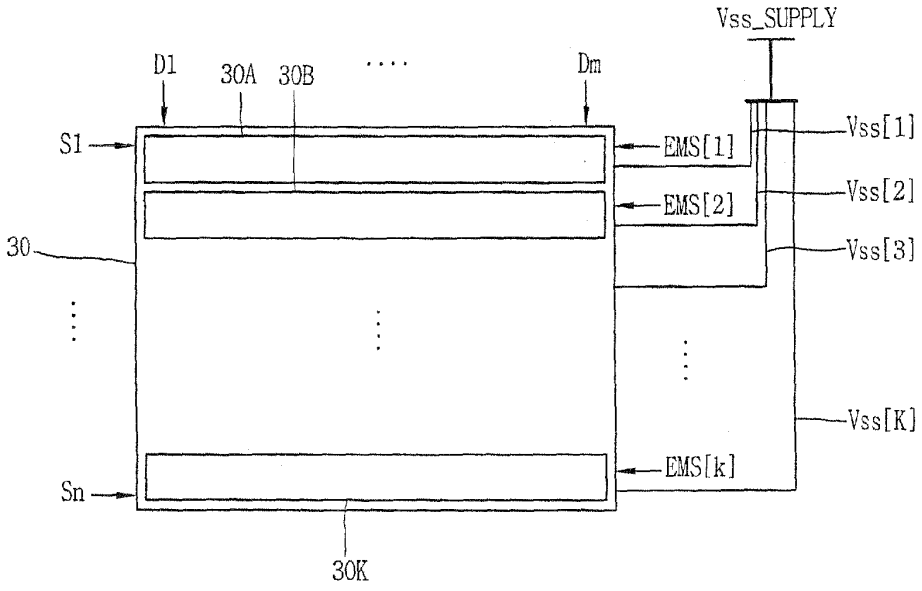
(54) Pixel driving method and apparatus for organic light emitting device

(57) A pixel driving method and apparatus for an organic light emitting device, capable of preventing a driving voltage of a driving transistor inside a pixel from dropping by charging a data voltage to a storage capacitor, in a state that supply of a power supply voltage to an organic light emitting diode (OLED) is cut-off, and then by starting to supply the power supply voltage to the OLED, and capable of sufficiently obtaining a data voltage emission period. The method comprises: defining a display panel of the organic light emitting device into a plurality of display panel regions in a horizontal direction such that a plurality of adjacent scan lines can be included; making pixels inside the plurality of display panel regions share one lower power supply voltage among a plurality of lower power supply voltages supplied from a lower power supply voltage supply terminal by being diverged; and determining a data voltage programming period and a data voltage emission period in one frame period according to each of the display panel regions.

FIG. 9



EP 2 040 248 A2

Description

RELATED APPLICATION

[0001] The present disclosure relates to subject matter contained in priority Korean Application No. 10-2007-096141, filed on September 20, 2007, which is herein expressly incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present disclosure relates to a method for driving a panel for an organic light emitting device (OLED), and more particularly, to a pixel driving method and apparatus for an OLED capable of preventing a non-uniform brightness due to different levels of a common voltage at each position inside a panel, and capable of preventing a flicker phenomenon due to a short data voltage emission period at a large panel.

2. Description of the Background Art

[0003] Generally, an organic light emitting device (OLED)is one of plane-type light emitting devices. According to the OLED, an organic light emitting layer is disposed between two electrodes facing each other, and when a voltage is applied between the two electrodes, electrons injected from one electrode are combined with holes injected from another electrode at the organic light emitting layer. By the coupling, molecules on the light emitting layer are excited to be in a ground level, and thereby light is emitted. The OLED is being spotlighted as the next generation display apparatus owing to an excellent viewing characteristic, a light weight, a thin thickness, and a low voltage driving.

[0004] The OLED is classified into an Active-Matrix type OLED and a Passive-Matrix type OLED according to whether a switching device provided at a unit pixel of a panel exists.

[0005] FIG. 1A is a block diagram showing an OLED in accordance with the conventional art.

[0006] As shown, the conventional OLED comprises a scan driving unit 10 for sequentially outputting scan signals to drive scan lines (S1~Sn) on a display panel 30 under control of a signal controller (not shown); a data driving unit 20 for outputting data voltages to data lines (D1~Dm) on the display panel 30; and a display panel 30 having a plurality of pixels (PXs) at intersections between the scan lines (S1~Sn) and the data lines (D1~Dm).

[0007] The pixels of the active-matrix type OLED are classified into voltage writing pixels, current writing pixels, and digital driving pixels according to a driving method.

[0008] FIG. 1 B is a circuit for driving pixels (PXs) on the display panel 30 of FIG. 1A.

[0009] As shown, the pixel circuit includes a switching transistor (T11) transmitting data voltages (Data) supplied through the data lines (D) to a storage capacitor (C11) by being driven by the scan signals supplied through the scan lines(S); a storage capacitor (C11) charging the data voltage (Data) by being connected between a gate terminal of a driving transistor (T12) and a lower power supply voltage terminal(Vss); a driving transistor (T12) for supplying a driving current corresponding to the data voltage (Data) charged to the storage capacitor (C11) to an organic light emitting diode (OLED11); and an OLED 11 emitting light having a brightness corresponding to the driving current by having an anode connected to an upper power supply voltage terminal (ELVDD) and having a cathode connected to a drain of the driving transistor (T12) Here, the transistors T11 and T12 are implemented as N-channel type thin film transistors (TFTs).

[0010] The operation of the conventional circuit for driving pixels will be explained with reference to FIGS. 2 and 3.

[0011] In each frame period, positive scan signals (Scan [1]~ Scan [N]) are sequentially supplied from the scan driving unit 10 to the scan lines (S1~Sn) on the display panel 30, thereby driving the pixels (PXs) on a corresponding scan line (horizontal line).FIG. 1B is an exemplary view showing one of a plurality of pixels (including a driving circuit) connected to an optional scan line.

[0012] The switching transistor (T11) is turned ON by a corresponding scan signal among the scan signals (Scan [1] ~ Scan [N]). And, the data voltage (Data) supplied from the data driving unit 20 through a corresponding data line among the data lines (D1~Dm) is charged to the storage capacitor (C11) through the switching transistor (T11), and is maintained for a data voltage emission period.

[0013] The driving transistor (T12) is turned ON by the data voltage (Data) charged to the storage capacitor (C11), and a certain amount of driving current corresponding to the data voltage (Data) flows through the organic light emitting diode (OLED 11). Accordingly, the OLED 11 emits light with the corresponding brightness.

[0014] Here, the driving current (I_{OLED}) flowing on the OLED 11 is expressed as the following equation 1.

【Equation 1】

$$I_{OLED} = \frac{1}{2} \cdot \frac{W}{L} \cdot C_{SINx} \cdot \{V_{DATA} - V_{SS} - V_{TH}\}^2$$

[0015] Here, the "L" denotes a channel length of the driving transistor (T12), the "W" denotes a channel width of the driving transistor (T12), the "C_{SINx}" is a capacitor component of a gate insulator, the "V_{TH}" denotes a threshold voltage, and the "V_{DATA}" is a data voltage charged to the storage capacitor (C11).

[0016] FIG. 3 is a schematic view showing an array structure of each power supply voltage supply line on the display panel 30.

[0017] As shown, a lower power supply voltage (Vss) supply line 32 is arrayed on an array portion 31 with a mesh structure so as to minimize a resistance. On each outer periphery of the array portion 31 and the display panel 30, other lower power supply voltage supply lines 33 and 34 having a wider width are arrayed, thereby smoothly supplying the lower power supply voltage (Vss).

[0018] As shown in FIG. 2, an upper power supply voltage (ELVDD) of a certain level (i.e., 15V) is continuously supplied to the anode of the OLED 11 for one frame period.

[0019] In a data voltage programming period, when data voltages are charged to the storage capacitors (C11) of the pixels (PXs) inside the display panel 30, about1㎂ of current flows through the OLED 11 and the driving transistor (T12). The current flows to the lower power supply voltage supply lines 33 and 34 through the lower power supply voltage supply line 32. Accordingly, the current flowing in the display panel 30 has a total amount corresponding to several~several tens of mA, and thus a potential on the lower power supply voltage supply line 32 is increased. The increased lower power supply voltage (Vss') is expressed as the following equation 2.

【Equation 2】

$$V_{SS}' = V_{SS} + I_{OLED} \cdot R_{line}$$

[0020] Here, the driving current (I_{OLED}) of the OLED 11, and the resistance (R_{line})of the lower power supply voltage supply line 32 have different values according to each position inside the display panel 30.

[0021] As the potential on the lower power supply voltage supply line 32 is increased, a driving voltage of the driving transistor (T12) inside the pixel is lowered, thereby lowering a brightness of the OLED 11. As the lower power supply voltage (Vss) changes to the Vss', the driving current (I_{OLED}) of the OLED 11 is lowered, which is expressed as the following equation 3.

【Equation 3】

$$I_{OLED} = \frac{1}{2} \cdot \frac{W}{L} C_{SINx} \{V_{DATA} - V_{SS}' - V_{TH}\}^2 \leq \frac{1}{2} \cdot \frac{W}{L} C_{SINx} \{V_{DATA} - V_{SS} - V_{TH}\}^2$$

[0022] The conventional organic light emitting device has the following problems. At the time of programming the data voltages, the potential on the lower power supply voltage supply line 32 is increased due to the organic light emitting diode (OLED) of each pixel, the lower power supply voltage supply line 32 having a mesh structure, and the current flowing therethrough. Accordingly, the driving voltage of the driving transistor inside the pixel is lowered, thereby lowering a brightness of the organic light emitting diode.

[0023] Furthermore, since the brightness is lowered at the respective pixels by different levels, a non-uniform brightness is entirely caused.

SUMMARY OF THE INVENTION

[0024] Therefore, an object of the present disclosure is to provide a pixel driving method and apparatus for an organic

light emitting device, capable of preventing a driving voltage of a driving transistor inside a pixel from dropping by charging a data voltage to a storage capacitor, in a state that supply of a power supply voltage to an organic light emitting diode (OLED) is cut-off, and then by starting to supply the power supply voltage to the OLED.

[0025] Another object of the present disclosure is to provide a pixel driving method and apparatus for an organic light emitting device, capable of sufficiently obtaining a data voltage programming period and a lighting duration of an organic light emitting diode regardless of a size of a display panel.

[0026] To achieve these and other advantages and in accordance with the purpose of the present disclosure, as embodied and broadly described herein, there is provided a pixel driving method for an organic light emitting device, comprising: in a data voltage programming period, charging a data voltage supplied through a data line to a storage capacitor, by cutting off supply of a power supply voltage to an organic light emitting diode (OLED) and by driving a switching transistor; and in a data voltage emission period, supplying the power supply voltage to the OLED, and making the OLED emit light by the data voltage charged to the storage capacitor.

[0027] According to another aspect of the present invention, there is provided a pixel driving method for an organic light emitting device, comprising: defining a display panel of the organic light emitting device into a plurality of display panel regions in a horizontal direction such that a plurality of adjacent scan lines can be included; making pixels inside the plurality of display panel regions share one lower power supply voltage among a plurality of lower power supply voltages supplied by being diverged; and determining a data voltage programming period and a data voltage emission period in one frame period according to each of the display panel regions.

[0028] To achieve these and other advantages and in accordance with the purpose of the present disclosure, as embodied and broadly described herein, there is also provided a pixel driving apparatus for an organic light emitting device, comprising a display panel, wherein the display panel defines a plurality of display panel regions in a horizontal direction such that a plurality of adjacent scan lines can be included; makes pixels inside the plurality of display panel regions share one lower power supply voltage among a plurality of lower power supply voltages supplied by being diverged; and determines a data voltage programming period and a data voltage emission period in one frame period according to each of the display panel regions.

[0029] The foregoing and other objects, features, aspects and advantages of the present disclosure will become more apparent from the following detailed description of the present disclosure when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

In the drawings:

[0031]

FIG. 1A is a block diagram showing an organic light emitting device (OLED) in accordance with the conventional art;
FIG. 1 B is a pixel circuit in accordance with the conventional art;
FIG. 2 is a waveform of FIGS. 1A and 1B;
FIG. 3 is a schematic view showing an arrangement structure of power supply voltage supply lines on a display panel;
FIG. 4A is a view of a pixel circuit to which a pixel driving method according to the present invention is applied;
FIG. 4B is a view of another pixel circuit to which the pixel driving method according to the present invention is applied;
FIG. 5 is a waveform showing the pixel circuit of FIG. 4A;
FIG. 6A is a view of still another pixel circuit to which the pixel driving method according to the present is applied;
FIG. 6B is a view of yet still another pixel circuit to which the pixel driving method according to the present is applied;
FIG. 7 is a waveform showing the pixel circuit of FIG. 6A;
FIG. 8 is a view of further yet still another pixel circuit to which the pixel driving method according to the present is applied;
FIG. 9 is an exemplary view of a display panel of an organic light emitting device (OLED) according to the present invention;
FIGS. 10A and 10B are exemplary views showing each lower power supply voltage; and
FIGS.11A to 11E are timing diagrams showing a display panel driving according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0032] Reference will now be made in detail to the preferred embodiments of the present disclosure, examples of which are illustrated in the accompanying drawings.

[0033] FIG. 4A is a view of a pixel circuit to which a pixel driving method according to the present invention is applied, which is implemented as an N-channel thin film transistor (TFT).

[0034] As shown, the pixel circuit according to the present invention includes a switching transistor (T41) driven by scan signals, for transmitting data voltages (Data) supplied through data lines to a storage capacitor C41, in a state that supply of an upper power supply voltage (ELVDD) is cut-off; a storage capacitor (C41)connected between a gate terminal of a driving transistor (T42) and a lower power supply voltage terminal (Vss), for charging the data voltage (Data), in a state that supply of the upper power supply voltage (ELVDD) is cut-off; a driving transistor (T42) for supplying a driving current corresponding to the data voltage (Data) charged to the storage capacitor (C41) to an organic light emitting diode (OLED 41), in a state that the upper power supply voltage (ELVDD) is supplied; and an organic light emitting diode (OLED 41) having an anode connected to the upper power supply voltage (ELVDD) and a cathode connected to a drain of the driving transistor (T42), for emitting light with a brightness corresponding to the driving current.

[0035] Hereinafter, a pixel driving method on the pixel circuit will be explained in more detail with reference to FIG. 5.

[0036] The ELVDD of a 'high' level is not supplied to the anode of the OLED 41 during all of one frame period. Rather, the ELVDD of a 'low' level (OV) is supplied during the data voltage programming period (P1) of said one frame period.

[0037] In this state, positive scan signals (Scan[1]~Scan[N])are sequentially supplied to the respective horizontal lines, thereby driving the pixels on the horizontal lines.

[0038] FIG. 4A is an exemplary view showing one of a plurality of pixels (including a driving circuit) arrayed on an optional horizontal line.

[0039] Here, the data voltage (data) supplied trough the corresponding data line is charged to the storage capacitor (C41) through the switching transistor (T41), and is maintained for a data voltage emission period (P2).

[0040] The data voltage (Data) of a 'high' level charged to the storage capacitor (C41) is supplied to the gate terminal of the driving transistor (T42), thereby turning on the driving transistor (T42). However, since supply of the upper power supply voltage (ELVDD) to the anode of the OLED 41 is cut-off, a voltage between drain and source terminals (Vds) becomes 'OV'.

[0041] Accordingly, a current does not flow to the lower power supply voltage (Vss) supply line 32 through the OLED 41 and the driving transistor (T42). That is, the driving current (I_{OLED}) of the OLED 41 becomes '0'.

[0042] Since the current does not flow to the lower power supply voltage supply line 32 through the OLED 41, a voltage of a lower power supply voltage node (A) is maintained as the original level (0V) regardless of a resistance of the lower power supply voltage supply line 32.

[0043] Accordingly, the data voltage (Data) having a desired level can be charged to the storage capacitor (C41).

[0044] Next, when the data voltage programming operation (scanning operation) is completed, the switching transistor (T41) is turned-off and thereby a gate node (B) is in an electrical floating status.

[0045] Next, in the data voltage emission period (P2), the ELVDD of a 'high' level is supplied to the anode of the OLED 41.

[0046] Since the gate terminal of the driving transistor (T42) is being supplied with the data voltage (Data) stored at the storage capacitor (C41), the driving transistor (T42) is turned-ON.

[0047] Here, since the current flows to the lower power supply voltage supply line 32 through the OLED 41 and the driving transistor (T42), the OLED 41 emits light.

[0048] As all the pixels on the display panel 30 are operated, a large amount of current flows to the lower power supply voltage supply line 32. Accordingly, the voltage (Vss) of the lower power supply voltage node (A) is increased to Vss' according to the Ohm' law (V=IR).

[0049] Here, since the switching transistor (T41) is turned-OFF, the gate node (B) is in an electrical floating status. Therefore, when the voltage (Vss) of the lower power supply voltage node (A) is increased to the Vss', the voltage of the gate node (B)is also increased by a coupling with the storage capacitor (C41).

[0050] The voltage (V_B)of the gate node (B) is expressed as the following equation 4.

【Equation 4】

$$V_B = Data.[N] + Vss' - Vss$$

[0051] A current flows to the lower power supply voltage node (A) through the OLED 41 and the driving transistor (T42) by the supplied ELVDD in the data voltage emission period (P2), and thus the voltage of the lower power supply voltage node (A) changes from the Vss to the Vss'. However, since the voltage of the gate node (B) also changes, a

voltage (Vgs) between the gate and source terminals of the driving transistor (T42) does not change.

[0052] Accordingly, the driving current (I_{OLED}) of the OLED 41 is not influenced by the voltage change of the lower power supply voltage node (A), but is influenced by the data voltage stored in the storage capacitor (C41).

[0053] The driving current (I_{OLED})of the OLED 41 is expressed as the following equation 5.

【Equation 5】

$$I_{OLED} = \frac{1}{2} \cdot \frac{W}{L} \cdot C_{SIN} \cdot \{V_B - Vss' - V_{TH}\}^2 = \frac{1}{2} \cdot \frac{W}{L} \cdot C_{SIN} \cdot \{Data.[N] - Vss - V_{TH}\}^2$$

[0054] The following table shows each change of the voltages of the nodes (A) and (B), and the driving current (I_{OLED}) of the OLED 41 in the data voltage programming period (P1) and the data voltage emission period (P2).

Operation	**Period 1**	**Period 2**
Node 'A'	*Vss*	*Vss'* (potential rising)
Node 'B'	*Data*.[*N*]	*Data*.[*N*]+*Vss'*-*Vss*
I_{OLED}	0	$k\,(Data[N]\text{-}Vss\text{-}V_{TH})^2$

[0055] In the data voltage programming period (P1) of one frame period, so as to prevent a current from flowing to the lower power supply voltage (Vss) supply line 32 through the OLED 41 and the driving transistor (T42), supply of the ELVDD may be cut-off by various methods.

[0056] FIG. 4B shows a method for cutting-off supply of the ELVDD by using a switching transistor.

[0057] More concretely, a drain and a source of the switching transistor (T43) are respectively connected between the cathode of the OLED 41 and the drain of the driving transistor (T42). And, the switching transistor (T43) is turned-OFF as a switching control signal (EMS) of a 'low' level is outputted to the gate of the switching transistor (T43) by a signal controller (not shown) in the data voltage programming period (P1).

[0058] FIG. 6A is a view of a pixel circuit to which the pixel driving method according to the present is applied, which shows a P-channel type Thin Film Transistor (TFT).

[0059] As shown, the P-channel type TFT includes a switching transistor (T61) driven by a scan signal, for transmitting a data voltage(Data) supplied through a data line to a storage capacitor (C61), in a state that supply of a lower power supply voltage (Vss) is cut-off; a storage capacitor (C61) connected between a gate terminal of a driving transistor (T62) and an upper power supply voltage terminal(ELVDD), for charging the data voltage (Data) in a state that supply of the lower power supply voltage (Vss) is cut-off; a driving transistor (T62) for supplying a driving current corresponding to the data voltage (Data) charged to the storage capacitor (C61) to an organic light emitting diode (OLED61), in a state that the lower power supply voltage (Vss) is supplied; and an OLED 61 having an anode connected to a source terminal of the driving transistor (T62) and having a cathode connected to the lower power supply voltage (Vss), for emitting light having a brightness corresponding to the driving current.

[0060] Hereinafter, a pixel driving method on the pixel circuit will be explained in more detail with reference to FIG. 7.

[0061] The lower power supply voltage (Vss) of a 'low' level is not supplied to the cathode of the OLED 61 during all of one frame period. Rather, the Vss of a 'high' level is supplied during the data voltage programming period (P1) of said one frame period.

[0062] In this state, negative scan signals (Scan[1]~Scan[N])are sequentially supplied to the respective horizontal lines, thereby driving the pixels on the horizontal lines. FIG. 6A is an exemplary view showing one of a plurality of pixels (including a driving circuit) arrayed on an optional horizontal line.

[0063] Here, the data voltage (data) supplied trough the corresponding data line is charged to the storage capacitor (C61) through the switching transistor (T61), and is maintained for the data voltage emission period (P2).

[0064] The data voltage (Data) of a 'low' level charged to the storage capacitor (C61) is supplied to the gate terminal of the driving transistor (T62), thereby turning on the driving transistor (T62). However, since supply of the lower power supply voltage (Vss) to the cathode of the OLED 61 is cut-off, a voltage between drain and source terminals (Vds) becomes 'OV'.

[0065] Accordingly, the current does not flow to the OLED 61 through the upper power supply voltage (ELVDD) supply

line. That is, the driving current (I_{OLED})of the OLED 61 becomes '0'.

[0066] Since the current does not flow to the OLED 61 through the upper power supply voltage (ELVDD) supply line, a voltage of an upper power supply voltage node (A) is maintained as the original level (15V) during the data voltage programming period (P1) regardless of a resistance of the upper power supply voltage (ELVDD) supply line.

[0067] Accordingly, the data voltage (Data) having a desired level can be charged to the storage capacitor (C61).

[0068] Next, when the data voltage programming operation (scanning operation) is completed, the switching transistor (T61) is turned-off and thereby the gate node (B) is in an electrical floating status.

[0069] Next, in the data voltage emission period (P2), the low power supply voltage (Vss) of a 'low' level (OV) is supplied to the cathode of the OLED 61.

[0070] Since the gate terminal of the driving transistor (T62) is being supplied with the data voltage (Data) stored at the storage capacitor (C61), the driving transistor (T62) is turned-ON.

[0071] Here, since the upper power supply voltage (ELVDD) is supplied to the OLED 61 and the driving transistor (T62), the OLED 61 emits light.

[0072] As all the pixels on the display panel 30 are operated, a large amount of current flows to upper power supply voltage supply line. Accordingly, the voltage (VDD) of the upper power supply voltage node (A) is decreased to VDD' according to the Ohm' law (V=IR).

[0073] Here, since the switching transistor (T61) is turned-OFF, the gate node (B) is in an electrical floating status. Therefore, when the voltage (VDD) of the upper power supply voltage node (A) is lowered to the VDD', the voltage of the gate node (B) is also lowered by a coupling with the storage capacitor (C61). The voltage (V_B)of the gate node (B) is expressed as the following equation 6.

【Equation 6】

$$V_B = Data[N] + VDD' - VDD$$

[0074] A current flows from the upper power supply voltage node (A) to the OLED 41 through the driving transistor (T62) by the supplied lower power supply voltage (Vss) in the data voltage emission period (P2), and thus the voltage of the upper power supply voltage node (A) changes from the VDD to the VDD'. However, since the voltage of the gate node (B) also changes, a voltage (Vgs) between the gate and source terminals of the driving transistor (T62) does not change. Accordingly, the driving current (I_{OLED})of the OLED 61 is not influenced by the voltage change of the upper power supply voltage node (A), but is influenced by the data voltage stored in the storage capacitor (C61). The driving current (I_{OLED})of the OLED 61 is expressed as the following equation 7.

【Equation 7】

$$I_{OLED} = \frac{1}{2}\frac{W}{L} C_{SBK} \{V_B - VDD' - V_{TH}\}^2 = \frac{1}{2}\frac{W}{L} C_{SBK} \{V_{DATA}[N] - VDD - V_{TH}\}^2$$

[0075] The following table shows each change of the voltages of the nodes (A) and (B), and the driving current (I_{OLED}) of the OLED 61 in the data voltage programming period (P1) and the data voltage emission period (P2).

Operation	**Period 1**	**Period 2**
Node 'A'	*VDD*	*VDD'(potential drop)*
Node 'B'	*Data*.[*N*]	*Data*.[*N*]+*VDD'-VDD*
I_{OLED}	0	k (*Data*[*N*]-*VDD*-V_{TH})^2

[0076] In order to prevent a current from flowing to the lower power supply voltage (Vss) supply line 32 through the OLED 61 and the driving transistor (T62) in the data voltage programming period (P1) for one frame period, supply of the UPPER POWER SUPPLY VOLTAGE (ELVDD)may be cut-off by various methods.

[0077] FIG. 6B shows a method for cutting-off supply of the ELVDD by using a switching transistor in the same manner

as FIG. 4B.

[0078] More concretely, a drain and a source of the switching transistor (T63) are respectively connected between the anode of the OLED 61 and the drain of the driving transistor (T62). And, the switching transistor (T63) is turned-OFF as a switching control signal (EMS) of a 'high' level is outputted to the gate of the switching transistor (T63) by a signal controller (not shown) in the data voltage programming period (P1).

[0079] FIG. 8 is a view of an anode contact type-pixel circuit in which the driving transistor comes in contact with the anode of the organic light emitting diode, which shows an N-channel TFT in the same manner as FIG. 6A.

[0080] As shown, the pixel circuit according to the present invention includes a switching transistor (T81) driven by a scan signal, for transmitting a data voltage (Data) supplied through a data line to a storage capacitor C81, in a state that supply of an upper power supply voltage (ELVDD) is cut-off; a storage capacitor (C81)connected between a gate terminal and a source terminal of a driving transistor (T82), for charging the data voltage (Data), in a state that supply of the upper power supply voltage (ELVDD) is cut-off; a driving transistor (T82) for supplying a driving current corresponding to the data voltage (Data) charged to the storage capacitor (C81) to an organic light emitting diode (OLED 81), in a state that supply of the upper power supply voltage (ELVDD) is cut-off; and an organic light emitting diode (OLED 81) having an anode connected to the source terminal of the driving transistor (T82) and a cathode connected to a lower power supply voltage terminal (Vss), for emitting light with a brightness corresponding to the driving current.

[0081] Hereinafter, a pixel driving method at the pixel circuit will be explained in more detail with reference to FIG. 5.

[0082] The ELVDD of a 'high' level is not supplied to the drain of the driving transistor (T82) during all of one frame period. Rather, the ELVDD of a 'low' level is supplied during the data voltage programming period (P1) of said one frame period.

[0083] In this state, positive scan signals (Scan[1]~Scan[N]) are sequentially supplied to the respective horizontal lines, thereby driving the pixels on the horizontal lines.

[0084] FIG. 8 is an exemplary view showing one of a plurality of pixels (including a driving circuit) arrayed on an optional horizontal line.

[0085] Here, the data voltage (data) supplied trough the corresponding data line is charged to the storage capacitor (C81) through the switching transistor (T81), and is maintained for the data voltage emission period (P2).

[0086] The data voltage (Data) of a 'high' level charged to the storage capacitor (C81) is supplied to the gate terminal_ of the driving transistor (T82), thereby turning on the driving transistor (T82). However, since supply of the upper power supply voltage (ELVDD) to the drain of the driving transistor (T82) is cut-off, a voltage between the drain and source terminals (Vds) becomes 'OV'.

[0087] Accordingly, the current does not flow to the lower power supply voltage (Vss) supply line 32 through the OLED 81 and the driving transistor (T82). That is, the driving current (I_{OLED}) of the OLED 81 becomes '0'.

[0088] Since the current does not flow to the lower power supply voltage supply line 32 through the OLED 81, a voltage of an anode node (A) is maintained as the original level (Vss) regardless of a resistance of the lower power supply voltage supply line 32.

[0089] Accordingly, the data voltage (Data) having a desired level can be charged to the storage capacitor (C81).

[0090] Next, when the data voltage programming operation (scanning operation) is completed, the switching transistor (T81) is turned-off and thereby the gate node (B) is in an electrical floating status.

[0091] Next, in the data voltage emission period (P2), the ELVDD of a 'high' level is supplied to the driving transistor (T82) in the data voltage emission period (P2).

[0092] Since the gate terminal of the driving transistor (T82) is being supplied with the data voltage (Data) stored at the storage capacitor (C81), the driving transistor (T82) is turned-ON.

[0093] Here, since the current flows to the lower power supply voltage supply line 32 through the OLED 81 and the driving transistor (T82), the OLED 81 emits light.

[0094] As all the pixels on the display panel 30 are operated, a large amount of current flow-S to the lower power supply voltage supply line 32. Accordingly, the voltage (Vss) of the anode node(A) is increased to V_{OLED} according to the Ohm' law (V=IR).

[0095] Here, since the switching transistor (T81) is turned-OFF, the gate node (B) is in an electrical floating status. Therefore, when the voltage (Vss) of the anode node (A) is increased to the V_{OLED}, the voltage of the gate node (B)is also increased by a coupling with the storage capacitor (C81).

[0096] The voltage (V_B)of the gate node (B) is expressed as the following equation 8.

【Equation 8】

$$V_B = Data[N] + V_{OLED} - V_{SS}$$

[0097] A current flows to the lower power supply voltage supply line 32 through the OLED 81 and the driving transistor (T82) by the supplied ELVDD in the data voltage emission period (P2), and thus the voltage of the anode node (A) changes from the Vss to the V_{OLED}. However, since the voltage of the gate node (B) also changes, a voltage (Vgs) between the gate and source terminals of the driving transistor (T82) does not change.

[0098] Accordingly, the driving current (I_{OLED}) of the OLED 81 is not influenced by the voltage change of the anode node (A), but is influenced by the data voltage stored in the storage capacitor (C81).

[0099] The driving current (I_{OLED}) of the OLED 81 is expressed as the following equation 9.

【Equation 9】

$$I_{OLED} = \frac{1}{2}\frac{W}{L} C_{SBM} \{Data[N] + V_{OLED} - V_{SS} - V_{OLED} - V_{TH}\}^2$$
$$= \frac{1}{2}\frac{W}{L} C_{SBM} \{Data[N] - V_{SS} - V_{TH}\}^2$$

[0100] The following table shows each change of the voltages of the nodes (A) and (B), and the driving current (I_{OLED}) of the OLED 81 in the data voltage programming period (P1) and the data voltage emission period (P2).

Operation	**Period 1**	**Period** 2
Node 'A'	*Vss*	V_{OLED}
Node 'B'	*Data*.[*N*]	*Data*.[*N*]+V_{OLED}-*Vss*
I_{OLED}	0	*k* (*Data*.[*N*]-*Vss*-V_{TH})^2

[0101] In the same manner as the aforementioned embodiment of the present invention, the data voltage programming period (P1) in one frame period is set, during which the data voltage is charged to the storage capacitor in a state that supply of the power supply voltage to the organic light emitting diode (OLED) is cut-off. Accordingly, a driving voltage of the driving transistor is prevented from dropping.

[0102] Herein, the following problem may be caused. Since time corresponding to the other period except the data voltage programming period (P1) in one frame period is determined as the data voltage emission period (P2), that is, a lighting duration of the OLED, an entire lighting duration of the organic light emitting diode is reduced.

[0103] When the preferred embodiment of the present invention is applied to a small type display panel 30 having relatively a small number of scan lines, the lighting duration of the organic light emitting diode can be obtained without being influenced by the data voltage programming period (P1)

[0104] On the contrary, when the preferred embodiment of the present invention is applied to a large type display panel 30 having relatively a large number of scan lines (i.e., 768 scan lines), the data voltage programming period (P1) becomes relatively longer. Accordingly, there is a difficulty in sufficiently obtaining the lighting duration of the organic light emitting diode, and thus a brightness flicker phenomenon occurs.

[0105] To solve the problem, in another embodiment of the present invention, the data voltage programming period and the lighting duration of the organic light emitting diode are sufficiently obtained regardless of the size of the display panel.

[0106] Hereinafter, the another embodiment of the present invention will be explained in more detail.

[0107] FIG. 9 is an exemplary view of a display panel of an organic light emitting device (OLED) according to the present invention.

[0108] Referring to FIG. 9, the display panel 30 is defined as a plurality of display panel regions (30A~30K) in a horizontal direction so that a plurality of adjacent scan lines can be included. Then, pixels inside the plurality of display panel regions (30A~30K) share one lower power supply voltage among a plurality of lower power supply voltages (Vss [1]~Vss[K]) supplied from the lower power supply voltage supply terminals (Vss_supply) by being diverged. And, a data voltage programming period and a data voltage emission period are determined in one frame period according to each of the display panel regions (30A~30K).

[0109] The operation of the pixel driving apparatus for an organic light emitting device according to another embodiment of the present invention will be explained with reference to FIGS. 10 and 11.

[0110] Scan lines (S1~Sn) and data lines (D1~Dm) are arrayed on the display panel 30 in the same manner as a general display panel.

[0111] The display panel 30 is defined as a plurality of display panel regions (30A~30K) in a horizontal direction so that a plurality of adjacent scan lines can be included. Then, a plurality of lower power supply voltages (Vss[1]~Vss[K]) are supplied to the display panel regions (30A~30K), respectively.

[0112] For instance, a large display panel 30 having 760 scan lines (S1~Sn) is defined as 10 display panel regions (30A~30K).Here, each of the ten display panel regions (30A~30K) is implemented to include 76 scan lines [(S1~S76), (S77~S152)···(S685~S760)].

[0113] For reference, the display panel 30 of the present invention has to be provided with 768 scan lines (S1~Sn) since it is implemented as an XGA-type (1024 × 768). However, the display panel 30 is supposed to have 760 scan lines for convenience.

[0114] The lower power supply voltages (Vss[1]~Vss[k]) are respectively supplied to the display panel regions (30A~30K). FIGS. 10A and 10B show examples for distributing the lower power supply voltages (Vss[1]~Vss[k]).

[0115] Referring to FIGS. 10A and 10B, the lower power supply voltage (Vss) supplied through a main line connected to the lower power supply voltage supply terminal(Vss_supply) is distributed to 10 sub-lines (k=10).

[0116] The lower power supply voltages (Vss) is supplied to 9 sub-lines among the 10 sub-lines, and a data voltage emission operation is performed at the other one sub-line by a switching control signal (EMS) in a state that supply of the lower power supply voltage (Vss) is cut-off.

[0117] FIG. 10A is an exemplary view showing a method for obtaining lower power supply voltages (Vss[1]~Vss[k]) by sequentially diverging a power supplied to the lower power supply voltage supply terminal (Vss_supply) from an external power supply unit (not shown), and then for supplying the obtained lower power supply voltages (Vss[1]~Vss[k]) to each of the display panel regions (30A~30K). Here, due to distribution resistance values, voltages are diverged from distribution nodes (S1~Sk)in the order of "Vss[1]>Vss[2]>···Vss[k-1]>Vss[k]". Here, the previously diverged voltage is higher than the next one by a small degree.

[0118] Referring to FIG. 10B, a voltage of a common node (SO) is expressed as a lower power supply voltage rising (Vss rising) by current applied to the diverged 9 lines. The Vss rising maintains a nearly constant value even if it may be varied little by little by an image change.

[0119] FIG. 10B is an exemplary view showing a method for obtaining lower power supply voltages (Vss[1]~Vss[k]) by diverging a power supplied to the lower power supply voltage supply terminal (Vss_supply) from an external power supply unit (not shown) at the same position, and then for supplying the obtained lower power supply voltages (Vss[1]~Vss[k]) to each of the display panel regions (30A~30K). Here, since distribution resistance values are equal to each other, each of the lower power supply voltages (Vss[1]~Vss[k]) has the same level as the common node (SO).

[0120] Accordingly, it is preferable to utilize the voltage diverging method shown in FIG. 10B rather than the voltage diverging method shown in FIG. 10A.

[0121] In an assumption that a voltage of SO varied at the gate according to a switching control signal (EMS) is V_{SO}, current of the rest display panel regions currently undergoing a light emitting operation can be expressed as the following equation 10.

【Equation 10】

$$I_{OLED} = \frac{\beta}{2} \cdot \{(V_{DATA} + \Delta V_{SO}) - (V_{SO} + \Delta V_{SO}) - V_{TH}\}^2 = \frac{\beta}{2} \cdot \{V_{DATA} - V_{SO} - V_{TH}\}^2$$

[0122] Here, it can be seen that the current on the display panel regions currently performing a light emitting operation is not varied. Accordingly, the problem of the Vss rising is solved, thereby not causing non-uniformity of a brightness according to each position on the large display panel 30.

[0123] The lower power supply voltages (Vss[1]~Vss[k]) are respectively supplied to the corresponding lower power supply voltage supply lines in the display panel regions (30A~30K) by being diverged as shown in FIG. 10B. For instance, in the display panel region 30A, the lower power supply voltage (Vss1) is diverged into 76 lower power supply voltages in the same manner as FIG. 10B, and is supplied to the corresponding lower power supply voltage supply line.

[0124] FIGS. 11A to 11E are timing diagrams showing a data voltage programming period (P1), a data voltage emission period (P2), scan signals, and data voltages on the display panel regions (30A~30K) to which the lower power supply voltages (Vss[1]~Vss[k]) are respectively supplied.

[0125] More concretely, FIGS. 11A and 11B show examples of the data voltage programming period (P1) and the

data voltage emission period (P2) with respect to each of the display panel regions (30A~30K). When the display panel 30 is defined as 10 display panel regions (30A~30K), 1/10 of one frame period is set as the data voltage programming period (P1) with respect to each of the display panel regions (30A~30K), and the rest 9/10of the one frame period is set as the data voltage emission period (P2).

[0126] FIGS. 11C and 11D are timing diagrams showing scan signals with respect to each of the display panel regions (30A~30K), which are same as general timing diagrams.

[0127] FIG. 11E is a timing diagram showing data voltages supplied through data lines (D1~Dn) with respect to each of the display panel regions (30A~30K), which are same as a general timing diagram.

[0128] With taking the pixel circuit of FIG. 4B and the display region (30A) among the display panel regions (30A~30K) on the display panel 30 as examples, data voltage programming and emission operations will be explained.

[0129] The data voltage programming period (P1) is set with respect to the first display panel region (30A) including all the pixels (PXs) connected to first to 76th scan lines (G1~G76).

[0130] As shown in FIG. 11A, since a switching control signal (EMS[1]) of a 'low' level is applied to the gate of the switching transistor (T43) inside all the pixels (PXs) connected to the first to 76th scan lines (G1~G76), the switching transistor (T43) is turned-OFF. Accordingly, the lower power supply voltage (Vss) from the lower power supply voltage supply line is not supplied to the corresponding pixel (PX).

[0131] As shown in FIGS. 11C and 11D, the 76 scan signals (Scan[1]~Scan[76]) are sequentially supplied to the first to 76th scan lines (G1~G76) in the data voltage programming period (P1), thereby turning-ON the switching transistors (T41) connected to the scan signals inside all the pixels (PXs). Here, data voltages (DATA) are supplied to the switching transistors (T41) through the data lines (D1~Dm). The data voltage (DATA) is charged to each storage capacitor (C41) through the switching transistors (T41) inside the respective pixels (PXs), and is maintained for the data voltage emission period (P2).

[0132] The data voltage programming and emission operations for the other display panel regions (30B~30K) are performed in the same manner as the display panel region 30A.

[0133] Accordingly, the data voltage programming period and the lighting duration of the organic light emitting diode can be sufficiently obtained regardless of the size of the display panel 30.

[0134] In the pixel driving method and apparatus for an organic light emitting device according to the present invention, in the data voltage programming period, a data voltage of a desired level can be precisely charged by charging the data voltage to the storage capacitor in a state that supply of the power supply voltage supplied to the organic light emitting diode (OLED) is cut-off. Also, in the data voltage emission period, the power supply to the OLED is started, thereby preventing a driving voltage of the driving transistor from changing. Accordingly, a non-uniform brightness of the OLED is solved.

[0135] The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present disclosure. The present teachings can be readily applied to other types of apparatuses. This description is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. The features, structures, methods, and other characteristics of the exemplary embodiments described herein may be combined in various ways to obtain additional and/or alternative exemplary embodiments.

[0136] As the present features may be embodied in several forms without departing from the characteristics thereof, it should also be understood that the above-described embodiments are not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its scope as defined in the appended claims, and therefore all changes and modifications that fall within the metes and bounds of the claims, or equivalents of such metes and bounds are therefore intended to be embraced by the appended claims.

Claims

1. A pixel driving method for an organic light emitting device, comprising:

a first step of charging a data voltage supplied through a data line to a storage capacitor by driving an N-channel switching transistor, when cutting off supply of an upper power supply voltage to an organic light emitting diode ; and

a second step of making the organic light emitting diode emit light by driving the N-channel driving transistor by the data voltage charged to the storage capacitor, when supplying the upper power supply voltage.

2. The method of claim 1, wherein the N-channel switching transistor is driven by positive scan signals.

3. The method of claim 1, wherein the storage capacitor is connected between a gate terminal of the N-channel driving

transistor and a lower power supply voltage terminal.

4. The method of claim 3, wherein the lower power supply voltage terminal is connected to a lower power supply voltage supply line having a mesh structure.

5. The method of claim 1, wherein the storage capacitor is connected between a gate terminal and a source terminal of the N-channel driving transistor.

6. The method of claim 1, wherein the organic light emitting diode has an anode connected to an upper power supply voltage terminal, and a cathode connected to a drain of the N-channel driving transistor.

7. The method of claim 1, wherein the organic light emitting diode has an anode connected to a source terminal of the N-channel driving transistor, and a cathode connected to a lower power supply voltage terminal.

8. The method of claim 1, wherein supply or cut-off of the upper power supply voltage to the organic light emitting diode is controlled by a switching transistor connected between the organic light emitting diode and the driving transistor.

9. A pixel driving method for an organic light emitting device, comprising:

a first step of charging a data voltage supplied through a data line to a storage capacitor by driving a P-channel switching transistor, when cutting off supply of a lower power supply voltage to an organic light emitting diode; and
a second step of making the organic light emitting diode emit light by driving the P-channel driving transistor by the data voltage charged to the storage capacitor, when supplying the lower power supply voltage.

10. The method of claim 9, wherein the P-channel switching transistor is driven by negative scan signals.

11. The method of claim 9, wherein the storage capacitor is connected between a gate terminal of the P-channel driving transistor and an upper power supply voltage terminal.

12. The method of claim 9, wherein the organic light emitting diode has an anode connected to a source terminal of the P-channel driving transistor, and a cathode connected to a lower power supply voltage terminal.

13. The method of claim 9, wherein supply or cut-off of the lower power supply voltage to the organic light emitting diode is controlled by a switching transistor connected between the organic light emitting diode and the driving transistor.

14. A pixel driving method for an organic light emitting device, comprising:

defining a display panel of the organic light emitting device into a plurality of display panel regions in a horizontal direction such that a plurality of adjacent scan lines can be included in each region;
making pixels inside each of the plurality of display panel regions share one lower power supply voltage among a plurality of lower power supply voltages supplied from a lower power supply voltage supply terminal by being diverged; and
determining a data voltage programming period and a data voltage emission period in one frame period according to each of the display panel regions.

15. The method of claim 14, wherein the plurality of lower power supply voltages are supplied by being diverged from one common point.

16. The method of claim 14, wherein scan signals are sequentially supplied to the scan lines in one frame period.

17. The method of claim 14, wherein the data voltage programming period is determined by dividing the one frame period by the number of the display panel regions.

18. The method of claim 14, wherein the data voltage emission period corresponds to other period except the data voltage programming period in one frame period.

19. A pixel driving apparatus for an organic light emitting device, comprising;

a first switching transistor for transmitting data voltages supplied through data lines to a storage capacitor by being driven by scan signals, in a state that supply of an upper power supply voltage is cut-off;
a storage capacitor for charging the data voltage, in a state that supply of the upper power supply voltage is cut-off, by being connected between a gate terminal of a driving transistor and a lower power supply voltage terminal;
a driving transistor for supplying a driving current corresponding to the data voltage charged to the storage capacitor to an organic light emitting diode, in a state that the upper power supply voltage is supplied;
a second switching transistor being turned-off by a switching control signal of a 'low' level in the time of supplying scan signals by being connected between the cathode of the OLED and the drain of the driving transistor;
an organic light emitting diode for emitting light with a brightness corresponding to the driving current by having an anode connected to the upper power supply voltage and a cathode connected to a drain of the second switching transistor.

20. A pixel driving apparatus for an organic light emitting device, comprising a display panel,
wherein the display panel is configured to:

define a plurality of display panel regions in a horizontal direction such that a plurality of adjacent scan lines can be included in each region;
make pixels inside each of the plurality of display panel regions share one lower power supply voltage among a plurality of lower power supply voltages supplied by being diverged; and
determine a data voltage programming period and a data voltage emission period in one frame period according to each of the display panel regions.

FIG. 1A
CONVENTIONAL ART

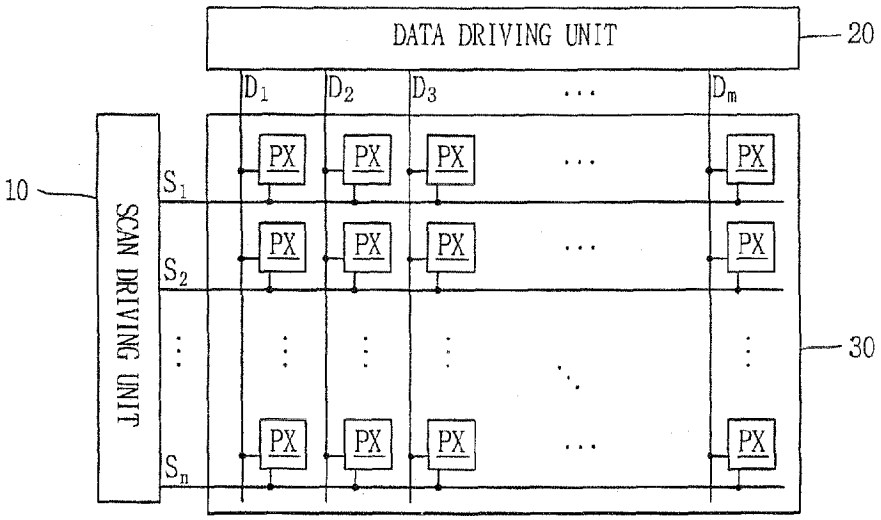


FIG. 1B
CONVENTIONAL ART

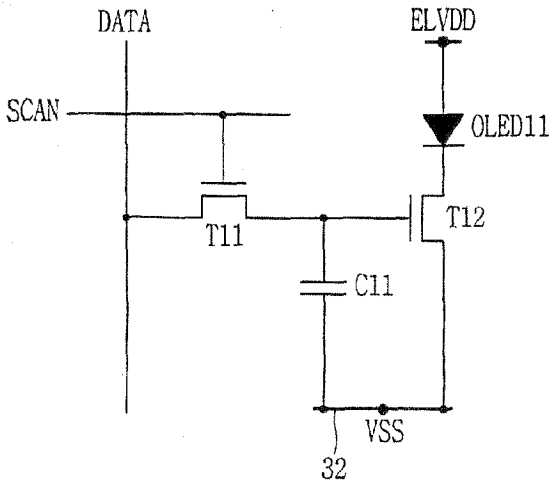


FIG. 2
CONVENTIONAL ART

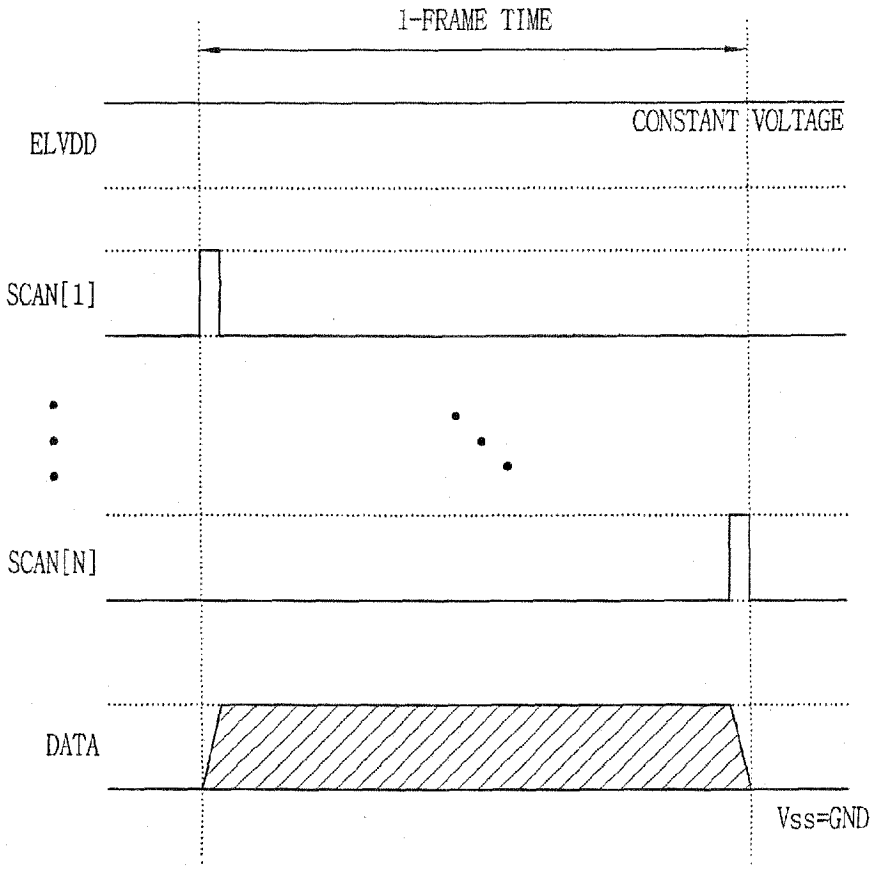


FIG. 3

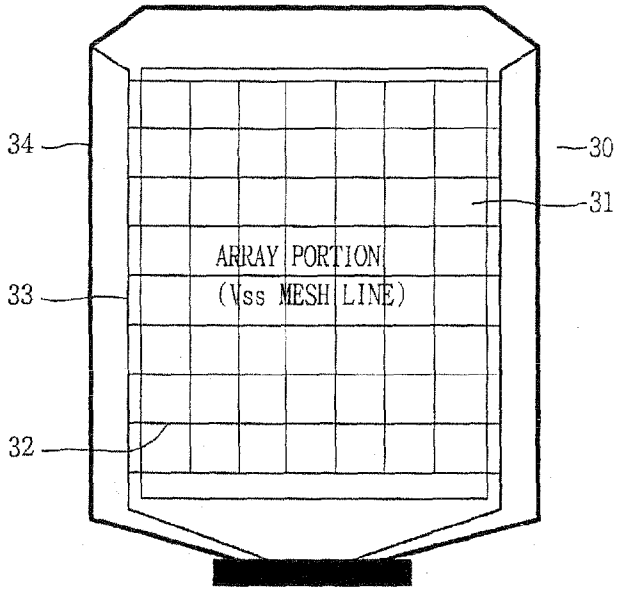

34
30
31
ARRAY PORTION
(Vss MESH LINE)
33
32

FIG. 4A

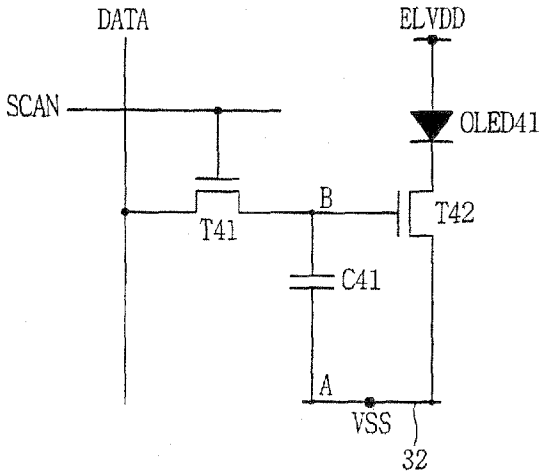

DATA
ELVDD
SCAN
OLED41
B
T42
T41
C41
A
VSS
32

FIG. 4B

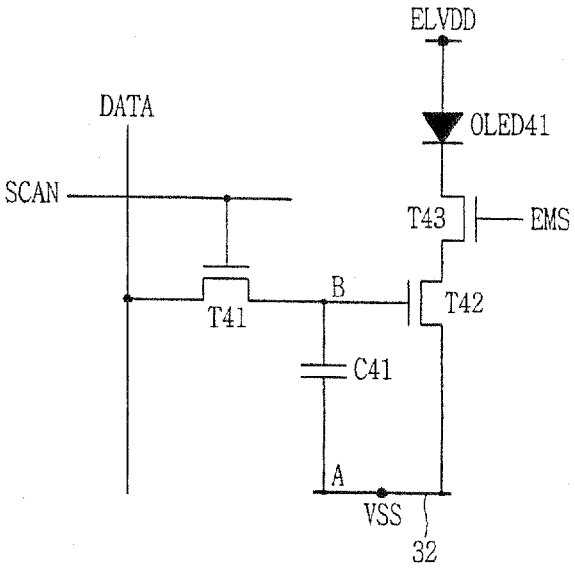


FIG. 5

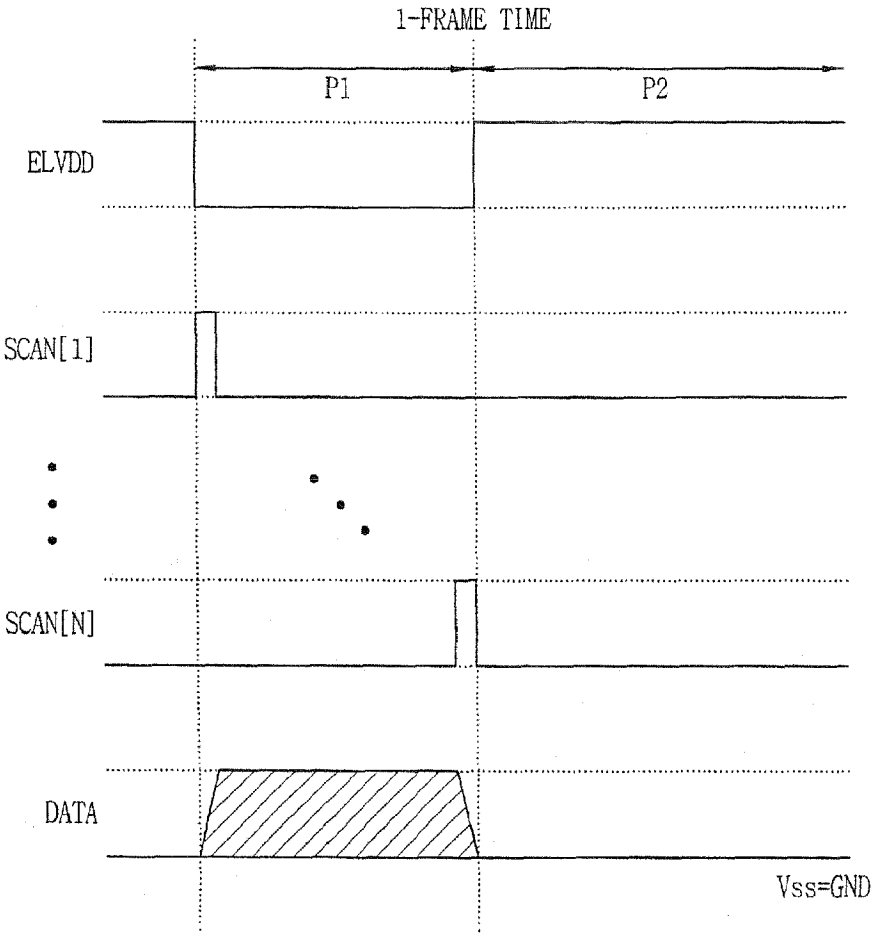


FIG. 6A

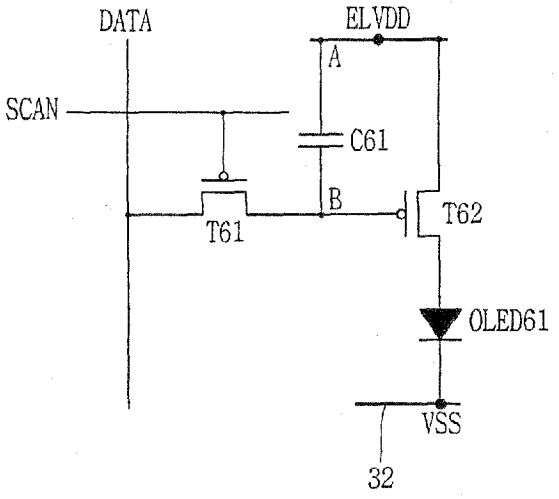

DATA
ELVDD
A
SCAN
C61
B
T61
T62
OLED61
VSS
32

FIG. 6B

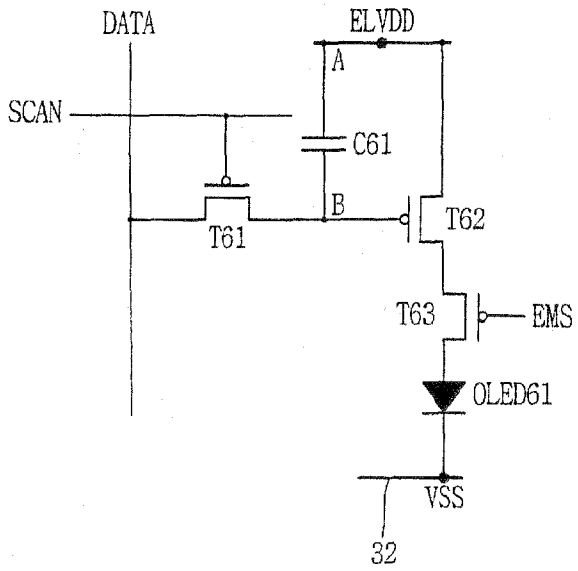

DATA
ELVDD
A
SCAN
C61
B
T61
T62
T63
EMS
OLED61
VSS
32

FIG. 7

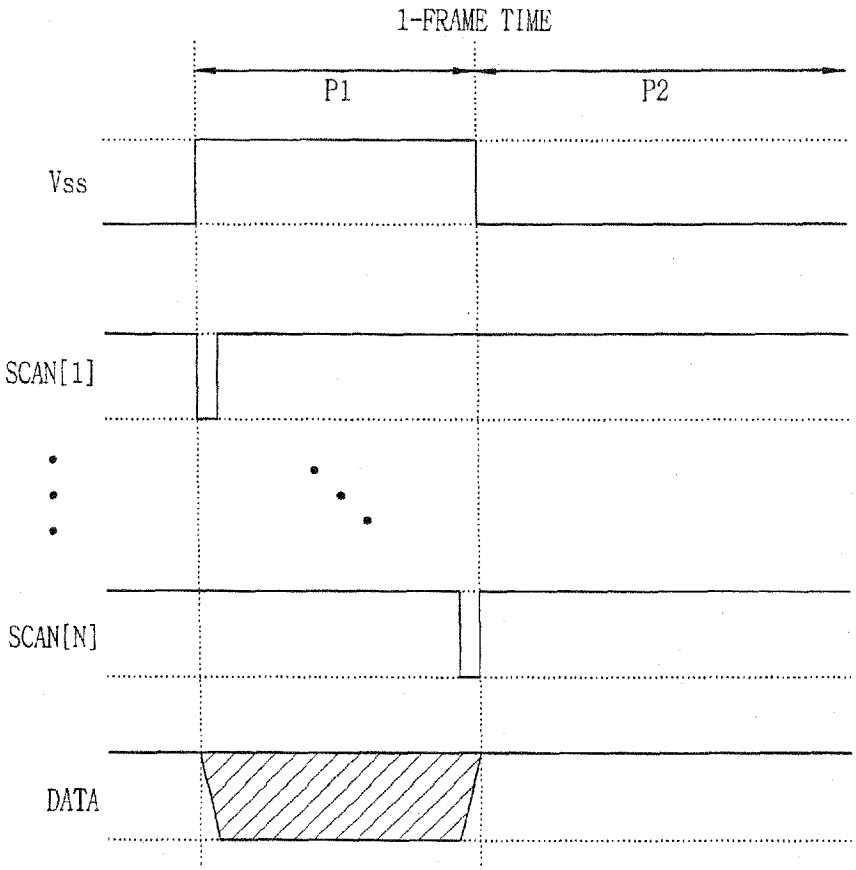


FIG. 8

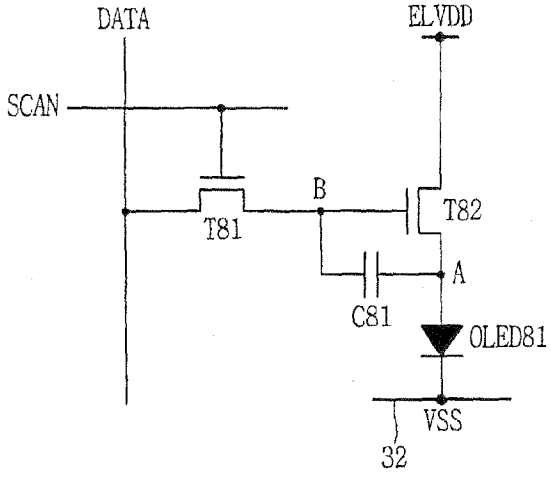

DATA
ELVDD
SCAN
B
T82
T81
A
C81
OLED81
VSS
32

FIG. 9

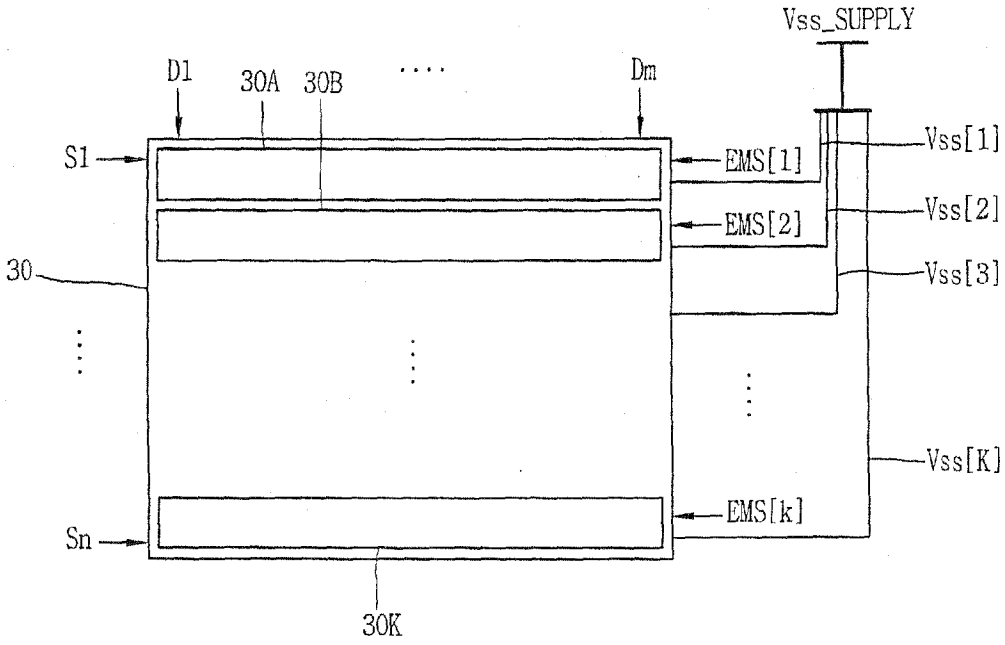

Vss_SUPPLY
D1
30A
30B
Dm
S1
EMS[1]
Vss[1]
EMS[2]
Vss[2]
30
Vss[3]
Vss[K]
EMS[k]
Sn
30K

FIG. 10A

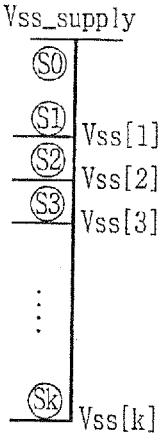


FIG. 10B

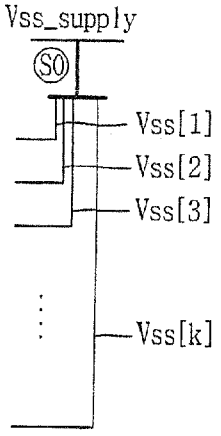
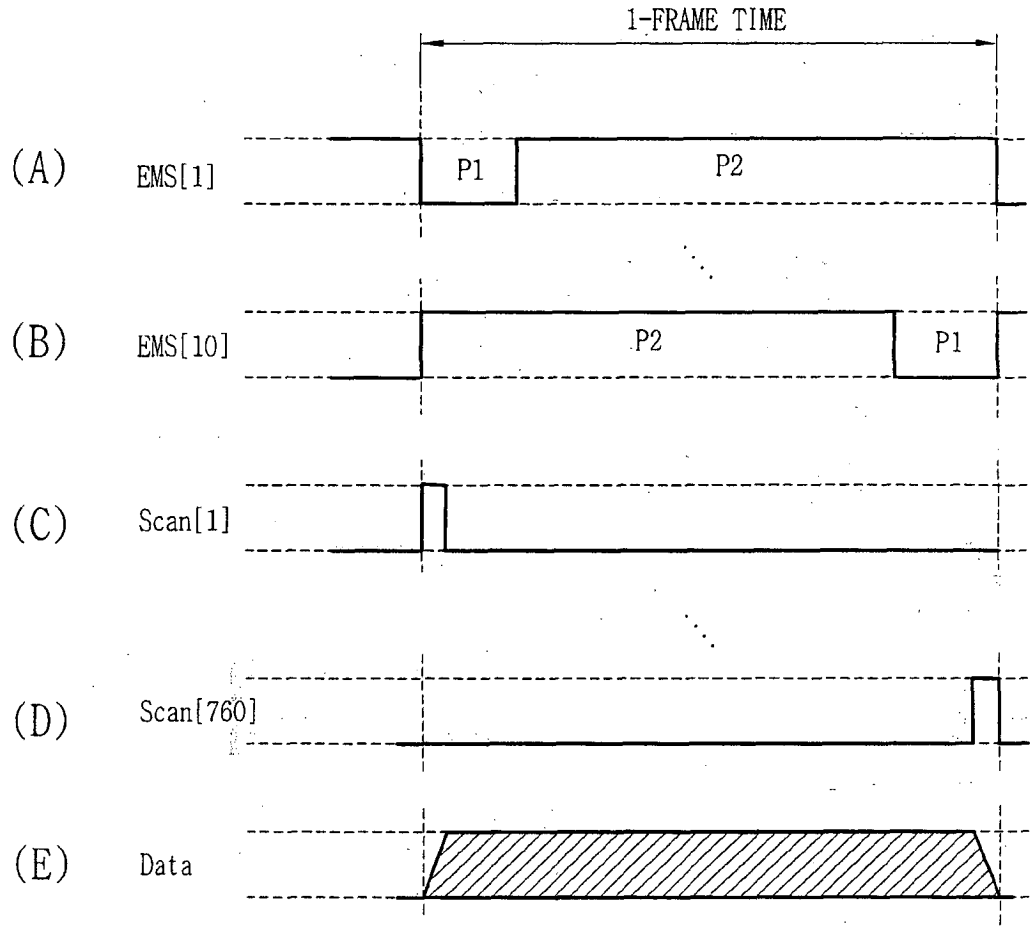


FIG. 11



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 102007096141 **[0001]**

专利名称(译)	用于有机发光器件的像素驱动方法和装置		
公开(公告)号	EP2040248A2	公开(公告)日	2009-03-25
申请号	EP2007124161	申请日	2007-12-28
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	NAM WOO JIN		
发明人	NAM, WOO-JIN		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G2300/0842 G09G2300/0861 G09G2300/0866 G09G2310/0218 G09G2320/0223 G09G2320/0247		
代理机构(译)	庆祝活动，JENTSCHURA & PARTNER		
优先权	1020070096141 2007-09-20 KR		
其他公开文献	EP2040248A3		
外部链接	Espacenet		

摘要(译)

一种用于有机发光装置的像素驱动方法和装置，能够通过将电源电压充电到存储电容器来防止像素内的驱动晶体管的驱动电压下降，其中电源电压提供给存储电容器。切断有机发光二极管（OLED），然后开始向OLED供应电源电压，并且能够充分地获得数据电压发射时段。该方法包括：将有机发光装置的显示面板在水平方向上限定为多个显示面板区域，使得可以包括多个相邻的扫描线;使得在多个显示面板区域内的像素通过发散而从较低电源电压供应端子供应的多个较低电源电压中共享一个较低电源电压;根据每个显示面板区域确定一个帧周期中的数据电压编程周期和数据电压发射周期。

FIG. 9