(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 2 009 618 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
31.12.2008 Bulletin 2009/01

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(21) Application number: **08158645.5**

(22) Date of filing: **20.06.2008**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MT NL NO PL PT RO SE SI SK TR
Designated Extension States:
AL BA MK RS

(30) Priority: **22.06.2007 KR 20070061496**

(71) Applicant: **Samsung SDI Co., Ltd.**
Suwon-si
Gyeonggi-do (KR)

(72) Inventor: **Chung, Kyung-Hoon**
Samsung SDI Co., Ltd.
Suwon-si,
Gyeonggi-do (KR)

(74) Representative: **Hengelhaupt, Jürgen et al**
Gulde Hengelhaupt Ziebig & Schneider
Patentanwälte - Rechtsanwälte
Wallstrasse 58/59
10179 Berlin (DE)

(54) Pixel, organic light emitting display and associated methods

(57) A pixel includes an organic light emitting diode, a first transistor having a source connected to a first power source, a control gate connected to a first node, and a drain connected to a second node, wherein the first transistor includes a floating gate and an insulating layer between the floating gate and the control gate, a second transistor having a source connected to a data line, a drain connected to the first node, and a gate connected to a scan line, a third transistor having a source connected to the second node, a drain connected to the organic light emitting diode, and a gate connected to one of a light emitting control line and the scan line, and a capacitor connected between the first power source and the second node.

EP 2 009 618 A2

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] Embodiments relate to a pixel, an organic light emitting display exhibiting improved image quality, and a method of driving the same.

2. Description of the Related Art

[0002] Active matrix-type flat panel displays that display images using thin film transistors have been widely used. An organic light emitting display may exhibit excellent luminous efficiency, brightness, and viewing angle, and may have a rapid response speed. The organic light emitting display displays images by using a plurality of organic light emitting diodes (OLEDs). The organic light emitting diode may include an anode electrode, a cathode electrode, and an organic light emitting layer between the anode electrode and the cathode electrode.

[0003] FIG. 1 is a circuit view showing a structure of a pixel of a general organic light emitting display (US 2007/0057877 A1). Referring to FIG. 1, a pixel includes a first transistor, a second transistor, a third transistor, a capacitor, and an organic light emitting diode (OLED).

[0004] The source of the first transistor M1 is connected to a first power supply line, the drain thereof is connected to the source of the third transistor, and the gate thereof is connected to a first node N1. The first transistor M1 allows current to flow from the source to the drain corresponding to the voltage of the first node N1.

[0005] The source of the second transistor M2 is connected to a data line Dm, the drain thereof is connected to a first node N1, and the gate thereof is connected to a scan line Sn. The second transistor M2 performs a switching operation by means of the scan signal transferred through the scan line Sn to allow the data signal flowed through the data line Dm to be selectively transferred to the first node N1.

[0006] The source of the third transistor M3 is connected to the drain of the first transistor, the drain thereof is connected to the organic light emitting diode, and the gate thereof is connected to a light emitting line En. The third transistor M3 performs turn-on and turn-off operations by means of the light emitting control signal transferred through the light emitting line to allow the current flowing from the source of the first transistor to the drain thereof to be transferred to the organic light emitting diode (OLED).

[0007] The first electrode of the capacitor Cst is connected to a first power supply line ELVDD and the second electrode thereof is connected to a first node N1. When the data signal is transferred to the first node N1, the capacitor Cst allows the voltage of the transferred data signal to be maintained until the next data signal is transferred to the first node N1. Therefore, the gate of the first transistor M1 has the voltage of the data signal by the capacitor Cst.

[0008] The organic light emitting diode (OLED) includes an anode electrode, a cathode electrode, and a light emitting layer positioned between the anode electrode and the cathode electrode, wherein the light emitting layer emits light when current flows. Therefore, if the current corresponding to the data signal is generated and provided by means of the first transistor M1, the current flows from the anode electrode to the cathode electrode so that the light emitting diode (OLED) emits light.

[0009] In the organic light emitting display comprising the circuit constituted as above, the semiconductor layer of each transistor may use polysilicon or similar suitable materials. However, polysilicon inevitably is subject to process deviations. Therefore, if the transistor is formed using polysilicon, difference occurs in charge carrier mobility and the threshold voltage of transistorswhich causes deviations of the current flowing into the pixel. On such a ground, pixel circuits capable of compensating for the threshold voltage are commonly used. However, the structure of the pixel circuit compensating for the threshold voltage is complicated and increases the area of the pixel circuit at the cost of the light emitting OLED area. Thus, display brightness decreases and it becomes difficult to reduce the pitch of the pixels in order to increase display resolution.

SUMMARY OF THE INVENTION

[0010] Aspects of the invention are therefore directed to an organic light emitting display and a method of driving the same, which overcome one or more of the problems due to the limitations and disadvantages of the related art.

[0011] Accordingly, a first aspect of the invention provides an organic light emitting display, comprising a pixel unit having a plurality of pixels, a data driver connected to data lines of the pixel unit, and a scan driver connected to scan lines of the pixel unit. Each pixel includes first through third transistors, a capacitor and an organic light emitting diode. The first transistor has a first electrode connected to a first power source, a control gate connected to a first node, and a second electrode. The second transistor has a first electrode connected to a data line, a second electrode connected to the first node, and a gate connected to a scan line. The third transistor has a first electrode connected to the second electrode of the first transistor, a gate connected to one of a light emitting control line and the scan line, and a second electrode. The capacitor is connected between the first power source and the first node. The organic light emitting diode has an anode connected to the second electrode of the third transistor and a cathode connected to a second power source. According to the invention, the first transistor includes a floating gate and an insulating layer between the floating gate and the control gate.

[0012] The scan driver may be connected to light emitting control lines of the pixel unit and the gate of the third

transistor of each pixel may be connected to a light emitting control line.

[0013] The first, second, and third transistors may be PMOS transistors.

[0014] Alternatively, the first transistor may be an NMOS transistor, and the second and third transistors may be PMOS transistors.

[0015] In a preferred embodiment of the invention, the gate of the third transistor of each pixel may beconnected to the scan line and the third transistor of each pixel may be of an opposite conduction type as the second transistor of the pixel.

[0016] Then, the first and second transistors may be PMOS transistors, and the third transistor may be an NMOS transistor.

[0017] A second aspect of the invention is directed to a method of driving an organic light emitting display, including determining a current flowing into a first transistor of a pixel, determining a deviation of a threshold voltage of the first transistor using the determined current, and compensating for the deviation of the threshold voltage. The first transistor may be a floating gate transistor, and compensating for the deviation of the threshold voltage may include storing a voltage corresponding to the deviation of the threshold voltage in the first transistor.

[0018] Storing the voltage corresponding to the deviation of the threshold voltage may include controlling an amount of electrons stored in a floating gate of the floating gate transistor. The method may further include extracting electrons stored in the floating gate into a channel region of the first transistor to lower the threshold voltage. Extracting electrons into the channel region may include providing a high state voltage to a source of the first transistor and providing a low state voltage to a control gate of the first transistor. The method may further include injecting electrons into the floating gate to raise the threshold voltage. Injecting electrons into the floating gate may include providing a low state voltage to a source of the first transistor and providing a high state voltage to a control gate of the first transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The above and other features and advantages will become more apparent to those of ordinary skill in the art by describing in detail example embodiments with reference to the attached drawings, in which:

FIG. 1 is a circuit view showing a structure of a pixel of a general organic light emitting display;
FIG. 2 illustrates a schematic view of an organic light emitting display according to an embodiment;
FIG. 3 illustrates a cross-sectional view of a transistor having a non-volatile memory element;

[0020] FIG. 4 illustrates a graph of current flowing into a drain of a transistor as a function of control gate voltage and changes in the threshold voltage of the transistor;

[0021] FIG. 5 illustrates a graph of a relationship between threshold voltage and stress time;

[0022] FIG. 6 illustrates a circuit view of a portion of a pixel unit of the organic light emitting display of FIG. 2; and

[0023] FIGS. 7 and 8 illustrate embodiments of pixel circuits in the organic light emitting display of FIG. 2.

DETAILED DESCRIPTION OF THE INVENTION

[0024] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0025] In the figures, the dimensions of layers and regions may be exaggerated for clarity of illustration. It will also be understood that when a layer or element is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Further, it will be understood that when a layer is referred to as being "under" another layer, it can be directly under, and one or more intervening layers may also be present. In addition, it will also be understood that when a layer is referred to as being "between" two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present. Like reference numerals refer to like elements throughout.

[0026] Where an element is described as being connected to a second element, the element may be directly connected to the second element, or may be indirectly connected to the second element via one or more other elements. Further, where an element is described as being connected to a second element, it will be understood that the elements may be electrically connected, e.g., in the case of transistors, capacitors, power sources, nodes, etc. Where two or more elements are described as being connected to a node, the elements may be directly connected to the node, or may be connected via conductive features to which the node is common. Thus, where embodiments are described or illustrated as having two or more elements that are connected to a common point, it will be appreciated that the elements may be connected to respective points on a conductive feature that extends between the respective points.

[0027] FIG. 2 illustrates a schematic view of an organic light emitting display according to an embodiment. Referring to FIG. 2, the organic light emitting display includes a pixel unit 100, a data driver 110, and a scan driver 120.

[0028] The pixel unit 100 includes a plurality of pixels 101. Each pixel 101 includes an organic light emitting diode configured to emit light corresponding to a flow of current. The pixel unit 100 includes n scan lines S1, S2, ... Sn-1, and Sn transferring scan signals, the scan lines

extending in a row direction, n light emitting control lines E1, E2, ... En-1, and En transferring light emitting control signals, the light emitting control lines extending in the row direction, and m data lines D1, D2, ... Dm-1, and Dm transferring data signals, the data lines extending in a column direction.

[0029] The pixel unit 100 is connected to external first and second power sources ELVDD and ELVSS, respectively. The pixel unit 100 displays an image by light emitting the organic light emitting diodes using the scan signals, the data signals, the light emitting control signals, the first power source ELVDD and the second power source ELVSS. A low state voltage may be provided by the second power source ELVSS during an image-display operation of the organic light emitting diode, i.e., when current flows in the organic light emitting diode to display images. As described in detail below, one or both of the first and second power sources may supply various voltages, such that ELVDD may supply a higher or lower voltage than ELVSS, in order to facilitate compensation of a threshold voltage of a non-volatile memory element.

[0030] The data driver 110 generates the data signals by receiving video data with red, blue, and green components, and applies the data signals to the pixel unit 100. The data driver 110 applies the data signals to the pixel unit 100 via the data lines D1, D2, ..., Dm-1, and Dm of the pixel unit 100.

[0031] The scan driver 120 includes a scan driving circuit generating the scan signals and a light emitting control signal driving circuit generating the light emitting control signals, and applies the scan signals and light emitting control signals to the pixel unit 100. The scan driving circuit is connected to the scan lines S1, S2, ..., Sn-1, and Sn to transfer the scan signals to a specific row of the pixel unit 100. The light emitting control signal driving circuit is connected to the light emitting control lines E1, E2, ..., En-1, and En to transfer the light emitting control signals to a specific row of the pixel unit 100.

[0032] In an implementation, the light emitting control signal driving circuit may be connected to first and second light emitting control lines to transfer the first and second light emitting control signals to a specific row of the pixel unit 100. The data signals output from the data driver 110 are supplied to the pixel 101 to which the scan signals are transferred. As a result, a driving current may be generated in the pixel 101, the generated driving current being supplied to the organic light emitting diode by the first and second light emitting control signals.

[0033] FIG. 3 illustrates a cross-sectional view of a transistor having a non-volatile memory (NVM) element, which may be implemented in each pixel of the organic light emitting display shown in FIG. 2. Referring to FIG. 3, an insulating film 204, e.g., a tunnel oxide film, may be formed on a silicon substrate 201, e.g., an N-type silicon substrate. The silicon substrate 201 may be polysilicon. A floating gate 205 may be formed on the oxide film, an oxide-nitride-oxide (ONO) layer 206 may be formed on the floating gate 205, and a control gate 207 may be formed on the ONO layer 206. A source 202 and a drain 203 may be formed on sides of the gate electrode made up of the floating gate 205 and the control gate 207.

[0034] To raise the threshold voltage of the NVM element, hot electrons beyond the energy barrier of the tunnel oxide film may be injected into a potential well formed in the floating gate 205 using hot electron injection. The injection of electrons into the floating gate may raise the threshold voltage of the transistor.

[0035] To lower the threshold voltage of the NVM element, electrons stored in the potential well of the floating gate 205 may be extracted into the silicon substrate using tunneling. The removal of electrons from the floating gate may lower the threshold voltage.

[0036] FIG. 4 illustrates a graph of current flowing into the drain of a transistor as a function of control gate voltage and changes in the threshold voltage of the transistor. In FIG. 4, the horizontal axis represents the voltage V_{CG} of the control gate and the vertical axis represents the current I_D flowing into the drain of the transistor. A thick curve in FIG. 4 represents an ideal curve. FIG. 5 illustrates a graph of a relationship between threshold voltage and stress time.

[0037] Referring to FIG. 4, if the threshold voltage is controlled, the amount of the current I_D flowing into the drain of the transistor changes corresponding to the voltage V_{CG} of the control gate. In particular, if the threshold voltage is raised, the curve moves from left to right (hereinafter referred to a "positive" (+) shift). If the threshold voltage is lowered, the curve moves from right to left (a "negative" (-) shift).

[0038] With respect to the curve representing the ideal change, the threshold voltage of the transistor is compensated to allow the amount of current flowing into the drain of the transistor corresponding to the voltage V_{CG} of the control gate to follow the ideal curve.

[0039] In FIG. 5, the vertical axis represents a variation value of ΔV_{th} of the threshold voltage and the horizontal axis represents time. The variation value ΔV_{th} of the threshold voltage can be changed by controlling the stress time and the voltage of the control gate.

[0040] As shown in FIG. 5, if the voltage V_{CG} of the control gate is large, the variation value ΔV_{th} of the threshold voltage may become large. If the voltage V_{CG} of the control gate is small, the variation value ΔV_{th} of the threshold voltage may become small.

[0041] FIG. 6 illustrates a circuit view of a portion of a pixel unit 100 of the organic light emitting display of FIG. 2. Referring to FIG. 6, a 2x2 portion of the pixel unit 100 is illustrated, including first to fourth pixels 101a, 101b, 101c, and 101d. As shown in FIG. 6, each pixel 101 may include a first transistor M1, a second transistor M2, a third transistor M3, a capacitor Cst, and an organic light emitting diode OLED. Each first transistor M1 may include an NVM element, e.g., the NVM element illustrated in FIG. 3.

[0042] The amount of current flowing into any one of the first to fourth pixels 101a, 101b, 101c, and 101d may

be measured as described below.

[0043] In order to measure the current flowing into the first pixel 101a, a first voltage, e.g., 0V, is supplied to a first power line from the first power source ELVDD, and a second voltage, e.g., a negative voltage, is supplied to a second power line from the second power source ELVSS. Data signals, e.g., having voltage of -15 V to +15 V, are supplied to a first data line D1, and third voltage, e.g., a high voltage, is applied to a second data line D2. Scan signals having a fourth voltage, e.g., a voltage much lower than the voltage of the data signals provided to the first data line D1, are supplied to a first scan line S1. Scan signals having a fifth voltage, e.g., a high state voltage, are supplied to a second scan line S2. Light emitting control signals having a sixth voltage, e.g., a low state voltage, are supplied to a first light emitting control line E1. Light emitting control signals having a seventh voltage, e.g., a high state voltage, are supplied to a second light emitting control line E2. The third voltage, the fifth voltageand the seventh voltage may be the same.

[0044] With the power sources and signals provided as described above, in the first pixel 101a, the data signals flow through the first data line D 1, and the second transistor M2 is turned-on by the voltage applied through the first scan line S1. Thus, the voltage of the data signals is supplied to a first node N1. Additionally, the voltage of the data signals is supplied from the first node N1 to the gate of the first transistor M1. The voltage of 0 V is supplied from the first power source ELVDD to the source of the first transistor M1. The third transistor M3 is turned-on by the light emitting control signal transferred through the first light emitting control line E1, so that current flows from the source to the drain of the first transistor M1, through the third transistor M3, and to the organic light emitting diode OLED.

[0045] However, with respect to the second pixel 101b, although the second transistor M2 is turned-on by the scan signals transferred through the first scan line S1 and the third transistor M3 is turned-on by the light emitting control signals transferred through the first light emitting control line E1, the first transistor M1 is turned-off by the high state data signals transferred through the second data line D2, thereby blocking the generation of current.

[0046] In the case of the third pixel 101c, the second transistor M2 is turned-off by the scan signals transferred through the second scan line S2, preventing the data signals transferred through the first data line D1 from being supplied to the control gate of the first transistor M1. Also, the third transistor M3 is turned-off by the light emitting control signals transferred through the second light emitting control line E2, blocking the generation of current.

[0047] In the case of the fourth pixel 101d, the high state data signals are transferred through the second data line D2. Further, the scan signals transferred through the second scan line S2 have the high state voltage, so that the second transistor M2 is turned-off. The third transistor M3 is turned-off by the light emitting control signals transferred through the second light emitting control line E2, blocking the generation of current. Thus, with the power sources and signals provided as described above, current flows only in the first pixel 101a.

[0048] The above-described operations may be extended such that the current flowing into the second pixel 101b, the third pixel 101c, and the fourth pixel 101d can be measured in sequence. In particular, it will be appreciated that the operation of the above-described first through fourth pixels 101a through 101d may be controlled by the data signals transferred through the data lines D1 and D2, the scan signals transferred through the scan lines S1 and S2, and the voltage of the light emitting control signals transferred through the light emitting control lines E1 and E2, such that the current flowing into the second pixel 101b, the third pixel 101c, and the fourth pixel 101d can be measured in sequence.

[0049] Compensation of the threshold voltage of the first transistor M1 will now be described. The compensation value for compensating the threshold voltage of the first transistor M1 in the first pixel 101a may be determined using the current measured above.

[0050] The compensation value can be determined using the values of the voltage of the control gate and the current flowing into the first pixel 101a. The case of compensating the threshold voltage by raising the threshold voltage, as well as the case of compensating the threshold voltage by lowering the threshold voltage, may be based on the determined value, as will now be described in detail.

[0051] The case where the threshold voltage of the first pixel 101a is compensated by raising the threshold voltage will now be described.

[0052] For the first pixel 101a, the first power source ELVDD applies a voltage much lower than the low state, and the second power source ELVSS applies the voltage of 0V Data signals having the high state voltage are transferred through the first data line D1, the scan signal having the low state voltage is transferred through the first scan line S1, and the light emitting signal transferred through the first light emitting control line E1 becomes a high state. Accordingly, electrons are injected into the floating gate of the first transistor M1 in the first pixel 101a, so that the threshold voltage is raised. Electrons may be caused to flow into the floating gate of the first transistor M1 at a rate that depends on the voltage of the data signals.

[0053] As described above, electrons may be caused to flow into the floating gate of the first transistor M1 of the first pixel 101a, thereby increasing the threshold voltage of the first transistor, when a high state voltage, i.e., a data signal having a high voltage, is transferred to the gate of the first transistor M1, a voltage lower than a low state voltage is provided by the first power source ELVDD to the source of the first transistor M1, and a voltage of 0V is supplied from the second power source ELVSS. The low state voltage may be provided by the second

power source ELVSS during an image-display operation of the organic light emitting diode, i.e., when current flows in the organic light emitting diode to display images.

[0054] Additionally, data signals having the low state voltage are transferred through the second data line D2, scan signals having the high state voltage are transferred through the second scan line S2, and the light emitting signal transferred through the second light emitting control line E2 becomes a high state.

[0055] It will be appreciated that the compensation of the threshold voltage can be controlled by changing the voltage of the first power source ELVDD. In particular, to increase the compensation of the threshold voltage, the voltage of the first power source ELVDD may be lowered. To reduce the compensation of the threshold voltage, the voltage of the first power source ELVDD may be raised.

[0056] With respect to the second pixel 101b, although the scan signals transferred thorough the first scan line S1 are in a low state, the data signals transferred through the second data line D2 have the low state voltage. Accordingly, the second transistor M2 is turned-off and the control gate of the first transistor M1 is turned-off, so that the threshold voltage of the first transistor M1 in the second pixel 101b is not compensated.

[0057] In the case of the third pixel 101c, although the data signals transferred through the first data line D1 are in a high state, the scan signals transferred through the second scan line S2 are in a high state. Accordingly, the second transistor M2 is turned-off and the control gate of the first transistor M1 is thus placed in a floating state. Therefore, the threshold voltage of the first transistor M1 in the third pixel 101c is not compensated.

[0058] In the case of the fourth pixel 101 d, the scan signals transferred through the second scan line S2 are in a high state, so that the second transistor M2 is turned off and the control gate of the first transistor M1 is placed in a floating state. Therefore, the threshold voltage of the first transistor M1 in the fourth pixel 101d is not compensated.

[0059] The above-described operations may be extended to the remaining pixels. In particular, if the voltages of the data signals and the scan signals are sequentially controlled, the threshold voltages of the second pixel to the fourth pixel 101b, 101c, and 101d may also be compensated.

[0060] The case where the threshold voltage of the first pixel 101a is compensated by lowering the threshold voltage will now be described.

[0061] For the first pixel 101a, the first power source ELVDD applies the high state voltage and the second power source ELVSS applies the voltage of 0V. Data signals having a voltage much lower than the low state are transferred through the first data line D1. The scan signal transferred through the first scan line S1 has a voltage much lower than the voltage of the data signals flowing into the first data line D 1. The light emitting signal transferred through the first light emitting control line E1 becomes a high state. Accordingly, electrons stored in the floating gate are extracted into the channel region of the first transistor M1 so that the threshold voltage of the first transistor M1 of the first pixel 101a is lowered.

[0062] Additionally, the data signals having the high state voltage are transferred through the second data line D2, the scan signals transferred through the second scan line S2 have the high state voltage, and the light emitting signal transferred through the second light emitting control line E2 becomes a high state.

[0063] The compensation of the threshold voltage can be controlled by changing the voltage of the first data line D1. In particular, to increase the compensation of the threshold voltage, the voltage of the first data line D1 may be lowered. To reduce the compensation of the threshold voltage, the voltage of the first data line D 1 may be raised.

[0064] With respect to the second pixel 101b, the scan signals transferred through the first scan line S1 are in a low state and the data signals transferred through the second data line D2 have the high state voltage. As a result, the first transistor M1 of the second pixel 101b is turned-off. Accordingly, the threshold voltage of the first transistor M1 of the second pixel 101b is not compensated.

[0065] In the case of the third pixel 101c, the data signals transferred through the first data line D1 are in a high state and the scan signals transferred through the second scan line S2 are in a high state. Accordingly, the second transistor M2 is turned-off and the control gate of the first transistor M1 is placed in a floating state. Therefore, the threshold voltage of the first transistor M1 of the third pixel 101c is not compensated.

[0066] In the case of the fourth pixel 101 d, the scan signals transferred through the second scan line S2 are in a high state. Accordingly, the second transistor M2 is turned off so that the control gate of the first transistor M1 is placed in a floating state. Therefore, the threshold voltage of the first transistor M 1 of the fourth pixel 101d is not compensated.

[0067] The above-described operations may be extended to the remaining pixels. In particular, if the voltages of the data signals and the scan signals are sequentially controlled, the threshold voltages of the second pixel to the fourth pixel 101b, 101c, and 101d may also be compensated.

[0068] If the threshold voltages of the first transistors M1 are compensated using the operations described above, the organic light emitting display may display a uniform screen. Additionally, the pixel circuits may be simplified by eliminating the need for a separate threshold voltage compensation circuit.

[0069] FIGS. 7 and 8 illustrate embodiments of pixel circuits in the organic light emitting display of FIG. 2. Referring to FIG. 7, the first transistor M1 may be implemented as an NVM element of an NMOS type. As illustrated in FIG. 5, if the voltage of the control gate is lowered, the threshold voltage is lowered and, if the voltage of the control gate is raised, the threshold voltage is

raised.

[0070] Referring to FIG. 8, the third transistor M3 may be implemented as an NMOS transistor. Further, the second transistor M2 and the third transistor M3 may be connected to a same scan line Sn. Accordingly, the second transistor M2 and the third transistor M3 may be alternately turned-on. Therefore, when the data signals are supplied to the pixel, the third transistor M3 is turned-off, and then the third transistor M3 is turned-on after a predetermined time so that current flows in the pixel.

[0071] As described above, a threshold voltage of a transistor may be compensated by storing a compensation value for the threshold voltage in the transistor using a non-volatile memory element. Accordingly, a separate threshold compensation circuit may be omitted, thereby simplifying the circuit structure.

Claims

1. An organic light emitting display, comprising:

a pixel unit (100) having a plurality of pixels (101);
a data driver (110) connected to data lines (D1...Dm) of the pixel unit (100); and
a scan driver (120) connected to scan lines (S1...Sn) of the pixel unit (100), wherein each pixel (101) includes:

a first transistor (M1) having a first electrode connected to a first power source (ELVDD), a control gate connected to a first node (N1), and a second electrode;
a second transistor (M2) having a first electrode connected to a data line (D1...Dm), a second electrode connected to the first node (N1), and a gate connected to a scan line (S1...Sn);
a third transistor (M3) having a first electrode connected to the second electrode of the first transistor (M1), a gate connected to one of a light emitting control line (E1...En) and the scan line (S1...Sn), and a second electrode;
a capacitor (Cst) connected between the first power source (ELVDD) and the first node (N1); and
an organic light emitting diode (OLED) having an anode connected to the second electrode of the third transistor (M3) and a cathode connected to a second power source (ELVSS),

characterised in that the first transistor (M1) includes a floating gate and an insulating layer between the floating gate and the control gate.

2. The organic light emitting display as claimed in claim 1, wherein:

the scan driver (120) is connected to light emitting control lines (E1...En) of the pixel unit (100), and
the gate of the third transistor (M3) of each pixel is connected to a light emitting control line (E1...En).

3. The organic light emitting display as claimed in one of the claims 1 or 2, wherein the first (M1), second (M2), and third transistors (M3) are PMOS transistors.

4. The organic light emitting display as claimed in one of the claims 1 or 2, wherein the first transistor (M1) is an NMOS transistor, and the second (M2) and third transistors (M3) are PMOS transistors.

5. The organic light emitting display as claimed in claim 1, wherein:

the gate of the third transistor (M3) of each pixel (101) is connected to the scan line (51...Sn), and the third transistor (M3) of each pixel (101) is of an opposite conduction type as the second transistor (M2) of the pixel (101).

6. The organic light emitting display as claimed in claim 5, wherein the first (M1) and second transistors (M2) are PMOS transistors, and the third transistor (M3) is an NMOS transistor.

7. A method of manufacturing an organic light emitting display, comprising:

determining a current flowing into a first transistor (M1) of a pixel (101);
determining a deviation of a threshold voltage of the first transistor (M1) using the determined current; and
compensating for the deviation of the threshold voltage, wherein:

the first transistor (M1) is a floating gate transistor, and
compensating for the deviation of the threshold voltage includes storing a voltage corresponding to the deviation of the threshold voltage in the first transistor (M1).

8. The method as claimed in claim 7, wherein storing the voltage corresponding to the deviation of the threshold voltage includes controlling an amount of electrons stored in a floating gate (205) of the floating gate transistor.

9. The method as claimed in claim 8, further comprising extracting electrons stored in the floating gate (205) into a channel region of the first transistor (M1) to lower the threshold voltage.

10. The method as claimed in claim 9, wherein extracting electrons into the channel region includes providing a high state voltage to a source of the first transistor (M1) and providing a low state voltage to a control gate (207) of the first transistor (M1).

11. The method as claimed in claim 8, further comprising injecting electrons into the floating gate (205) to raise the threshold voltage.

12. The method as claimed in claim 11, wherein injecting electrons into the floating gate (205) includes providing a low state voltage to a source of the first transistor (M1) and providing a high state voltage to a control gate of the first transistor (M1).

FIG. 1
(PRIOR ART)

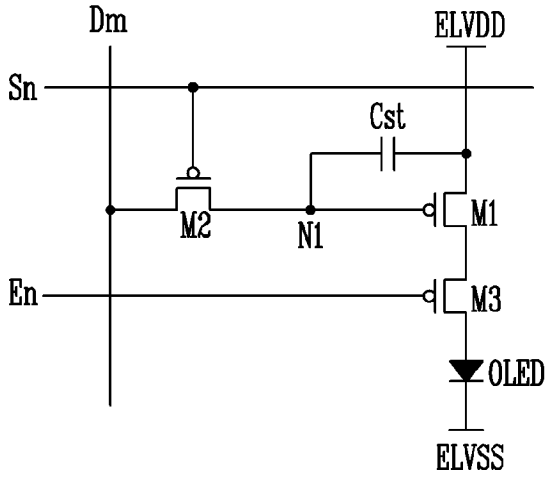


FIG. 2

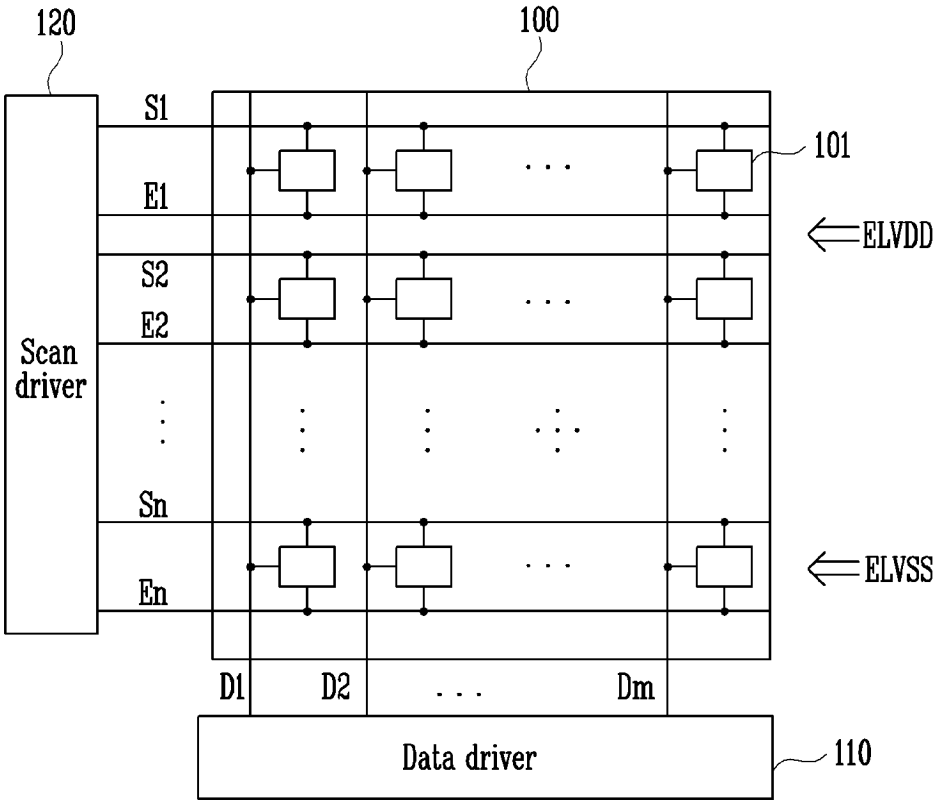


FIG. 3

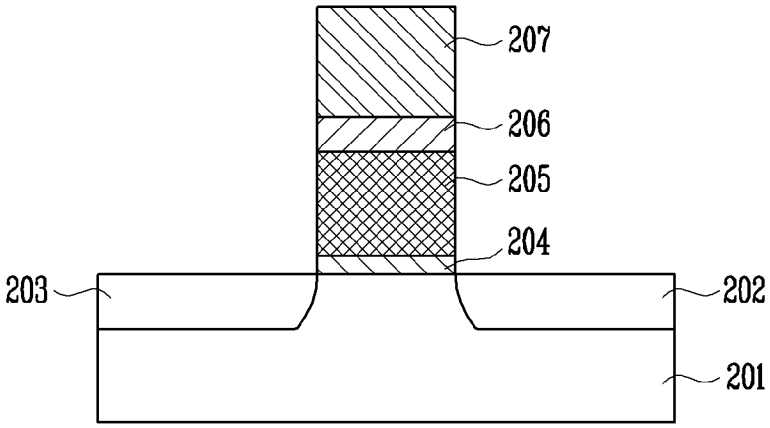


FIG. 4

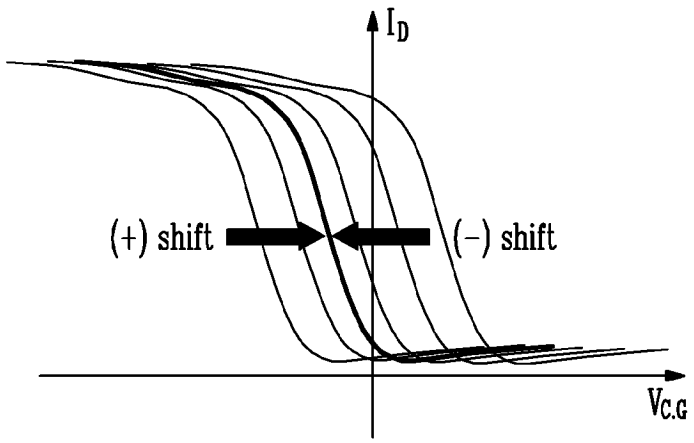


FIG. 5

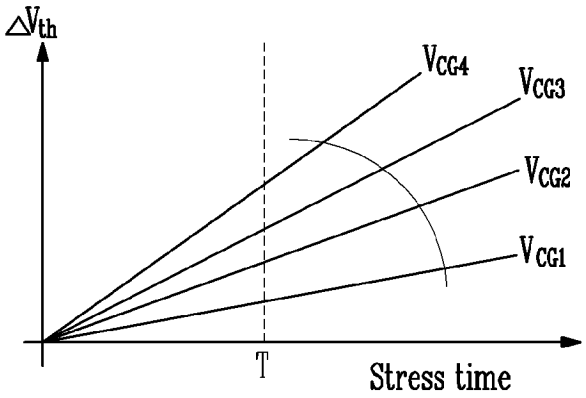


FIG. 6

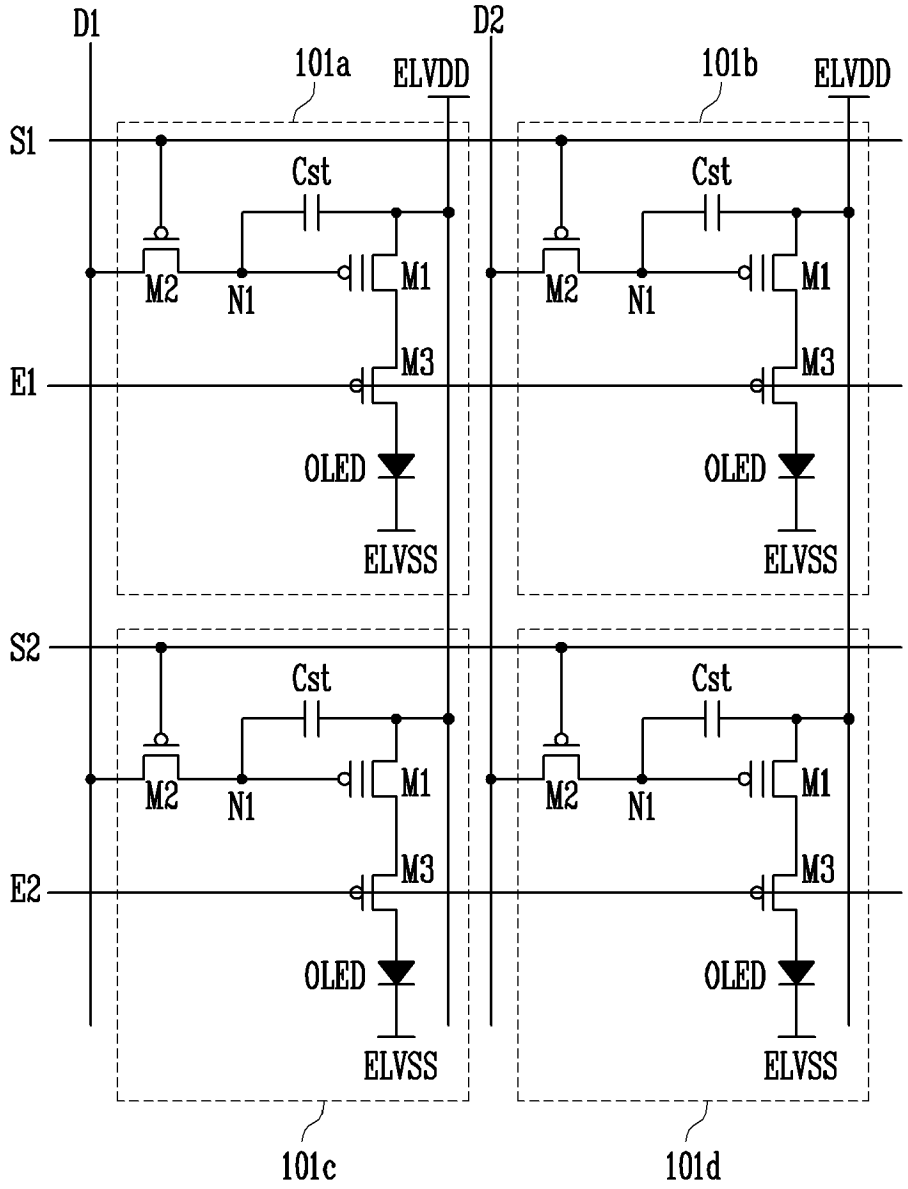

D1
D2
101a
ELVDD
101b
ELVDD
S1
Cst
M2
N1
M1
M3
E1
OLED
ELVSS
S2
E2
101c
101d

FIG. 7

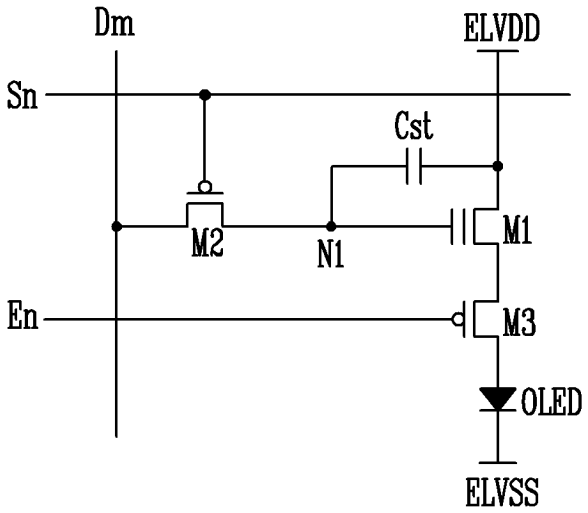
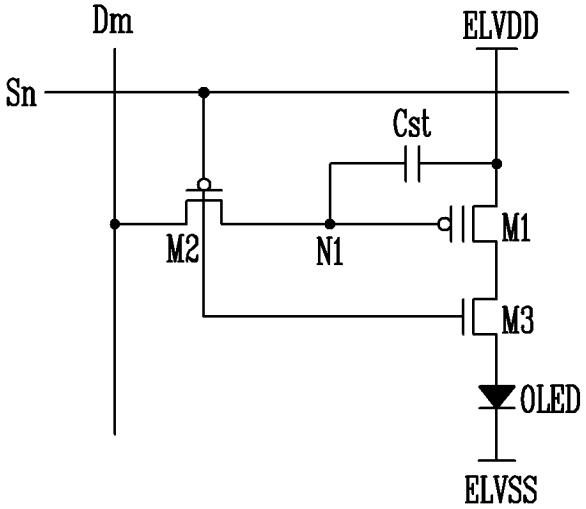

Dm
ELVDD
Sn
Cst
M2
N1
M1
En
M3
OLED
ELVSS

FIG. 8


Dm
ELVDD
Sn
Cst
M2
N1
M1
M3
OLED
ELVSS

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 20070057877 A1 **[0003]**

专利名称(译)	像素，有机发光显示器和相关方法		
公开(公告)号	EP2009618A2	公开(公告)日	2008-12-31
申请号	EP2008158645	申请日	2008-06-20
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星移动显示器有限公司.		
[标]发明人	CHUNG KYUNG HOON SAMSUNG SDI CO LTD		
发明人	CHUNG, KYUNG-HOON SAMSUNG SDI CO., LTD.		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G2300/0819 G09G2300/0852 G09G2300/0857 G09G2300/0861 G09G2320/0295		
代理机构(译)	hengelhaupt，Jürgen		
优先权	1020070061496 2007-06-22 KR		
其他公开文献	EP2009618A3 EP2009618B1		
外部链接	Espacenet		

摘要(译)

像素包括有机发光二极管，具有连接到第一电源的源极的第一晶体管，连接到第一节点的控制栅极，以及连接到第二节点的漏极，其中第一晶体管包括浮置栅极和浮栅和控制栅之间的绝缘层，第二晶体管，其源极连接到数据线，漏极连接到第一节点，栅极连接到扫描线，第三晶体管，源极连接到第二晶体管节点，连接到有机发光二极管的漏极，连接到发光控制线和扫描线之一的栅极，以及连接在第一电源和第二节点之间的电容器。

FIG. 1
(PRIOR ART)

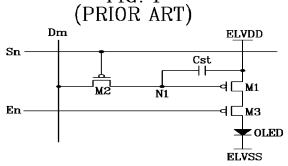


FIG. 2