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(54) **Plixel, organic light emitting display usig the same, and associated methods**

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] Embodiments relate to a pixel, an organic light emitting display using the same, and associated methods, in which degradation of an organic light emitting diode is automatically compensated.

2. Description of the Related Art

[0002] In the manufacture and operation of a display, e.g., a display used to reproduce text, images, video, etc., uniform operation of pixel elements of the display is highly desirable. However, providing such uniform operation may be difficult. For example, in some display technologies, e.g., those utilizing electroluminescent elements such as organic light emitting diodes (OLEDs), operational characteristics, e.g., luminance, of the pixel elements may change over time. Accordingly, there is a need for a display adapted to compensate for changes in the operational characteristics of pixel elements.

[0003] US 2006/253755 A1 proposes compensating for the increasing OLED voltage drift with time by increasing the gate-source voltage of the driving transistor of a pixel.

[0004] EP 1 970 885 A1 deals with automatic compensation of an organic light emitting diode in a display device.

[0005] EP 1 968 039 A1 relates to an organic light emitting display that can suppress image sticking due to a decrease in efficiency of an organic light emitting diode and can compensate for a threshold voltage of a drive transistor.

[0006] "A Self-compensated Voltage Programming Pixel Structure for Active-Matrix Organic Light Emitting Diodes" by S.M. Choi et alteres , published in Proceedings of the International Display Workshops, pages 535 to 538, January 1, 2003, discloses a pixel structure for an AMOLED display that can display full colour images by compensating threshold voltage variation of the driving transistor.

SUMMARY OF THE INVENTION

[0007] Therefore, it is an object of the present invention to provide a pixel, an organic light emitting display device and a driving method thereof capable of compensating for a deterioration of an organic light emitting diode.

[0008] In order to accomplish the above object, there is provided a pixel according to claim 1, an organic light emitting display device as set forth in claim 12, and a driving method of such an organic light emitting display device as set forth in claim 14. Preferred embodiments of the invention are subject of the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The above and other features and advantages will become more apparent to those of ordinary skill in the art by describing in detail exemplary embodiments thereof with reference to the attached drawings, in which:

[0010] FIG. 1 illustrates a schematic view of an organic light emitting display according to a first embodiment;

[0011] FIG. 2 illustrates a schematic view of a pixel according to the first embodiment;

[0012] FIG. 3 illustrates waveforms for driving the pixel illustrated in FIG. 2;

[0013] FIG. 4 illustrates a schematic view of a pixel according to a second embodiment; and

[0014] FIG. 5 illustrates waveforms for driving the pixel illustrated in FIG. 4.

DETAILED DESCRIPTION OF THE INVENTION

[0015] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0016] In the figures, the dimensions of layers and regions may be exaggerated, or elements may be omitted, for clarity of illustration. It will also be understood that when a layer or element is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Further, it will be understood that when a layer is referred to as being "under" another layer, it can be directly under, and one or more intervening layers may also be present. In addition, it will also be understood that when a layer is referred to as being "between" two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present.

[0017] Similarly, where an element is described as being coupled to a second element, the element may be directly coupled to the second element, or may be indirectly coupled to the second element via one or more other elements. Further, where an element is described as being coupled to a second element, it will be understood that the elements may be electrically coupled, e.g., in the case of transistors, capacitors, power sources, nodes, etc. Where two or more elements are described as being coupled to a node, the elements may be directly coupled to the node, or may be coupled via conductive features to which the node is common. Thus, where embodiments are described or illustrated as having two or more elements that are coupled at a common point, it will be appreciated that the elements may be coupled at respective points on a conductive feature that extends between the respective points. Like reference numerals refer to like elements throughout.

[0018] As used herein, in the context of PMOS transistors, when a scan signal is described as being supplied, the scan signal has a LOW polarity, and when the scan signal is described as being stopped, the scan signal has a HIGH polarity. Further, when a light emitting control signal is described as being supplied, the light emitting control signal has a HIGH polarity, and when the light emitting control signal is described as being stopped, the light emitting control signal has a LOW polarity. When signals are described as overlapping, the signals are concurrently supplied.

[0019] FIG. 1 illustrates a schematic view of an organic light emitting display 100 according to a first embodiment, and FIG. 2 illustrates a schematic view of a pixel 140 according to the first embodiment. Referring to FIG. 1, the organic light emitting display 100 may include a pixel unit 130 including pixels 140 coupled to scan lines S0 to Sn+1, light emitting control lines E1 to En+1, and data lines D1 to Dm. The organic light emitting display 100 may further include a scan driver 110 for driving the scan lines S0 to Sn+1 and the light emitting control lines E1 to En+1, a data driver for driving the data lines D1 to Dm, and a timing controller 150 for controlling the scan driver 110 and the data driver 120.

[0020] The scan driver 110 may be supplied with a scan driving control signal SCS from the timing controller 150. The scan driver 110 may generate scan signals in response to the scan driving control signal SCS and sequentially supply the generated scan signals to the scan lines S0 to Sn+1. The scan driver 110 may also generate light emitting control signals in response to the scan driving control signal SCS and sequentially supply the generated light emitting control signals to the light emitting control lines E1 to En+1.

[0021] FIG. 3 illustrates waveforms for driving the pixel illustrated in FIG. 2 Referring to FIG. 3, a pulse width of the light emitting control signal may be greater than a pulse width of the scan signal. The light emitting control signal supplied to an i^{th} light emitting control line Ei (i is a natural number from 1 to n, inclusive) may overlap with the scan signals supplied to an $i\text{-}1^{th}$ scan line Si-1 and an i^{th} scan line Si. The polarity of the pulse of the light emitting control signal may be different, e.g., opposite, from the polarity of the pulse of the scan signal. For example, if the scan line is set to a low polarity, the light emitting control signal may be set to a high polarity.

[0022] The data driver 120 may be supplied with the data driving control signal DSC from the timing controller 150. The data driver 120 may generate data signals in response to the data driving control signal DCS, and may sequentially supply the generated data signals to the data lines D1 to Dm in synchronization with the scan signals.

[0023] The timing controller 150 may generate the data driving control signal DCS and the scan driving control signal SCS corresponding to externally supplied synchronizing signals. The data driving control signal DCS generated from the timing controller 150 may be supplied to the data driver 120, and the scan driving control signal SCS may be supplied to the scan driver 110. The timing controller 150 may also supply externally-provided data DATA to the data driver 120.

[0024] The pixel unit 130 may be supplied with voltages of a first power source ELVDD and a second power source ELVSS, and may distribute the voltages to each pixel 140. The first and second power sources ELVDD and ELVSS may be external to the pixel unit 130.

[0025] Each pixel 140 may generate light, e.g., one of red (R), green (G), or blue (B), corresponding to the data signals. The pixel 140 may generate light having a desired brightness by compensating for deterioration of an organic light emitting diode (OLED) included in the pixel 140, such as deterioration that results in an increase in resistance of the organic light emitting diode (OLED). Further, the pixel 140 may compensate for changes in the threshold voltage of a driving transistor included in the pixel 140. The pixel 140 may be provided with a compensating unit 144 for compensating the deterioration of the organic light emitting diode (OLED) and a pixel circuit 142 that compensates for the threshold voltage of the driving transistor.

[0026] For convenience of explanation, FIG. 2 illustrates only a pixel 140 positioned at i^{th} horizontal line and coupled to a j^{th} data line Dj (j is a natural number from 1 to m, inclusive). Referring to FIGS. 1 and 2, in order to drive the compensating unit 144 and the pixel circuit 142 included in the pixel 140, the pixel 140 positioned at the i^{th} horizontal line may be coupled to the $i\text{-}1^{th}$ scan line Si-1, the i^{th} scan line Si, the $i+1^{th}$ scan line Si+1, the i^{th} light emitting control line Ei, and the $i+1^{th}$ light emitting control line.

[0027] Referring to FIG. 2, the pixels 140 according to the first embodiment may include an organic light emitting diode (OLED), the pixel circuit 142 that compensates for the threshold voltage of a second transistor M2 (driving transistor) supplying current to the organic light emitting diode (OLED), and the compensating unit 144 that compensates for the deterioration of the organic light emitting diode (OLED). The compensating unit 144 may control the voltage of a second node N2 coupled to a gate electrode of the second transistor M2 by lowering the voltage as the organic light emitting diode (OLED) deteriorates, in order to compensate for the deterioration of the organic light emitting diode (OLED).

[0028] An anode electrode of the organic light emitting diode (OLED) may be coupled to the pixel circuit 142, and a cathode electrode of the organic light emitting diode (OLED) may be coupled to the second power source ELVSS. The organic light emitting diode (OLED) may generate a predetermined brightness of light corresponding to an amount of current supplied from the second transistor M2. The first power source ELVDD may be set to a voltage higher than that of the second power source ELVSS. The pixel circuit 142 may supply current to the organic light emitting diode (OLED) and compensate for the threshold voltage of the second transistor M2, and may include first to sixth transistors M1 to M6, and a

storage capacitor Cst.

[0029] A gate electrode of the first transistor M1 may be coupled to the i^{th} scan line Si, and a first electrode of the first transistor M1 may be coupled to the data line Dj. A second electrode of the first transistor M1 may be coupled to a first electrode of the second transistor M2 via a first node N1. The first transistor M1 may be turned-on when the scan signal is supplied to the i^{th} scan line Si, and may thus supply a data signal from the data line Dj to the first electrode of the second transistor M2.

[0030] The gate electrode of the second transistor M2 may be coupled to the second node N2, and a first electrode of the second transistor M2 may be coupled to the second electrode of the first transistor M1 via the first node N1. A second electrode of the second transistor M2 may be coupled to a first electrode of the fifth transistor M5 via a third node N3. The second transistor M2 may supply current, in correspondence with a voltage applied to the second node N2, to the organic light emitting diode (OLED).

[0031] A first electrode of the third transistor M3 may be coupled to the second electrode of the second transistor M2 via the third node N3, and a second electrode of the third transistor M3 may be coupled to the second node N2. A gate electrode of the third transistor M3 may be coupled to the i^{th} scan line Si. The third transistor M3 may be turned-on when the scan signal is supplied to the i^{th} scan line Si, and may thus diode-connect the second transistor M2.

[0032] A first electrode of the fourth transistor M4 may be coupled to the first power source ELVDD, and a second electrode of the fourth transistor M4 may be coupled to the first electrode of the second transistor M2 via the first node N1. A gate electrode of the fourth transistor M4 may be coupled to the i^{th} light emitting control line Ei. The fourth transistor M4 may be turned-on when the light emitting control signal is not supplied to the i^{th} light emitting control line Ei, and may thus electrically connect the first power source ELVDD to the first electrode of the second transistor M2 via the first node N1.

[0033] A first electrode of the fifth transistor M5 may be coupled to the second electrode of the second transistor M2 via the third node N3, and a second electrode of the fifth transistor M5 may be coupled to the organic light emitting diode (OLED). A gate electrode of the sixth transistor may be coupled to the i^{th} light emitting control line Ei. The fifth transistor M5 may be turned-on when the light emitting control line is not supplied to the i^{th} light control line En, and may thus electrically connect the second transistor M2 to the organic light emitting diode (OLED).

[0034] A first electrode of the sixth transistor M6 may be coupled to the second node N2, and a second electrode of the sixth transistor M6 may be coupled to an initialization power source Vint. A gate electrode of the sixth transistor M6 may be coupled to the i-1^{th} scan line Si-1. The sixth transistor M6 may be turned-on when the scan signal is supplied to the i-1^{th} scan line Si-1, and may thus initialize the voltage of the second node N2 with the initialization power source Vint.

[0035] The storage capacitor Cst may be coupled between the second node N2 and the first power source ELVDD. The storage capacitor Cst may be charged with a predetermined voltage corresponding to the voltage applied to the second node N2.

[0036] The compensating unit 144 may control, via the second node N2, the voltage of the gate electrode of the second transistor M2 in correspondence with deterioration of the organic light emitting diode (OLED). For example, the compensating unit 144 may control the voltage of the second node N2 to be lowered as the organic light emitting diode (OLED) is deteriorated, thereby compensating for the deterioration of the organic light emitting diode (OLED). The compensating unit 144 may include seventh to ninth transistors M7 to M9, a first feedback capacitor Cfb1, and a second feedback capacitor Cfb2.

[0037] A first electrode of the seventh transistor M7 may be coupled to a fourth node N4 and a second electrode of the seventh transistor M7 may be coupled to an anode electrode of the organic light emitting diode (OLED). A gate electrode of the seventh transistor M7 may be coupled to the i+1^{th} scan line Si+1. The seventh transistor M7 may be turned-on when the scan signal is supplied to the i+1^{th} scan line Si+1, and may thus electrically connect the fourth node N4 to the organic light emitting diode (OLED).

[0038] A first electrode of the eighth transistor M8 may be coupled to the first power source ELVDD, and a second electrode of the eighth transistor M8 may be coupled to the fourth node N4. A gate electrode of the eighth transistor M8 may be coupled to the i+1^{th} light emitting control line Ei+1. The eighth transistor M8 may be turned-on when the light emitting control signal is not supplied to the i+1^{th} light emitting control line Ei+1, and may thus electrically connect the first power source ELVDD to the fourth node N4.

[0039] A first terminal of the first feedback capacitor Cfb1 may be coupled to the fourth node N4, and a second terminal of the first feedback capacitor Cfb1 may be coupled to a fifth node N5, which may be common to the first and second feedback capacitors Cfb1 and Cfb2. The first feedback capacitor Cfb1 may change the voltage of the fifth node N5 corresponding to an amount of change in voltage of the fourth node N4.

[0040] A first terminal of the second feedback capacitor Cfb2 may be coupled to the fifth node N5, and a second terminal of the second feedback capacitor Cfb2 may be coupled to the second node N2. The feedback capacitor Cfb2 may change the voltage of the second node N2 corresponding to an amount of change in voltage of the fifth node N5.

[0041] As described above, the first feedback capacitor Cfb1 and the second feedback capacitor Cfb2 may be coupled between the fourth node N4 and the second node N2, and may change the voltage of the second node N2 corresponding to the amount of change in voltage of

the fourth node N4.

[0042] A first electrode of the ninth electrode N9 may be coupled to the first power source ELVDD, and a second electrode of the ninth electrode N9 may be coupled to the fifth node N5. A gate electrode of the ninth transistor M9 may be coupled to the $i+1^{th}$ light emitting control line Ei+1. The ninth transistor M9 may be turned-on when the light emitting control signal is supplied to the $i+1^{th}$ light emitting control line Ei+1, and may thus electrically connect the fifth node N5 to the first power source ELVDD. The ninth transistor M9 may have a conductivity type that is different from the other transistors M1 to M8. For example, if the transistors M1 to M8 are PMOS transistors, the ninth transistor M9 may be an NMOS transistor.

[0043] Operation of the above-described pixel 140 will now be described in connection with the waveforms illustrated in FIG. 3. Referring to FIGS. 2 and 3, during a first period T1 illustrated in FIG. 3, the scan signal may be supplied to the scan line Si-1, and the light emitting control signal may be supplied to the i^{th} light emitting control signal Ei.

[0044] When the light emitting control signal is supplied to the light emitting control line Ei, the fourth transistor M4 and the fifth transistor M5 may be turned-off, and when the scan signal is supplied to the scan line Si-1, the sixth transistor M6 may be turned-on. Accordingly, when the sixth transistor M6 is turned-on, the second node N2 may be initialized with the voltage of the initialization power source Vint. The initialization power source Vint may be set to a voltage that is lower than that of the data signal.

[0045] During a second period T2, the supply of the scan signal to the scan line Si-1 may stop, while the supply of the light emitting control signal to the light emitting control line Ei+1 may be maintained. When the supply of the scan signal to the scan line Si-1 stops, the sixth transistor M6 may be turned-off. Further, during the second period T2, the scan signal supplied to the subsequent scan line Si may turn on the first transistor M1 and the third transistor M3. When the third transistor M3 is turned-on, the second transistor M2 may be diode-connected. Further, when the first transistor M1 is turned-on, the data signal from the data line Dj may be supplied to the first electrode of the second transistor M2.

[0046] As described above, the voltage of the second node N2 may be initialized with the voltage of the initialization power source Vint during the first period T1, and the second transistor M2 may be turned-on. Accordingly, the data signal supplied via the first transistor M1 may be supplied to the second node N2 via the second transistor M2 and the third transistor M3. Thus, the second node N2 may be supplied with a signal, the voltage of which corresponds to the data signal and the threshold voltage of the second transistor M2. The storage capacitor Cst may be charged with a voltage corresponding to the voltage supplied to the second node N2.

[0047] Also during the second period T2, when the light emitting control signal is supplied to the $i+1^{th}$ light emitting control line Ei+1, the ninth transistor M9 may be turned-on and the eighth transistor M8 may be turned-off. When the ninth transistor M9 is turned-on, the voltage of the first power source ELVDD may be supplied to the fifth node N5. Thus, the fifth node N5 may maintain the voltage of the first power source ELVDD during the period when the voltage corresponding to the data signal is applied.

[0048] During a third period T3, the light emitting control signal supplied to the light emitting control line Ei and the scan signal supplied to the scan line Si may stop. When the supply of the scan signal to the scan line Si stops, the first transistor M1 and the third transistor M3 may be turned-off. When the supply of the light emitting control signal to the light emitting control line Ei stops, the fourth transistor M4 and the fifth transistor M5 may be turned-on. When the fourth transistor M4 and the fifth transistor M5 are turned-on, the first power source ELVDD, the fourth transistor M4, the second transistor M2, the fifth transistor M5, and the organic light emitting diode (OLED) may be electrically coupled. Thus, the second transistor M2 may supply a current, corresponding to the voltage applied to the second node N2, to the organic light emitting diode (OLED), so as to illuminate the organic light emitting diode (OLED).

[0049] Also during the third period T3, the seventh transistor M7 may be maintained in the turned-on state by a scan signal supplied to the next scan line Si+1. Accordingly, the fourth node N4 may be supplied with a voltage Voled applied to the organic light emitting diode (OLED) during the third period T3.

[0050] Thereafter, during a fourth period T4, the scan signal supplied to the scan line Si+1 and the light emitting control signal supplied to the light emitting control line Ei+1 may stop. When the supply of the scan signal to the scan line Si+1 stops, the seventh transistor M7 may be turned-off When the supply of the light emitting control line to the light emitting control signal Ei+1 stops, the ninth transistor M9 may be turned off and the eighth transistor M8 may be turned-on.

[0051] When the eighth transistor M8 is turned-on, the voltage of the fourth node N4 may rise from the voltage Voled of the organic light emitting diode (OLED) to the voltage of the first power source ELVDD. Further, since the ninth transistor M9 may be turned-off during the fourth period T4, the fifth node N5 may be set to a floating state. Accordingly, the voltage of the fifth node N5 may rise by an amount corresponding to the increase in voltage of the fourth node N4. Likewise, the voltage of the second node N2, which may also be in a floating state, may rise by an amount corresponding to the rise in the voltage of the fifth node N5. Thus, the voltage of the second node N2 may be controlled corresponding to the amount of voltage rise of the fourth node N4 in the fourth period T4, and, subsequently, the second transistor M2 may supply the current corresponding to the voltage applied to the second node N2 to the organic light emitting diode (OLED).

[0052] The organic light emitting diode (OLED) may deteriorate over time, e.g., due to exposure to air and/or moisture, or due to operation of the organic light emitting diode (OLED). If the organic light emitting diode (OLED) is deteriorated, the voltage Voled applied to the organic light emitting diode (OLED) may rise, i.e., when the current is supplied to the organic light emitting diode (OLED), the voltage applied to the organic light emitting diode (OLED) may rise as the organic light emitting diode (OLED) is deteriorated.

[0053] As the organic light emitting diode (OLED) is deteriorated, the amount of the voltage rise at the fourth node N4 may become smaller due to a rise in the voltage Voled of the organic light emitting diode (OLED) supplied to the fourth node N4. When the voltage Voled applied to the organic light emitting diode (OLED) rises, the amount of voltage rise may be reduced when the voltage of the first power source ELVDD is supplied to the fourth node N4. Moreover, as the amount of the voltage rise of the fourth node N4 is reduced, the amount of the voltage rise of the fifth node N5 and the second node N2 may be correspondingly reduced. Accordingly, the amount of current supplied from the second transistor M2 to the organic light emitting diode (OLED) may increase for a given data signal. Thus, according to the first embodiment, as the organic light emitting diode (OLED) deteriorates, the amount of current supplied from the second transistor M2 may increase so that degradation in brightness due to the deterioration of the organic light emitting diode (OLED) may be compensated.

[0054] FIG. 4 illustrates a schematic view of a pixel 140' according to a second embodiment. For convenience of explanation, FIG. 4 illustrates a pixel 140' positioned at the i^{th} horizontal line and coupled to the i^{th} data line (Dj).

[0055] The pixel 140' may be similar to the pixel 140 described above. In particular, the pixel 140' may include the pixel circuit 142, which may be coupled to light emitting control line Ei, scan lines Si-1 and Si, and data line Dj, in the same manner as the pixel circuit 142 described above in connection with the first embodiment. The pixel 140' may also include a compensating unit 144', which may be similar to the compensation unit 144 described above in connection with the first embodiment, except for the construction of a seventh transistor M7' and the configuration of the signal lines coupled to the compensation unit 144'. In particular, the compensating unit 144' may have an NMOS transistor as the seventh transistor M7', whereas the compensating unit 144 may have a PMOS transistor as the seventh transistor M7. Further, in the compensating unit 144', the seventh transistor M7' and the eighth transistor M8 may both be coupled to an $i+2^{th}$ light emitting control line Ei+2. Additionally, in the compensating unit 144', the ninth transistor M9 may be coupled to the initialization power source Vint, whereas, in the compensating unit 144, the ninth transistor M9 may be coupled to the first power source ELVDD. In an organic light emitting display including pixels 140', scan lines S0 to Sn and light emitting control lines E1 to En+2 may be provided (not shown), which may be coupled to a suitably configured scan driver. In the following description of the second embodiment, the description of features that are the same as those in the first embodiment may be omitted in order to avoid repetition.

[0056] Referring to FIG. 4, the pixel 140' at the i^{th} horizontal line may be coupled to the $i-1^{th}$ scan line Si-1, the i^{th} scan line Si, the i^{th} light emitting control line Ei, the $i+1^{th}$ light emitting control line Ei+1, and the i+2 light emitting control line Ei+2.

[0057] In the pixel 140' according to the second embodiment, the ninth transistor M9 may be coupled between the fifth node N5 and the initialization power source Vint. The ninth transistor M9 may be turned-on when the light emitting control signal is supplied to the $i+1^{th}$ light emitting control line Ei+1, and may thus supply the initialization power source Vint to the fifth node N5.

[0058] The initialization power source Vint supplied to the fifth node N5 may maintain the voltage of the fifth node N5 constant, irrespective of a voltage change of the second node N2. The ninth transistor M9 may be coupled to the initialization power source Vint or the first power source ELVDD to allow the voltage of the fifth node N5 to be maintained constant.

[0059] Also, in the pixel 140' according to the second embodiment, the gate electrodes of the seventh transistor M7' and the eighth transistor M8 may be coupled to the i+2 light emitting control line Ei+2. The seventh transistor M7' and the eighth transistor M8 may thus be alternately turned-on and turned-off, i.e., they may operate in opposition such that one is turned-off while the other is turned-on. In an implementation, the seventh transistor M7' may be an NMOS transistor and the eighth transistor M8 may be a PMOS transistor.

[0060] FIG. 5 illustrates waveforms for driving the pixel 140' illustrated in FIG. 4. In particular, FIG. 5 illustrates the waveforms shown in FIG. 3, in addition to a waveform applied to the $i+2^{th}$ light emitting control line Ei+2.

[0061] Referring to FIGS. 4 and 5, during the first period T1, the scan signal may be supplied to the $i-1^{th}$ scan line Si-1 and the light emitting control signal may be supplied to the i^{th} light emitting control line Ei. When the light emitting control signal is supplied to the i^{th} light emitting control line Ei, the fourth transistor M4 and the fifth transistor M5 may be turned-off. When the scan signal is supplied to the $i-1^{th}$ scan line Si-1, the sixth transistor M6 may be turned-on. When the sixth transistor M6 is turned-on, the voltage of the second node N2 may be initialized with the initialization power source Vint. The initialization power source Vint may be set to a voltage that is lower than that of the data signal.

[0062] During the second period T2, the supply of the scan signal to the $i-1^{th}$ scan line Si-1 may stop. A light emitting control signal may be supplied to the $i+1^{th}$ light emitting control line Ei+1 during the second period T2. When the supply of the scan signal to the scan line Si-1 stops, the sixth transistor M6 may be turned-off. The scan

signal may be supplied to the subsequent scan line Si during the second period T2, such that the first transistor M1 and the third transistor M3 may be turned-on.

[0063] When the third transistor M3 is turned-on, the second transistor M2 may be diode-connected. When the first transistor M1 is turned-on, the data signal supplied to the data line Dj may be supplied to the first electrode of the second transistor M2 via the first node N1. As described above, the voltage of the second node N2 may be initialized with the voltage of the initialization power source Vint during the first period T1, and the second transistor M2 may be turned-on. Accordingly, during the second period T2, the data signal supplied by the first transistor M1 may be supplied to the second node N2 via the second transistor M2, the third node N3, and the third transistor M3. Accordingly, the second node N2 may be supplied with a voltage corresponding to the data signal and the threshold voltage of the second transistor M2. The storage capacitor Cst may be charged with a voltage corresponding to the voltage supplied to the second node N2.

[0064] Also during the second period T2, when the light emitting control signal is supplied to the $i+1^{th}$ light emitting control line Ei+1, the ninth transistor M9 may be turned-on. When the ninth transistor M9 is turned-on, the voltage of the initialization power source Vint may be supplied to the fifth node N5. Thus, the fifth node N5 may maintain the voltage of the initialization power source Vint during the period where the voltage corresponding to the data signal is applied.

[0065] The light emitting control signal supplied to the i^{th} light emitting control line Ei and the scan signal supplied to the i^{th} scan line Si may stop during a third period T3. When the supply of the scan signal to the i^{th} scan line Si stops, the first transistor M1 and the third transistor M3 may be turned-off. When the supply of the light emitting control signal to the light emitting control line Ei stops, the fourth transistor M4 and the fifth transistor M5 may be turned-on. When the fourth transistor M4 and the fifth transistor M5 are turned-on, the first power source ELVDD, the fourth transistor M4, the second transistor M2, the fifth transistor M5, and the organic light emitting diode (OLED) may be electrically coupled. Thus, the second transistor M2 may supply a current, corresponding to the voltage applied to the second node N2, to the organic light emitting diode (OLED), so as to illuminate the organic light emitting diode (OLED).

[0066] Meanwhile, when the light emitting control signal is supplied to the $i+2^{th}$ light emitting control line Ei+2, the seventh transistor M7' may be turned-on, and the voltage Voled applied to the organic light emitting diode OLED may be supplied to the fourth node N4.

[0067] During the fourth period T4, the supply of the light emitting control signal to the $i+1^{th}$ light emitting control line Ei+1 may stop. When the supply of the light emitting control signal to the light emitting control line Ei+1 stops, the ninth transistor M9 may be turned-off, and the fifth node N5 may thus be placed in a floating state.

[0068] During a fifth period T5, the supply of the light emitting control signal to the $i+2^{th}$ light emitting control line Ei+2 may stop. Accordingly, during the fifth period T5, the seventh transistor M7' may be turned-off, and the eighth transistor M8 may be turned-on. When the eighth transistor M8 is turned-on, the voltage of the fourth node N4 may rise from the voltage Voled of the organic light emitting diode (OLED) to the voltage of the first power source ELVDD. At this time, since the fifth node N5 may be in a floating state, the voltage of the fifth node N5 may rise by an amount corresponding to the amount of voltage rise of the fourth node N4. Further, the voltage of the second node N2 set to the floating state may rise by a voltage amount corresponding to the amount of voltage rise of the fifth node N5. Thus, the voltage of the second node N2 may be controlled corresponding to the amount of voltage rise of the fourth node N4 in the fifth period T5. Subsequently, the second transistor M2 may supply current, in an amount corresponding to the voltage applied to the second node N2, to the organic light emitting diode (OLED).

[0069] As in the first embodiment, the organic light emitting diode (OLED) may deteriorate over time. As the organic light emitting diode (OLED) deteriorates, the voltage applied to the organic light emitting diode (OLED) may rise, i.e., when the current is supplied to the organic light emitting diode (OLED), the voltage Voled applied to the organic light emitting diode (OLED) may rise as the organic light emitting diode (OLED) deteriorates. Then, the current amount supplied from the second transistor M2 to the organic light emitting diode (OLED) may increase for a given data signal. Thus, as the organic light emitting diode (OLED) deteriorates, the amount of current supplied from the second transistor M2 may increase so that a degradation in brightness due to the deterioration of the organic light emitting diode (OLED) may be compensated.

[0070] As described above, embodiments may compensate for a deterioration in characteristics of an organic light emitting diode by controlling a voltage of a gate electrode of a driving transistor in correspondence with the deterioration of the organic light emitting diode. Further, the threshold voltage of the driving transistor may be compensated, such that images with uniform brightness may be displayed despite deviation in the threshold voltage.

Claims

1. A pixel (140, 140') comprising:

an organic light emitting diode (OLED);
a second transistor (M2) for supplying current to the organic light emitting diode (OLED);
a storage capacitor (Cst) coupled between a first node (N2) and a first power supply (ELVDD); and

a compensating unit (144, 144') for controlling the voltage of a gate electrode of the second transistor (M2) in order to compensate for a deterioration of the organic light emitting diode (OLED),
wherein the compensating unit (144, 144') includes:

a seventh transistor (M7) having a first electrode coupled to a second node (N4) and a second electrode coupled to an anode of the organic light emitting diode (OLED), wherein the first electrode of seventh transistor (M7) is a first one of a drain electrode and a source electrode and wherein the second electrode of the seventh transistor (M7) is a remaining one of the drain electrode and the source electrode;
an eighth transistor (M8) having a first electrode coupled to the first power supply (ELVDD) and a second electrode coupled to the second node (N4), wherein the first electrode of eighth transistor (M8) is a first one of a drain electrode and a source electrode and wherein the second electrode of the eighth transistor (M8) is a remaining one of the drain electrode and the source electrode; and
a first capacitor (Cfb1) having a first electrode connected to the second node (N4);
characterised in that the pixel further comprises a pixel circuit (142, 142') for compensating for the threshold voltage of the second transistor (M2) and **in that** the compensating unit further comprises:

a second feedback capacitor (Cfb2) having a first electrode coupled to a second electrode of the first feedback capacitor (Cfb1) and a second electrode coupled to the first node (N2) electrically coupled to the gate electrode of the second transistor (M2); and
a ninth transistor (M9) having a first electrode coupled to a third node (N5), which is a common node of the first and second feedback capacitors (Cfb1, Cfb2), and a second electrode coupled to a predetermined voltage supply (ELVDD, Vint), wherein the ninth transistor (M9) is of a different conductivity type than the second transistor (M2) and the eighth transistor (M8) and wherein the first electrode of ninth transistor (M9) is a first one of a drain electrode and a source electrode and wherein the second electrode of the ninth transistor (M9) is a remaining one of the drain electrode and the source electrode.

2. The pixel (140, 140') as claimed in claim 1, wherein the pixel circuit (142, 142') includes:

a first transistor (M1) coupled to an i^{th} scan line (Si) and data line (Dj) and turned-on when a scan signal is supplied to the i^{th} scan line (Si) to supply a data signal supplied to the data line (Dj) to the first electrode of the second transistor (M2);
a third transistor (M3) coupled between the second electrode of the second transistor (M2) and the first node (N2) and turned-on when the scan signal is supplied to the i^{th} scan line (Si);
a fourth transistor (M4) coupled between an initialization power supply (Vint) and the first node (N2), and turned-on when the scan signal is supplied to an i-1^{th} scan line (Si-1);
a fifth transistor (M5) coupled between the first electrode of the second transistor (M2) and the first power supply (ELVDD) and turned-on when a light emitting control signal is not supplied to an i^{th} light emitting control line (Ei); and
a sixth transistor (M6) coupled between the second electrode of the second transistor (M2) and the organic light emitting diode (OLED) and turned-on when the light emitting control signal is not supplied to the i^{th} light emitting control line (Ei).

3. The pixel (140, 140') as claimed in claim 2, wherein the initialization power supply (Vint) is set to a voltage value lower than the data signal.

4. The pixel (140, 140') as claimed in one of claims 2 or 3, wherein the seventh and eighth transistors (M7, M8) are alternatively turned-on and turned-off.

5. The pixel (140, 140') as clamed in claim 4, wherein the light emitting control signal supplied to the i^{th} light emitting control line (Ei) is supplied to be overlapped with the scan signals supplied to the i-1^{th} scan line (Si-1) and the i^{th} scan line (Si).

6. The pixel (140, 140') as claimed in claim 5, wherein the seventh transistor (M7) is turned on when the scan signal is supplied to i+1^{th} scan line (Si+1) to supply the voltage applied to the organic light emitting diode (OLED) to the second node (N4); and
the eighth transistor (M8) is turned on when the light emitting control signal is not supplied to i+1^{th} light emitting control line (Ei+1) to supply the voltage of the first power supply (ELVDD) to the second node (N4).

7. The pixel (140, 140') as claimed in claim 5, wherein the seventh transistor (M7) is turned on when the light emitting control signal is supplied to an i+2^{th} light emitting control line (Ei+2) to supply the voltage applied to the organic light emitting diode (OLED) to the second node (N4); and

the eighth transistor (M8) is turned on when the light emitting control signal is not supplied to an i+2th light emitting control line (Ei+2) to supply the voltage of the first power (ELVDD) supply to the second node (N4).

8. The pixel (140, 140') as claimed in claim 7, wherein the seventh transistor (M7) is formed in an NMOS, and the eighth transistor (M8) is formed in a PMOS.

9. The pixel (140, 140') as claimed in claim 5, wherein the ninth transistor (M9) is turned on when the light emitting control signal is supplied to i+1th light emitting control line (Ei+1) to maintain the voltage of the third node (N5) with the predetermined voltage supply (ELVDD, Vint).

10. The pixel (140, 140') as claimed in claim 9, wherein the ninth transistor (M9) is formed in an NMOS.

11. The pixel (140, 140') as claimed in claim 9, wherein the predetermined voltage supply (ELVDD, Vint) is any one of the first power supply (ELVDD) and the initialization power supply (Vint).

12. An organic light emitting display device (100) including:

a scan driver (110) for sequentially supplying scan signals to scan lines (S0...Sn+1) and sequentially supplying light emitting control signals to light emitting control lines (E0...En+1);
a data driver (120) for supplying data signals to data lines (D1...Dm); and
pixels (140, 140') positioned in regions partitioned by the scan lines (S0...Sn+1) and the data lines (D1...Dm),
characterised in that each of the pixels is a pixel according to one of the preceding claims.

13. The organic light emitting display device (100) as claimed in claim 12, wherein the scan driver (110) supplies the light emitting control signals to an ith light emitting control line (Ei) to be overlapped with the scan signals supplied to an i-1th (i is a natural number) scan line (Si-1) and an ith scan line (Si).

14. A driving method of the organic light emitting display device (100) according to one of claims 12 or 13, the driving method including the steps of:

initializing the voltage of the gate electrode of the second transistor (M2) with the voltage of an initialization power supply (Vint);
then charging the voltage corresponding to the threshold voltage of the second transistor (M2) and a data signal in a storage transistor (Cst) by connecting the second transistor (M2) in the form of a diode;
then supplying the current corresponding to the voltage charged in the storage capacitor (Cst) to the organic light emitting diode (OLED);
applying the voltage of the organic light emitting diode (OLED) to the second node (N4) when said current is supplied to the organic light emitting diode (OLED);
then maintaining a third node (N5), which is a common terminal of the first and second feedback capacitors (Cfb1, Cfb2) at a constant voltage during the steps of charging the voltage in the storage capacitor (Cst) and of applying the voltage of the organic light emitting diode (OLED) to the second node (N4); and
then controlling the voltage of the gate electrode of the driving transistor (M2) by setting the third node (N5) to the state of floating and at the same time, raising the voltage of the second node (N4) to the voltage of the first power supply (ELVDD).

15. The driving method of an organic light emitting display device (100) as claimed in claim 14, wherein the constant voltage is the voltage supplied from any one of the initialization power supply (Vint) and the first power supply (ELVDD).

16. The driving method of an organic light emitting display device (100) as claimed in one of claims 14 or 15, wherein the initialization power supply (Vint) is set to a voltage value lower than the data signal.

17. The driving method of an organic light emitting display device (100) as claimed in one of the claims 14 through 16, wherein the first and second transistors (M7, M8) are alternatively turned-on and turned-off.

Patentansprüche

1. Pixel (140, 140') umfassend:

eine organische Leuchtdiode (OLED);
einen zweiten Transistor (M2) zum Zuführen von Strom an die organische Leuchtdiode (OLED);
einen zwischen einen ersten Knoten (N2) und eine erste Stromversorgung (ELVDD) gekoppelten Speicherkondensator (Cst); und
eine Kompensationseinheit (144, 144') zum Steuern der Spannung einer Gate-Elektrode des zweiten Transistors (M2) zum Kompensieren einer Verschlechterung der organischen Leuchtdiode (OLED),

wobei die Kompensationseinheit (144, 144') umfasst:

einen siebten Transistor (M7) mit einer ersten Elektrode, die mit einem zweiten Knoten (N4) gekoppelt ist, und einer zweiten Elektrode, die mit einer Anode der organischen Leuchtdiode (OLED) gekoppelt ist, wobei die erste Elektrode des siebten Transistors (M7) eine erste einer Drain-Elektrode und einer Source-Elektrode ist und wobei die zweite Elektrode des siebten Transistors (M7) eine verbleibende der Drain-Elektrode und der Source-Elektrode ist;
einen achten Transistor (M8) mit einer ersten Elektrode, die mit der ersten Stromversorgung (ELVDD) gekoppelt ist, und einer zweiten Elektrode, die mit dem zweiten Knoten (N4) gekoppelt ist, wobei die erste Elektrode des achten Transistors (M8) eine erste einer Drain-Elektrode und einer Source-Elektrode ist und wobei die zweite Elektrode des achten Transistors (M8) eine verbleibende der Drain-Elektrode und der Source-Elektrode ist;
einen ersten Kondensator (Cfb1) mit einer ersten Elektrode, die mit dem zweiten Knoten (N4) verbunden ist;
dadurch gekennzeichnet, dass
das Pixel weiterhin eine Pixelschaltung (142, 142') zum Kompensieren der Schwellenspannung des zweiten Transistors (M2) umfasst, und **dadurch**, dass die Kompensationseinheit weiterhin umfasst:

einen zweiten Feedback-Kondensator (Cfb2) mit einer ersten Elektrode, die mit einer zweiten Elektrode des ersten Feedback-Kondensators (Cfb1) gekoppelt ist,
und eine zweite Elektrode, die mit dem ersten Knoten (N2) gekoppelt ist, der elektrisch mit der Gate-Elektrode des zweiten Transistors (M2) gekoppelt ist; und
einen neunten Transistor (M9) mit einer ersten Elektrode, die mit einem dritten Knoten (N5) gekoppelt ist, der ein gemeinsamer Knoten des ersten und zweiten Feedback-Kondensators (Cfb1, Cfb2) ist, und einer zweiten Elektrode, die mit einer vorgegebenen Spannungsversorgung (ELVDD, Vint) gekoppelt ist, wobei der neunte Transistor (M9) von einem anderen Leitfähigkeitstyp ist als der zweite Transistor (M2) und der achte Transistor (M8), und wobei die erste Elektrode des neunten Transistors (M9) eine erste einer Drain-Elektrode und einer Source-Elektrode ist und
wobei die zweite Elektrode des neunten Transistors (M9) eine verbleibende der Drain-Elektrode und der Source-Elektrode ist.

2. Pixel (140, 140') nach Anspruch 1, wobei die Pixelschaltung (142, 142') umfasst:

einen ersten Transistor (M1) der mit einer i'ten Abtastzeile (Si) und Datenleitung (Dj) gekoppelt ist und eingeschaltet wird, wenn der i'ten Abtastzeile (Si) ein Abtastsignal zugeführt wird, um ein der Datenleitung (Dj) zugeführtes Datensignal der ersten Elektrode des zweiten Transistors (M2) zuzuführen;
einen dritten Transistor (M3), der zwischen die zweite Elektrode des zweiten Transistors (M2) und den ersten Knoten (N2) gekoppelt ist und eingeschaltet wird, wenn das Abtastsignal der i'ten Abtastzeile (Si) zugeführt wird;
einen vierten Transistor (M4), der zwischen eine Initialisierungsstromversorgung (Vint) und den ersten Knoten (N2) gekoppelt ist und eingeschaltet wird, wenn das Abtastsignal einer i-1'ten Abtastzeile (Si-1) zugeführt wird;
einen fünften Transistor (M5), der zwischen die erste Elektrode des zweiten Transistors (M2) und die erste Stromversorgung (ELVDD) gekoppelt ist und eingeschaltet wird, wenn ein lichtemittierendes Steuersignal nicht einer i'ten lichtemittierenden Steuerleitung (Ei) zugeführt wird; und
einen sechsten Transistor (M6), der zwischen die zweite Elektrode des zweiten Transistors (M2) und die organische Leuchtdiode (OLED) gekoppelt ist und eingeschaltet wird, wenn das lichtemittierende Steuersignal nicht der i'ten lichtemittierenden Steuerleitung (Ei) zugeführt wird.

3. Pixel (140, 140') nach Anspruch 2, wobei die Initialisierungsstromversorgung (Vint) auf einen Spannungswert niedriger als das Datensignal gesetzt wird.

4. Pixel (140, 140') nach einem der Ansprüche 2 oder 3, wobei der siebte und achte Transistor (M7, M8) abwechselnd ein- und ausgeschaltet werden.

5. Pixel (140, 140') nach Anspruch 4, wobei das der i'ten lichtemittierenden Steuerleitung (Ei) zugeführte lichtemittierende Steuersignal so zugeführt wird, das es mit den Abtastsignalen, die der i-1'ten Abtastzeile (Si-1) und der i'ten Abtastzeile (Si) zugeführt werden, überlappt.

6. Pixel (140, 140') nach Anspruch 5, wobei der siebte Transistor (M7) eingeschaltet wird, wenn das Abtastsignal der i+1'ten Abtastzeile (Si+1) zugeführt wird, um die an der organischen Leuchtdiode (OLED) anliegende Spannung dem zweiten Knoten (N4) zuzuführen; und
der achte Transistor (M8) eingeschaltet wird, wenn das lichtemittierende Steuersignal nicht der i+1'ten

lichtemittierenden Steuerleitung (Ei+1) zugeführt wird, um die Spannung der ersten Stromversorgung (ELVDD) dem zweiten Knoten (N4) zuzuführen.

7. Pixel (140, 140') nach Anspruch 5, wobei der siebte Transistor (M7) eingeschaltet wird, wenn das lichtemittierende Steuersignal einer i+2'ten lichtemittierenden Steuerleitung (Ei+2) zugeführt wird, um die an der organischen Leuchtdiode (OLED) anliegende Spannung dem zweiten Knoten (N4) zuzuführen; und
der achte Transistor (M8) eingeschaltet wird, wenn das lichtemittierende Steuersignal nicht einer i+2'ten lichtemittierenden Steuerleitung (Ei+2) zugeführt wird, um die Spannung der ersten Stromversorgung (ELVDD) dem zweiten Knoten (N4) zuzuführen.

8. Pixel (140, 140') nach Anspruch 7, wobei der siebte Transistor (M7) in einem NMOS ausgebildet ist und der achte Transistor (M8) in einem PMOS ausgebildet ist.

9. Pixel (140, 140') nach Anspruch 5, wobei der neunte Transistor (M9) eingeschaltet wird, wenn das lichtemittierende Steuersignal der i+1'ten lichtemittierenden Steuerleitung (Ei+1) zugeführt wird, um die Spannung des dritten Knotens (N5) mit der vorgegebenen Spannungsversorgung (ELVDD, Vint) aufrechtzuerhalten.

10. Pixel (140, 140') nach Anspruch 9, wobei der neunte Transistor (M9) in einem NMOS ausgebildet ist.

11. Pixel (140, 140') nach Anspruch 9, wobei die vorgegebene Spannungsversorgung (ELVDD, Vint) entweder die erste Stromversorgung (ELVDD) oder die Initialisierungsstromversorgung (Vint) ist.

12. Organische lichtemittierende Anzeigevorrichtung (100) umfassend:

einen Abtasttreiber (110) zum aufeinanderfolgenden Zuführen von Abtastsignalen an Abtastzeilen (S0...Sn+1) sowie zum aufeinanderfolgenden Zuführen von lichtemittierenden Steuersignalen an lichtemittierende Steuerleitungen (E0...En+1);
eine Datentreiber (120) zum Zuführen von Datensignalen an Datenleitungen (D1...Dm); und
Pixel (140, 140'), die sich in durch die Abtastzeilen (S0...Sn+1) und die Datenleitungen (D1...Dm) unterteilten Regionen befinden,
dadurch gekennzeichnet, dass
jedes der Pixel ein Pixel nach einem der vorangegangenen Ansprüche ist.

13. Organische lichtemittierende Anzeigevorrichtung (100) nach Anspruch 12, wobei der Abtasttreiber (110) die lichtemittierenden Steuersignale einer i'ten lichtemittierenden Steuerleitung (Ei) derart zuführt, dass sie mit den Abtastsignalen, die einer i'-1'ten (i ist eine natürliche Zahl) Abtastzeile (Si-1) und einer i'ten Abtastzeile (Si) zugeführt werden, überlappen.

14. Verfahren zum Ansteuern der organischen lichtemittierenden Anzeigevorrichtung (100) nach einem der Ansprüche 12 oder 13, wobei das Ansteuerverfahren folgende Schritte umfasst:

Initialisieren der Spannung der Gate-Elektrode des zweiten Transistors (M2) mit der Spannung einer Initialisierungsstromversorgung (Vint);
dann Laden der Spannung entsprechend der Schwellenspannung des zweiten Transistors (M2) und eines Datensignals in einen Speichertransistor (Cst) durch Verbinden des zweiten Transistors (M2) in Form einer Diode;
dann Zuführen des der in den Speicherkondensator (Cst) geladenen Spannung entsprechenden Stroms an die organische Leuchtdiode (OLED);
Anlegen der Spannung der organischen Leuchtdiode (OLED) an den zweiten Knoten (N4), wenn der Strom der organischen Leuchtdiode (OLED) zugeführt wird;
dann Aufrechterhalten einer konstanten Spannung an einem dritten Knoten (N5), der ein gemeinsamer Anschluss des ersten und zweiten Feedback-Kondensators (Cfb1, Cfb2) ist, während der Schritte des Ladens der Spannung in den Speicherkondensator (Cst) und des Anlegens der Spannung der organischen Leuchtdiode (OLED) an den zweiten Knoten (N4); und
dann Steuern der Spannung der Gate-Elektrode des Treibertransistors (M2) durch Versetzen des dritten Knotens (N5) in den Schwebezustand und gleichzeitig Erhöhen der Spannung des zweiten Knotens (N4) auf die Spannung der ersten Stromversorgung (ELVDD).

15. Verfahren zum Ansteuern einer organischen lichtemittierenden Anzeigevorrichtung (100) nach Anspruch 14, wobei die konstante Spannung die Spannung ist, die entweder von der Initialisierungsstromversorgung (Vint) oder der ersten Stromversorgung (ELVDD) zugeführt wird.

16. Verfahren zum Ansteuern einer organischen lichtemittierenden Anzeigevorrichtung (100) nach einem der Ansprüche 14 oder 15, wobei die Initialisierungsstromversorgung (Vint) auf einen Spannungswert gesetzt wird, der niedriger ist als das Datensignal.

17. Verfahren zum Ansteuern einer organischen lichtemittierenden Anzeigevorrichtung (100) nach einem der Ansprüche 14 bis 16, wobei der erste und zweite

Transistor (M7, M8) abwechselnd ein- und ausgeschaltet werden.

Revendications

1. Pixel (140, 140'), comprenant :

une diode électro-luminescente organique (OLED) ;
un deuxième transistor (M2) pour délivrer un courant à la diode électro-luminescente organique (OLED) ;
un condensateur de stockage (Cst) couplé entre un premier noeud (N2) et une première alimentation (ELVDD) ; et
une unité de compensation (144, 144') pour commander la tension d'une électrode de grille du deuxième transistor (M2) afin de compenser une détérioration de la diode électro-luminescente organique (OLED),
dans lequel l'unité de compensation (144, 144') comprend :

un septième transistor (M7) comportant une première électrode couplée à un deuxième noeud (N4) et une deuxième électrode couplée à une anode de la diode électroluminescente organique (OLED), la première électrode du septième transistor (M7) étant une première électrode parmi une électrode de drain et une électrode de source, et la deuxième électrode du septième transistor (M7) étant une électrode restante parmi l'électrode de drain et l'électrode de source ;
un huitième transistor (M8) comportant une première électrode couplée à la première alimentation (ELVDD) et une deuxième électrode couplée au deuxième noeud (N4), la première électrode du huitième transistor (M8) étant une première électrode parmi une électrode de drain et une électrode de source, et la deuxième électrode du huitième transistor (M8) étant une électrode restante parmi l'électrode de drain et l'électrode de source ; et
un premier condensateur (Cfb1) comportant une première électrode connectée au deuxième noeud (N4) ;
caractérisé en ce que le pixel comprend de plus un circuit de pixel (142, 142') pour compenser la tension de seuil du deuxième transistor (M2), et **en ce que** l'unité de compensation comprend de plus :

un deuxième condensateur de rétroaction (Cfb2) comportant une première électrode couplée à une deuxième électrode du premier condensateur de rétroaction (Cfb1) et une deuxième électrode couplée au premier noeud (N2) électriquement couplé à l'électrode de grille du deuxième transistor (M2) ; et
un neuvième transistor (M9) comportant une première électrode couplée à un troisième noeud (N5), qui est un noeud commun aux premier et deuxième condensateurs de rétroaction (Cfb1, Cfb2), et une deuxième électrode couplée à une alimentation en tension prédéterminée (ELVDD, Vint), le neuvième transistor (M9) étant d'un type de conductivité différent de celui du deuxième transistor (M2) et du huitième transistor (M8), et la première électrode du neuvième transistor (M9) étant une première électrode parmi une électrode de drain et une électrode de source, et la deuxième électrode du neuvième transistor (M9) étant une électrode restante parmi l'électrode de drain et l'électrode de source.

2. Pixel (140, 140') selon la revendication 1, dans lequel le circuit de pixel (142, 142') comprend :

un premier transistor (M1) couplé à une $i^{ème}$ ligne de balayage (Si) et à une ligne de données (Dj), et rendu passant lorsqu'un signal de balayage est délivré à la $i^{ème}$ ligne de balayage (Si) de façon à délivrer un signal de données délivré à la ligne de données (Dj) à la première électrode du deuxième transistor (M2) ;
un troisième transistor (M3) couplé entre la deuxième électrode du deuxième transistor (M2) et le premier noeud (N2) et rendu passant lorsque le signal de balayage est délivré à la $i^{ème}$ ligne de balayage (Si) ;
un quatrième transistor (M4) couplé entre une alimentation d'initialisation (Vint) et le premier noeud (N2), et rendu passant lorsque le signal de balayage est délivré à une $i\text{-}1^{ème}$ ligne de balayage (Si-1) ;
un cinquième transistor (M5) couplé entre la première électrode du deuxième transistor (M2) et la première alimentation (ELVDD) et rendu passant lorsqu'un signal de commande d'émission de lumière n'est pas délivré à une $i^{ème}$ ligne de commande d'émission de lumière (Ei) ; et
un sixième transistor (M6) couplé entre la deuxième électrode du deuxième transistor (M2) et la diode électroluminescente organique (OLED) et rendu passant lorsque le signal de commande d'émission de lumière n'est pas délivré à la $i^{ème}$ ligne de commande d'émission de lumière (Ei).

3. Pixel (140, 140') selon la revendication 2, dans lequel l'alimentation d'initialisation (Vint) est établie à

une valeur de tension inférieure à celle du signal de données.

4. Pixel (140, 140') selon l'une des revendications 2 ou 3, dans lequel les septième et huitième transistors (M7, M8) sont rendus passants et bloqués en alternance.

5. Pixel (140, 140') selon la revendication 4, dans lequel le signal de commande d'émission de lumière délivré à la i^{ème} ligne de commande d'émission de lumière (Ei) est délivré de façon à être chevauché avec les signaux de balayage délivrés à la i-1ème ligne de balayage (Si-1) et à la i^{ème} ligne de balayage (Si).

6. Pixel (140, 140') selon la revendication 5, dans lequel le septième transistor (M7) est rendu passant lorsque le signal de balayage est délivré à une i+1ème ligne de balayage (Si+1) afin de délivrer la tension appliquée à la diode électro-luminescente organique (OLED) au deuxième noeud (N4) ; et
le huitième transistor (M8) est rendu passant lorsque le signal de commande d'émission de lumière n'est pas délivré à la i+1ème ligne de commande d'émission de lumière (Ei+1) afin de délivrer la tension de la première alimentation (ELVDD) au deuxième noeud (N4).

7. Pixel (140, 140') selon la revendication 5, dans lequel le septième transistor (M7) est rendu passant lorsque le signal de commande d'émission de lumière est délivré à une i+2ème ligne de commande d'émission de lumière (Ei+2) afin de délivrer la tension appliquée à la diode électro-luminescente organique (OLED) au deuxième noeud (N4) ; et
le huitième transistor (M8) est rendu passant lorsque le signal de commande d'émission de lumière n'est pas délivré à la i+2ème ligne de commande d'émission de lumière (Ei+2) afin de délivrer la tension de la première alimentation (ELVDD) au deuxième noeud (N4).

8. Pixel (140, 140') selon la revendication 7, dans lequel le septième transistor (M7) est formé sous la forme métal-oxyde-semiconducteur N (NMOS), et le huitième transistor (M8) est formé sous la forme métal-oxyde-semiconducteur P (PMOS).

9. Pixel (140, 140') selon la revendication 5, dans lequel le neuvième transistor (M9) est rendu passant lorsque le signal de commande d'émission de lumière est délivré à la i+1ème ligne de commande d'émission de lumière (Ei+1) de façon à maintenir la tension du troisième noeud (N5) avec l'alimentation en tension prédéterminée (ELVDD, Vint).

10. Pixel (140, 140') selon la revendication 9, dans lequel le neuvième transistor (M9) est formé sous la forme métal-oxyde-semiconducteur N (NMOS).

11. Pixel (140, 140') selon la revendication 9, dans lequel l'alimentation en tension prédéterminée (ELVDD, Vint) est l'une quelconque parmi la première alimentation (ELVDD) et l'alimentation d'initialisation (Vint).

12. Dispositif d'affichage à émission de lumière organique (100), comprenant :

un dispositif d'attaque de balayage (110) pour délivrer de façon séquentielle des signaux de balayage à des lignes de balayage (S0, ..., Sn+1) et délivrer de façon séquentielle des signaux de commande d'émission de lumière à des lignes de commande d'émission de lumière (E0, ..., En+1) ;
un dispositif d'attaque de données (120) pour délivrer des signaux de données à des lignes de données (D1, ..., Dm) ; et
des pixels (140, 140') positionnés dans des régions séparées par les lignes de balayage (S0, ..., Sn+1) et les lignes de données (D1, ..., Dm),
caractérisé en ce que chacun des pixels est un pixel selon l'une des revendications précédentes.

13. Dispositif d'affichage à émission de lumière organique (100) selon la revendication 12, dans lequel le dispositif d'attaque de balayage (110) délivre les signaux de commande d'émission de lumière à une i^{ème} ligne de commande d'émission de lumière (Ei) de façon à être chevauchés avec les signaux de balayage délivrés à une i-1ème (i est un nombre naturel) ligne de balayage (Si-1) et une i^{ème} ligne de balayage (Si).

14. Procédé d'attaque du dispositif d'affichage à émission de lumière organique (100) selon l'une des revendications 12 ou 13, le procédé d'attaque comprenant les étapes consistant à :

initialiser la tension de l'électrode de grille du deuxième transistor (M2) avec la tension d'une alimentation d'initialisation (Vint) ;
puis charger la tension correspondant à la tension de seuil du deuxième transistor (M2) et un signal de données dans un transistor de stockage (Cst) par connexion du deuxième transistor (M2) sous la forme d'une diode ;
puis délivrer le courant correspondant à la tension chargée dans le condensateur de stockage (Cst) à la diode électro-luminescente organique (OLED) ;
appliquer la tension de la diode électrolumines-

cente organique (OLED) au deuxième noeud (N4) lorsque ledit courant est délivré à la diode électro-luminescente organique (OLED) ;
puis maintenir un troisième noeud (N5), qui est une borne commune des premier et deuxième condensateurs de rétroaction (Cfb1, Cfb2), à une tension constante durant les étapes de charge de la tension dans le condensateur de stockage (Cst) et d'application de la tension de la diode électro-luminescente organique (OLED) au deuxième noeud (N4) ; et
ensuite, commander la tension de l'électrode de grille du transistor d'attaque (M2) par établissement du troisième noeud (N5) à l'état flottant, et, en même temps, élever la tension du deuxième noeud (N4) à la tension de la première alimentation (ELVDD).

15. Procédé d'attaque d'un dispositif d'affichage à émission de lumière organique (100) selon la revendication 14, dans lequel la tension constante est la tension délivrée à partir de l'une quelconque parmi l'alimentation d'initialisation (Vint) et la première alimentation (ELVDD).

16. Procédé d'attaque d'un dispositif d'affichage à émission de lumière organique (100) selon l'une des revendications 14 ou 15, dans lequel l'alimentation d'initialisation (Vint) est établie à une valeur de tension inférieure à celle du signal de données.

17. Procédé d'attaque d'un dispositif d'affichage à émission de lumière organique (100) selon l'une des revendications 14 à 16, dans lequel les premier et deuxième transistors (M7, M8) sont rendus passants et bloqués en alternance.

FIG. 1

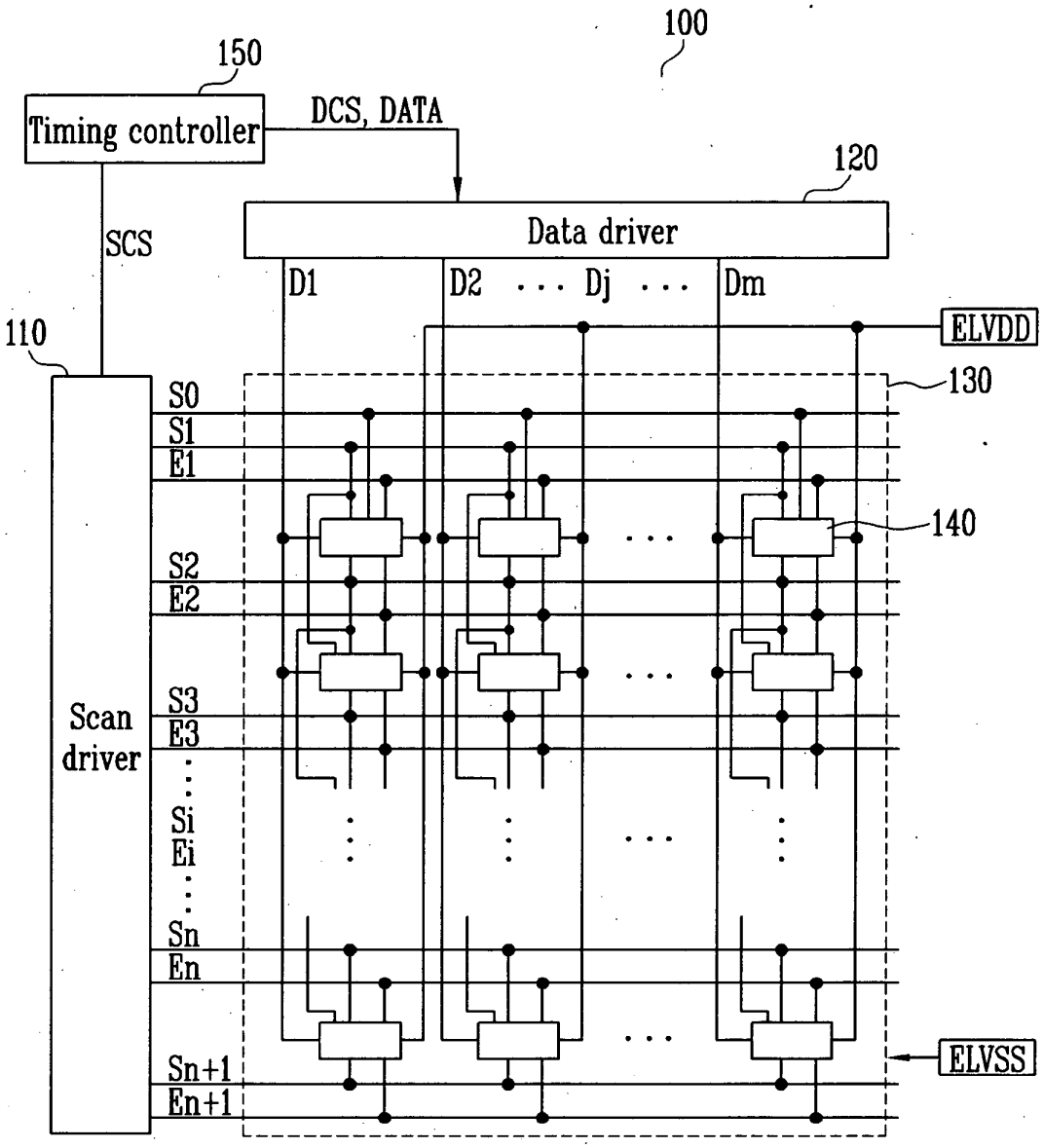

100
150
Timing controller
DCS, DATA
120
Data driver
SCS
D1
D2 ... Dj ... Dm
ELVDD
110
130
S0
S1
E1
140
S2
E2
S3
E3
Scan driver
Si
Ei
Sn
En
Sn+1
En+1
ELVSS

FIG. 2

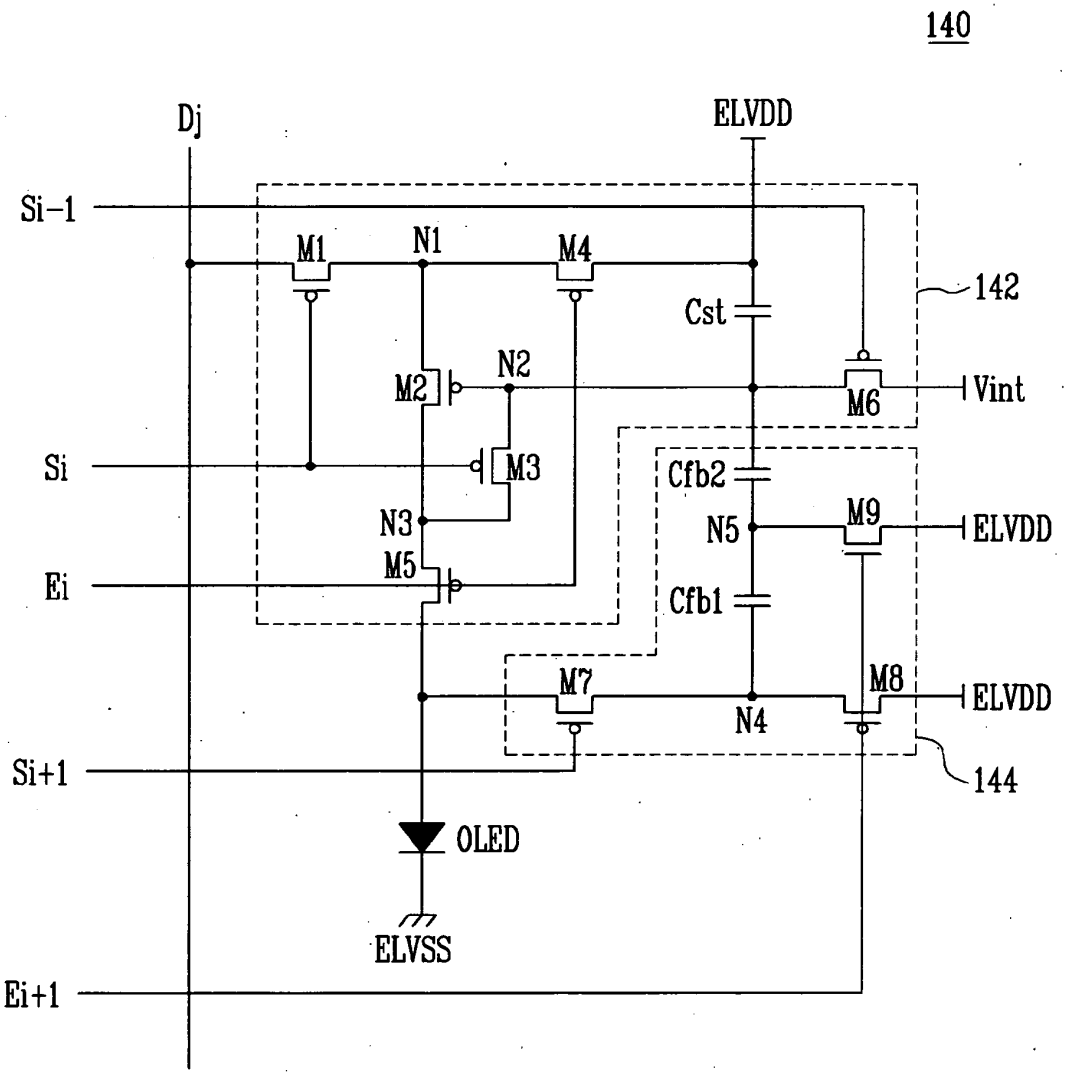

140
Dj
ELVDD
Si-1
M1
N1
M4
142
Cst
N2
M2
M6
Vint
Si
M3
Cfb2
N3
N5
M9
ELVDD
Ei
M5
Cfb1
M7
M8
ELVDD
N4
Si+1
144
OLED
ELVSS
Ei+1

FIG. 3

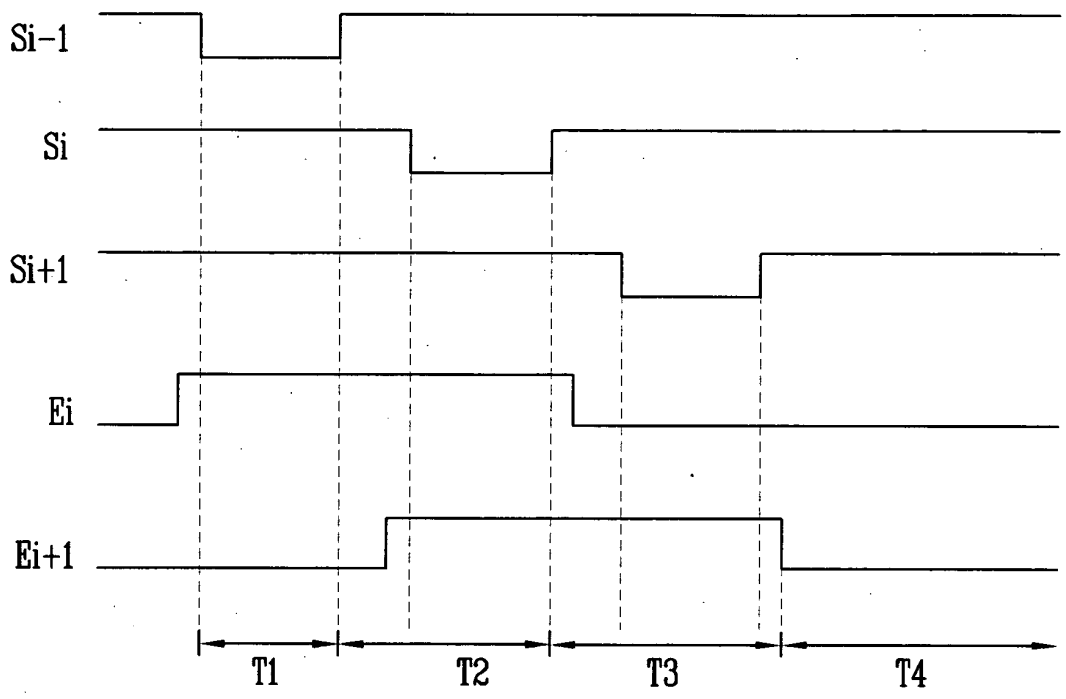


FIG. 4

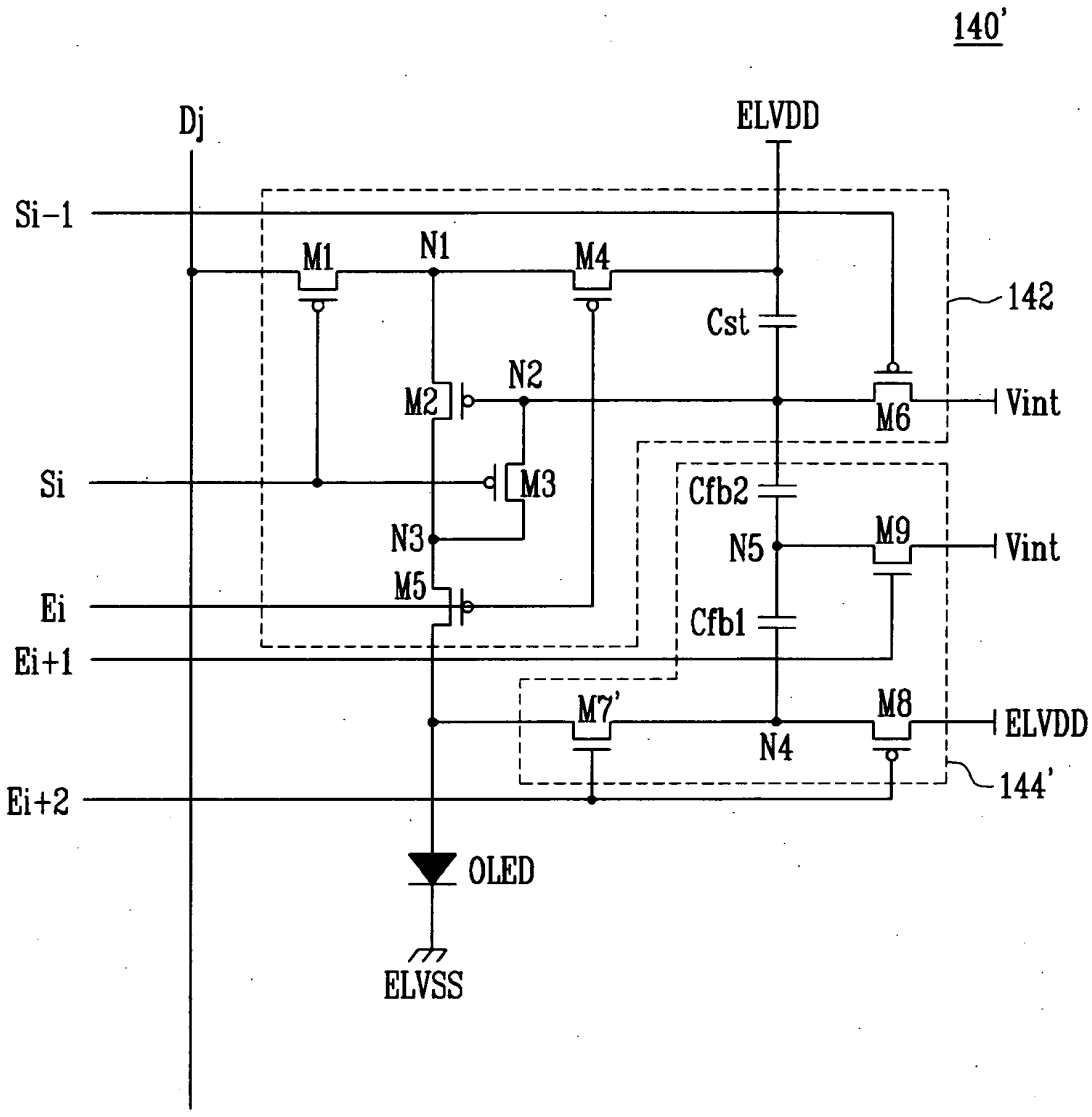
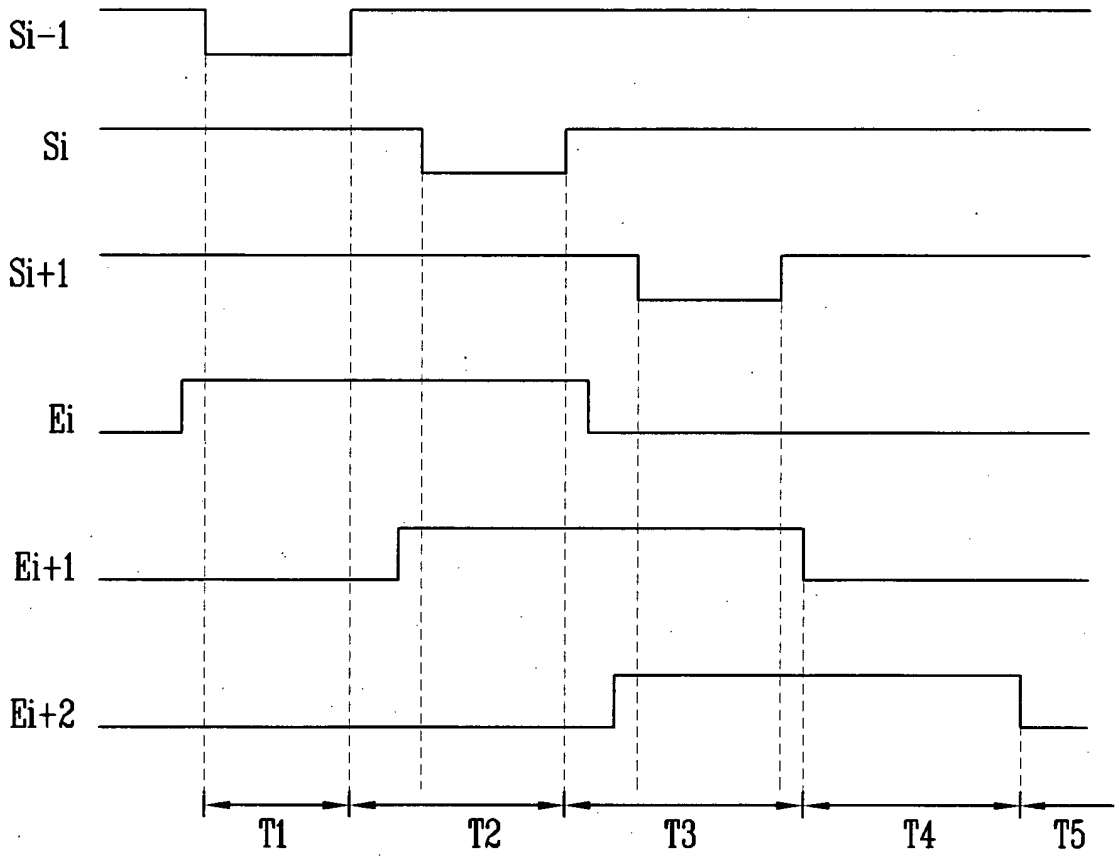

140'
Dj
ELVDD
Si-1
M1
N1
M4
142
Cst
N2
M2
M6
Vint
Si
M3
Cfb2
N3
N5
M9
Vint
M5
Ei
Cfb1
Ei+1
M7'
M8
ELVDD
N4
144'
Ei+2
OLED
ELVSS

FIG. 5



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2006253755 A1 **[0003]**
- EP 1970885 A1 **[0004]**
- EP 1968039 A1 **[0005]**

Non-patent literature cited in the description

- **S.M. Choi.** A Self-compensated Voltage Programming Pixel Structure for Active-Matrix Organic Light Emitting Diodes. *Proceedings of the International Display Workshops,* 01 January 2003 **[0006]**

专利名称(译)	PIxel，使用其的有机发光显示器以及相关方法		
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摘要(译)

像素，包括有机发光二极管，数据线和第一节点之间的第一晶体管，第一节点和第三节点之间的第二晶体管，第二节点和第三节点之间的第三晶体管，第四晶体管之间的第四晶体管第一电源和第一节点，第三节点和有机发光二极管之间的第五晶体管，初始化电源和第二节点之间的第六晶体管，第二节点和第一电源之间的存储电容器，第一第四节点和第二节点之间串联的第二反馈电容器，第四节点和有机发光二极管之间的第七晶体管，第一电源和第四节点之间的第八晶体管，以及第五节点之间的第九晶体管和预定的电压源。

FIG. 1