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(54) **Organic light emitting display**

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Affichage électroluminescent organique

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- **CHOI S-M ET AL: "AN IMPROVED VOLTAGE PROGRAMMED PIXEL STRUCTURE FOR LARGE SIZE AND HIGH RESOLUTION AM-OLED DISPLAYS" 2004 SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS. SEATTLE, WA, MAY 25 - 27, 2004, SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS, SAN JOSE, CA : SID, US, vol. VOL. 35 PRT 1, 25 May 2004 (2004-05-25), pages 260-263, XP001222795**

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Description

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to a pixel, an organic light emitting display including such a pixel, and a method for driving the organic light emitting display.

2. Discussion of Related Art

[0002] Recently, various flat panel displays having advantages such as reduced weight and volume over cathode ray tubes (CRT) displays have been developed. Flat panel displays include liquid crystal displays (LCD), field emission displays (FED), plasma display panels (PDP), and organic light emitting displays.

[0003] Among the flat panel displays, the organic light emitting displays make use of organic light emitting diodes that emit light by re-combination of electrons and holes. The organic light emitting display has advantages such as high response speed and low power consumption.

[0004] FIG. 1 is a circuit diagram showing a pixel 4 of a conventional organic light emitting display.

[0005] With reference to FIG. 1, the pixel 4 of a conventional organic light emitting display includes an organic light emitting diode (OLED) and a pixel circuit 2. The pixel circuit 2 is coupled to a data line Dm and a scan line Sn, and controls light emission of the organic light emitting diode (OLED).

[0006] An anode electrode of the organic light emitting diode (OLED) is coupled to a pixel circuit 2, and a cathode electrode thereof is coupled to a second power supply ELVSS. The organic light emitting diode (OLED) generates light of a predetermined luminance corresponding to an electric current from the pixel circuit 2.

[0007] When a scan signal is supplied to the scan line Sn, the pixel circuit 2 controls the amount of electric current provided to the organic light emitting diode (OLED). The amount of current corresponds to a data signal provided to the data line Dm. The pixel circuit 2 includes a second transistor M2, a first transistor M1, and a storage capacitor Cst. The second transistor M2 is coupled to a first power supply ELVDD and the organic light emitting diode (OLED). The first transistor M1 is coupled between the data line Dm and the scan line Sn. The storage capacitor Cst is coupled between a gate electrode and a first electrode of the second transistor M2.

[0008] A gate electrode of the first transistor M1 is coupled to the scan line Sn, and a first electrode thereof is coupled to the data line Dm. A second electrode of the first transistor M1 is coupled with one terminal of the storage capacitor Cst. The first electrode can be either a source electrode or a drain electrode, and the second electrode is the other one of the source electrode or the drain electrode. For example, when the first electrode is the source electrode, the second electrode is the drain electrode. When a scan signal is supplied to the first transistor M1 coupled with the scan line Sn and the data line Dm, the first transistor M1 is turned-on to provide a data signal from the data line Dm to the storage capacitor Cst. At this time, the storage capacitor Cst is charged with a voltage corresponding to the data signal.

[0009] The gate electrode of the second transistor M2 is coupled to one terminal of the storage capacitor Cst, and a first electrode thereof is coupled to another terminal of the storage capacitor Cst and a first power supply ELVDD. Further, a second electrode of the second transistor M2 is coupled with the anode electrode of the organic light emitting diode (OLED). The second transistor M2 controls the amount of electric current flowing from the first power supply ELVDD to a second power supply ELVSS through the organic light emitting diode such that the current corresponds to the voltage charged in the storage capacitor Cst. At this time, the organic light emitting diode (OLED) emits light corresponding to the amount of electric current supplied from the second transistor M2.

[0010] However, the pixel 4 of the conventional organic light emitting display may not display an image of substantially uniform luminance. Threshold voltages of the second transistors M2 (drive transistors) in the pixels 4 vary according to process deviations during fabrication. When the threshold voltages of the second transistors M2 vary, although data signals corresponding to the same luminance are supplied to the pixels 4, the second transistors M2 provide different amounts of current to the organic light emitting diodes (OLEDs) which therefore emit light of different luminance levels.

[0011] A number of circuits have been proposed to address this problem, for example, according to a pixel circuit disclosed in WO 2006/054189 fig. 6, each pixel comprises a light emitting display element, a drive transistor, first and second capacitors connected in series between the gate electrode and a first terminal of the drive transistor, an input transistor connected between an input data line and the junction between the first and second capacitors arranged to apply a data voltage and a reference voltage to said junction, a diode-connected transistor connected between the gate and said first terminal of the drive transistor to reset the voltage at the gate of the drive transistor to a known voltage. According to this pixel circuit, the diode-connected transistor is connected to the power supply line which varies depending on the position of the pixel.

[0012] Accordingly, the present invention provides an organic light emitting display according to claim 1.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] These and/or other aspects and features of the invention will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompanying drawings of

which:

FIG. 1 is a circuit diagram showing a conventional pixel;

FIG. 2 is a schematic diagram showing an organic light emitting display according to a comparative example;

FIG. 3 is a circuit diagram showing an example of the pixel shown in FIG. 2;

FIG. 4 is a waveform diagram showing a method of driving the pixel shown in FIG. 3;

FIG. 5 is a schematic diagram showing an organic light emitting display according to an embodiment of the present invention;

FIG. 6 is a circuit diagram showing an example of the pixel shown in FIG. 5; and

FIG. 7 is a waveform diagram showing a method of driving the pixel shown in FIG. 6.

DETAILED DESCRIPTION

[0014] Hereinafter, exemplary embodiments according to the present invention will be described with reference to the accompanying drawings. Here, when one element is referred to as being connected to a second element, the one element may be not only directly connected to the second element but instead may be indirectly connected to the second element via another element. Further, some elements not necessary for a complete description are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0015] FIG. 2 is a schematic diagram showing an organic light emitting display according to a comparative example.

[0016] With reference to FIG. 2, the organic light emitting display, according to a first embodiment of the present invention, includes a pixel region 130, a scan driver 110, a data driver 120, and a timing control unit 150. The pixel region 130 includes a plurality of pixels 140, which are coupled to scan lines S1 to Sn, emission control lines E1 to En, and data lines D1 to Dm. The scan driver 110 is adapted to drive the scan lines S1 to Sn and the emission control lines E1 to En. The data driver 120 is adapted to drive the data lines D1 to Dm. The timing control unit 150 is adapted to control the scan driver 110 and the data driver 120.

[0017] The pixel region 130 includes the pixels 140, which are formed at areas defined by the scan lines S1 to Sn, the emission control lines E1 to En, and the data lines D1 to Dm. The pixels 140 receive a voltage from a first power supply ELVDD, a voltage from a second power supply ELVSS, and a voltage from an exterior reference power supply Vref. Each of the pixels 140, having received the voltage from Vref, compensates for the voltage drop of the first power supply ELVDD and a threshold voltage of a drive transistor using a difference between the voltage of the first power supply ELVDD and the voltage of the reference power supply Vref.

[0018] Further, the pixels 140 provide an electric current, which may be predetermined, from the first power supply ELVDD to the second power supply ELVSS through an organic light emitting diode (shown in FIG. 3) according to a data signal supplied thereto. Accordingly, the organic light emitting diode emits light of a predetermined luminance.

[0019] Each of the pixels 140 is coupled with two scan lines to be driven. In other words, when a scan signal is supplied to an (i-1)th ('i' is an integer) scan line Si-1, a pixel 140 disposed at an i-th horizontal line performs an initialization and a a threshold voltage compensation. Moreover, when the scan signal is supplied to an (i)th scan line Si, the pixel 140 is charged with a voltage corresponding to the data signal. The organic light emitting display of FIG. 2 includes a zero-th scan line S0 coupled to pixels 140 at a first horizontal line.

[0020] The timing control unit 150 generates a data drive control signal DCS and a scan drive control signal SCS according to externally supplied synchronous signals. The data drive control signal DCS generated by the timing control unit 150 is provided to the data driver 120, and the scan drive control signal SCS is provided to the scan driver 110. Furthermore, the timing control unit 50 provides externally supplied data (Data) to the data driver 120.

[0021] The scan driver 110 generates a scan signal in response to a scan drive control signal (SCS) from the timing control unit 150, and sequentially provides the generated scan signal to the scan lines S1 to Sn. Then, the scan driver 110 sequentially provides an emission control signal to the emission control lines E1 to En. The emission control signal is activated such that it overlaps with two scan signals during at least a part of the activated time period. Thus, the time period of activation for the emission control signal is equal to or greater than that of the first scan signal.

[0022] The data driver 120 receives the data drive control signal DCS from the timing control unit 150, and generates a data signal.

[0023] FIG. 3 is a circuit diagram showing an example of the pixel shown in FIG. 2. For convenience of description, FIG. 3 shows a single pixel, which is positioned at an n-th horizontal line and is coupled with an m-th data line Dm.

[0024] With reference to FIG. 3, the pixel 140 includes an organic light emitting diode (OLED) and a pixel circuit 142 for supplying an electric current to the organic light emitting diode (OLED).

[0025] The organic light emitting diode (OLED) emits light having a predetermined color corresponding to the electric current from the pixel circuit 142. For example, the organic light emitting diode (OLED) generates red, green, or blue light having a luminance corresponding to the amount of the electric current supplied by the pixel circuit 142.

[0026] When the scan signal is supplied to an (n-1)th scan line Sn-1, the pixel circuit 142 compensates for a

voltage drop of the first power supply ELVDD and a threshold voltage of the second transistor M2 (drive transistor). When the scan signal is provided to the n-th scan line Sn, the pixel circuit 142 is charged with a voltage corresponding to the data signal. So as to do this, the pixel circuit 142 includes first to fifth transistors M1 to M5, and first and second capacitors C1 and C2.

[0027] A first electrode of the first transistor M1 is coupled to a data line Dm, and a second electrode thereof is coupled with a first node N1. Further, the gate electrode of the first transistor M1 is coupled to the n-th scan line Sn. When the scan signal is supplied to the n-th scan line Sn, the first transistor M1 is turned-on to electrically connect the data line Dm and the first node N1 to each other.

[0028] A first electrode of the second transistor M2 is coupled with the first power supply ELVDD, and a second electrode thereof is coupled with a first electrode of the fifth transistor M5. Further, a gate electrode of the second transistor M2 is coupled with a second node N2. The second transistor M2 provides an electric current to a first electrode of the fifth transistor M5 where the current corresponds to a voltage applied to the second node N2, namely, a voltage charged in the first and second capacitors C1 and C2.

[0029] A second electrode of the third transistor M3 is coupled to the second node N2, and a first electrode thereof is coupled with the second electrode of the second transistor M2. Moreover, a gate electrode of the third transistor M3 is coupled to the (n-1)th scan line Sn-1. When the scan signal is supplied to the (n-1)th scan line Sn-1, the third transistor M3 is turned-on to diode-connect the second transistor M2.

[0030] A first electrode of the fourth transistor M4 is coupled to the reference power supply Vref, and a second electrode thereof is coupled to the first node N1. In addition, a gate electrode of the fourth transistor M4 is coupled to the (n-1)th scan line Sn-1. When the scan signal is provided to the (n-1)th scan line Sn-1, the fourth transistor M4 is turned-on to electrically connect the first node N1 to the reference power supply Vref.

[0031] A first electrode of the fifth transistor M5 is coupled to the second electrode of the second transistor M2, and a second electrode thereof is coupled to an anode electrode of the organic light emitting diode (OLED). Further, a gate electrode of the fifth transistor M5 is coupled with an n-th emission control line. When an emission control signal is provided to the n-th emission control line En, the fifth transistor M5 is turned-off. In contrast to this, when the emission control signal is not supplied, the fifth transistor M5 is turned-on. Here, the emission control signal supplied to the n-th emission control line En partially overlaps with a scan signal supplied to the (n-1)th scan line Sn-1, and completely overlaps with a scan signal supplied to the n-th scan line Sn. Accordingly, while the first capacitor C1 and the second capacitor C2 are being charged with a voltage (e.g., a predetermined voltage), the fifth transistor M5 is turned-off. In contrast to this, during remaining time periods, the fifth transistor M5 electrically connects the second transistor M2 to the organic light emitting diode (OLED).

[0032] The first power supply ELVDD is coupled to the pixels 140, and supplies a current thereto. Accordingly, voltage drops vary according to the positions of the pixels 140 and the image being displayed by the pixels. However, the reference power supply Vref does not provide an electric current to the pixels 140, thereby maintaining the same voltage value regardless of the positions of the pixels 140. The voltage values of the first power supply ELVDD and the reference power supply Vref can be equally set to each other.

[0033] FIG. 4 is a waveform diagram showing a method of driving the pixel shown in FIG. 3. Referring to FIG. 4, the fifth transistor M5 maintains a turned-on state during a first time period T1, which is a part of a time period when the scan signal is supplied to the (n-1)th scan line Sn-1. Accordingly, during the first time period T1, the third transistor M3 and the fourth transistor M4 are turned-on.

[0034] When the third transistor M3 is turned-on, a gate electrode of the second transistor M2 is electrically connected to the organic light emitting diode (OLED) through the third transistor M3. Accordingly, a voltage of the gate electrode of the second transistor M2, namely, the second node N2, is pulled down and initialized with a voltage determined by the second power supply ELVSS. That is, the first time period T 1 is used to initialize a voltage of the second node N2 such that the transistor M2 is safely switched on for the subsequent threshold compensation independent of the previous pixel voltage stored in the second node N2.

[0035] Next, during a second time period T2 of a time period when the scan signal is supplied to the (n-1)th scan line Sn-1 other than the first time period, the fifth transistor M5 is turned-off by an emission control signal supplied to an n-th emission control line En. Accordingly, a voltage obtained by subtracting a threshold voltage of the second transistor M2 from a voltage of the first power supply ELVDD, is applied to a gate electrode of the second transistor M2, which is diode-connected by the third transistor M3.

[0036] Further, the first node N1 is set as a voltage of the reference power supply Vref by the fourth transistor M4, which has maintained turning-on state during the second time period T2. Here, assuming that voltages of the reference power supply Vref and the first power supply ELVDD are identical with each other, the second capacitor C2 is charged with a voltage corresponding to a threshold voltage of the second transistor M2. Moreover, when a voltage drop occurs in the first power supply ELVDD, the second capacitor C2 is charged with a threshold voltage of the second transistor M2 and the voltage drop of the first power supply ELVDD. That is, the second capacitor C2 is charged with a threshold voltage of the second transistor M2 and the voltage drop of the first power supply ELVDD, and accordingly the threshold voltage of the second transistor M2 and the

voltage drop of the first power supply ELVDD can be concurrently compensated.

[0037] Then, during a third time period T3, the scan signal is provided to the n-th scan line Sn. When the scan signal is supplied to the n-th scan line Sn, the first transistor M1 is turned-on. When the first transistor M1 is turned-on, a data signal is supplied to the first node N1. Accordingly, a voltage of the first node N1 drops to a voltage of the data signal from a voltage of the reference power supply Vref. A voltage of the second node N2 set as a floating state during the third time period T3 also drops corresponding to a voltage drop of the first node N1. Namely, during the third time period T3, a voltage charged in the second capacitor C2 is stably maintained. On the other hand, during the third time period T3, the first capacitor C1 is charged with a predetermined voltage corresponding to the data signal, which is applied to the first node N1.

[0038] Thereafter, during a fourth time period T4, after the supply of the scan signal to the n-th scan line stops, the supply of the emission control signal to the n-th emission control line En is terminated. When the supply of the emission control signal stops, the fifth transistor M5 is turned-on. When the fifth transistor M5 is turned-on, the second transistor M2 provides an electric current to the organic light emitting diode (OLED) corresponding to the voltages charged in the first capacitor C1 and the second capacitor C2, so that the light emitting diode (OLED) generates light having a luminance corresponding to the current.

[0039] As illustrated earlier, the pixel 140 shown in FIG. 3 is capable of displaying a desired image irrespective of the threshold voltage of the drive transistor M2 and the voltage drop of the first power supply ELVDD. However, during a short time period when the second node N2 of the pixel 140 is initialized a current independent of actual image data may flow through the organic light emitting diode, thereby causing display quality to be deteriorated.

[0040] In detail, during the first time period T1, which is a part of a time period when the scan signal is supplied to the (n-1)th scan line Sn-1, the pixel 140 initializes the second node N2. During a second time period T2 among a time period when the scan signal is supplied to the (n-1)th scan line Sn-1 other than the first time period T1, the second capacitor C2 is charged with a voltage corresponding the threshold voltage of the second transistor M2. If the second time period T2 is set as a short time period, the voltage corresponding to the threshold voltage of the second transistor M2 may be insufficiently charged. In particular, as the size of the panel is increased and the resolution becomes higher, the second time period T2 becomes shorter.

[0041] On the other hand, during the first time period T1, a voltage of the second node N2 is approximately initialized with a voltage of the second power supply ELVSS. Here, the initialized voltage of the second node N2 can vary for different pixels based on the voltage drop of the second power supply ELVSS. When the initialized voltage of the second node N2 varies, the voltage of the second node N2 is not changed to a desired value during the second time period T2, which may result in the display of a non-uniform image. Further, in the pixel shown in FIG. 3, a current may be supplied to the organic light emitting diode during the first time period T1 so as to generate undesirable light.

[0042] FIG. 5 is a schematic diagram showing an organic light emitting display according to an embodiment of the present invention.

[0043] With reference to FIG. 5, the organic light emitting display according to the second embodiment of the present invention includes a pixel region 230, a scan driver 210, a data driver 220, and a timing control unit 250. The pixel region 230 includes a plurality of pixels 240, which are coupled with scan lines S1 to Sn, emission control lines E1 to En, and data lines D1 to Dm. The scan driver 210 drives the scan lines S1 to Sn and the emission control lines E1 to En. The data driver 220 drives the data lines D1 to Dm. The timing control unit 150 controls the scan driver 210 and the data driver 220.

[0044] The pixel region 230 includes the pixels, which are formed at areas defined by the scan lines S1 to Sn, the emission control lines E1 to En, and the data lines D1 to Dm. The pixels 240 receive a voltage from the first power supply ELVDD, a voltage from the second power supply ELVSS, and an exterior voltage from a reference power supply Vref. Each of the pixels 240 having received the voltage of the reference power supply Vref compensates for a voltage drop of the first power supply ELVDD and a threshold voltage of a drive transistor using a difference between the voltage of the first power supply ELVDD and the voltage of the reference power supply Vref.

[0045] Further, the pixels 240 provide an electric current from the first power supply ELVDD to the second power supply ELVSS through an organic light emitting diode (shown in FIG. 6) according to a data signal supplied thereto. Accordingly, the organic light emitting diode emits light having a predetermined luminance.

[0046] The pixels 240 are coupled with three scan lines to be driven. In other words, when a scan signal is supplied to an (i-2)th ('i' is integer) scan line Si-2, a pixel 240 disposed at an i-th horizontal line is initialized. When the scan signal is supplied to an (i-1)th scan line Si-1, a pixel 140 disposed at an i-th horizontal line performs an initialization and a compensation of a threshold voltage. Moreover, when the scan signal is supplied to an i scan line Si, the pixel 140 is charged with a voltage corresponding to the data signal.

[0047] The timing control unit 250 generates a data drive control signal DCS and a scan drive control signal SCS according to externally supplied synchronous signals. The data drive control signal DCS generated by the timing control unit 250 is provided to the data driver 220, and the scan drive control signal SCS is provided to the scan driver 210. Furthermore, the timing control unit 50

provides externally supplied data (Data) to the data driver 220.

[0048] The scan driver 210 generates a scan signal in response to a scan drive control signal SCS from the timing control unit 250, and sequentially provides the generated scan signal to the scan lines S1 to Sn. Then, the scan driver 210 sequentially provides an emission control signal to the emission control lines E1 to En. The emission control signal is activated such that it overlaps with three scan signals. In other words, the emission control signal is supplied to the i-th emission control line Ei to overlap with the scan signals, which are supplied to the (i-2)th scan line Si-2, the (i-1)th scan line Si-1, and the i-th scan line Si.

[0049] The data driver 220 receives the data drive control signal DCS from the timing control unit 250, and generates a data signal.

[0050] FIG. 6 is a circuit diagram showing an example of the pixel shown in FIG. 5. For convenience of description, FIG. 6 shows a single pixel, which is positioned at an i-th horizontal line and is coupled with an m-th data line Dm.

[0051] With reference to FIG. 6, the pixel 240 in one embodiment of the present invention includes an organic light emitting diode (OLED) and a pixel circuit 242 for supplying an electric current to the organic light emitting diode (OLED).

[0052] The organic light emitting diode (OLED) emits light having a color (e.g., predetermined color) corresponding to the electric current from the pixel circuit 242. For example, the organic light emitting diode (OLED) generates red, green, or blue light having a luminance corresponding to the amount of the electric current supplied by the pixel circuit 242.

[0053] When the scan signal is supplied to an (i-2)th scan line Si-2, the pixel circuit 242 initializes a second node N2. Further, when the scan signal is supplied to an (i-1)th scan line Si-1, the pixel circuit 242 compensates for a voltage drop of the first power supply ELVDD and a threshold voltage of the second transistor M2 (drive transistor). In order to do this, a voltage of the reference power supply Vref is set to be greater than a voltage of the data signal, and to be less than a voltage of the first power supply ELVDD.

[0054] When the scan signal is provided to an i-th scan line Si, the pixel circuit 242 is charged with a voltage corresponding to the data signal. To do this, the pixel circuit 142 includes first to sixth transistors M1 to M6, and first and second capacitors C1 and C2.

[0055] A first electrode of the first transistor M1 is coupled to the data line Dm, and a second electrode thereof is coupled with a first node N1. Further, a gate electrode of the first transistor M1 is coupled to an i-th scan line Si. When the scan signal is supplied to the i-th scan line Si, the first transistor M1 is turned-on to electrically connect the data line Dm and the first node N1 to each other.

[0056] A first electrode of the second transistor M2 is coupled with the first power supply ELVDD, and a second electrode thereof is coupled with a first electrode of the fifth transistor M5. Further, a gate electrode of the second transistor M2 is coupled with a second node N2. The second transistor M2 provides an electric current to the first electrode of the fifth transistor M5 where the electric current corresponds to a voltage applied to the second node N2, namely, a voltage charged in the first and second capacitors C1 and C2.

[0057] A second electrode of the third transistor M3 is coupled to the second node N2, and a first electrode thereof is coupled with the second electrode of the second transistor M2. Moreover, a gate electrode of the third transistor M3 is coupled to the (i-1)th scan line Si-1. When the scan signal is supplied to the (i-1)th scan line Si-1, the third transistor M3 is turned-on to diode-connect the second transistor M2.

[0058] A first electrode of the fourth transistor M4 is coupled to the reference power supply Vref, and a second electrode thereof is coupled to the first node N1. In addition, a gate electrode of the fourth transistor M4 is coupled to an (i-1)th scan line Si-1. When the scan signal is provided to the (i-1)th scan line Si-1, the fourth transistor M4 is turned-on to electrically connect the first node N1 to the reference power supply Vref.

[0059] A first electrode of the fifth transistor M5 is coupled to the second electrode of the second transistor M2, and a second electrode thereof is coupled to an anode electrode of the organic light emitting diode (OLED). Further, a gate electrode of the fifth transistor M5 is coupled with an n-th emission control line. When an emission control signal is provided to an i-th emission control line Ei, the fifth transistor M5 is turned-off. In contrast to this, when the emission control signal is not supplied, the fifth transistor M5 is turned-on.

[0060] A first electrode of the sixth transistor M6 is coupled to the reference power supply Vref, and a second electrode thereof is coupled to the second node N2. Further, a gate electrode of the sixth transistor M6 is coupled with an (i-2)th scan line Si-2. When the scan signal is supplied to the (i-2)th scan line Si-2, the sixth transistor M6 is turned-on to electrically connect the second node N2 to the reference power supply Vref.

[0061] FIG. 7 is a waveform diagram showing a method of driving the pixel shown in FIG. 6. Referring to FIG. 7, firstly, the scan signal is provided to the (i-2)th scan line Si-2. When the scan signal is provided to the (i-2)th scan line Si-2, the sixth transistor M6 is turned-on. When the sixth transistor M6 is turned-on, a voltage of the reference power supply Vref is supplied to the second node N2. Namely, when the scan signal is provided to the (i-2)th scan line Si-2, a voltage of the second node N2 is initialized with the voltage of the reference power supply Vref. Accordingly, all pixels 240 included in the pixel region 230 receive the same voltage in the second node N2 at an initialization step. In other words, because the second node N2 is initialized using the reference power supply Vref in which a voltage drop does not occur, each of the second nodes N2 of the pixels 240 may be initial-

ized with the same voltage regardless of the locations of the pixels 240 in the pixel region 230.

[0062] Next, the scan signal is provided to the (i-1)th scan line Si-1. When the scan signal is provided to the (i-1)th scan line Si-1, the third transistor M3 and the fourth transistor M4 are turned-on. When the third transistor M3 is turned-on, the second transistor M2 is diode-connected. Here, the second node N2 is initialized with a voltage of the reference power supply Vref that is less than a voltage of the first power supply ELVDD and the second transistor M2 is turned-on, so that a voltage obtained by subtracting a threshold voltage of the second transistor M2 from a voltage of the first power supply ELVDD is applied to the second node N2.

[0063] When the fourth transistor M4 is turned-on, a voltage of the reference power supply Vref is applied to the first node N1. Accordingly, the second capacitor C2 is charged with a voltage including a voltage drop of the first power supply ELVDD and a threshold voltage of the second transistor M2.

[0064] Then, the scan signal is provided to an i-th scan line Si. When the scan signal is provided to the i-th scan line Si, the first transistor M1 is turned-on. When the first transistor M1 is turned-on, a data signal supplied to the data line Dm is provided to the first node N1. Accordingly, a voltage of the first node N1 drops from a voltage of the reference power supply Vref to a voltage of the data signal.

[0065] At this time, a voltage of the second node N2 set as a floating state also drops corresponding to the voltage drop of the first node N1, so that the voltage charged in the second capacitor C2 is stably maintained. The first capacitor C1 is charged with a voltage corresponding to the data signal, which is applied to the first node N1.

[0066] Next, as a supply of the emission control signal stops, the fifth transistor M5 is turned-on. When the fifth transistor M5 is turned-on, the second transistor M2 provides an electric current corresponding to voltages charged in the first and second capacitors C1 and C2 to the organic light emitting diode (OLED), so that the organic light emitting diode (OLED) generates light having a luminance corresponding to the current.

[0067] As described previously, in the pixel 240 according to the embodiment of the present invention, while the scan signal is supplied to the (i-2)th scan line Si-2, the gate electrode of the second transistor M2 is initialized with a voltage of the reference power supply Vref. Accordingly, when the pixel 240 are used the gate electrode of the second transistor M2 included in each of the pixels 240 can be initialized with the same voltage. Accordingly, this embodiment of the present invention may stably compensate for the threshold voltage of the second transistor M2 while the scan signal is being provided to the (i-1)th scan line Si-1. The embodiment of the present invention is applicable to a panel of large size and high resolution.

[0068] As mentioned above, in accordance with embodiments including a pixel, an organic light emitting display, and a method for driving an organic light emitting display using the pixel of the present invention, a threshold voltage of a drive transistor and a voltage drop of a first power supply may be compensated for, thereby displaying an image of substantially uniform luminance. Further, since the embodiments of the present invention initialize pixels using a reference voltage, it can initialize all pixels with the same voltage. In addition, embodiments of the present invention can stably compensate for the threshold voltage of a drive transistor, which supplies a scan signal to one scan line.

Claims

1. An organic light emitting display comprising:

a scan driver adapted to sequentially provide a scan signal to a plurality of scan lines, and to sequentially provide an emission control signal to a plurality of emission control lines;
a data driver adapted to provide a data signal to a plurality of data lines in synchronization with the scan signal; and
a plurality of pixels arranged in a plurality of rows, wherein each row of pixels is connected to a corresponding one of the scan lines (Si), and wherein each of the pixels comprises a pixel circuit (242) coupled to the corresponding one of the scan lines (Si), a second scan line (Si-1), and a third scan line (Si-2), the second scan line (Si-1) being a corresponding scan line of a first preceding row of pixels and the third scan (Si-2) line being a corresponding scan line of a second preceding row of pixels preceding the first preceding row of pixels, the pixel circuit comprising:

an organic light emitting diode (OLED);
a first transistor (M1) having a gate electrode connected to the corresponding one of the scan lines (Si), a first terminal connected to a data line (Dm), and a second terminal connected to a first node (N 1);
a second transistor (M2) configured to allow an electric current to flow from a first power supply (ELVDD) to a second power supply (ELVSS) through the organic light emitting diode (OLED) and having a first terminal connected to the first power supply (ELVDD) and a gate electrode connected to a second node (N2);
a third transistor (M3) having a gate electrode connected to the second scan line (Si-1), a first terminal connected to the second node (N2), and a second terminal connected to a second terminal of the second tran-

sistor (M2);
a first capacitor (C1) having a first terminal connected to the first power supply (ELVDD) and a second terminal connected to the first node (N1); and
a second capacitor (C2) having a first terminal connected to the first node (N1) and a second terminal connected to the second node (N2),
the pixel circuit (242) being **characterised by**
a fourth transistor (M4) having a gate electrode connected to the second scan line (Si-1), a first terminal connected to a reference power supply (Vref), and a second terminal connected to the first node (N1); and
a fifth transistor (M6) having a gate electrode connected to the third scan line (Si-2), a first terminal connected to the reference power supply (Vref), and a second terminal connected to the second node (N2).

2. The organic light emitting display as claimed in claim 1, wherein a voltage of the reference power supply is greater than a maximum voltage of the data signal.

3. The organic light emitting display as claimed in claim 2, wherein the voltage of the reference power supply is less than the voltage of the first power supply.

4. The organic light emitting display according to one of the previous claims, further comprising a sixth transistor coupled between the second transistor and the organic light emitting diode, the sixth transistor being configured to be turned-on or turned-off according to an emission control signal supplied to an emission control line coupled to the pixel.

Patentansprüche

1. Eine organische lichtemittierende Anzeige, umfassend:

einen Abtasttreiber, der dazu ausgelegt ist, ein Abtastsignal sequenziell einer Vielzahl von Abtastleitungen bereitzustellen und ein Emissionssteuersignal sequenziell einer Vielzahl von Emissionssteuerleitungen bereitzustellen;
einen Datentreiber, der dazu ausgelegt ist, einer Vielzahl von Datenleitungen in Synchronisation mit dem Abtastsignal ein Datensignal bereitzustellen; und
eine Vielzahl von in einer Vielzahl von Zeilen angeordneten Pixeln, wobei jede Pixelzeile mit einer entsprechenden der Abtastleitungen (Si) verbunden ist und wobei jedes der Pixel eine mit der entsprechenden der Abtastleitungen (Si), einer zweiten Abtastleitung (Si-1) sowie einer dritten Abtastleitung (Si-2) verbundene Pixelschaltung (242) umfasst, wobei die zweite Abtastleitung (Si-1) eine entsprechende Abtastleitung einer ersten vorangehenden Pixelzeile ist und die dritte Abtastleitung (Si-2) eine entsprechende Abtastleitung einer zweiten vorangehenden Pixelzeile, die der ersten vorangehenden Pixelzeile vorangeht, ist, wobei die Pixelschaltung Folgendes umfasst:

eine organische Leuchtdiode (OLED);
einen ersten Transistor (M1), der eine mit der entsprechenden der Abtastleitungen (Si) verbundene Gate-Elektrode, einen mit einer Datenleitung (Dm) verbundenen ersten Anschluss sowie einen mit einem ersten Knoten (N1) verbundenen zweiten Anschluss aufweist;
einen zweiten Transistor (M2), der derart konfiguriert ist, dass er einem elektrischen Strom erlaubt, durch die organische Leuchtdiode (OLED) von einer ersten Stromversorgung (ELVDD) zu einer zweiten Stromversorgung (ELVSS) zu fließen, und der einen mit der ersten Stromversorgung (ELVDD) verbundenen ersten Anschluss sowie eine mit einem zweiten Knoten (N2) verbundene Gate-Elektrode aufweist;
einen dritten Transistor (M3), der eine mit der zweiten Abtastleitung (Si-1) verbundene Gate-Elektrode, einen mit dem zweiten Knoten (N2) verbundenen ersten Anschluss sowie einen mit einem zweiten Anschluss des zweiten Transistors (M2) verbundenen zweiten Anschluss aufweist;
einen ersten Kondensator (C1), der einen mit der ersten Stromversorgung (ELVDD) verbundenen ersten Anschluss sowie einen mit dem ersten Knoten (N1) verbundenen zweiten Anschluss aufweist; und
einen zweiten Kondensator (C2), der einen mit dem ersten Knoten (N1) verbundenen ersten Anschluss sowie einen mit dem zweiten Knoten (N2) verbundenen zweiten Anschluss aufweist,
wobei die Pixelschaltung (242) **gekennzeichnet ist durch**
einen vierten Transistor (M4), der eine mit der zweiten Abtastleitung (Si-1) verbundene Gate-Elektrode, einen mit einer Referenzstromversorgung (Vref) verbundenen ersten Anschluss sowie einen mit dem ersten Knoten (N1) verbundenen zweiten Anschluss aufweist; und
einen fünften Transistor (M6), der eine mit der dritten Abtastleitung (Si-2) verbundene Gate-Elektrode, einen mit der Referenz-

stromversorgung (Vref) verbundenen ersten Anschluss sowie einen mit dem zweiten Knoten (N2) verbundenen zweiten Anschluss aufweist.

2. Die organische lichtemittierende Anzeige nach Anspruch 1, wobei eine Spannung der Referenzstromversorgung größer als eine maximale Spannung des Datensignals ist.

3. Die organische lichtemittierende Anzeige nach Anspruch 2, wobei die Spannung der Referenzstromversorgung geringer als die Spannung der ersten Stromversorgung ist.

4. Die organische lichtemittierende Anzeige gemäß einem der vorhergehenden Ansprüche, ferner einen zwischen den zweiten Transistor und die organische Leuchtdiode geschalteten sechsten Transistor umfassend, wobei der sechste Transistor derart konfiguriert ist, dass er gemäß einem Emissionssteuersignal, das einer mit dem Pixel verbundenen Emissionsteuerleitung geliefert wird, eingeschaltet oder ausgeschaltet wird.

Revendications

1. Affichage électroluminescent organique comprenant :

un circuit d'attaque de balayage apte à fournier séquentiellement un signal de balayage à une pluralité de lignes de balayage, et à fournir séquentiellement un signal de commande d'émission à une pluralité de lignes de commande d'émission;
un circuit d'attaque de données apte à fournir un signal de donnée à une pluralité de lignes de données en synchronisme avec le signal de balayage ; et
une pluralité de pixels agencés en une pluralité de rangées, dans lequel chaque rangée de pixels est connectée à l'une, correspondante, des lignes (Si) de balayage, et dans lequel chacun des pixels comprend un circuit (242) de pixel associé à la ligne correspondante des lignes (Si) de balayage, à une deuxième ligne (Si-1) de balayage, et à une troisième ligne (Si-2) de balayage, la deuxième ligne (Si-1) de balayage étant une ligne de balayage correspondante d'une première rangée précédente de pixels et la troisième ligne (Si-2) de balayage étant une ligne de balayage correspondante d'une deuxième rangée précédente de pixels précédant la première rangée précédente de pixels, le circuit de pixel comprenant :

une diode électroluminescente organique (OLED) ;
un premier transistor (M1) ayant une électrode de grille connectée à la ligne correspondante des lignes (Si) de balayage, une première borne connectée à une ligne (Dm) de données, et une seconde borne connectée à un premier noeud (N1) ;
un deuxième transistor (M2) configuré pour permettre qu'un courant électrique s'écoule depuis une première alimentation (ELVDD) jusqu'à une seconde alimentation (ELVSS) à travers la diode électroluminescente organique (OLED) et ayant une première borne connectée à la première alimentation (ELVDD) et une électrode de grille connectée à un second noeud (N2) ;
un troisième transistor (M3) ayant une électrode de grille connectée à la deuxième ligne (Si-1) de balayage, une première borne connectée au second noeud (N2), et une seconde borne connectée à la seconde borne du deuxième transistor (M2) ;
un premier condensateur (C1) ayant une première borne connectée à la première alimentation (ELVDD) et une seconde borne connectée au premier noeud (N1) ;
et
un second condensateur (C2) ayant une première borne connectée au premier noeud (N1) et une seconde borne connectée au second noeud (N2),
le circuit (242) de pixel étant **caractérisé par** :

un quatrième transistor (M4) ayant une électrode de grille connectée à la deuxième ligne (Si-1) de balayage, une première borne connectée à une alimentation (Vref) de référence, et une seconde borne connectée au premier noeud (N1) ; et
un cinquième transistor (M6) ayant une électrode de grille connectée à la troisième ligne (Si-2) de balayage, une seconde borne connectée à l'alimentation (Vref) de référence, et une seconde borne connectée au second noeud (N2).

2. Affichage électroluminescent organique selon la revendication 1, dans lequel la tension de l'alimentation de référence est plus grande que la tension maximale du signal de donnée.

3. Affichage électroluminescent organique selon la revendication 2, dans lequel la tension de l'alimentation de référence est plus petite que la tension de la

première alimentation.

4. Affichage électroluminescent organique selon l'une des revendications précédentes, comprenant en outre un sixième transistor raccordé entre le deuxième transistor et la diode électroluminescente organique, le sixième transistor étant constitué pour être passant ou bloqué en fonction d'un signal de commande d'émission fourni à une ligne de commande d'émission associée au pixel.

FIG. 1
(PRIOR ART)

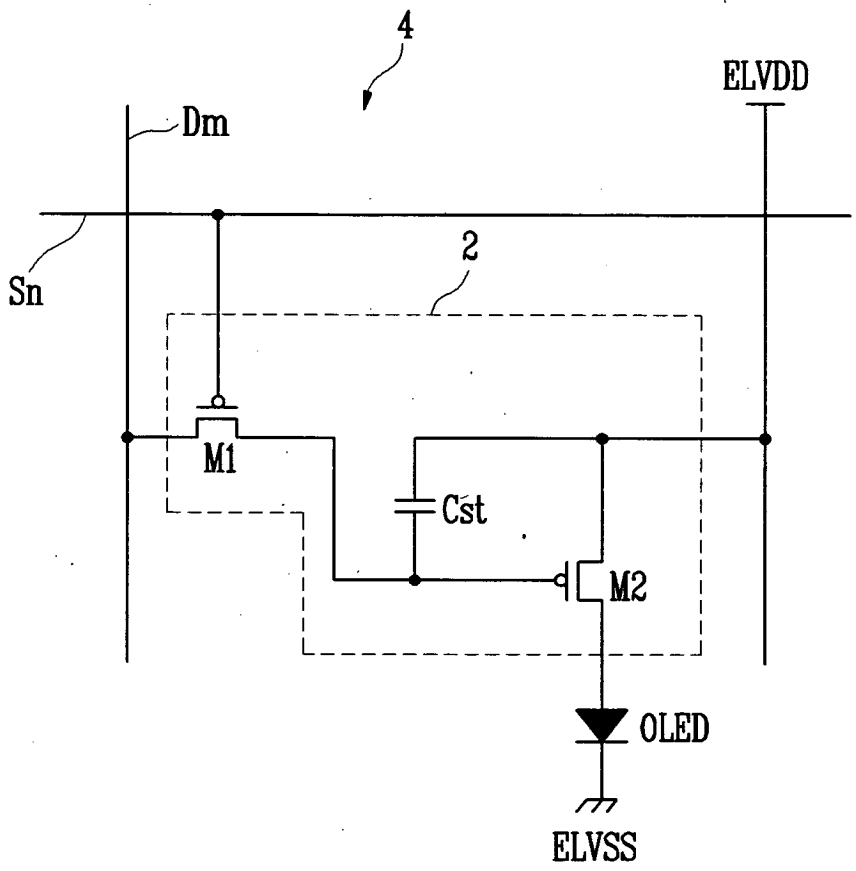


FIG. 2

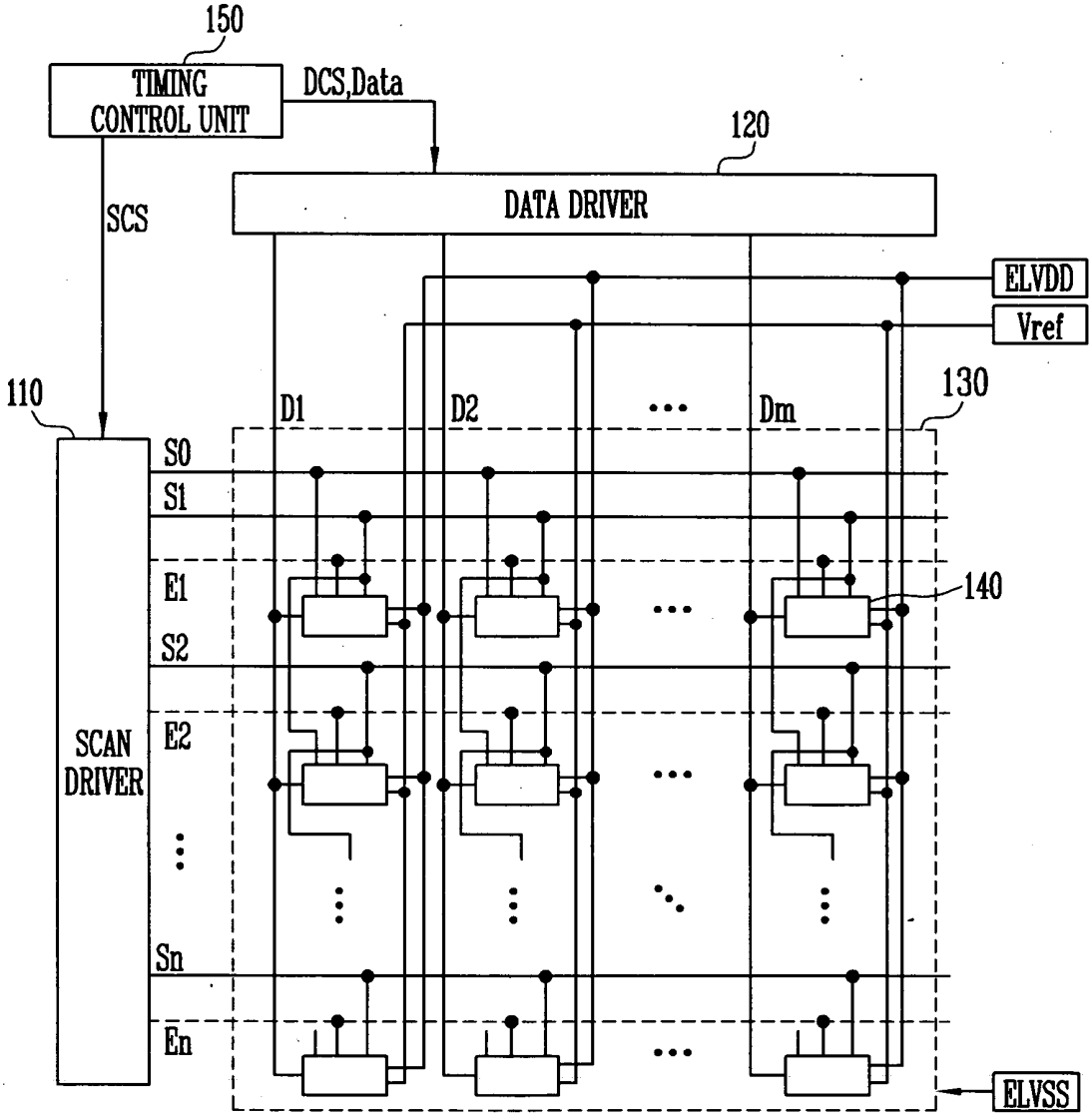

150
TIMING CONTROL UNIT
DCS,Data
120
DATA DRIVER
SCS
ELVDD
Vref
110
130
D1
D2
Dm
S0
S1
E1
140
S2
E2
SCAN DRIVER
Sn
En
ELVSS

FIG. 3

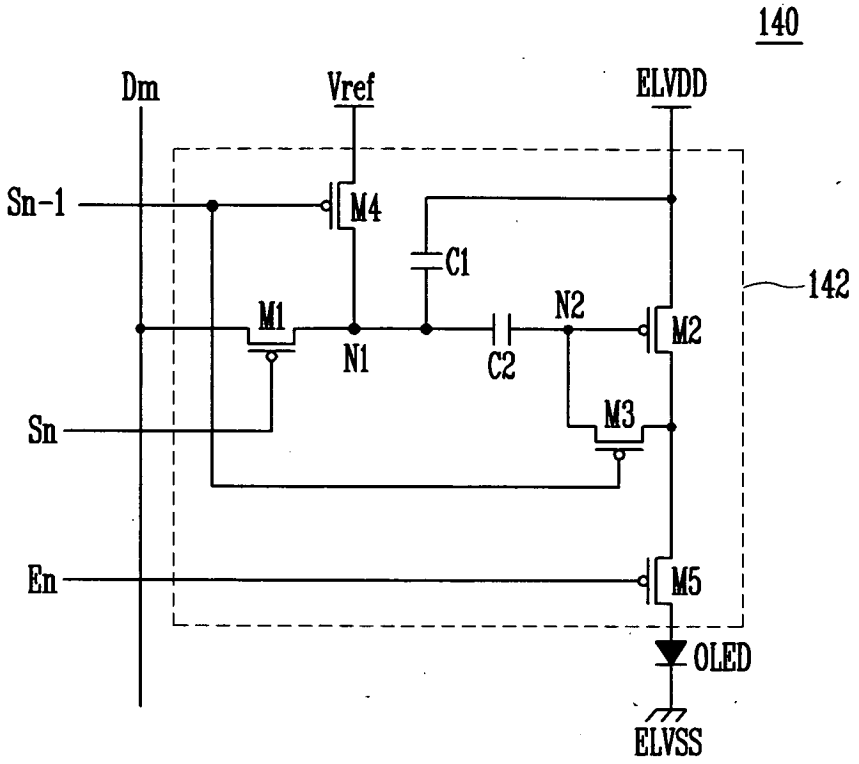

140
Dm
Vref
ELVDD
Sn-1
M4
C1
142
M1
N2
M2
N1
C2
Sn
M3
En
M5
OLED
ELVSS

FIG. 4

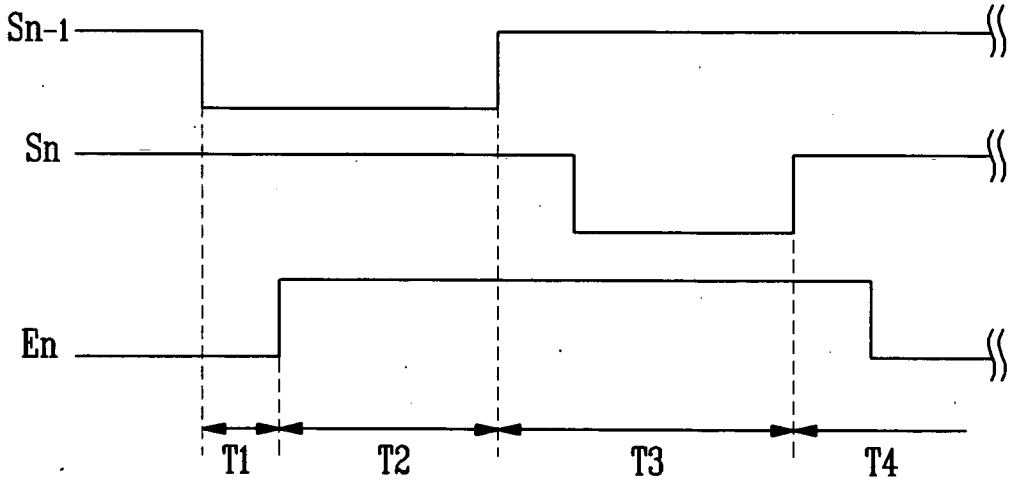

Sn-1
Sn
En
T1
T2
T3
T4

FIG. 5

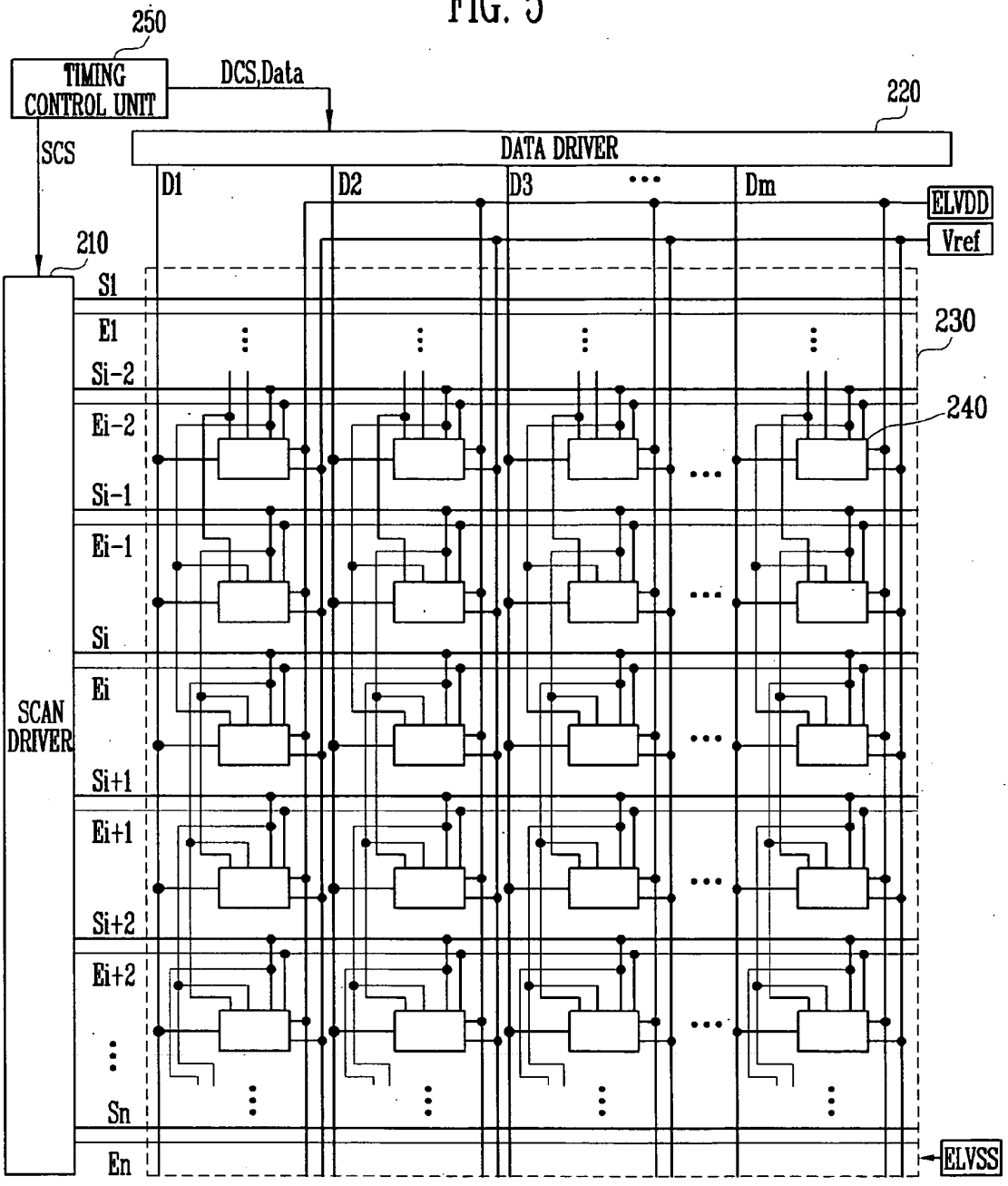

250
TIMING CONTROL UNIT
DCS,Data
220
SCS
DATA DRIVER
D1
D2
D3
Dm
ELVDD
Vref
210
S1
E1
Si-2
Ei-2
Si-1
Ei-1
Si
Ei
Si+1
Ei+1
Si+2
Ei+2
Sn
En
SCAN DRIVER
230
240
ELVSS

FIG. 6

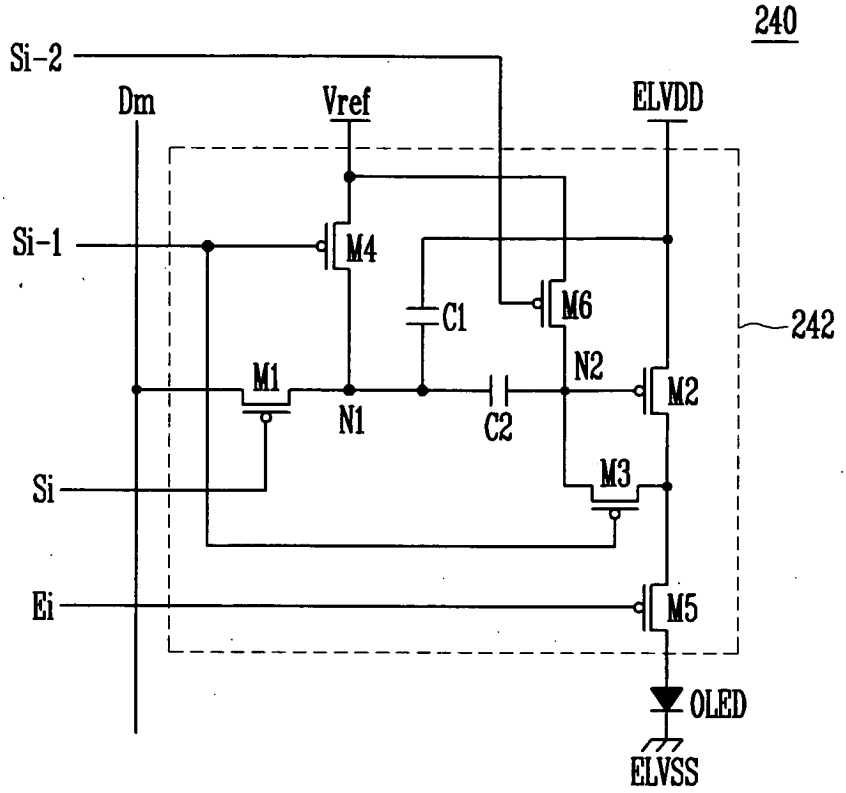
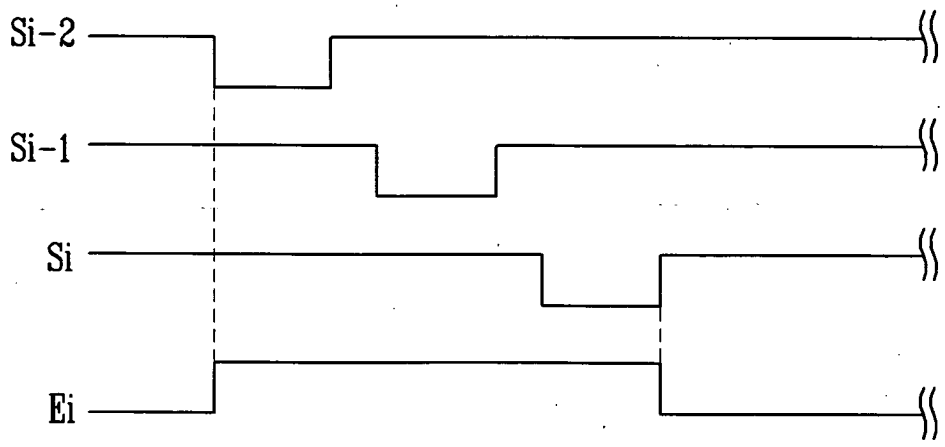

240
Si-2
Dm
Vref
ELVDD
Si-1
M4
C1
M6
242
M1
N2
M2
N1
C2
Si
M3
Ei
M5
OLED
ELVSS

FIG. 7


Si-2
Si-1
Si
Ei

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- WO 2006054189 A **[0011]**

专利名称(译)	有机发光显示器		
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申请号	EP2007114036	申请日	2007-08-08
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
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IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G2300/043 G09G2300/0819 G09G2300/0852 G09G2300/0861 G09G2310/0251 G09G2310/0262 G09G2320/0233 G09G2320/043 G09G2320/045		
代理机构(译)	hengelhaupt，Jürgen		
优先权	1020060074589 2006-08-08 KR		
其他公开文献	EP1887552A1		
外部链接	Espacenet		

摘要(译)

像素（242），有机发光显示器和使用像素（242）驱动有机发光显示器的方法，其可以显示具有基本均匀亮度的图像。在一个实施例中，用于驱动有机发光显示器的方法具有设置在第i水平线上的像素（242），该像素具有用于使电流能够流到有机发光二极管的驱动晶体管（M2），该方法包括向驱动晶体管（M2）的栅极提供参考电压（Vref），用驱动晶体管的阈值电压对第二电容器（C2）充电，用对应于电压的电压对第一电容器（C1）充电数据信号，并将与第一和第二电容器中的电压相对应的电流提供给有机发光二极管。