(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 1 764 774 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
29.04.2009 Bulletin 2009/18

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(21) Application number: **06254884.7**

(22) Date of filing: **20.09.2006**

(54) **Scan driving circuit and organic light emitting display using the same**

Zeilentreiber für eine Treiberschaltung einer Anzeigetafel und organische lichtemittierende Anzeige damit

Circuit de commande à balayage pour circuit de commande de panneau et affichage à diodes électroluminescentes organiques l'utilisant

(84) Designated Contracting States:
DE FR GB

(30) Priority: **20.09.2005 KR 20050087425**

(43) Date of publication of application:
21.03.2007 Bulletin 2007/12

(73) Proprietor: **Samsung Mobile Display Co., Ltd.**
Suwon-si
Gyeonggi-do (KR)

(72) Inventor: **Shin, Dony Yong**
c/o Samsung SDI Co, Ltd
Yongin-Si, Gyeonggi-do (DE)

(74) Representative: **Mounteney, Simon James**
Marks & Clerk LLP
90 Long Acre
London
WC2E 9RA (GB)

(56) References cited:
JP-A- 2004 325 940
US-B1- 6 392 628
US-B1- 6 556 646

EP 1 764 774 B1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to an organic light emitting display, and more particularly to a light emitting display and a driving method and circuit thereof, which may reduce the number of output lines in a data driver.

2. Description of the Related Technology

[0002] In general, an organic light emitting display electrically excites an organic compound such that it emits light. Circuits use voltage or current to drive an array of organic emitting cells so as to display images. Such an organic emitting cell often includes an anode formed of indium tin oxide (ITO), an organic thin film, and a cathode layer formed of metal.

[0003] The organic thin film has a multi-layer structure including an emitting layer (EML), an electron transport layer (ETL), and a hole transport layer (HTL) so as to maintain balance between electrons and holes and improve emitting efficiencies. The organic thin film may further include an electron injection layer (EIL) and a hole injecting layer (HIL).

[0004] Methods for driving organic emitting cells include a passive matrix method, and an active matrix method using thin film transistors (TFTs) or metal oxide semiconductor field effect transistors (MOSFETs). The passive matrix has cathode lines and anode lines crossing with each other, and selectively drives a cathode line and an anode line. The active matrix connects a TFT and a capacitor with each ITO pixel electrode to store a voltage according to the capacitor. The active matrix method is classified as either a voltage programming method or a current programming method according to signals supplied for storing the voltage at the capacitor.

[0005] The active matrix type of organic light emitting display includes a display panel, a data driving circuit, a scan driving circuit, and a timing controller. The scan driving circuit receives a scan drive control signal from the timing controller, generates a scan signal, and sequentially provides the scan signal to scan lines of the display panel.

[0006] That is, the scan driving circuit functions to sequentially generate the scan signal to be provided to the display panel in order to drive pixels included in the display panel.

[0007] FIG. 1 is a block diagram showing a conventional scan driving circuit. With reference to FIG. 1, the conventional scan driving circuit includes a plurality of stages ST 1 to STn, which are connected to a start pulse SP input line. The plurality of stages ST1 to STn sequentially shifts a clock pulse in response to a start clock SP so as to generate output signals SO1 to Son. In this case, each of second to n-th stages ST2 to STn receives and shifts an output signal of a previous stage as a start pulse.

[0008] Accordingly, the stages generate output signals SO1 to SOn in such a way that the start pulse is sequentially shifted, and provide the output signals to a matrix pixel array.

[0009] FIG. 2 is a circuit diagram of a stage in the scan driving circuit shown in FIG. 1. FIG. 3 is an input/output waveform diagram of the stage shown in FIG. 2. Referring to FIG. 2 and FIG. 3, each stage uses a master-slave flip-flop. When a clock clk is at low level, such a flip-flop continues to receive an input and maintains a previous output.

[0010] In contrast, when the clock elk has a high logic level, the flip-flop maintains an input IN received when the clock clk is at the low level, and outputs the received signal even if the input IN changes.

[0011] In the aforementioned circuit, an inverter included in the flip-flop, shown in FIG. 2, has a problem in that a static current flows when an input thereof is at low level. Furthermore, in the flip-flop, the number of inverters having received a high-level input is the same number as that of inverters having received a low-level input. Accordingly, the static current constantly flows through half of the inverters in the flip-flop, thereby causing excessive power consumption.

[0012] In addition, FIG. 2 shows an embodiment of the inverter circuit. According to this embodiment the high level output of the inverter is determined according to the ratio of resistance values of first and second PMOS transistors M1 and M2. The low level output of the inverter is determined according to the threshold voltage of the first PMOS transistor M1.

[0013] Due to manufacturing variations, resistance and threshold parameters vary significantly from transistor to transistor. This is a significant problem because the transistors for organic light emitting displays often have high manufacturing variability. As a result, the performance of the circuit of FIG. 2 is uncertain. For example, threshold variation causes the low level output of each inverter to vary. As a result, when a low level output from a first inverter having an uncertain value is provided as the input to a second inverter, the second inverter may have a degraded high output level because the uncertain low value results in uncertain pull-up resistance in the first PMOS transistor of the second inverter.

[0014] Furthermore, in the inverter, when outputting a high level, a constant electric current flows through both the first and second PMOS transistors M1 and M2. This results in constant power consumption. Also, the constant electric current flowing in the second PMOS transistor M2 causes slower rise times for the inverter output signal.

JP 2004 325940 discloses an active matrix type display device and its driving method. The luminance of a display screen is controlled by changing the length of a display output period using shift registers.

US 6392 628 discloses a semiconductor display device which performs image display by driving pixel TFTs ar-

ranged in a matrix state.

In US 6 556 646, a shift register for driving a pixel row in a liquid crystal display device is disclosed.

[0015] The present invention sets out to overcome the above problems with the prior art.

[0016] Accordingly, a first aspect of the invention provides a scan driving circuit as set out in Claim 1; a second aspect of the invention provides a scan driving circuit as set out in Claim 16.

[0017] Preferred features of the invention are as set-out in the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] These and/or other aspects and advantages will become apparent and more readily appreciated from the following description of embodiments, taken in conjunction with the accompanying drawings of which:

[0019] FIG. 1 is a block diagram showing a conventional scan driving circuit;

[0020] FIG. 2 is a circuit diagram of a stage in the scan driving circuit shown in FIG. 1;

[0021] FIG. 3 is an input/output waveform diagram of the stage shown in FIG. 2;

[0022] FIG. 4 is a block diagram showing an organic light emitting display according to one embodiment;

[0023] FIG. 5 is a circuit diagram showing an example of a pixel circuit arranged at each pixel region of the organic light emitting display shown in FIG. 4;

[0024] FIG. 6 is a waveform diagram of selection and emission signals that are supplied to the pixel circuit shown in FIG. 5;

[0025] FIG. 7 is a block diagram showing a configuration of a scan driving circuit according to one embodiment;

[0026] FIG. 8 is a circuit diagram of a stage in the scan driving circuit shown in FIG. 7; and

[0027] FIG. 9 is an input/output waveform diagram of the stage shown in FIG. 8.

DETAILED DESCRIPTION OF CERTAIN INVENTIVE EMBODIMENTS

[0028] Hereinafter, certain inventive embodiments will be described with reference to the accompanying drawings. Here, when a first element is connected to a second element, the first element may be directly connected to the second element or may be indirectly connected to the second element via a third element. Further, non-relevant, elements are omitted for clarity. Also, like reference numerals refer to like elements throughout.

[0029] FIG. 4 is a block view showing an organic light emitting display according to one embodiment.

[0030] As shown in FIG. 4, the organic light emitting display according to one inventive embodiment includes an organic light emitting display panel (referred to as "display panel" hereinafter) 100, a data driving circuit 200, and a scan driving circuit. The scan driving circuit includes a first scan driver 310 and a second scan driver 320. The first scan driver 310 provides a selection signal. The second scan driver 320 provides an emission signal.

[0031] The display panel 100 includes a plurality of data lines D 1 through Dn, a plurality of signal lines S1 to Sm and E1 to Em, and a plurality of pixel circuits 110. The plurality of data lines D1 through Dn are arranged in a row direction. The plurality of signal lines S1 to Sm and E1 to Em are arranged in a column direction. The plurality of pixel circuits 110 are arranged in a matrix pattern.

[0032] Here, the signal lines S1 to Sm and E1 to Em include a plurality of selection signal lines S1 to Sm for transferring a selection signal so as to select a pixel, and a plurality of emission signal lines E1 to Em for transferring an emission signal to control an emission period of an organic light emitting diode.

[0033] Further, pixel circuits 110 are formed at a pixel regions defined by the data lines D1 through Dn, the selection signal lines S1 to Sm, and the emission signal lines E1 to Em.

[0034] The data driving circuit 200 applies a data current I_{DATA} to the data lines D1 through Dn. The first scan driver 310 of the scan driving circuit 300 sequentially applies a selecting signal for selecting a pixel circuit 110 to the selection signal lines S 1 to Sm. Further, the second scan driver 320 applies an emission signal for controlling a luminance of the pixel circuit 110 to the emission signal lines E 1 to Em.

[0035] FIG. 5 is a circuit diagram showing an example of a pixel circuit shown in FIG. 4. However, in order to help understanding of the pixel circuit, only a pixel circuit connected to a j-th data line Dj and i-th signal lines Si and Ei is shown in FIG. 5.

[0036] As shown in FIG. 5, the pixel circuit according to one embodiment includes an organic light emitting diode OLED, transistors m1 to m4, and a capacitor Cst. Here, although PMOS transistors are used for each of the transistors m1 to m4, NMOS and CMOS implementations are also possible.

[0037] A first transistor m1 is coupled between a power supply VDD and an organic light emitting diode OLED, and controls an electric current through the organic light emitting diode OLED. In detail, a source of the first transistor m1 is coupled with the power supply VDD, and a drain thereof is coupled with a cathode of the organic light emitting diode OLED through a third transistor m3.

[0038] Furthermore, in response to a selection signal from the selection signal line Si, the second transistor m2 passes a voltage from the data line Dj to a gate of the first transistor m1. A fourth transistor m4 diode-connects the first transistor m1 in response to the selection signal.

[0039] Moreover, the capacitor Cst is coupled between a gate and a source of the first transistor m1, and is charged with a voltage corresponding to the gate voltage of the first transistor m1 sourcing the data current I_{DATA} to the data line Dj. A third transistor m3 passes an electric current flowing through the first transistor m1 to the or-

ganic light emitting diode OLED in response to an emission signal from the emission signal line Ei.

[0040] FIG. 6 is a waveform diagram of selection and emission signals that are supplied to the pixel circuit shown in FIG. 5.

[0041] As shown in FIG. 6, a selection signal to turn-on the second transistor m2 and the fourth transistor m4 is sequentially applied to selection signal lines Si, Si+1, and Si+2. When the second transistor m2 and the fourth transistor m4 are turned on, the capacitor Cst is charged with a voltage corresponding to the gate voltage of the first transistor m1 in response to the first transistor m1 sourcing the data current I_{DATA} to the data lines D1 to Dn while being diode connected by the second and fourth transistors m2 and m4. Accordingly, the capacitor Cst stores a voltage corresponding to the gate voltage of the first transistor m1 while sourcing the data current I_{DATA}.

[0042] After the charge is stored, the selection signal Si is removed and the emission signal Ei is applied. In response, the second and fourth transistors m2 and m4 are turn off, and the third transistor m3 is turns on. Because the first transistor m1 gate voltage is maintained by the capacitor Cst, a data current I_{DATA} flows through the first and third transistors m1 and m3 to the OLED.

[0043] In some embodiments, the emission signal may be applied to the emission signal lines Ei, Ei+1, and Ei+2 during the rest of the frame time in such a way that the level is changed. For example, as shown in FIG. 6 a low level and a high level may be sequentially applied to the signal lines Ei, Ei+1, and Ei+2.

[0044] In this embodiment, when the emission signal applied to the emission signal lines Ei, Ei+1, and Ei+2 has a low level, the third transistor m3 is turned on, and thus an electric current sourced from the first transistor m1 is supplied to the organic light emitting diode OLED, with the result that the organic light emitting diode OLED emits light in response to the electric current. In contrast to this, when the emission signal is at a high level, the third transistor m3 is turned off, thus electric current applied from the first transistor m1 is not supplied to the organic light emitting diode OLED, with the result that the organic light emitting diode OLED does not emit light

[0045] Accordingly, during a recording period Pw the emission signal line is high such that the third transistor m3 is off, and the selection signal Si is low such that the first transistor m1 is diode connected and the capacitor Cst is charged with a voltage corresponding to the data current I_{DATA} from the data lines D1 to Dn.

[0046] Next, during an on period Pon, the emission signal line Ei is low such that the current sourced from the first transistor is applied to the OLED, which emits light in response to the applied current. Next, during an off period Poff, the emission signal line Ei is high such that the OLED receives substantially no current and is accordingly dark. As shown in FIG. 6 on periods Pon and off periods Poff may be sequentially alternated. In some embodiments, on periods Pon and off periods Poff may be of unequal durations. In some embodiments the alternating on periods Pon and off periods Poff may continue throughout the frame period. In such embodiments the portion of on time for the OLED may be regulated by control of the duty cycle of the emission signal Ei. For example a duty cycle on emission signal Ei of about 50% corresponds to the OLED being on about 50% of the frame period.

[0047] As seen from FIG. 4, the selection signal and the emission signal are provided to a panel through the first scan driver 310 and the second scan driver 320, respectively. Construction and operation of the scan driving circuit according to some embodiments will be explained. In these embodiments the selection signal and the emission signal have waveforms as shown in FIG. 6, but other waveforms and corresponding embodiments are also possible.

[0048] FIG. 7 is a block diagram showing an embodiment of a scan driving circuit. As noted previously, the scan driving circuit 300 includes a first scan driver 310 and a second scan driver 320. The first scan driver 310 outputs a selection signal for driving a m by n pixel array. The second scan driver 320 outputs an emission signal. The first driver 310 includes first n stages that are coupled with a first input signal IN1 line. The second driver 320 includes second n stages that are coupled with a second input signal IN2 line.

[0049] First output lines of the first n stages are coupled with first n row lines S 1 to Sn in the pixel array, and provide a selection signal to the pixel rows. Second output lines of the second n stages are coupled with second n row lines E1 to En in the pixel array, and provide an emission signal to the pixel rows.

[0050] Here, a first input signal IN1 is supplied to a first stage in the first scan driver 310, and a second input signal IN2 is supplied to a first stage in the second scan driver 320. Output signals of first to (n-1) th stages are supplied to respective next stages as input signals.

[0051] Further, each stage of the first scan driver 310 includes a first clock terminal CLKa and a second clock terminal CLKb. First and second opposite phase clock signals CLK1 and CLK2 are supplied to the first clock terminal CLKa and the second clock terminal CLKb. A first clock signal CLK1 is supplied to the first clock terminal CLKa of odd-numbered stages in the first scan driver 310, and a second clock signal CLK2 is supplied to the second clock terminal CLKb. In contrast to this, the second clock signal CLK2 is supplied to first clock terminal CLKa of even-numbered stages, and the first clock signal CLK1 is supplied to a second clock terminal CLKb of the even-numbered stages.

[0052] Each stage receives the first input signal IN1 or an output voltage gi of a previous stage, and the first and second clock signals CLK1 and CLK2. In response, each stage sequentially outputs a low-level signal through an output line.

[0053] Similarly, each stage of the second scan driver 320 includes a first clock terminal CLKa and a second clock terminal CLKb. First and second phase inverted

clock signals CLK1 and CLK2, are supplied to the first clock terminal CLKa and the second clock terminal CLKb. The second clock signal CLK2 is supplied to the first clock terminal CLKa of odd-numbered stages in the second scan driver 320, and a first clock signal CLK1 is supplied to the second clock terminal CLKb. In contrast to this, the first clock signal CLK1 is supplied to a first clock terminal CLKa of even-numbered stages, and the second clock signal CLK2 is supplied to a second clock terminal CLKb of the even-numbered stages.

[0054] Each stage receives the first input signal IN2, or an output voltage gi of a previous stage, and the first and second clock signals CLK1 and CLK2. In response, each stage sequentially outputs an emission signal through an output line in such a way that the emission signal alternate between low and high levels.

[0055] FIG. 8 is a circuit diagram of a stage in the scan driving circuit shown in FIG. 7. FIG. 8 shows a detailed circuit arrangement of an odd-numbered stage 312 of the first scan driver, and a detailed circuit arrangement of an odd-numbered stage 322 of the second scan driver. FIG. 9 is an input/output waveform diagram of the stage shown in FIG. 8.

[0056] With reference to FIG. 8 and FIG. 9, one cycle of input clock signals CLK1 and CLK2 is divided into first and second time periods. Odd-numbered stages 312 and 322 of the first scan driver and the second scan driver each perform a precharge operation during the first time period. The odd-numbered stages 312 and 322 perform an evaluation operation during the second time period that causes a pulse of a low level to be shifted and output for a half period of the clock signal. The odd-numbered stages 312 and 322 each output a high-level signal during the precharge period, and output a signal corresponding to an input received during the evaluation period.

[0057] Moreover, by arranging the evaluation period of the odd-numbered stages so as to coincide with the precharge period of even-numbered stages, a low-level signal is transferred sequentially through all stages, where transfers occur at times corresponding to a half periods of the clock.

[0058] Hereinafter, operation of odd numbered stage 312 will be explained in detail by reference to a circuit arrangement of an odd-numbered stage shown in FIG. 8. Other stages including even numbered stages of the first scan driver, as well as the stages of the second scan driver have similar structure.

[0059] PMOS thin film transistors will be now described as an example of transistors included in the stages. However, an embodiment of the present invention is not limited thereto. For example, NMOS transistors may additionally or alternatively be used.

[0060] Referring to FIG. 8, the odd numbered stage 312 includes a first PMOS transistor M1, a second PMOS transistor M2, a third PMOS transistor M3, a fourth PMOS transistor M4, and a fifth PMOS transistor M5. The first PMOS transistor M1 receives an output voltage gi of a previous stage or a first input signal IN1. A gate terminal of the first PMOS transistor M1 is coupled with a first clock terminal CLK1. The second PMOS transistor M2 is coupled with a second clock terminal CLK2 and an output line OUT, and a gate terminal of the second PMOS transistor M2 is coupled with an output terminal of the first PMOS transistor M1. The third PMOS transistor M3 is coupled between a second power supply VSS and a first node N1, and has a gate terminal coupled with the first clock terminal CLK1. The fourth PMOS transistor M4 is coupled between the first clock terminal and the first node N1, and has a gate terminal coupled with an output terminal of the first PMOS transistor M1. The fifth PMOS transistor M5 is coupled between a first power supply VDD and the output line OUT, and has a gate terminal coupled with the first node N1. The odd numbered stage 312 further includes a first capacitor C 1 that is coupled between an output terminal of the first PMOS transistor M1 and the output line OUT.

[0061] As shown, odd-numbered stage 312 of the first scan driver has a first clock signal CLK1 supplied to the first clock terminal, and a second clock signal CLK2 supplied to the second clock terminal. Odd numbered stage 322 of the second scan driver has the second clock signal CLK2 supplied to the first clock terminal, and the first clock signal CLK1 supplied to the second clock terminal.

[0062] In contrast to this, when the stage is an even numbered stage of the first scan driver, a first clock signal CLK1 is supplied to the second clock terminal, and a second clock signal CLK2 is supplied to the first clock terminal. Also, when the stage is an even numbered stage of the second scan driver, the first clock signal CLK1 is supplied to the first clock terminal, and the second clock signal CLK2 is supplied to the second clock terminal.

[0063] Furthermore, a negative supply voltage may be applied to the second power supply VSS. The second power supply VSS may be grounded as shown in FIG. 8.

[0064] Each stage includes a transfer unit, an inversion unit, and a buffer unit. In the embodiment of FIG. 8, the transfer unit is composed of a first PMOS transistor M1, a second PMOS transistor M2, and a first capacitor C1. The inversion unit is composed of first, third, and fourth PMOS transistors M1, M3, and M5.

[0065] Assuming that the stage is an odd-numbered stage 312 of the first scan driver, a time period when the first clock signal CLK1 has a low level and the second clock signal CLK2 has a high level becomes a precharge period. A time period when the first clock signal CLK1 has a high level and the second clock signal CLK2 has a low level becomes an evaluation period. The odd-numbered stage 312 of the first scan driver outputs a high-level signal during the precharge period, and during the evaluation period outputs a signal corresponding to an input received during the precharge period.

[0066] In contrast to this, assuming that the stage is an odd-numbered stage 322 of the second scan driver, a time period when the first clock signal CLK1 has a high level and the second clock signal CLK2 has a low level

becomes a precharge period. A time period when the first clock signal CLK1 has a low level and the second clock signal CLK2 has a high level becomes an evaluation period. The odd-numbered stage 322 of the second scan driver outputs a high-level signal during the precharge period, and during the evaluation period outputs a signal corresponding an input received during the precharge period.

[0067] An operation of the odd-numbered stage 312 of the first scan driver will be explained with reference to FIG. 8 and FIG. 9. First, during the precharge period the first clock signal CLK1 of a low level and the second clock signal CLK2 of a high level are input. Accordingly, the first and third transistors M 1 and M3 are turned on, whereby an input signal IN1 is passed to gate terminals of the second and fourth transistors M2 and M4.

[0068] Accordingly, since an output voltage of a previous stage or an input signal IN1 is stored in the first capacitor C1 as an input signal, and a first node N1 is charged with a first clock signal CLK1 or a low-level signal from the second power supply VSS, the fifth transistor M5 is turned-on, with the result that a first power supply VDD of a high level is output to an output terminal OUT. That is, during the precharge period, the output of the buffer unit of the stage is a high level.

[0069] Moreover, during the evaluation period, the first clock signal CLK1 of a high level and the second clock signal CLK2 of a low level are input. Accordingly, the first transistor M1 is turned off, thus blocking the input signal IN1 and the third transistor M3 is accordingly turned off.

[0070] During the evaluation period, the capacitor C1 maintains the level of the input signal charged during the precharge period. When the input voltage received during the precharge period is at a high level, the fourth transistor M4 remains off during the evaluation period, and the buffer unit continues to output a high-level signal.

[0071] In contrast to this, when the input voltage received during the precharge period is at a low level, the fourth transistor M4 is on during the evaluation period, and the node N1 is connected to the first clock signal CLK1. Additionally, the second transistor M2 is on, and the output OUT of the buffer unit is connected to the second clock signal CLK2.

[0072] In summary, during the evaluation period, when a signal received during the precharge period, namely, an output voltage of a previous stage or an input signal IN1 is at a low level, the stage outputs a highlevel signal. Similarly, when the signal received during the precharge period is at a high level, the stage outputs a high level signal during the evaluation period.

[0073] Accordingly, each stage of the first scan driver receives a first input signal IN1, or an output voltage gi of a previous stage, and first and second clock signals CLK1 and CLK2. According to those input signals, each stage performs a precharge operation during a first time period, and performs an evaluation operation during a second time period. As the stages are serially connected, a low-level pulse is shifted and output by each sequential stage for a half period of input clock CLK1 and CLK2. Consequently, a low-level signal is sequentially output through an output line of each stage. The output lines of the stages are therefore configured for use as a selection signal for the pixel rows of the array.

[0074] The odd-numbered stage 322 of the second scan driver shown in FIG. 8 and described by timing signals in FIG. 9 has the same circuit arrangement as that of the odd-numbered stage 312 of the first scan driver described above, and thus the detailed description thereof is omitted.

[0075] In the odd-numbered stage 322 of the second scan driver, a second clock signal CLK2 is supplied to a first clock terminal and a first clock signal CLK1 is supplied to a second clock terminal. That is, signal/input correspondence is opposite that of the odd-numbered stage of the first scan driver.

[0076] Consequently, precharge periods and evaluation periods of the first and second scan drivers overlap. Namely, clock signals input to first and second clock terminals of even numbered stages of the first scan driver are identical with clock signals input to first and second clock terminals of odd numbered stages of the second scan driver. Similarly, clock signals input to first and second clock terminals of odd numbered stages of the first scan driver are identical to clock signals input to first and second clock terminals of even numbered stages of the second scan driver. Accordingly, when the odd-numbered stage of the first scan driver outputs a low-level signal, the odd-numbered stage of the second scan driver outputs a high-level signal.

[0077] Moreover, as shown in FIG. 9, a first input signal IN2 is supplied to the second scan driver during a time period corresponding to several periods of the clock signal, unlike a first input signal IN1 supplied to the first scan driver. In some embodiments, the time period has a constant duration for each data frame.

[0078] Consequently, in response to the first input signal IN2, and according to the operation described above, each stage of the second scan driver sequentially outputs a series of low-levels and high-levels The output signals of the stages are therefore configured for use as emission signals, to be provided to the pixel rows of a display array.

[0079] In some embodiments, the first input signal IN2 may be applied throughout the frame period. In such embodiments, the portion of on time for the OLED may be regulated by control of the duty cycle of the first and second clock signals CLK1 and CLK2, and consequently of the emission signal Ei. For example a duty cycle on emission signal Ei of about 50% corresponds to the OLED being turned on about 50% of the frame period.

[0080] As is made apparent from the above description, and in accordance with a scan driving circuit of these embodiments, a first scan driver providing a selection signal, and a second scan driver providing an emission signal cause the emission signal to be applied during a data frame period at least once so as to prevent the degradation of the pixels, which can occur when constant

current is drawn by conventional pixels.

[0081] Furthermore, because the stage circuits have substantially no static current, the stage circuits have minimal power consumption. Similarly, when driving purely capacitive loads, such as a pixel row, there is substantially no static output current, and power consumption is accordingly minimized. Consequently, for large capacitive loads, operation speed can be optimized without significant increase in power consumption.

[0082] Although embodiments of the present invention have been shown and described, it will be appreciated by those skilled in the art that many variations and modifications are possible without departing from the scope of the invention.

Claims

1. A scan driving circuit comprising:

a first scan driver (310) comprising a plurality of first stages (312) and configured to sequentially output a selection signal (Sn); and
a second scan driver (320) comprising a plurality of second stages (322) and configured to sequentially output an emission signal (En), **characterized in that**,
wherein each of the first (312) and second stages (322) comprises:

a first transistor (M1) configured to receive an output voltage of a previous stage (gi) or a first input signal (IN1, IN2), and comprising a gate terminal coupled to a first clock terminal (CLK1) and an output terminal;
a second transistor (M2) coupled between a second clock terminal (CLK2) and an output line (OUT), and comprising a gate terminal coupled to the output terminal of the first transistor (M1);
a first capacitor (C1) coupled between the output terminal of the first transistor (M1) and the output line (OUT).
a third transistor (M3) coupled between a second power supply (VSS) and a first node (N1), comprising a gate terminal coupled to the first clock terminal (CLK1);
a fourth transistor (M4) coupled between the first clock terminal (CLK1) and the first node (N1), and comprising a gate terminal coupled to the output terminal of the first transistor (M1); and
a fifth transistor (M5) coupled between a first power supply (VDD) and the output line (OUT), and comprising a gate terminal coupled to the first node (N1).

2. A scan driving circuit as claimed in claim 1, further comprising first and second clock input lines configured to receive first (CLK1) and second clock signals (CLK2) respectively.

3. A scan drive circuit as claimed in claim 1 or 2, wherein each stage (312, 322) is configured to perform a precharge operation outputting a high-level signal and receiving the input signal (IN1, IN2), wherein the precharge operation is performed during a first portion of a period of at least one of the first clock signal (CLK1) and the second clock signal (CLK2), and to output a level corresponding to the level of the input signal (IN1, IN2), wherein the plurality of stages (312, 322) are collectively configured to sequentially generate a series of low level pulses, and wherein the low level pulses are generated substantially once every half period of at least one of the first (CLK1) and second clock signals (CLK2).

4. A scan driving circuit as claimed in any of claims 1 to 3, wherein each of the first and second stages (312, 322) are configured to receive a signal at the first clock terminal (CLK1) and a signal at the second clock terminal (CLK2) having phases substantially inverted with respect to one another.

5. A scan driving circuit as claimed in any of claims 2 to 4, wherein the first clock input line is coupled to the first clock terminal (CLK1) of a plurality of odd numbered stages (312) of the first scan driver (310), and the second clock input line is coupled to the second clock terminal (CLK2) of the plurality of odd numbered stages (312) of the first scan driver (310).

6. A scan driving circuit as claimed in claim 5, wherein each of the plurality of odd numbered stages (312) of the first scan driver (310) is configured to perform a precharge operation when the first clock signal (CLK1) has a low level, and to perform an evaluation operation when the fist clock signal (CLK1) has a high level.

7. A scan driving circuit as claimed in claim 6, wherein performing the precharge operation comprises outputting a high level output and receiving an input signal (IN1, IN2), and performing the evaluation operation comprises outputting a level corresponding to the input signal (IN1, IN2), wherein the plurality of first stages (312) are collectively configured to sequentially generate a series of selection signals (Sn), and wherein the selection signals (Sn) are generated substantially once every half period of at least one of the first (CLK1) and second clock signals (CLK2).

8. A scan driving circuit as claimed in any of claims 1, wherein the second clock input line is coupled to the first clock terminal (CLK1) of a plurality odd numbered stages (312) of the second scan driver (320),

and the first clock input line is coupled to the second clock terminal (CLK2) of the plurality of odd numbered stages (322) of the second scan driver (320).

9. A scan driving circuit as claimed in claim 8, wherein each of the plurality of odd numbered stages (322) of the second scan driver (320) is configured to perform a precharge operation when the second clock signal (CLK2) has a low level, and to perform an evaluation operation when the second clock signal (CLK2) has a high level.

10. A scan driving circuit as claimed in claim 9, wherein performing the precharge operation comprises outputting a high level output and receiving an input signal (IN1, IN2), and performing the evaluation operation comprises outputting a level corresponding to the input signal (IN1, IN2), wherein the plurality of second stages (322) are collectively configured to sequentially generate a series of emission signals (En), wherein the emission signals (En) are generated substantially once every half period of at least one of the first (CLK1) and second clock signals (CLK2).

11. A scan driving circuit as claimed in any preceding claim, wherein each of the clock signals (CLK1, CLK2) input to each of the first (CLK1) and second clock terminals (CLK2) of an odd numbered stage (312) of the first scan driver (310) are substantially identical to each of the clock signals (CLK1, CLK2) input to each of the first (CLK1) and second clock terminals (CLK2) of an even-numbered stage of the second scan driver (320).

12. A scan driving circuit as claimed in any preceding claim, wherein each of the clock signals (CLK1, CLK2) input to each of the first (CLK1) and second clock terminals (CLK2) of an even numbered stage of the first scan driver (310) are substantially identical to each of the clock signals (CLK1, CLK2) input to each of the first (CLK1) and second clock terminals (CLK2) of an odd numbered stage (322) of the second scan driver (320).

13. A scan driving circuit as claimed in any of claims 2 to 12, wherein the plurality of stages (322) of the second scan driver (320) is configured to receive an input signal (IN2) of a duration substantially equal to an integral number of periods of at least one of the first (CLK1) and second clock signals (CLK2).

14. A scan driving circuit as claimed in claim 13, wherein the duration is substantially constant during different data frame periods.

15. A scan driving circuit as claimed in claim 13, wherein each stage (322) of the second scan driver (320) is configured to output a series of alternating high and low levels in response to the input signal (IN2).

16. An organic light emitting display comprising:

a pixel array coupled to selection signal lines (S1... Sm), data lines (D1...Dn), and light emitting signal lines (E1...Em);
a data driving circuit (200) configured to supply a data signal to the data lines (D1...Dn); and
a scan driving circuit according to any one of claims 1 to 15.

Patentansprüche

1. Abtasttreiberschaltung, umfassend:

einen ersten Abtasttreiber (310), der eine Vielzahl von ersten Stufen (312) umfasst und dafür konfiguriert ist, ein Auswahlsignal (Sn) sequentiell auszugeben; und
einen zweiten Abtasttreiber (320), der eine Vielzahl von zweiten Stufen (322) umfasst und dafür konfiguriert ist, ein Emissionssignal (En) sequentiell auszugeben, **dadurch gekennzeichnet, dass**
jede der ersten (312) und zweiten Stufen (322) umfasst:

einen ersten Transistor (M1), der dafür konfiguriert ist, eine Ausgangsspannung einer vorherigen Stufe (gi) oder ein erstes Eingangssignal (IN1, IN2) zu empfangen, und der einen Gate-Anschluss, der mit einem ersten Taktanschluss (CLK1) gekoppelt ist, und einen Ausgangsanschluss umfasst;
einen zweiten Transistor (M2), der zwischen einen zweiten Taktanschluss (CLK2) und eine Ausgangsleitung (OUT) gekoppelt ist und der einen Gate-Anschluss umfasst, der mit dem Ausgangsanschluss des ersten Transistors (M1) gekoppelt ist;
einen ersten Kondensator (C1), der zwischen den Ausgangsanschluss des ersten Transistors (M1) und die Ausgangsleitung (OUT) gekoppelt ist;
einen dritten Transistor (M3), der zwischen eine zweite Stromversorgung (VSS) und einen ersten Knoten (N1) gekoppelt ist und der einen Gate-Anschluss umfasst, der mit dem ersten Taktanschluss (CLK1) gekoppelt ist;
einen vierten Transistor (M4), der zwischen den ersten Taktanschluss (CLK1) und den ersten Knoten (N1) gekoppelt ist und der einen Gate-Anschluss umfasst, der mit dem Ausgangsanschluss des ersten Transistors

(M1) gekoppelt ist; und
einen fünften Transistor (M5), der zwischen eine erste Stromversorgung (VDD) und die Ausgangsleitung (OUT) gekoppelt ist und der einen Gate-Anschluss umfasst, der mit dem ersten Knoten (N1) gekoppelt ist.

2. Abtasttreiberschaltung nach Anspruch 1, ferner umfassend erste und zweite Takteingangsleitungen, die dafür konfiguriert sind, erste (CLK1) bzw. zweite Taktsignale (CLK2) zu empfangen.

3. Abtasttreiberschaltung nach Anspruch 1 oder 2, wobei jede Stufe (312, 322) dafür konfiguriert ist, einen Vorladevorgang durchzuführen, wobei ein Hochpegelsignal ausgegeben und das Eingangssignal (IN1, IN2) empfangen wird, wobei der Vorladevorgang während eines ersten Abschnitts einer Periode zumindest eines des ersten Taktsignals (CLK1) und des zweiten Taktsignals (CLK2) durchgeführt wird, und einen Pegel auszugeben, der dem Pegel des Eingangssignals (IN1, IN2) entspricht, wobei die Vielzahl von Stufen (312, 322) insgesamt dafür konfiguriert ist, eine Serie von Tiefpegelimpulsen sequentiell zu erzeugen, und wobei die Tiefpegelimpulse im Wesentlichen einmal in jeder Halbperiode zumindest eines der ersten (CLK1) und zweiten Taktsignale (CLK2) erzeugt werden.

4. Abtasttreiberschaltung nach einem der Ansprüche 1 bis 3, wobei jede der ersten und zweiten Stufen (312, 322) dafür konfiguriert ist, ein Signal am ersten Taktanschluss (CLK1) und ein Signal am zweiten Taktanschluss (CLK2) zu empfangen, die Phasen aufweisen, die im Wesentlichen umgekehrt zueinander sind.

5. Abtasttreiberschaltung nach einem der Ansprüche 2 bis 4, wobei die erste Takteingangsleitung mit dem ersten Taktanschluss (CLK1) einer Vielzahl von ungeradzahligen Stufen (312) des ersten Abtasttreibers (310) gekoppelt ist und die zweite Takteingangsleitung mit dem zweiten Taktanschluss (CLK2) der Vielzahl von ungeradzahligen Stufen (312) des ersten Abtasttreibers (310) gekoppelt ist.

6. Abtasttreiberschaltung nach Anspruch 5, wobei jede aus der Vielzahl von ungeradzahligen Stufen (312) des ersten Abtasttreibers (310) dafür konfiguriert ist, einen Vorladevorgang durchzuführen, wenn das erste Taktsignal (CLK1) einen Tiefpegel hat, und einen Bewertungsvorgang durchzuführen, wenn das erste Taktsignal (CLK1) einen Hochpegel hat.

7. Abtasttreiberschaltung nach Anspruch 6, wobei die Durchführung des Vorladevorgangs Ausgeben eines Hochpegelausgangssignals und Empfangen eines Eingangssignals (IN1, IN2) umfasst und die Durchführung des Bewertungsvorgangs Ausgeben eines Pegels umfasst, der dem Eingangssignal (IN1, IN2) entspricht, wobei die Vielzahl von ersten Stufen (312) insgesamt dafür konfiguriert ist, eine Serie von Auswahlsignalen (Sn) sequentiell zu erzeugen, und wobei die Auswahlsignale (Sn) im Wesentlichen einmal in jeder Halbperiode zumindest eines der ersten (CLK1) und zweiten Taktsignale (CLK2) erzeugt werden.

8. Abtasttreiberschaltung nach Anspruch 1, wobei die zweite Takteingangsleitung mit dem ersten Taktanschluss (CLK1) einer Vielzahl von ungeradzahligen Stufen (312) des zweiten Abtasttreibers (320) gekoppelt ist und die erste Takteingangsleitung mit dem zweiten Taktanschluss (CLK2) der Vielzahl von ungeradzahligen Stufen (322) des zweiten Abtasttreibers (320) gekoppelt ist.

9. Abtasttreiberschaltung nach Anspruch 8, wobei jede aus der Vielzahl von ungeradzahligen Stufen (322) des zweiten Abtasttreibers (320) dafür konfiguriert ist, einen Vorladevorgang durchzuführen, wenn das zweite Taktsignal (CLK2) einen Tiefpegel hat, und einen Bewertungsvorgang durchzuführen, wenn das zweite Taktsignal (CLK2) einen Hochpegel hat.

10. Abtasttreiberschaltung nach Anspruch 9, wobei die Durchführung des Vorladevorgangs Ausgeben eines Hochpegelausgangssignals und Empfangen eines Eingangssignals (IN1, IN2) umfasst und die Durchführung des Bewertungsvorgangs Ausgeben eines Pegels umfasst, der dem Eingangssignal (IN1, IN2) entspricht, wobei die Vielzahl von zweiten Stufen (322) insgesamt dafür konfiguriert ist, eine Serie von Emissionssignalen (En) sequentiell zu erzeugen, wobei die Emissionssignale (En) im Wesentlichen einmal in jeder Halbperiode zumindest eines der ersten (CLK1) und zweiten Taktsignale (CLK2) erzeugt werden.

11. Abtasttreiberschaltung nach einem der vorhergehenden Ansprüche, wobei jedes der Taktsignale (CLK1, CLK2), das in jeden der ersten (CLK1) und zweiten Taktanschlüsse (CLK2) einer ungeradzahligen Stufe (312) des ersten Abtasttreibers (310) eingegeben wird, im Wesentlichen identisch ist mit jedem der Taktsignale (CLK1, CLK2), das in jeden der ersten (CLK1) und zweiten Taktanschlüsse (CLK2) einer geradzahligen Stufe des zweiten Abtasttreibers (320) eingegeben wird.

12. Abtasttreiberschaltung nach einem der vorhergehenden Ansprüche, wobei jedes der Taktsignale (CLK1, CLK2), das in jeden der ersten (CLK1) und zweiten Taktanschlüsse (CLK2) einer geradzahligen Stufe des ersten Abtasttreibers (310) eingegeben wird, im Wesentlichen identisch ist mit jedem

der Taktsignale (CLK1, CLK2), das in jeden der ersten (CLK1) und zweiten Taktanschlüsse (CLK2) einer ungeradzahligen Stufe (322) des zweiten Abtasttreibers (320) eingegeben wird.

13. Abtasttreiberschaltung nach einem der Ansprüche 2 bis 12, wobei die Vielzahl von Stufen (322) des zweiten Abtasttreibers (320) dafür konfiguriert ist, ein Eingangssignal (IN2) mit einer Dauer zu empfangen, die im Wesentlichen gleich einer ganzzahligen Anzahl von Perioden zumindest eines der ersten (CLK1) und zweiten Taktsignale (CLK2) ist.

14. Abtasttreiberschaltung nach Anspruch 13, wobei die Dauer während verschiedener Datenrahmenperioden im Wesentlichen konstant ist.

15. Abtasttreiberschaltung nach Anspruch 13, wobei jede Stufe (322) des zweiten Abtasttreibers (320) dafür konfiguriert ist, eine Serie von alternierenden Hoch- und Tiefpegeln als Antwort auf das Eingangssignal (IN2) auszugeben.

16. Organische lichtemittierende Anzeige, umfassend:

eine Pixelanordnung, die mit Auswahlsignalleitungen (S1 ... Sm), Datenleitungen (D1 ... Dn) und lichtemittierenden Signalleitungen (E1 ... Em) gekoppelt ist;
eine Datentreiberschaltung (200), die dafür konfiguriert ist, ein Datensignal an die Datenleitungen (D1 ... Dn) zu liefern; und
eine Abtasttreiberschaltung nach einem der Ansprüche 1 bis 15.

Revendications

1. Circuit pilote de balayage comportant :

un premier pilote de balayage (310) comportant une pluralité de premiers étages (312) et configuré de manière à générer en sortie séquentiellement un signal de sélection (Sn), et
un second pilote de balayage (320) comportant une pluralité de seconds étages (322) et configuré de manière à générer en sortie séquentiellement un signal d'émission (En), **caractérisé en ce que**,
chacun des premiers (312) et seconds étages (322) comporte :

un premier transistor (M1) configuré pour recevoir une tension de sortie d'un étage précédent (gi) ou un premier signal d'entrée (IN1, IN2), et comportant une borne de grille couplée à une première borne d'horloge (CLK1) et une borne de sortie ;
un deuxième transistor (M2) couplé entre une seconde borne d'horloge (CLK2) et une ligne de sortie (OUT), et comportant une borne de grille couplée à la borne de sortie du premier transistor (M1) ;
un premier condensateur (C1) couplé entre la borne de sortie du premier transistor (M1) et la ligne de sortie (OUT) ;
un troisième transistor (M3) couplé entre un second bloc d'alimentation (VSS) et un premier noeud (N1), comportant une borne de grille couplée à la première borne d'horloge (CLK1) ;
un quatrième transistor (M4) couplé entre la première borne d'horloge (CLK1) et le premier noeud (N1), et comportant une borne de grille couplée à la borne de sortie du premier transistor (M1) ; et
un cinquième transistor (M5) couplé entre un premier bloc d'alimentation (VDD) et la ligne de sortie (OUT), et comportant une borne de grille couplée au premier noeud (N1).

2. Circuit pilote de balayage selon la revendication 1, comportant en outre, des première et seconde lignes d'entrée d'horloge configurées pour recevoir des premier (CLK1) et second signaux d'horloge (CLK2), respectivement.

3. Circuit pilote de balayage selon la revendication 1 ou 2, dans lequel chaque étage (312, 322) est configuré pour mettre en oeuvre une opération de précharge générant en sortie un signal de niveau élevé et recevant le signal d'entrée (IN1, IN2), dans lequel l'opération de précharge est mise en oeuvre au cours d'une première partie d'une période d'au moins l'un du premier signal d'horloge (CLK1) et du second signal d'horloge (CLK2), et pour générer en sortie un niveau correspondant au niveau du signal d'entrée (IN1, IN2), dans lequel la pluralité d'étages (312, 322) est collectivement configurée pour générer de manière séquentielle une série d'impulsions de niveau bas, et dans lequel les impulsions de niveau bas sont générées sensiblement à chaque demi-période d'au moins un des premier (CLK1) et second signaux d'horloge (CLK2).

4. Circuit pilote de balayage selon l'une quelconque des revendications 1 à 3, dans lequel chacun des premiers et seconds étages (312, 322) est configuré pour recevoir un signal au niveau de la première borne d'horloge (CLK1) et un signal au niveau de la seconde borne d'horloge (CLK2) présentant des phases sensiblement inversées l'une par rapport à l'autre.

5. Circuit pilote de balayage selon l'une quelconque

des revendications 2 à 4, dans lequel la première ligne d'entrée d'horloge est couplée à la première borne d'horloge (CLK1) d'une pluralité d'étages impairs (312) du premier pilote de balayage (310), et la seconde ligne d'entrée d'horloge est associée à la seconde borne d'horloge (CLK2) de la pluralité d'étages impairs (312) du premier pilote de balayage (310).

6. Circuit pilote de balayage selon la revendication 5, dans lequel chaque étage de la pluralité d'étages impairs (312) du premier pilote de balayage (310) est configuré pour mettre en oeuvre une opération de précharge lorsque le premier signal d'horloge (CLK1) a un niveau bas, et pour mettre en oeuvre une opération d'évaluation lorsque le premier signal d'horloge (CLK1) a un niveau élevé.

7. Circuit pilote de balayage selon la revendication 6, dans lequel l'étape consistant à mettre en oeuvre l'opération de précharge comporte l'étape consistant à générer en sortie une sortie de niveau élevé et à recevoir un signal d'entrée (IN1, IN2), et l'étape consistant à mettre en oeuvre l'opération d'évaluation comporte l'étape consistant à générer en sortie un niveau correspondant à celui du signal d'entrée (IN1, IN2), dans lequel la pluralité de premiers étages (312) est collectivement configurée pour générer de manière séquentielle une série de signaux de sélection (Sn), et dans lequel les signaux de sélection (Sn) sont générés sensiblement à chaque demi-période d'au moins l'un des premier (CLK1) et second signaux d'horloge (CLK2).

8. Circuit pilote de balayage selon la revendication 1, dans lequel la seconde ligne d'entrée d'horloge est couplée à la première borne d'horloge (CLK1) d'une pluralité d'étages impairs (312) du second pilote de balayage (320), et la première ligne d'entrée d'horloge est couplée à la seconde borne d'horloge (CLK2) de la pluralité d'étages impairs (322) du second pilote de balayage (320).

9. Circuit pilote de balayage selon la revendication 8, dans lequel chaque étage de la pluralité d'étages impairs (322) du second pilote de balayage (320) est configuré pour mettre en oeuvre une opération de précharge lorsque le second signal d'horloge (CLK2) a un niveau bas, et pour mettre en oeuvre une opération d'évaluation lorsque le second signal d'horloge (CLK2) a un niveau élevé.

10. Circuit pilote de balayage selon la revendication 9, dans lequel l'étape consistant à mettre en oeuvre l'opération de précharge comporte l'étape consistant à générer en sortie une sortie de niveau élevé et à recevoir un signal d'entrée (IN1, IN2), et l'étape consistant à mettre en oeuvre l'opération d'évaluation comporte l'étape consistant à générer en sortie un niveau correspondant à celui du signal d'entrée (IN1, IN2), dans lequel la pluralité de seconds étages (322) est collectivement configurée pour générer de manière séquentielle une série de signaux d'émission (En), dans lequel les signaux d'émission (En) sont générés sensiblement à chaque demi-période d'au moins l'un des premier (CLK1) et second signaux d'horloge (CLK2).

11. Circuit pilote de balayage selon l'une quelconque des revendications précédentes, dans lequel chacun des signaux d'horloge (CLK1, CLK2) entrés au niveau de chacune des première (CLK1) et seconde bornes d'horloge (CLK2) d'un étage impair (312) du premier pilote de balayage (310) est sensiblement identique à chacun des signaux d'horloge (CLK1, CLK2) entrés au niveau de chacune des première (CLK1) et seconde bornes d'horloge (CLK2) d'un étage pair du second pilote de balayage (320).

12. Circuit pilote de balayage selon l'une quelconque des revendications précédentes, dans lequel chacun des signaux d'horloge (CLK1, CLK2) entrés au niveau de chacune des première (CLK1) et seconde bornes d'horloge (CLK2) d'un étage pair du premier pilote de balayage (310) est sensiblement identique à chacun des signaux d'horloge (CLK1, CLK2) entrés au niveau de chacune des première (CLK1) et seconde bornes d'horloge (CLK2) d'un étage impair (322) du second pilote de balayage (320).

13. Circuit pilote de balayage selon l'une quelconque des revendications 2 à 12, dans lequel la pluralité d'étages (322) du second pilote de balayage (320) est configurée pour recevoir un signal d'entrée (IN2) d'une durée sensiblement égale à un nombre entier de périodes d'au moins l'un des premier (CLK1) et second signaux d'horloge (CLK2).

14. Circuit pilote de balayage selon la revendication 13, dans lequel la durée est sensiblement constante au cours des différentes périodes de trames de données.

15. Circuit pilote de balayage selon la revendication 13, dans lequel chaque étage (322) du second pilote de balayage (320) est configuré pour générer en sortie une série de niveaux bas et élevés en alternance, en réponse au signal d'entrée (IN2).

16. Écran à diodes électroluminescentes organiques comportant :

un réseau de pixels couplé à des lignes de signaux de sélection (S1 ... Sm), à des lignes de données (D1 ... Dn), et à des lignes de signaux électroluminescents (E1 ... Em) ;

un circuit pilote de données (200) configuré pour délivrer un signal de données aux lignes de données (D1 ... Dn), et
un circuit pilote de balayage selon l'une quelconque des revendications 1 à 15.

FIG. 1
(PRIOR ART)

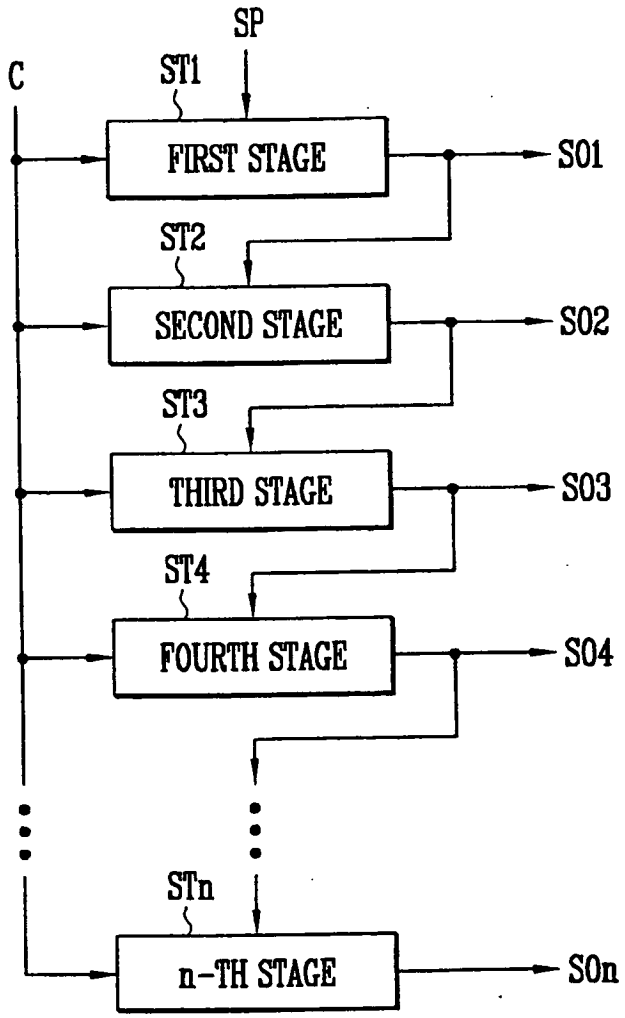


FIG. 2
(PRIOR ART)

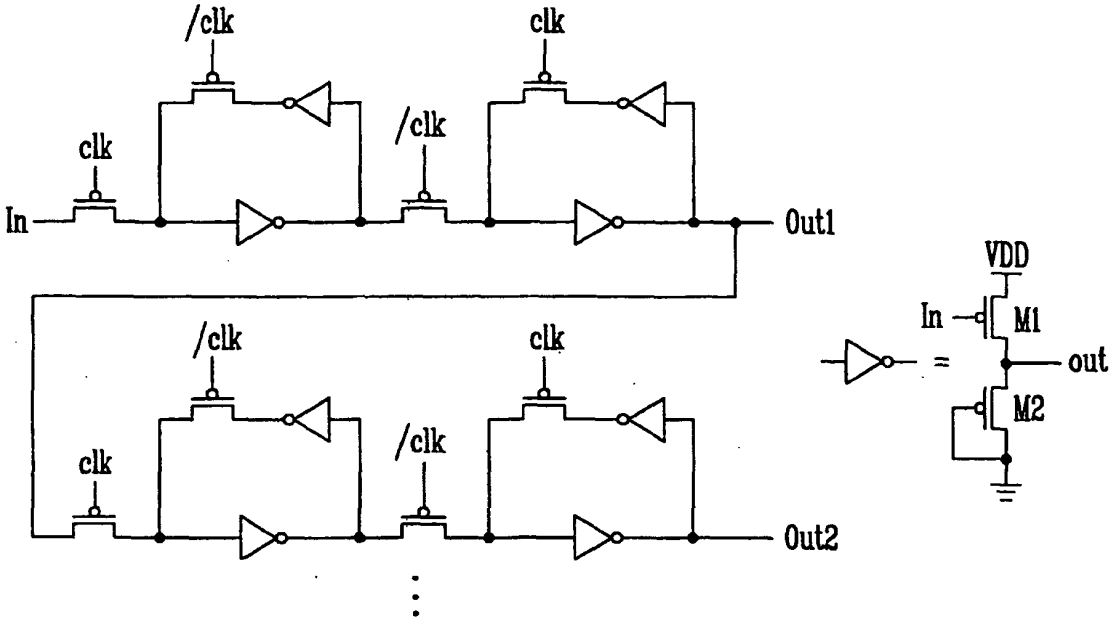


FIG. 3
(PRIOR ART)

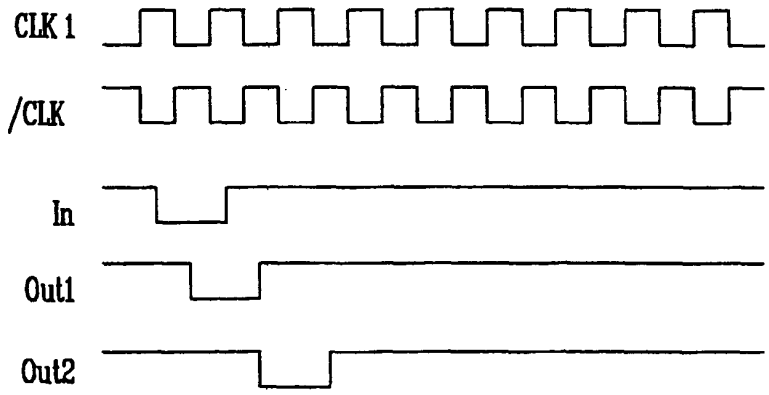


FIG. 4

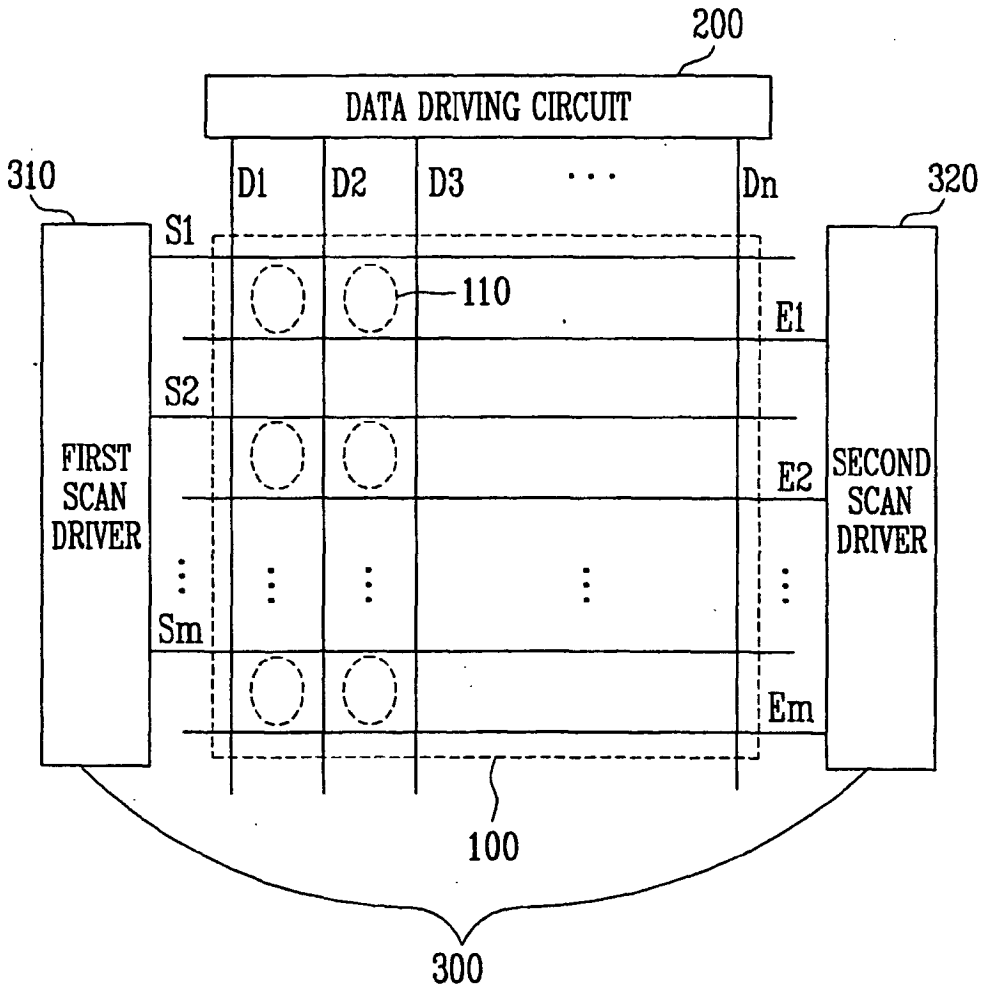

200
DATA DRIVING CIRCUIT
310
320
D1
D2
D3
Dn
S1
S2
Sm
110
E1
E2
Em
FIRST SCAN DRIVER
SECOND SCAN DRIVER
100
300

FIG. 5

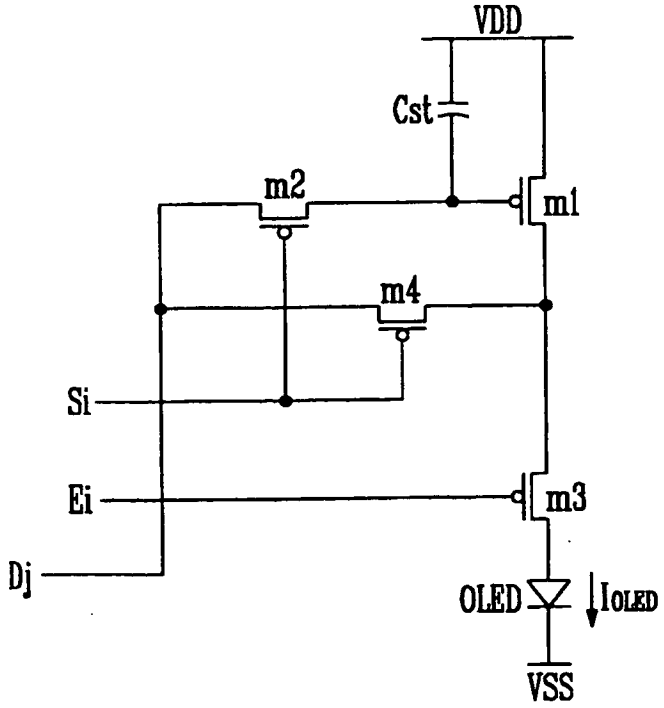

VDD
Cst
m2
m1
m4
Si
Ei
m3
Dj
OLED
IOLED
VSS

FIG. 6

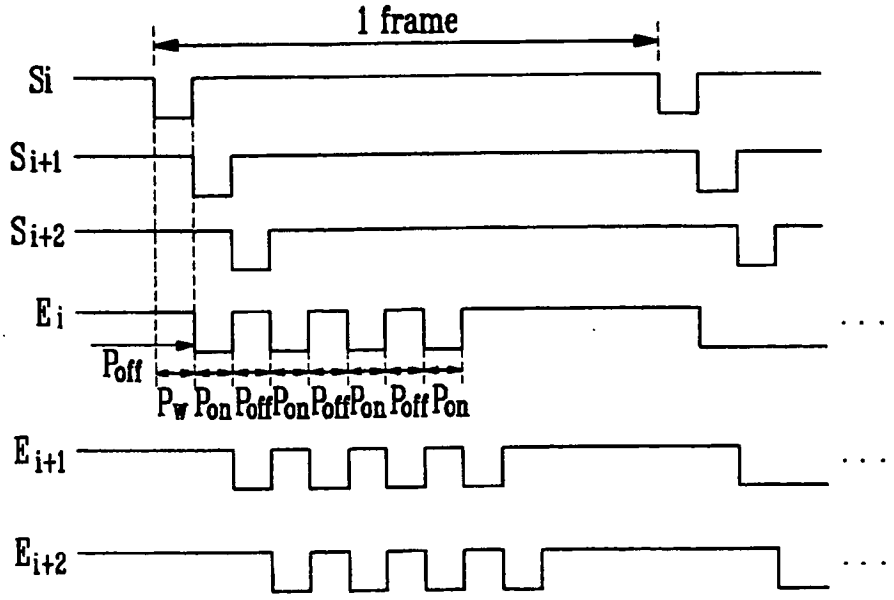

1 frame
Si
Si+1
Si+2
Ei
Poff
Pw Pon Poff Pon Poff Pon Poff Pon
Ei+1
Ei+2

FIG. 7

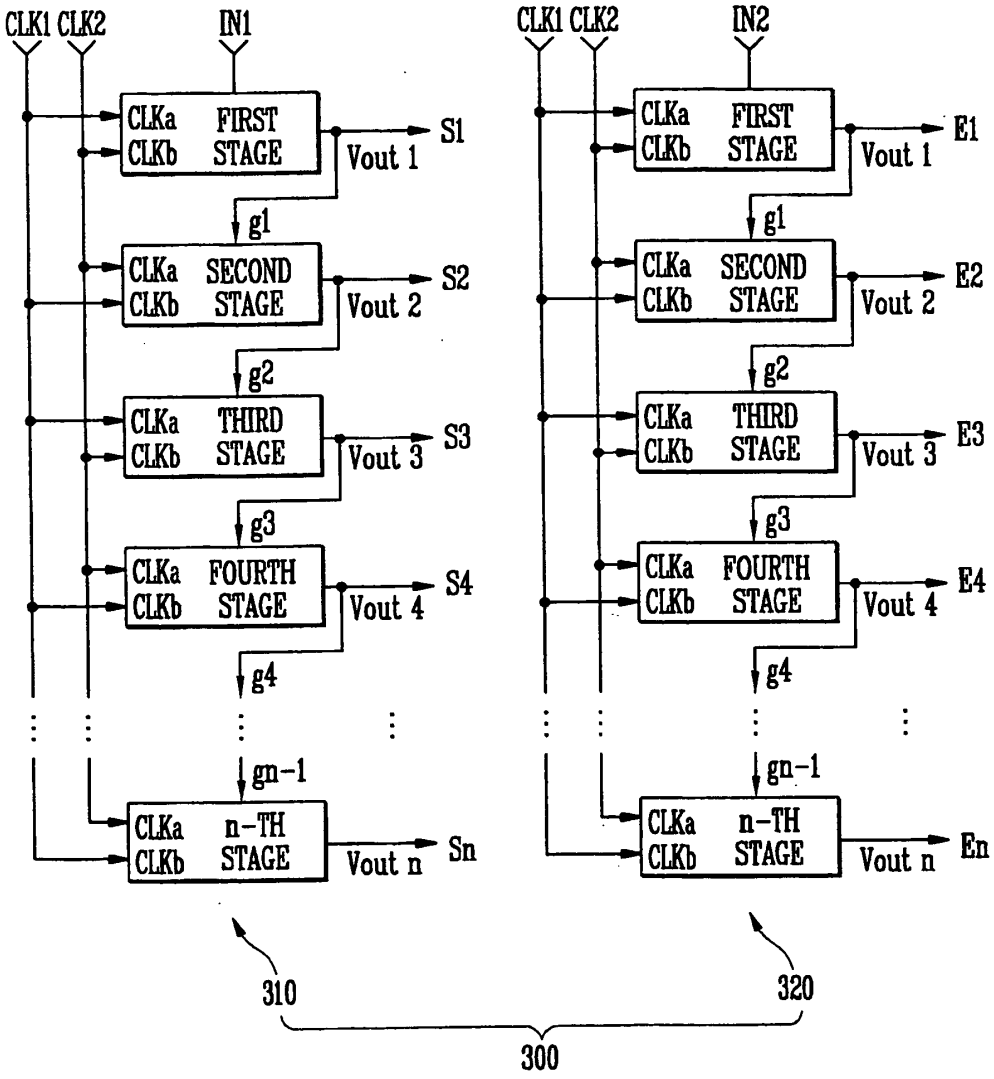

CLK1 CLK2
IN1
CLKa FIRST
CLKb STAGE
Vout 1
S1
g1
CLKa SECOND
CLKb STAGE
Vout 2
S2
g2
CLKa THIRD
CLKb STAGE
Vout 3
S3
g3
CLKa FOURTH
CLKb STAGE
Vout 4
S4
g4
gn-1
CLKa n-TH
CLKb STAGE
Vout n
Sn
CLK1 CLK2
IN2
CLKa FIRST
CLKb STAGE
Vout 1
E1
g1
CLKa SECOND
CLKb STAGE
Vout 2
E2
g2
CLKa THIRD
CLKb STAGE
Vout 3
E3
g3
CLKa FOURTH
CLKb STAGE
Vout 4
E4
g4
gn-1
CLKa n-TH
CLKb STAGE
Vout n
En
310
320
300

FIG. 8

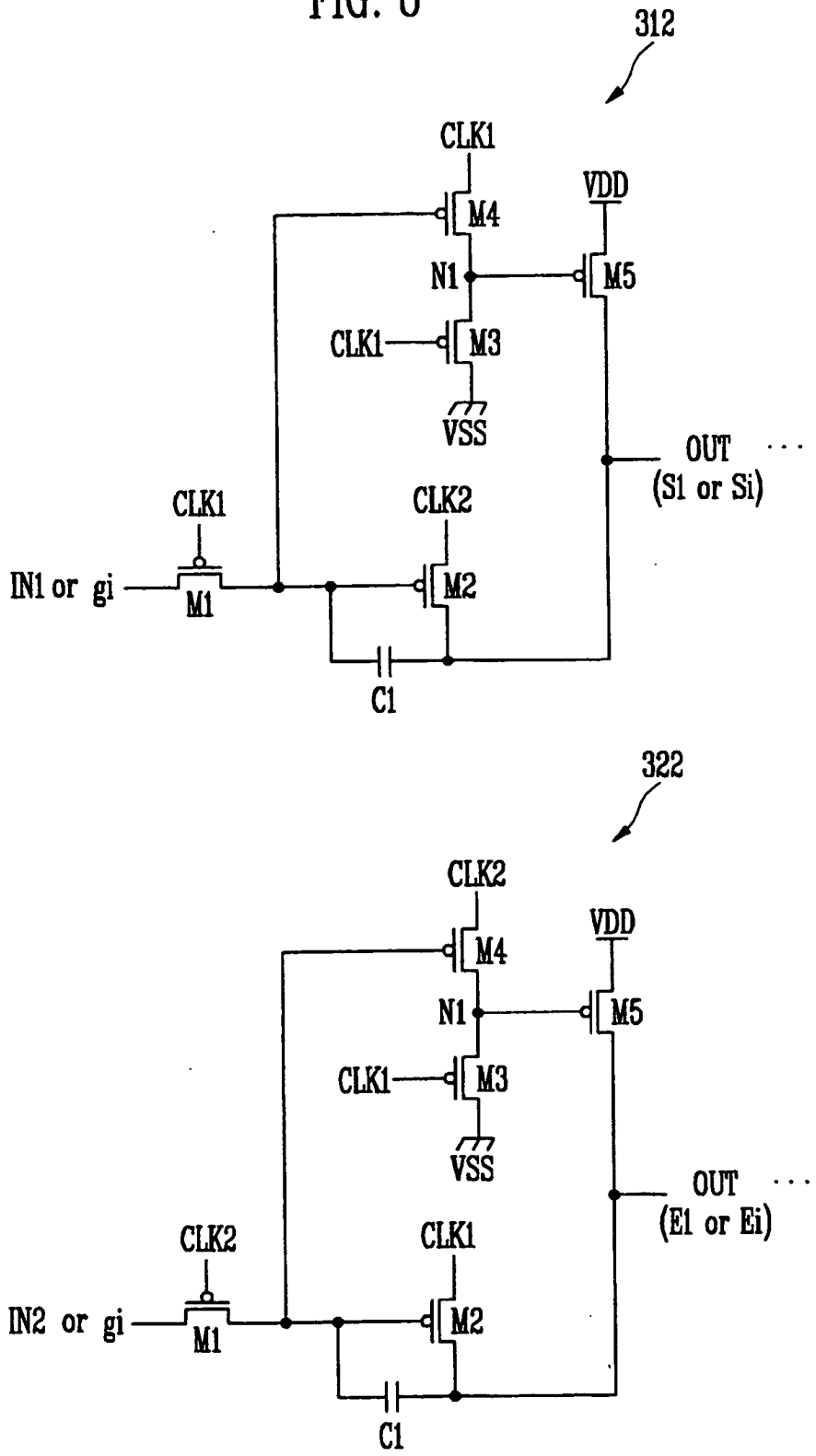
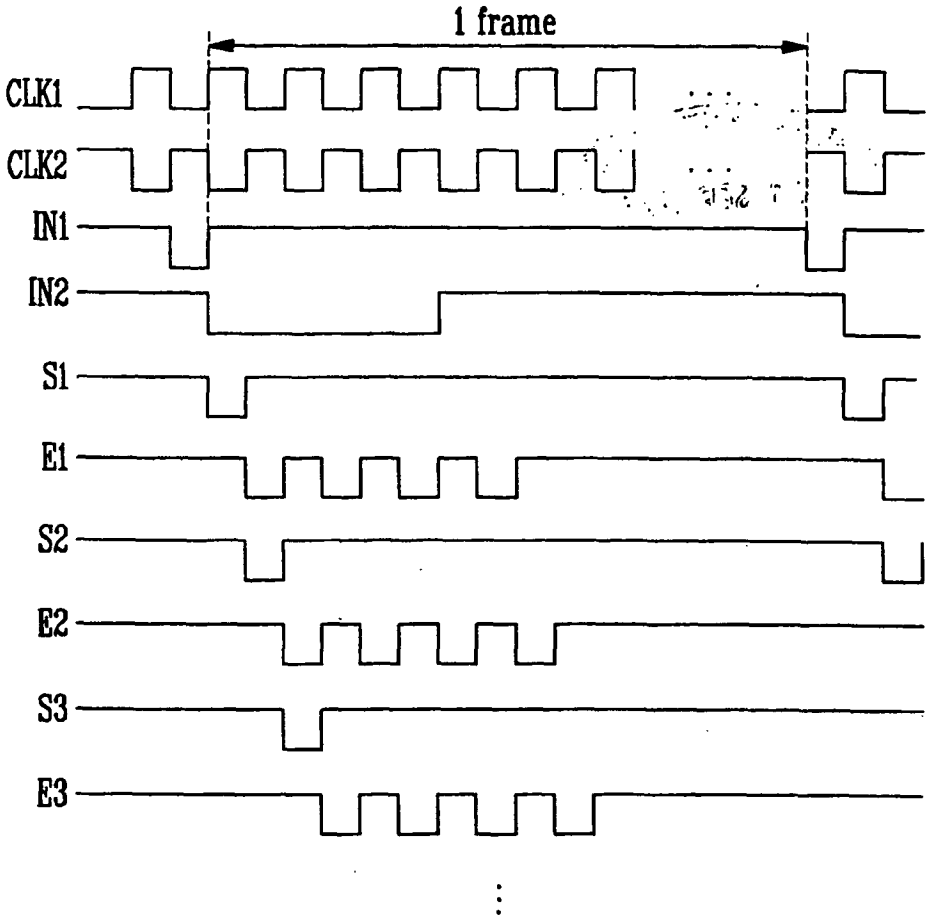

312
CLK1
VDD
M4
N1
M5
CLK1
M3
VSS
OUT
(S1 or Si)
CLK1
CLK2
IN1 or gi
M1
M2
C1
322
CLK2
VDD
M4
N1
M5
CLK1
M3
VSS
OUT
(E1 or Ei)
CLK2
CLK1
IN2 or gi
M1
M2
C1

FIG. 9



REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- JP 2004325940 A **[0014]**
- US 6392628 B **[0014]**
- US 6556646 B **[0014]**

专利名称(译)	扫描驱动电路和使用其的有机发光显示器		
公开(公告)号	EP1764774B1	公开(公告)日	2009-04-29
申请号	EP2006254884	申请日	2006-09-20
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星移动显示器有限公司.		
发明人	SHIN, DONY YONG C/O SAMSUNG SDI CO, LTD		
IPC分类号	G09G3/32		
CPC分类号	G09G3/325 G09G3/20 G09G3/3266 G09G2300/0842 G09G2310/0286 G09G2330/021 G11C19/184		
优先权	1020050087425 2005-09-20 KR		
其他公开文献	EP1764774A2 EP1764774A3		
外部链接	Espacenet		

摘要(译)

扫描驱动电路和使用其的有机发光显示器。具有多个第一级的第一扫描驱动器顺序输出选择信号，具有多个第二级的第二扫描驱动器顺序输出发射信号。第一级和第二级中的每一级被配置为具有基本为零的静态电流，并且可以优化操作速度而不会显着增加功耗。