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(54) **An organic light emitting display device and a method for generating scan signals for driving an organic light emitting display device having a scan driver**

Organische lichtemittierende Anzeigevorrichtung und Verfahren zur Erzeugung von Abtastsignalen zur Ansteuerung einer organischen lichtemittierenden Anzeigevorrichtung mit Zeilentreiber

Dispositif d'affichage émettant une lumière organique et procédé générant les signaux de lecture pour la commande d'un dispositif d'affichage émettant une lumière organique avec une commande de lecture

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Description

Background of the Invention

1. Field of the Invention

[0001] The present invention relates to an organic light emitting display (OLED) device and, more particularly, to a system on panel (SOP) type scan driver which generates scan signals for selecting pixels located on a display region, and an OLED device having the same.

2. Description of the Related Art

[0002] Recent years have seen considerable research into flat panel displays (FPDs) because they can be made smaller and lighter than display devices using cathode ray tubes (CRTs). As a result, liquid crystal displays (LCDs), field emission displays (FEDs), plasma display panels (PDPs), and organic light emitting displays (OLEDs) have been developed and put to practical use. Among these FPDs, the PDP can have a large screen but has low luminance and poor luminous efficiency resulting in high power consumption, and the LCD has a relatively slow response speed and consumes a lot of power since it employs a backlight.

[0003] However, as the OLED makes use of an organic material to emit light, it has a wider viewing angle and faster response speed than the LCD. Also, the OLED is an emissive display that obtains good contrast and visibility. Further, the OLED enables lower power consumption and can be made thin and lightweight because it needs no backlight.

[0004] Nevertheless, the dimensions of an electroluminescent (EL) panel for a glass substrate are limited due to fabricating process limitations and the OLED may not be easily constructed to have a large screen. Also, if the screen is large, there is a greater probability of a defect occurring somewhere on the screen and thus a reduction in yield is unavoidable. Further, it is difficult to obtain uniformity across the screen.

[0005] As a solution to the above problems of the OLED, a tiling technique was developed. In the tiling technique, EL panels are bonded together like tiles to form a single panel.

[0006] Each of the EL panels includes pixels to display a predetermined image similar to a conventional OLED. In each of the EL panels, a scan driver applies a scan signal to enable the pixels, and a data driver applies a data signal to a selected pixel. Also, an emission control driver applies an emission control signal to each of the pixels in order to control the exact programming of the data signal and the time taken for an emission operation.

[0007] As described above, the scan driver, the data driver, and the emission control driver, which transmit various signals to drive the EL panels, can be electrically coupled to each of the EL panels in various manners.

[0008] For example, the scan driver, the data driver,

and the emission control driver may be mounted as chips on a tape carrier package (TCP) that is bonded and electrically coupled to each of the EL panels. Alternatively, the drivers may be mounted as chips on a flexible printed circuit (FPC) or a film that is bonded and electrically coupled to each of the EL panels. The latter technique is referred to as a chip on flexible board (or chip on film) (COF) technique. In another method, the drivers are directly mounted on a glass substrate of the EL panel. This method is referred to as a chip on glass (COG) technique. These methods are costly and only complicate the modules, because the drivers should be separately designed and electrically coupled to one another.

[0009] To overcome these drawbacks, a system on panel (SOP) technique has been developed recently. Also, there have been attempts at designing a display region, scan and emission control drivers, and/or a data driver in each EL panel, in order to include all parts of the system in each of the EL panels.

[0010] In the OLED using the tiling technique, when each EL panel is formed as an SOP, it is easy to bond the EL panels to one another. Also, the SOP technique enables the area of drivers to be reduced and cost and labor for designing integrated circuits (ICs) of the respective drivers to be saved.

[0011] However, in order to develop the SOP-type OLED, it is necessary to consider many internal circumstances and conditions of the EL panels, such as a driving frequency and electron mobility of the data driver and/or the scan and emission control drivers. Up to present, it has been difficult to design the data driver within a panel because the data driver needs a high driving frequency.

[0012] Accordingly, the data driver is formed separately as an IC using complementary metal oxide semiconductor (CMOS) technology and subsequently coupled to the EL panel, while the scan driver and/or the emission control driver are formed within the EL panel.

[0013] Therefore, there is a need for a simple circuit construction in which an SOP-type scan driver and emission control driver can be optimally driven in the EL panel.

[0014] As an example of the shortcomings of the prior art, EP 1 531 450 A2 discloses an OLED display device comprising a data driver, a scan driver, an emission control driver and pixels coupled to the data driver, the scan driver and the emission control driver. However, the scan driver and the emission control driver are not integrated on the display panel because their structure is too complex to run at the required frequencies.

[0015] US 6,339,631 B1 discloses flip-flops which comprise only transistors of one conductivity type and therefore may be produced at low cost. However, the flip-flops are still not optimal with regard to simplicity and the area used which is an important factor when integrating the scan driver and emission control driver on the display panel.

[0016] US 5,644,653 discloses a shift-register having a very low complexity. However, it requires four clock signals and does not function securely when less clocks

are used.

SUMMARY OF THE INVENTION

[0017] The present invention, therefore, provides an organic light emitting display (OLED) device as set forth in claim 1. Preferred embodiments of the OLED device are set forth in dependent claims 2 through 6.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The above and other features of the present invention will be described in reference to certain exemplary embodiments thereof with reference to the attached drawings in which:

[0019] FIG. 1 is a block diagram of an organic light emitting display (OLED) device using a tiling technique;

[0020] FIG. 2 is a detailed block diagram of the OLED array shown in FIG. 1;

[0021] FIG. 3 is a block diagram of a scan driver for the OLED array ;

[0022] FIG. 4A is a circuit diagram of an odd flip-flop according to a comparative example of the present invention;

[0023] FIG. 4B is a circuit diagram of an even flip-flop according to a comparative example of the present invention;

[0024] FIG. 5 is a timing diagram illustrating the operation of the scan driver shown in FIG. 3;

[0025] FIG. 6A is a circuit diagram of an odd flip-flop according to an exemplary embodiment of the present invention; and

[0026] FIG. 6B is a circuit diagram of an even flip-flop according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION

[0027] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which comparative examples and an exemplary embodiment of the invention are shown.

[0028] FIG. 1 is a block diagram of an organic light emitting display (OLED) device using a tiling technique.

[0029] Referring to FIG. 1, the OLED device is formed by bonding OLED arrays 100. In FIG. 1, it is illustrated that eight OLED arrays 100, which are arranged four to a row and two to a column, are bonded to one another. However, the OLED device of the present invention may be designed to include a different number of OLED arrays 100 and to have various sizes.

[0030] Each of the OLED arrays 100 includes an electroluminescent (EL) panel 10 for displaying a predetermined image, and a data driver 20 for supplying a data signal to the EL panel 10.

[0031] The EL panels 10 have similar construction, and edges of the EL panels 10 are bonded to one another using an adhesive to form a combined EL panel. The

adhesive may be an ultraviolet (UV) curing resin or a thermal curing resin, for example, epoxy resin.

[0032] Each of the EL panels 10 can be produced by the same fabrication process as an EL panel for a conventional OLED array. Accordingly, a large combined EL panel can be fabricated by bonding EL panels that are obtained by the same fabrication process.

[0033] Each of the EL panels 10 includes a scan driver, an emission control driver, and pixels, and each of the drivers and pixels includes a thin film transistor (TFT), which has a polysilicon channel in order to obtain fast response speed and high uniformity. In this case, the polysilicon channel may be formed by forming an amorphous silicon (a-Si) layer on a glass substrate and crystallizing the a-Si layer using a low temperature polysilicon (LTPS) process.

[0034] The TFTs are formed of polysilicon that is obtained using the LTPS process. Thereafter, the display region, the scan driver, and the emission control driver are formed using the transistors in each of the EL panels 10. The display region includes red (R), green (G), and blue (B) sub-pixels, and the scan and emission control drivers select respective pixels and generate signals for controlling an emission operation. A detailed description of the EL panel 10 will be presented later.

[0035] Each of data drivers 20 is designed as an external integrated circuit (IC) using complementary metal oxide semiconductor (CMOS) technology and is electrically coupled to the corresponding EL panel 10. The EL panel 10 may be electrically coupled to the data driver 20 using a metal pattern that is printed on a flexible film. In that case, an output terminal of the data driver 20 is electrically coupled to one end of the metal pattern, and a data line located on the EL panel 10 is electrically coupled to the other end of the metal pattern. This method is referred to as a tape carrier package (TCP) technique. Each of the data drivers 20 transmits a data signal to the display region of the EL panel 10 through conductive lines that are located on the flexible film.

[0036] FIG. 2 is a detailed block diagram of the OLED array shown in FIG. 1.

[0037] Referring to FIG. 2, the OLED array 100 includes the EL panel 10 and the data driver 20. The EL panel 10 further includes a display region 12, a scan driver 14, and an emission control driver 16.

[0038] The display region 12 includes data lines D1-Dm, scan lines S1-Sn, emission control lines E1-En, and pixels P11-Pnm that are formed in pixel regions 18.

[0039] The data lines D1-Dm are electrically coupled to the data driver 20 and extend in a vertical direction of the exemplary embodiment shown in FIG. 2. The data lines D1-Dm transmit data signals to the respective pixels P11-Pnm. For example, the data line D1 is coupled to pixels P11-Pn1, the data line D2 is coupled to pixels P12-Pn2, and the data line Dm is coupled to pixels P1 m-Pnm.

[0040] Unlike in a conventional OLED device, the scan lines S1-Sn and the emission control lines E1-En extend in the same direction as the data lines D1-Dm (i.e., in the

vertical direction of the exemplary embodiment shown in FIG. 2). However, each of the scan and emission control lines S1-Sn and E1-En includes a contact hole in order to transmit the same scan and emission control signals to the pixels arranged in a horizontal direction of FIG. 2. Therefore, metal interconnections, which contact the scan and emission control lines S1-Sn and E1-En through the contact holes, extend in a horizontal direction so that scan and emission control signals are transmitted to the pixels arranged in the horizontal direction. For example, the scan control signal from the scan line S1 and the emission control signal from the emission control line E1 are transmitted to the pixels P11-P1m, the scan and emission control signals from S2 and E2 are transmitted to the pixels P21-P2m, and the scan and emission control signals from Sn and En are transmitted to the pixels Pn1-Pnm.

[0041] Each of the pixels P11-Pnm includes R, G, and B sub-pixels that are repeatedly arranged in rows and columns. The pixels include an organic emission layer that emits light. The organic emission layers in the R, G, and B sub-pixels are formed of different organic materials, but are the same in interconnection layout or circuit connection of a driving circuit. Accordingly, each of the pixels P11-Pnm emits R, G, or B light at a luminance corresponding to a data signal applied to the pixel and combines the R, G, and B lights to display a specific color.

[0042] In FIG. 2, the scan driver 14 is formed between the data driver 20 and the display region 12. Since a large panel is formed by bonding a number of EL panels 10 together, the scan driver 14 is formed on the same side as the data driver 20. The scan driver 14 is coupled to scan lines S1-Sn. Thus, the scan driver 14 sequentially transmits scan signals to the display region 12 and sequentially selects the pixels P11-Pnm.

[0043] In FIG. 2 shown, the emission control driver 16 is formed between the scan driver 14 and the display region 12 and is coupled to the emission control lines E1-En. Thus, the emission control driver 16 sequentially transmits emission control signals to the display region 12 and controls an emission time of each of the pixels P11-Pnm.

[0044] The data driver 20 may transmit data signals to the display region 12 of the EL panel 10 through conductive lines located on the flexible film as described above.

[0045] According to the above description, the OLED array 100 includes the EL panel 10 and the data driver 20, and the EL panel 10 includes the display region 12, the scan driver 14, and the emission control driver 16. Hereinafter, the structure and operation of the scan driver 14 will be described in detail.

[0046] FIG. 3 is a block diagram of a scan driver for the OLED array according to a comparative example of the present invention.

[0047] Referring to FIG. 3, the scan driver 14 includes flip-flops FF1, FF2, FF3 ... FF_n that are also labeled as a first flip-flop 14_1, a second flip-flop 14_2, a third flip-flop 14_3 and so on. The first flip-flop 14_1 receives a

start pulse SP (e.g., a start signal) and outputs a first output signal OUT1 in synchronization with a clock signal CLK and an inverted clock signal CLKB. The first output signal OUT1 is shifted and input to a second flip-flop 14_2. Also, the first output signal OUT1 becomes a first scan signal SCAN[1], which is used to select pixels located in a first row of pixels P11-P1m of the display region 12 of FIG. 2.

[0048] The second flip-flop 14_2 receives the first output signal OUT1 and outputs a second output signal OUT2 in synchronization with the clock signal CLK and the inverted clock signal CLKB that are shifted by a half cycle with respect to the first output signal OUT1. The second output signal OUT2 is input to a third flip-flop 14_3. Also, the second output signal OUT2 becomes a second scan signal SCAN[2], which is used to select pixels located in a second row of pixels P21-P2m of the display region 12.

[0049] The third flip-flop 14_3 receives the second output signal OUT2 and outputs a third output signal OUT3 in synchronization with the clock signal CLK and the inverted clock signal CLKB that are shifted by a half cycle of the clock signal CLK with respect to the second output signal OUT2. The third output signal OUT3 is input to a fourth flip-flop (not shown). Also, the third output signal OUT3 becomes a third scan signal that is used to select pixels located in a third row P31-P3m of the display region 12.

[0050] The flip-flops 14_1, 14_2, 14_3 and so forth alternately receive the clock signal CLK and the inverted clock signal CLKB, and output scan signals SCAN including SCAN[1], SCAN[2], SCAN[3] and so forth, that are shifted by a half cycle of the clock signal CLK. For example, a clock signal CLK input to an odd flip-flop 14_1 is input as an inverted clock signal CLKB to an even flip-flop 14_2, whereas the inverted clock signal CLKB input to the odd flip-flop 14_1 is input as a clock signal CLK to the even flip-flop 14_2. Thus, the scan signal SCAN can be output every half cycle of the clock signal CLK.

[0051] It is illustrated in FIG. 3 that the scan driver 14 includes three flip-flops 14_1, 14_2, and 14_3, but the present comparative example is not limited to this configuration. Rather, the scan driver 14 may include flip-flops in a number equal to the number of scan signals required (for example n in the case of the exemplary embodiment shown in FIG. 2).

[0052] FIG. 4A is a circuit diagram of an odd flip-flop, for example 14_1, 14_3, and the like, according to a comparative example of the present invention. The first flip-flop 14_1 is shown in FIG. 4A as an example of odd flip-flops.

[0053] Referring to FIG. 4A, the odd flip-flop includes three transistors M1, M2, and M3 and a capacitor C.

[0054] The first transistor M1 is coupled between a positive power supply voltage line V_{dd} and a node N1, and a clock signal CLK is input to a gate terminal of the first transistor M1. The node N1 is the signal line for the scan signal being generated by the flip-flop.

[0055] The second transistor M2 has a first electrode coupled to the node N1, and a gate terminal coupled to a node N2. The node N2 is the gate terminal of the second transistor M2. An inverted clock signal CLKB is input to a second electrode of the second transistor M2.

[0056] The third transistor M3 has a first electrode coupled to the node N2. A start pulse SP is input to a second electrode of the third transistor M3, and the clock signal CLK is input to a gate terminal thereof. In FIG. 4A, the inputs to the first flip-flop 14_1 are shown and therefore input to the second electrode of the third transistor M3 is shown as the start pulse SP which is the input to the first flip-flop 14_1. As described with reference to FIG. 3, each of flip-flops 14_2, 14_3,... other than the first flip-flop 14_1 receives an output signal of the previous flip-flop as an input signal. So other odd flip-flops, such as 14_3, would receive other input signals, such as SCAN[2], at the second electrode of their third transistor M3.

[0057] The first through third transistors M1, M2, and M3 are metal oxide semiconductor field effect transistors (MOSFETs) of the same conductivity type. In FIG. 4A and FIG. 4B, it will be described that the first through third M1, M2, and M3 are shown as p-type MOSFETs, but the present comparative example is not limited to this conductivity type.

[0058] The capacitor C is coupled between the nodes N1 and N2 and maintains a voltage between the first electrode and the gate terminal of the second transistor M2. The capacitor C allows the flip-flop to be pulled down and generally leads the flip-flop to be in the same full-swing as a driving voltage.

[0059] For example, when the clock signal CLK is at a low level, the inverted clock signal CLKB is at a high level, and the start pulse SP is at a low level, both the first and third transistors M1 and M3 are turned on. Thus, a low-level start pulse SP is input to the gate terminal of the second transistor M2, so that the second transistor M2 is also turned on. However, because the high-level inverted clock signal CLKB is applied to the second electrode of the second transistor M2, no current flows through the second transistor M2. Thus, a high-level scan signal SCAN, that is SCAN[1] in the exemplary case shown, is output through a scan line coupled to the node N1. In this case, since the inverted clock signal CLKB is elevated to a high level, a voltage difference between a source electrode and a drain electrode of the second transistor M2 becomes 0 V, thus static current is completely cut off from the second transistor M2.

[0060] Next, when the clock signal CLK is at a high level, the inverted clock signal CLKB is at a low level, and the start pulse SP is at a high level, both the first and third transistors M1 and M3 are turned off. In this case, since the low-level inverted clock signal CLKB is applied to the second electrode of the second transistor M2, the second transistor M2 is turned on. As current flows through the second transistor M2 due to a high-level voltage stored in the node N1, a voltage at the node N1 is dropped as much as the low-level inverted clock signal

CLKB. Specifically, as the third transistor M3 is turned off, the node N2 coupled to one terminal of the capacitor C is floated. Thus, a voltage at the node N2 is dropped as much as the voltage at the node N1 so that the voltage at the node N2 can be pulled down. As a result, a low-level scan signal SCAN[1] is output to a scan line coupled to the node N1.

[0061] FIG. 4B is a circuit diagram of an even flip-flop, for example 14_2, 14_4, and the like, according to a comparative example of the present invention. The second flip-flop 14_2 is shown in FIG. 4B as an example of even flip-flops.

[0062] Referring to FIG. 4B, the even flip-flop has the same construction as the odd flip-flop shown in FIG. 4A. That is, the even flip-flop includes three transistors M1, M2, and M3 and a capacitor C. For brevity of explanation, a description of the construction of the even flip-flop will be omitted here.

[0063] However, a clock signal CLK and an inverted clock signal CLKB are input in inverse relation to the odd flip-flop. Also, the output signal SCAN[1] of the previous odd flip-flop is input instead of the start pulse SP. Specifically, the inverted clock signal CLKB is input to a gate terminal of the first transistor M1 and a gate terminal of the third transistor M3, and the clock signal CLK is input to a second electrode of the second transistor M2. Also, the output signal SCAN[1] of the previous odd flip-flop is input to a second electrode of the third transistor M3.

[0064] The above-described even flip-flop operates in the same manner as the odd flip-flop as described with reference to FIG. 4A and outputs a scan signal SCAN[2] in synchronization with a clock signal CLK that is shifted by a half clock cycle with respect to the inverted clock signal CLKB input to the previous flip flop.

[0065] As described above, the scan driver alternately inputs a clock signal CLK and an inverted clock signal CLKB to each of the flip-flops and outputs a scan signal that is shifted by a half clock cycle.

[0066] In the comparative examples, each of the flip-flops includes the three transistors M1, M2, M3 and one capacitor C. Thus, layout area can be minimized owing to simplification of circuits. Also, when a high-level scan signal SCAN is output, the flow of static current is prevented due to a high-level signal that is applied to a drain terminal of the second transistor M2. As a result, power consumption can be reduced. Furthermore, since the capacitor C is coupled between the source and gate of the second transistor M2, when a low-level scan signal SCAN is output, sufficient pull-down operation is enabled.

[0067] Hereinafter, the operation of the scan driver including flip-flops will be described with reference to FIG. 5.

[0068] FIG. 5 is a timing diagram illustrating the operation of the scan driver shown in FIG. 3.

[0069] First, the operation of the first flip-flop 14_1 that is a representative odd flip-flop will be described with reference to FIGs. 3, 4A, 4B, and 5.

[0070] Referring to FIGs. 3 through 5, a low-level clock signal CLK, a high-level inverted clock signal CLKB, and a low-level start pulse SP are input. In this case, all the first, second, and third transistors M1, M2, and M3 are turned on. Thus, the node N1 outputs a high-level scan signal SCAN[1]. Here, the second transistor M2 is turned on, but a voltage between the source and drain of the second transistor M2 becomes 0V due to the high-level inverted clock signal CLKB applied to the second electrode of the second transistor M2, so that the flow of static current can be substantially cut off. As a result, power consumption caused by the static current is reduced.

[0071] Thereafter, the clock signal CLK is shifted by a half clock cycle so that a high-level clock signal CLK, a low-level inverted clock signal CLKB, and a high-level start pulse SP are input to the first flip-flop 14_1. Thus, both the first and third transistors M1 and M3 are turned off. In this case, one terminal of the capacitor C coupled to the node N2 is floated. While the second transistor M2 is being turned on, current flows due to a voltage difference between the source and gate of the second transistor M2 and a voltage difference between the source and drain of this transistor. Accordingly, a voltage at the node N1 is dropped as much as the low-level inverted clock signal CLKB, thus the node N1 outputs a low-level scan signal SCAN[1].

[0072] Thereafter, the clock signal CLK is shifted by a half clock cycle so that a low-level clock signal CLK, a high-level inverted clock signal CLKB, and a high-level start pulse SP are input to the first flip-flop 14_1. In this case, the second transistor M2 is turned off due to the high-level start pulse SP, and the node N1 outputs a high-level scan signal SCAN[1].

[0073] From the next cycle, although the clock signal CLK and the inverted clock signal CLKB make an upward or downward transition, since the start pulse SP is fixed at a high level, the node N1 always remains at a high level.

[0074] Next, the operation of the second flip-flop 14_2 that is a representative even flip-flop will be described. The second flip-flop 14_2 receives the clock signal CLK that is shifted by a half clock cycle.

[0075] Specifically, a high-level clock signal CLK, a low-level inverted clock signal CLKB, and a low-level scan signal SCAN[1] are input to the second flip-flop 14_2. In this case, all the first, second, and third transistors M1, M2, and M3 are turned on. Thus, the node N1 outputs a high-level scan signal SCAN[2]. Here, the second transistor M2 is turned on, but a voltage between the source and drain of the second transistor M2 becomes 0V due to the high-level clock signal CLK applied to the second electrode of the second transistor M2, so that the flow of static current can be substantially cut off. As a result, power consumption caused by the static current is reduced.

[0076] Thereafter, the clock signal CLK is shifted by a half clock cycle so that a low-level clock signal CLK, a high-level inverted clock signal CLKB, and a high-level scan signal SCAN[1] are input to the second flip-flop

14_2. Thus, both the first and third transistors M1 and M3 are turned off in response to the high-level inverted clock signal CLKB. In this case, one terminal of the capacitor C coupled to the node N2 is floated. While the second transistor M2 is being turned on due to a voltage difference between the source and gate thereof, a voltage difference between the source and drain of the second transistor M2 arises from the low-level clock signal CLK, so that current flows. Accordingly, a voltage at the node N1 is dropped as much as the low-level clock signal CLK, thus the node N1 outputs a low-level scan signal SCAN[2].

[0077] Thereafter, the clock signal CLK is shifted by a half clock cycle so that a high-level clock signal CLK, a low-level inverted clock signal CLKB, and a high-level scan signal SCAN[1] are input to the second flip-flop 14_2. In this case, the second transistor M2 is turned off due to the high-level scan signal SCAN[1], and the node N1 outputs a high-level scan signal SCAN[2].

[0078] From now on, although the clock signal CLK and the inverted clock signal CLKB make an upward or downward transition every half cycle, since the scan signal SCAN[1] is fixed at a high level, the node N1 always remains at a high level.

[0079] Subsequently, the remaining flip-flops 14_3, 14_4, and so forth, perform the same operations as the first and second flip-flops 14_1 and 14_2 and output scan signals SCAN.

[0080] As described above, the scan driver makes use of three transistors and one capacitor and outputs the scan signal SCAN[n] every half cycle of the clock signal CLK.

[0081] In FIGS. 4A and 4B, a clock signal CLK and an inverted clock signal CLKB are directly input to a gate terminal of a transistor. Thus, when the clock signal CLK is delayed due to a line load, an output signal (i.e., a scan signal SCAN) also may be delayed. In particular, when the transistor has a large size, a delay in the scan signal makes application of a data signal incorrect, thus an undesirable image may be displayed.

[0082] FIG. 6A is a circuit diagram of an odd flip-flop according to an exemplary embodiment of the present invention.

[0083] Referring to FIG. 6A, the odd flip-flop has almost the same construction as the odd flip-flop shown in FIG. 4A. Thus, a description of the same components will be omitted here.

[0084] Referring to FIG. 6A, a control signal input portion is coupled to gate terminals of a first transistor M1 and a third transistor M3. The control signal input portion includes two transistors M4 and M5. The fourth transistor M4 is coupled between a negative power supply voltage terminal Vss and the gate terminals of the first and third transistors M1 and M3, and a clock signal CLK is input to a gate terminal thereof. The fifth transistor M5 is coupled between a positive power supply voltage terminal Vdd and the gate terminals of the first and third transistors M1 and M3, and an inverted clock signal CLKB is input

to a gate terminal of the fifth transistor M5.

[0085] Accordingly, once a low-level clock signal CLK is input, the fourth transistor M4 is turned on, so that the negative power supply voltage Vss is commonly applied to the gate terminals of the first and third transistors M1 and M3. Also, once a low-level inverted clock signal CLKB is input, the fifth transistor M5 is turned on, so that a positive power supply voltage Vdd is commonly applied to the gate terminals of the first and third transistors M1 and M3. Since the operating principle of the odd flip-flop of FIG. 6A is the same as the odd flip-flop of FIG. 4A, a description thereof will be omitted here.

[0086] FIG. 6B is a circuit diagram of an even flip-flop according to an exemplary embodiment of the present invention.

[0087] Referring to FIG. 6B, the alternative even flip-flop has the same construction as the odd flip-flop shown in FIG. 6A. However, a clock signal CLK and an inverted clock signal CLKB are input in inverse relation to the odd flip-flop shown in FIG. 6A. Accordingly, in the even flip-flop of FIG. 6B, the inverted clock signal CLKB is input to a terminal to which the clock signal CLK is input in the odd flip-flop of FIG. 6A, while the clock signal CLK is input to a terminal to which the inverted clock signal CLKB is input in the odd flip-flop of FIG. 6A. Since the operations of the even flip-flop of FIG. 6B are the same as that of the even flip-flop of FIG. 4B, a description thereof will not be repeated here.

[0088] In the exemplary embodiment of the present invention, shown in FIGs. 6A and 6B, since each of the flip-flops includes the three transistors M1, M2, and M3 and a capacitor C, layout area can be minimized due to simplification of circuits. Also, when a high-level scan signal SCAN is output, the flow of static current is prevented due to a high-level signal that is applied to a drain terminal of the second transistor M2. As a result, power consumption can be reduced. Furthermore, since the capacitor C is coupled between a source terminal and a gate terminal of the second transistor M2, when a low-level scan signal SCAN is output, a sufficient pull-down operation is enabled. In addition, each of the odd and even flip-flops of the exemplary embodiment, includes the control signal input portion unlike the comparative example, with the result that a delay in an output signal caused by a delay in the clock signal CLK can be prevented.

[0089] According to the comparative examples and the exemplary embodiment of present invention as described above, a display panel includes flip-flops, each of which is comprised of three transistors and a capacitor, so that layout area is minimized with simplification of circuits while facilitating construction of an SOP-type display panel.

[0090] Also, when a high-level scan signal is output, the flow of static current into a second transistor is cut off, thus reducing power consumption.

[0091] Furthermore, as the capacitor is coupled between a source terminal and a gate terminal of the second transistor, a low-level scan signal can be output in the

same waveform as a driving voltage so that a sufficient pull-down operation is enabled.

[0092] Consequently, the comparative examples and the exemplary embodiment of present invention provides not only a simplified SOP type scan driver but also an OLED device that can minimize power consumption.

Claims

1. An organic light emitting display device (100) comprising:

a data driver (20) adapted for applying a data signal to selected pixels (P11...Pnm), wherein the data driver is adapted for generating data signals corresponding to an image to be displayed by the device; and

a scan driver (14) having flip-flops (14_1, 14_2, 14_3) and adapted for applying a scan signal to select the pixels, wherein flip-flops are coupled together in series, a first flip-flop (14_1) adapted to receive a control signal (CLK, CLKB) and a start pulse (SP) as an input signal and to generate a first scan signal (SCAN[1]) as an output signal, the flip-flops (14_2, 14_3) following the first flip-flop (14_1) being adapted to receive a control signal (CLK, CLKB) and the output signal of a previous one of the flip-flops (14_1, 14_2) as an input signal and to generate another scan signal (SCAN[2], SCAN[3]) as an output signal, the other scan signal (SCAN[2], SCAN[3]) being shifted by half a cycle of the clock signal with respect to the previous scan signal (SCAN[1], SCAN[2]), wherein the control signal applied to the flip-flops is either a clock signal (CLK) or an inverted clock signal (CLKB), and wherein the clock signal (CLK) and the inverted clock signal (CLKB) are alternately input to an odd flip-flop and an even flip-flop, respectively; and

an emission control driver (16) adapted for applying an emission control signal (E1...En) to control the exact programming of the data signal and the time taken for an emission operation; and

a display region (12) having pixels (P11...Pnm) for displaying a predetermined image, wherein the pixels (P11...Pnm) are coupled to the data driver (20), the scan driver (14) and the emission control driver (16), for receiving the data signals, the scan signals and the emission control signals, the pixels (P11...Pnm) being controlled by the scan signals and the emission control signals, the pixels (P11...Pnm) for generating light according to the data signals,

characterised in that at least one of the flip-flops (14_1, 14_2, 14_3) of the scan driver (14)

includes

a first transistor (M1), coupled between a positive power supply voltage terminal (Vdd) and a signal line for scan signals (SCAN[1], SCAN[2], SCAN[3]), and turned on/off according to a control signal applied to a gate terminal of the first transistor (M1);

a second transistor (M2), coupled between the signal line for the scan signal (SCAN[1], SCAN[2], SCAN[3]) and either a signal line for the clock signal (CLK) or a signal line for the inverted clock signal (CLKB) and turned on/off according to a voltage at a gate terminal of the second transistor (M2);

a third transistor (M3) having a first electrode and a second electrode,

wherein the first electrode of the third transistor (M3) is coupled to the gate of the second transistor (M2) and an input signal applied to the second electrode of the third transistor (M3) is transmitted to the first electrode of the third transistor (M3) according to the control signal applied to a gate terminal of the third transistor (M3); and

a control signal input portion, commonly coupled to the gate terminal of the first transistor (M1) and the gate terminal of the third transistor (M3) and applying the control signal of a low or high level in response to either the clock signal (CLK) or the inverted clock signal (CLKB),
said control signal input portion only including:

a fourth transistor (M4), coupled between a negative power supply voltage terminal (Vss) and the gate terminal of the first transistor (M1) and the gate terminal of the third transistor (M3), and turned on/off in response to either the clock signal (CLK) or the inverted clock signal (CLKB); and

a fifth transistor (M5), coupled between the positive power supply voltage terminal (Vdd) and the gate terminal of the first transistor (M1) and the gate terminal of the third transistor (M3), and turned on/off in response to either the inverted clock signal (CLKB) or the clock signal (CLK).

2. The organic light emitting display device according to claim 1, wherein the at least one of the flip-flops further includes a capacitor, coupled between a source terminal and the gate terminal of the second transistor for maintaining a voltage for a predetermined time.
3. The organic light emitting display device according to one of the claims 1 or 2, wherein the at least one of the flip-flops is for outputting the scan signal every half cycle of the clock signal.

4. The organic light emitting display device according to one of the preceding claims, wherein the first transistor (M1), the second transistor (M2), and the third transistor (M3) are PMOS transistors.

5. The organic light emitting display device according to one of the preceding claims, wherein the clock signal (CLK) and the inverted clock signal (CLKB) are alternately input to an odd flip-flop and an even flip-flop.

6. The organic light emitting display device according to claim 4 or to claim 5, wherein the fourth transistor (M4), and the fifth transistor (M5) are PMOS transistors.

Patentansprüche

1. Eine organische lichtemittierende Anzeigevorrichtung (100), umfassend:

einen Datentreiber (20), der dazu ausgelegt ist, ein Datensignal an ausgewählte Pixel (P11...Pnm) anzulegen, wobei der Datentreiber dazu ausgelegt ist, Datensignale zu generieren, die einem von der Vorrichtung anzuzeigenden Bild entsprechen; und

einen Abtasttreiber (14) mit Flip-Flops (14_1, 14_2, 14_3), der dazu ausgelegt ist, ein Abtastsignal anzulegen, um die Pixel auszuwählen, wobei Flip-Flops in Reihe zusammengeschaltet sind, wobei ein erstes Flip-Flop (14_1) dazu ausgelegt ist, ein Steuersignal (CLK, CLKB) und einen Startimpuls (SP) als Eingabesignal zu empfangen und ein erstes Abtastsignal (SCAN[1]) als Ausgabesignal zu generieren, und die auf das erste Flip-Flop (14_1) folgenden Flip-Flops (14_2, 14_3) dazu ausgelegt sind, ein Steuersignal (CLK, CLKB) und das Ausgabesignal eines vorherigen der Flip-Flops (14_1, 14_2) als Eingabesignal zu empfangen und ein weiteres Abtastsignal (SCAN[2], SCAN[3]) als Ausgabesignal zu generieren, wobei das weitere Abtastsignal (SCAN[2], SCAN[3]) bezüglich des vorherigen Abtastsignals (SCAN[1], SCAN[2]) um einen halben Takt des Taktsignals verschoben ist, wobei das an die Flip-Flops angelegte Steuersignal entweder ein Taktsignal (CLK) oder ein invertiertes Taktsignal (CLKB) ist, und wobei das Taktsignal (CLK) und das invertierte Taktsignal (CLKB) abwechselnd einem ungeradzahigen Flip-Flop beziehungsweise einem geradzahigen Flip-Flop eingegeben werden; und

einen Emissionssteuertreiber (16), der dazu ausgelegt ist, ein Emissionssteuersignal (E1...En) anzulegen, um die genaue Program-

mierung des Datensignals und die für eine Emissionsoperation benötigte Zeit zu steuern; und einen Anzeigebereich (12) mit Pixeln (P11...Pnm) zum Anzeigen eines vorbestimmten Bildes, wobei die Pixel (P11...Pnm) mit dem Datentreiber (20), dem Abtasttreiber (14) und dem Emissionssteuertreiber (16) verbunden sind, um die Datensignale, die Abtastsignale und die Emissionssteuersignale zu empfangen, wobei die Pixel (P11...Pnm) von den Abtastsignalen und den Emissionssteuersignalen gesteuert werden, wobei die Pixel (P11...Pnm) zum Generieren von Licht gemäß den Datensignalen dienen,

dadurch gekennzeichnet, dass mindestens eines der Flip-Flops (14_1, 14_2, 14_3) des Abtasttreibers (14) Folgendes beinhaltet:

einen ersten Transistor (M1), der zwischen einen positiven Stromversorgungsspannungsanschluss (Vdd) und eine Signalleitung für Abtastsignale (SCAN[1], SCAN[2], SCAN[3]) geschaltet ist und gemäß einem an einen Gateanschluss des ersten Transistors (M1) angelegten Steuersignal ein-/ausgeschaltet wird;
einen zweiten Transistor (M2), der zwischen die Signalleitung für das Abtastsignal (SCAN[1], SCAN[2], SCAN[3]) und entweder eine Signalleitung für das Taktsignal (CLK) oder eine Signalleitung für das invertierte Taktsignal (CLKB) geschaltet ist und gemäß einer Spannung an einem Gateanschluss des zweiten Transistors (M2) ein-/ausgeschaltet wird;
einen dritten Transistor (M3) mit einer ersten Elektrode und einer zweiten Elektrode;
wobei die erste Elektrode des dritten Transistors (M3) mit dem Gate des zweiten Transistors (M2) verbunden ist und ein an die zweite Elektrode des dritten Transistors (M3) angelegtes Eingabesignal gemäß dem an einen Gateanschluss des dritten Transistors (M3) angelegten Steuersignal an die erste Elektrode des dritten Transistors (M3) übertragen wird; und
einen Steuersignaleingabeteil, der mit dem Gateanschluss des ersten Transistors (M1) und dem Gateanschluss des dritten Transistors (M3) gemeinsam verschaltet ist und als Antwort auf entweder das Taktsignal (CLK) oder das invertierte Taktsignal (CLKB) das Steuersignal eines Low- oder High-Pegels anlegt,

wobei besagter Steuersignaleingabeteil lediglich Folgendes beinhaltet:

einen vierten Transistor (M4), der zwischen einen negativen Stromversorgungsspannungsanschluss (Vss) und den Gateanschluss des er-

sten Transistors (M1) und den Gateanschluss des dritten Transistors (M3) geschaltet ist und als Antwort auf entweder das Taktsignal (CLK) oder das invertierte Taktsignal (CLKB) ein-/ausgeschaltet wird; und
einen fünften Transistor (M5), der zwischen den positiven Stromversorgungsspannungsanschluss (Vdd) und den Gateanschluss des ersten Transistors (M1) und den Gateanschluss des dritten Transistors (M3) geschaltet ist und als Antwort auf entweder das invertierte Taktsignal (CLKB) oder das Taktsignal (CLK) ein-/ausgeschaltet wird.

2. Die organische lichtemittierende Anzeigevorrichtung gemäß Anspruch 1, wobei das mindestens eine der Flip-Flops ferner einen zwischen einem Sourceanschluss und dem Gateanschluss des zweiten Transistors geschalteten Kondensator zum Aufrechterhalten einer Spannung für eine vorbestimmte Zeit beinhaltet.
3. Die organische lichtemittierende Anzeigevorrichtung gemäß einem der Ansprüche 1 oder 2, wobei das mindestens eine der Flip-Flops zum Ausgeben des Abtastsignals in jedem halben Takt des Taktsignals dient.
4. Die organische lichtemittierende Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei der erste Transistor (M1), der zweite Transistor (M2) und der dritte Transistor (M3) PMOS-Transistoren sind.
5. Die organische lichtemittierende Anzeigevorrichtung nach einem der vorhergehenden Ansprüche, wobei das Taktsignal (CLK) und das invertierte Taktsignal (CLKB) abwechselnd einem ungeradzahligem Flip-Flop und einem geradzahligem Flip-Flop eingegeben werden.
6. Die organische lichtemittierende Anzeigevorrichtung nach Anspruch 4 oder Anspruch 5, wobei der vierte Transistor (M4) und der fünfte Transistor (M5) PMOS-Transistoren sind.

Revendications

1. Dispositif organique (100) d'affichage à émission de lumière comprenant :

un circuit d'attaque (20) de donnée apte à appliquer un signal de donnée à des pixels (P11...Pnm) sélectionnés, dans lequel le circuit d'attaque de donnée est apte à engendrer des signaux de donnée correspondant à une image à afficher par le dispositif ; et

un circuit d'attaque (14) de balayage ayant des bascules (14_1, 14_2, 14_3) et apte à appliquer un signal de balayage pour sélectionner les pixels, dans lequel des bascules sont associées les unes aux autres en série une première bascule (14_1) apte à recevoir un signal (CLK, CLKB) de commande et une impulsion (SP) de début comme signal d'entrée et à engendrer un premier signal (SCAN[1]) de balayage comme signal de sortie, les bascules (14_2, 14_3) suivant la première bascule (14_1) étant aptes à recevoir un signal (CLK, CLKB) de commande et un signal de sortie d'une précédente des bascules (14_1, 14_2) comme signal d'entrée et à engendrer un autre signal (SCAN[2], SCAN[3]) de balayage comme signal de sortie, l'autre signal (SCAN[2], SCAN[3]) de balayage étant décalé de la moitié d'un cycle du signal d'horloge par rapport au signal (SCAN[1], SCAN[2]) précédent, dans lequel le signal de commande appliqué aux bascules est soit un signal (CLK) d'horloge soit un signal (CLKB) d'horloge inversé, et dans lequel le signal (CLK) d'horloge et le signal (CLKB) d'horloge inversé sont entrés alternativement, respectivement, dans une bascule impaire et dans une bascule paire ; et un circuit d'attaque (16) de commande d'émission apte à appliquer un signal (E1...En) de commande d'émission pour commander la programmation exacte du signal de donnée et le temps pris pour une opération d'émission ; et une région (12) d'affichage comportant des pixels (P11...Pnm) destinée à afficher une image prédéterminée, dans lequel les pixels (P11...Pnm) sont associés au circuit d'attaque (20) de donnée, au circuit d'attaque (14) de balayage et au circuit d'attaque (16) de commande d'émission, pour recevoir les signaux de donnée, les signaux de balayage et les signaux de commande d'émission, les pixels (P11...Pnm) étant commandés par les signaux de balayage et les signaux de commande d'émission, les pixels (P11...Pnm) étant destinés à engendrer de la lumière d'après les signaux de donnée,

caractérisé en ce qu'au moins l'une des bascules (14_1, 14_2, 14_3) du circuit d'attaque (14) de balayage inclut :

un premier transistor (M1), raccordé entre une borne (Vdd) de tension d'alimentation positive et une ligne de signal pour les signaux (SCAN[1], SCAN[2], SCAN[3]) de balayage, et allumé ou éteint en fonction d'un signal de commande appliqué à une borne de grille du premier transistor (M1) ;
un deuxième transistor (M2), raccordé entre la

ligne de signal pour le signal (SCAN[1], SCAN[2], SCAN[3]) de balayage et soit une ligne de signal pour le signal (CLK) d'horloge soit une ligne de signal pour le signal (CLKB) d'horloge inversé et allumé ou éteint en fonction de la tension au niveau d'une borne de grille du deuxième transistor (M2) ;
un troisième transistor (M3) ayant une première électrode et une seconde électrode, dans lequel la première électrode du troisième transistor (M3) est raccordée à la grille du deuxième transistor (M2) et un signal d'entrée appliqué à la seconde électrode du troisième transistor (M3) est transmis à la première électrode du troisième transistor (M3) en fonction du signal de commande appliqué à une borne de grille du troisième transistor (M3) ; et
une section d'entrée de signal de commande, raccordée en commun à la borne de grille du premier transistor (M1) et à la borne de grille du troisième transistor (M3) et appliquant le signal de commande d'un niveau bas ou haut en réponse soit au signal (CLK) d'horloge soit au signal (CLKB) d'horloge inversé, ladite section d'entrée de signal de commande incluant seulement :

un quatrième transistor (M4), raccordé entre une borne (Vss) de tension d'alimentation négative et la borne de grille du premier transistor (M1) et la borne de grille du troisième transistor (M3), et allumé ou éteint en réponse soit au signal (CLK) d'horloge soit au signal (CLKB) d'horloge inversé ; et
un cinquième transistor (M5), raccordé entre la borne (Vdd) de tension d'alimentation positive et la borne de grille du premier transistor (M1) et la borne de grille du troisième transistor (M3), et allumé ou éteint en réponse soit au signal (CLKB) d'horloge inversé soit au signal (CLK) d'horloge.

2. Dispositif organique d'affichage à émission de lumière selon la revendication 1, dans lequel l'au moins une des bascules inclut en outre un condensateur, raccordé entre une borne de source et une borne de grille du deuxième transistor pour maintenir une tension pendant un temps prédéterminé.

3. Dispositif organique d'affichage à émission de lumière selon l'une des revendications 1 ou 2, dans lequel l'au moins une des bascules sert à sortir le signal de balayage tous les demi-cycles du signal d'horloge.

4. Dispositif organique d'affichage à émission de lumière selon l'une des revendications précédentes, dans lequel le premier transistor (M1), le deuxième transistor (M2) et le troisième transistor (M3) sont des

transistors métal-oxyde-semi-conducteur à canal P (PMOS).

5. Dispositif organique d'affichage à émission de lumière selon l'une des revendications précédentes, dans lequel le signal (CLK) d'horloge et le signal (CLKB) d'horloge inversé sont entrés alternativement dans une bascule impaire et dans une bascule paire. 5
6. Dispositif organique d'affichage à émission de lumière selon la revendication 4 ou la revendication 5, dans lequel le quatrième transistor (M4) et le cinquième transistor (M5) sont des transistors PMOS. 10

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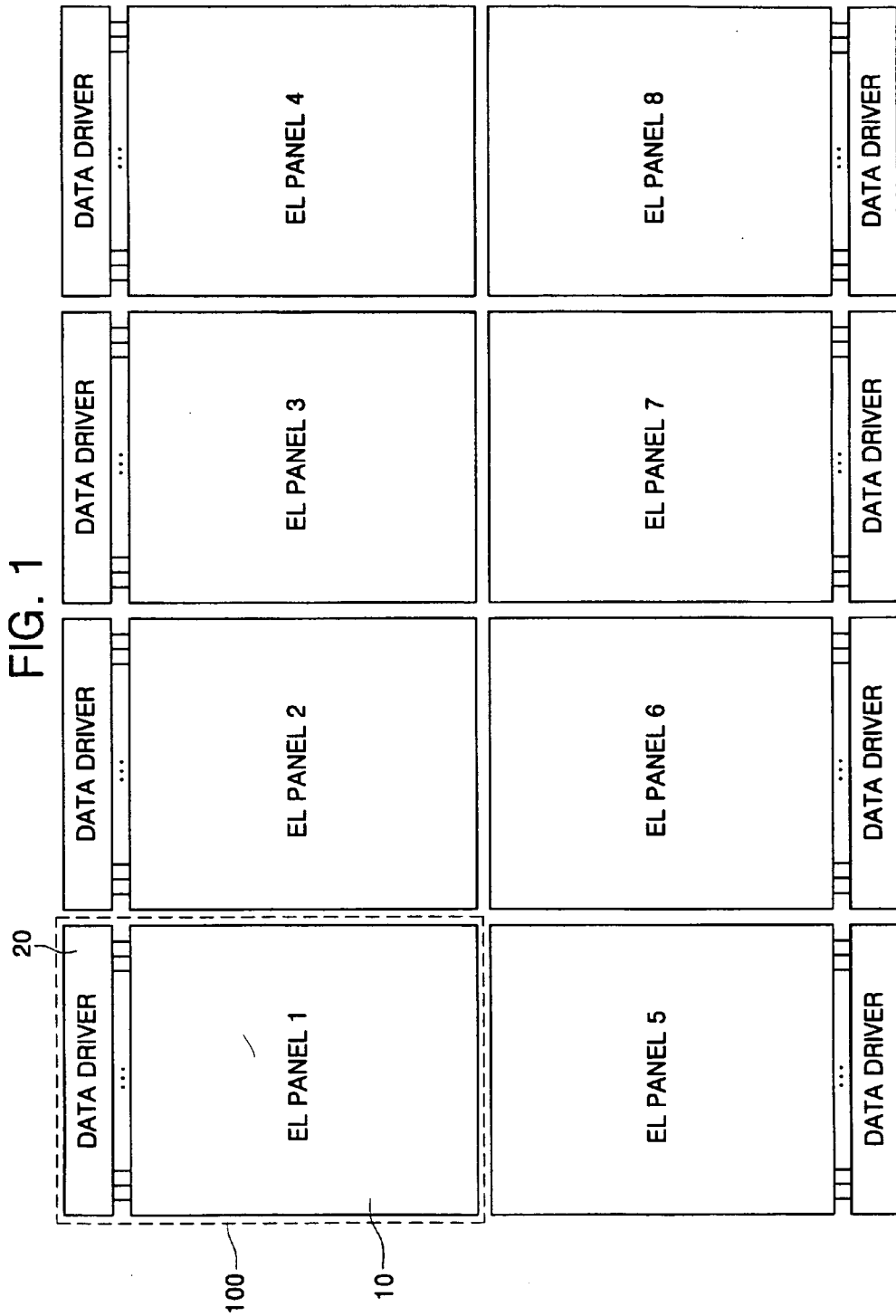


FIG. 2

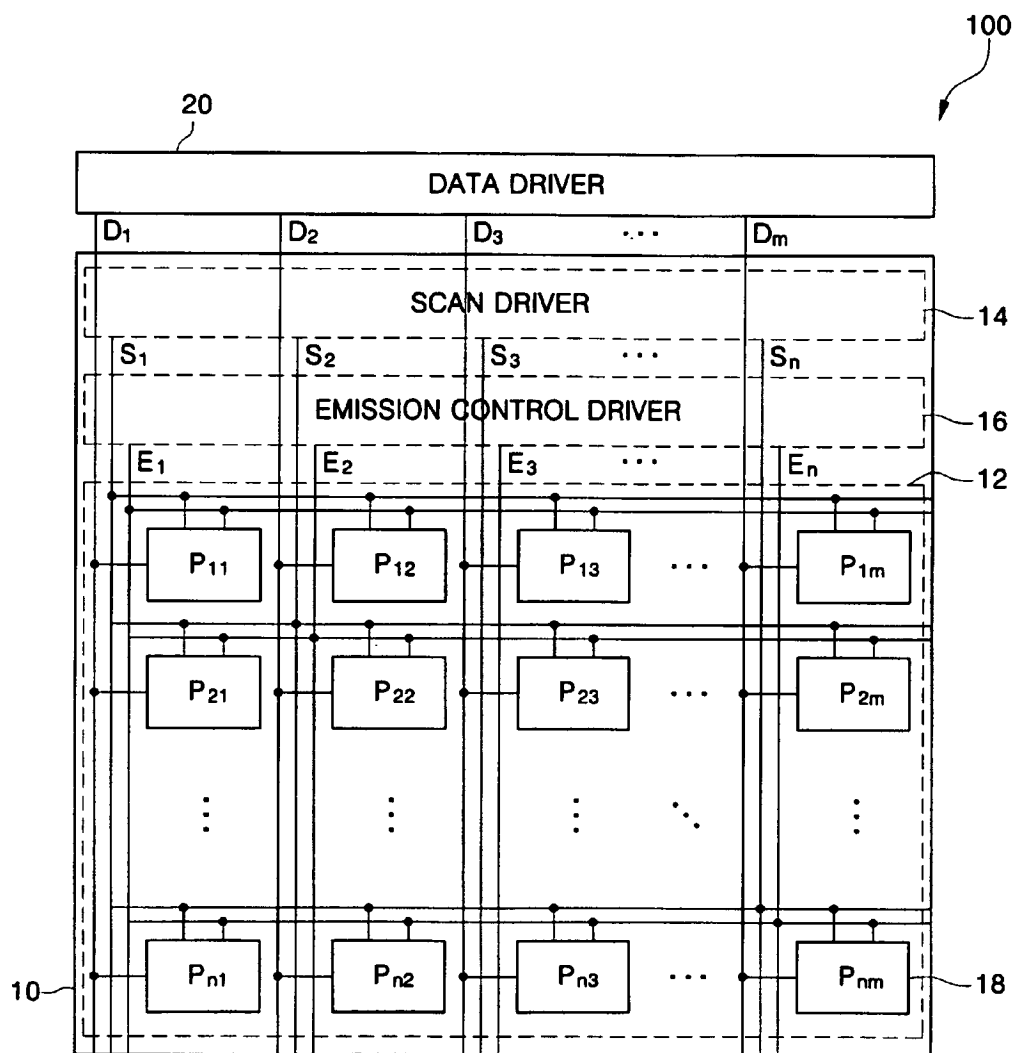


FIG. 3

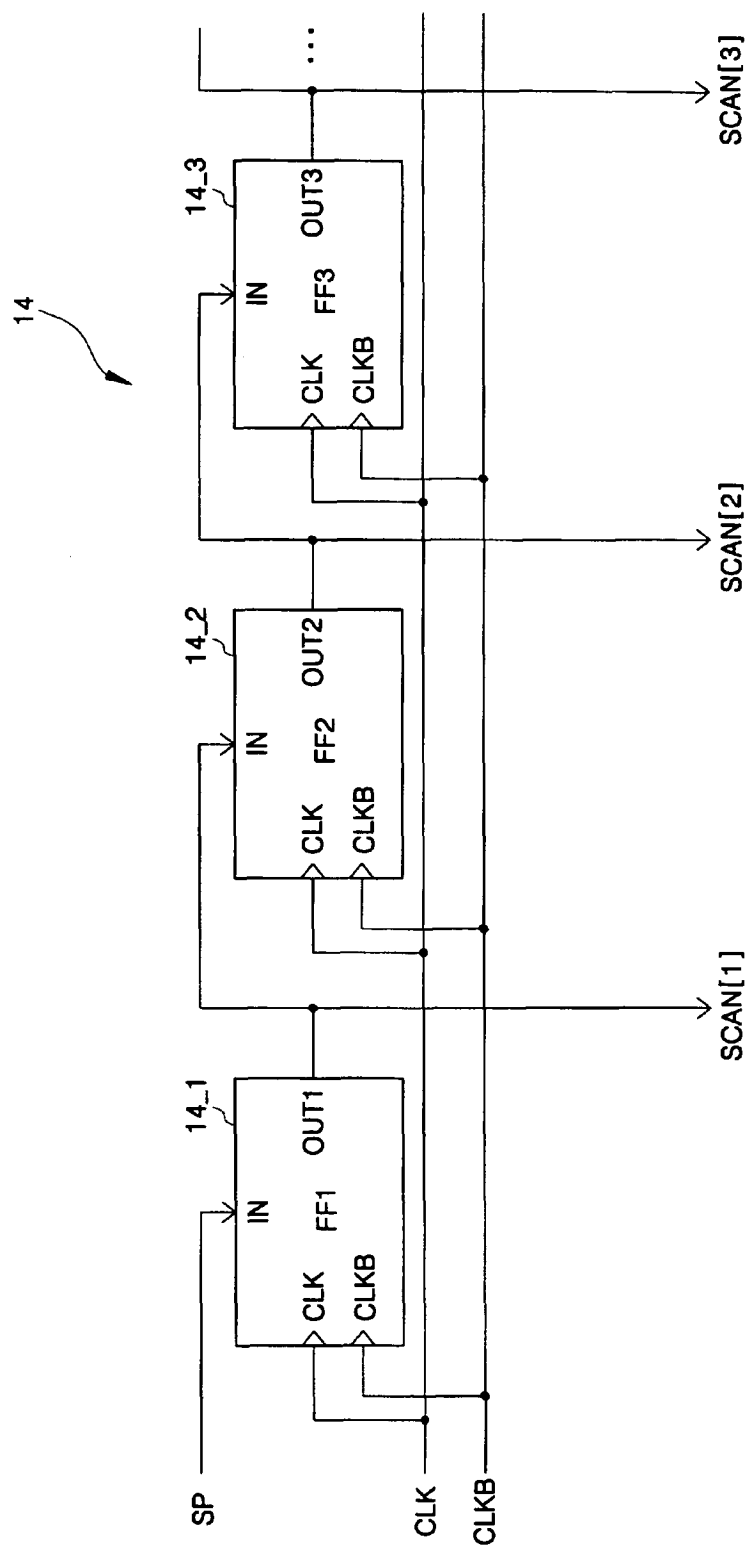


FIG. 4A

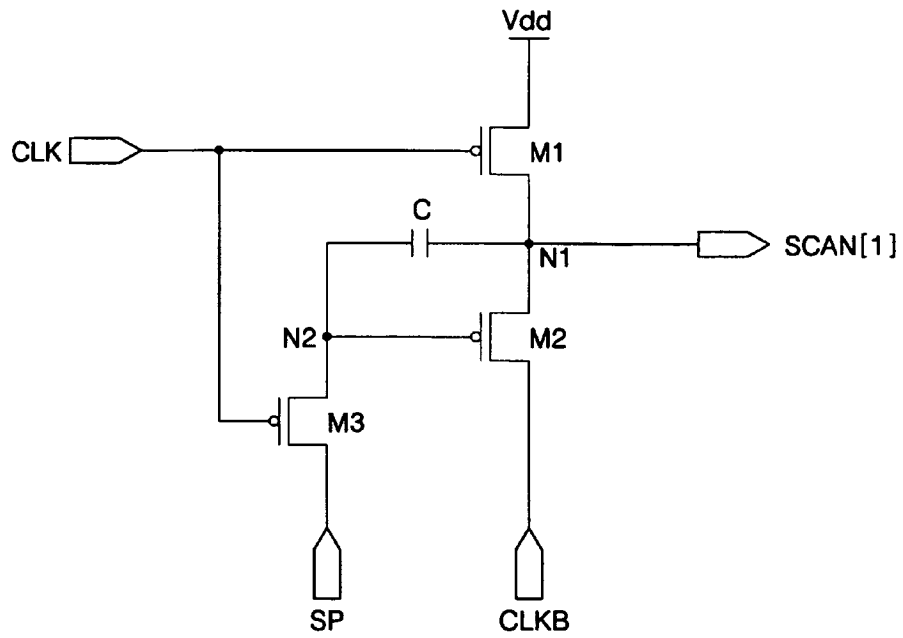


FIG. 4B

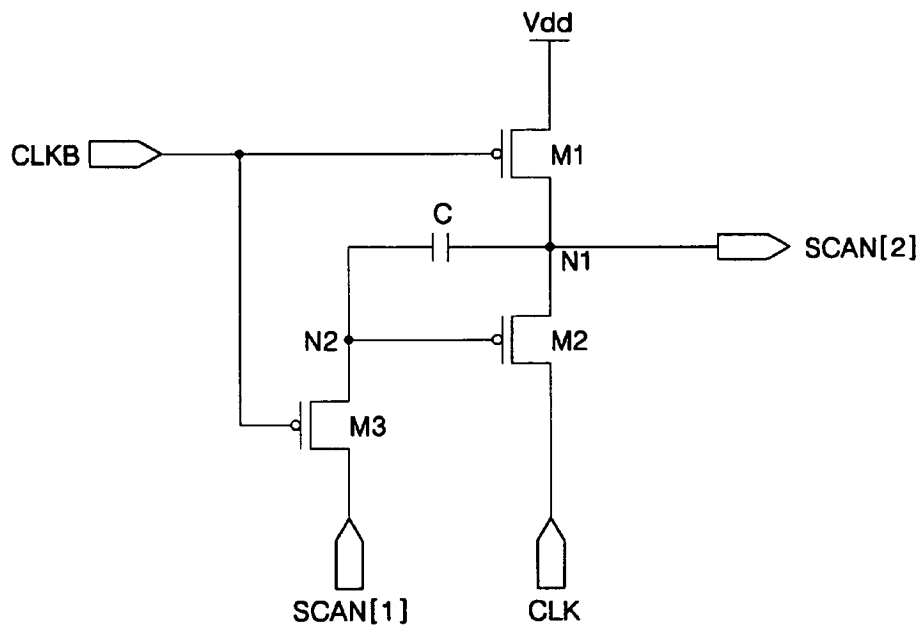


FIG. 5

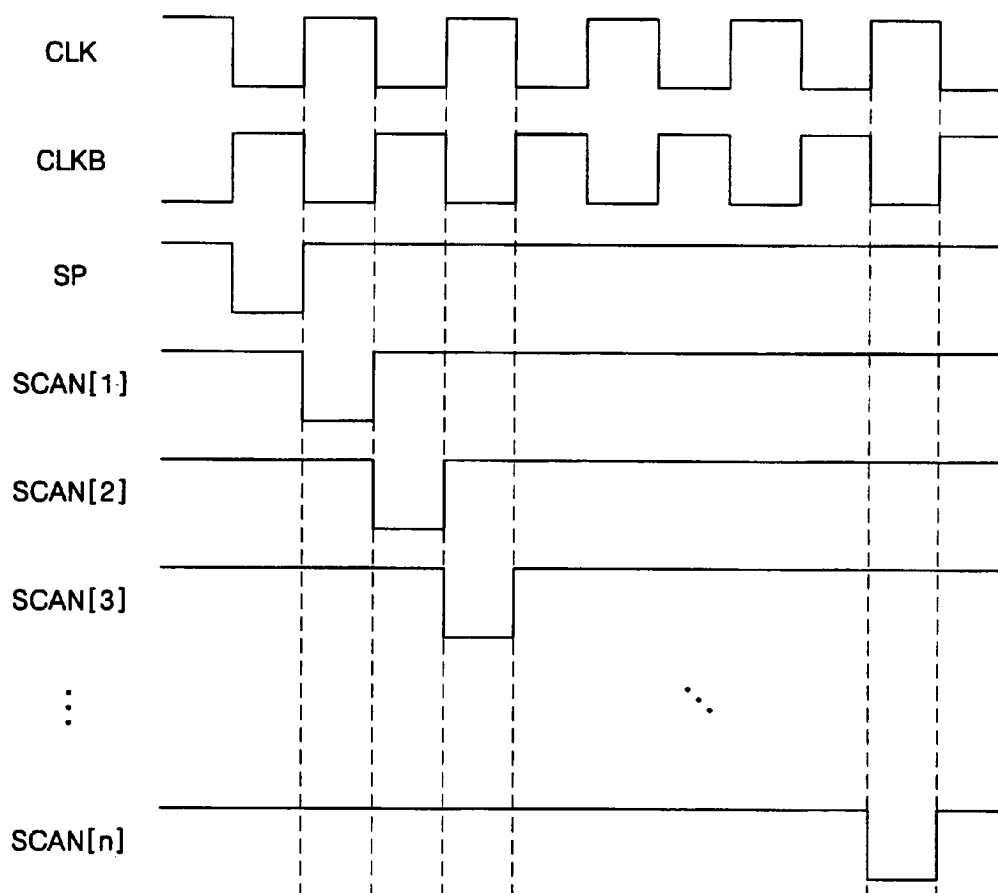


FIG. 6A

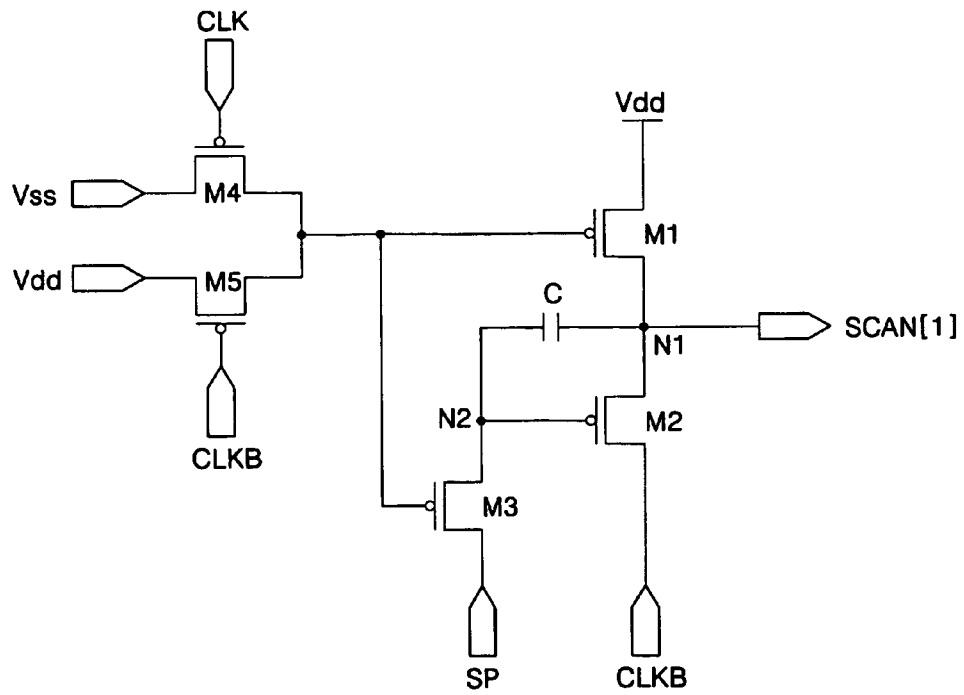
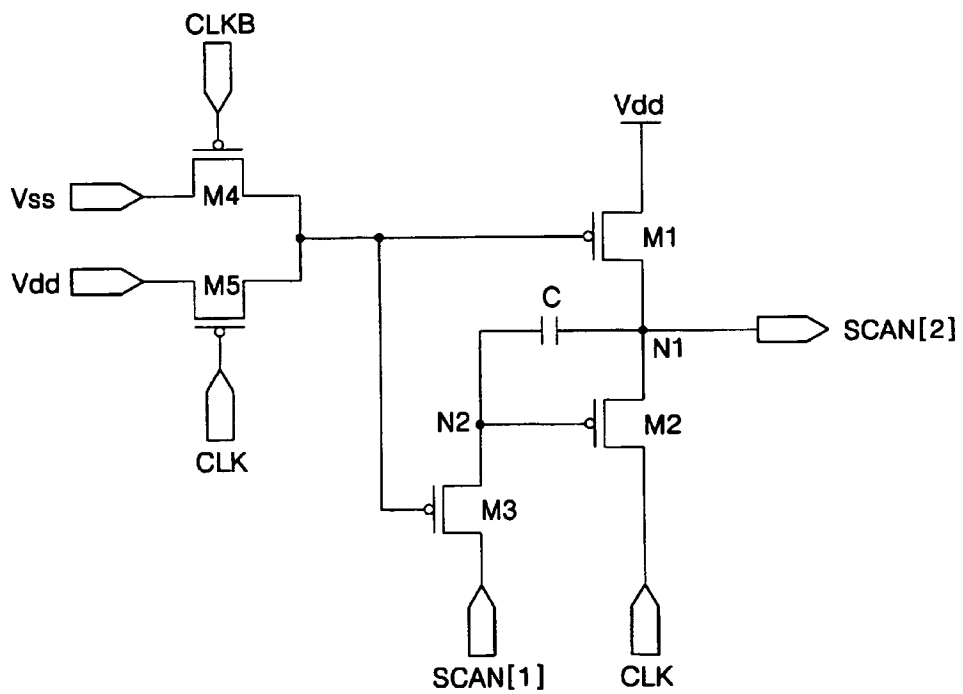


FIG. 6B



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 1531450 A2 [0014]
- US 6339631 B1 [0015]
- US 5644653 A [0016]

专利名称(译)	一种有机发光显示装置和用于产生扫描信号的方法，用于驱动具有扫描驱动器的有机发光显示装置		
公开(公告)号	EP1746566B1	公开(公告)日	2010-06-02
申请号	EP2006117723	申请日	2006-07-24
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO. , LTD.		
当前申请(专利权)人(译)	三星移动显示器有限公司.		
[标]发明人	CHUNG BO YONG LEGEL & IP TEAM CORP PLANNING STAFF		
发明人	CHUNG, BO-YONG LEGEL & IP TEAM CORP.PLANNING STAFF		
IPC分类号	G09G3/32		
CPC分类号	G11C19/28 G09G3/3266 G09G2300/026 G09G2300/0408 G09G2300/0417 G09G2300/0426 G09G2330/021		
代理机构(译)	hengelhaupt , Jürgen		
优先权	1020050066946 2005-07-22 KR		
其他公开文献	EP1746566A1		
外部链接	Espacenet		

摘要(译)

用于有机发光显示 (OLED) 器件的面板上系统 (SOP) 型扫描驱动器。扫描驱动器包括触发器。每个触发器接收输入信号，时钟信号和反相时钟信号，并输出扫描信号。扫描信号被移位并输入到相邻的触发器。每个触发器包括三个相同导电类型的晶体管和一个电容器。因此，由于电路的简化，布局面积被最小化，并且切断静电电流以降低功耗。

