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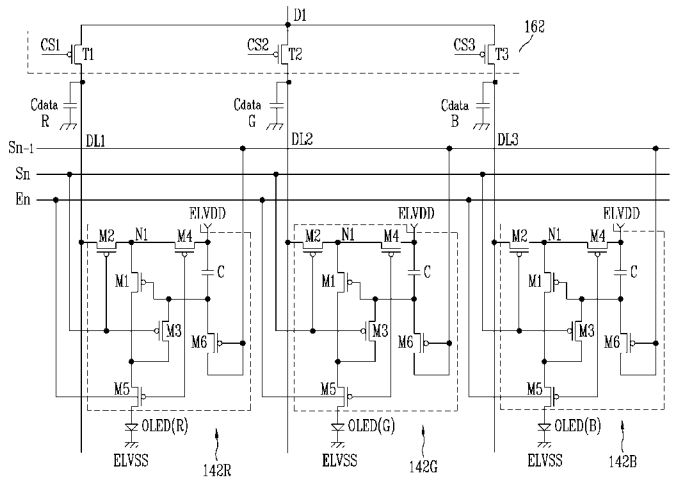
(54) Organic light emitting display

(57) An organic light emitting display including a demultiplexer on each data line that splits and supplies each data signal to a plurality of data lines, thereby decreasing the number of output lines required and reducing production cost. Further, voltages corresponding to the data signals are sequentially charged in data capacitors, while the charged voltages are supplied to the pixels simultaneously allowing the organic light emitting display to display an image with uniform brightness. Scan periods for supplying the scan signals do not overlap with data periods for supplying the data signals thus yielding a stable image. Further, the capacitance of a data capacitor is set depending on the emission efficiency of its corresponding organic light emitting diode, thereby keeping a proper white balance. Also, the capacitance of the data capacitor is set to compensate the voltage drop in the first power source line, thereby displaying an image with uniform brightness.

FIG. 6



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Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of Korean Patent Applications No. 2004-81811 and No. 2004-81812, filed on October 13, 2004, in the Korean Intellectual Property Office, the entire content of both of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to an organic light emitting display, and more particularly, to an organic light emitting display, in which the number of output lines provided in a data driver is decreased while the image is displayed with uniform brightness.

2. Discussion of Related Art

[0003] Recently, various flat panel displays have been developed, which are substituting for a cathode ray tube (CRT) display because the CRT display is relatively heavy and bulky. The flat panel displays include liquid crystal displays (LCD), field emission displays (FED), plasma display panels (PDP), and organic light emitting displays among other types.

[0004] Among the flat panel displays, the organic light emitting display includes organic light emitting diodes that emit light by electron-hole recombination. These organic light emitting displays have a faster response time than the LCDs that require a separate light source.

[0005] FIG. 1 illustrates a conventional organic light emitting display. A conventional organic light emitting display includes a pixel portion 30 including a plurality of pixels 40 formed in an intersection region of a plurality of scan lines S1 through Sn and a plurality of data lines D1 through Dm. A conventional organic light emitting display also includes a scan driver 10 to drive the scan lines S1 through Sn; a data driver 20 to drive the data lines D1 through Dm; and a timing controller 50 to control the scan driver 10 and the data driver 20.

[0006] The scan driver 10 generates scan signals in response to scan control signals SCS transmitted from the timing controller 50, and supplies the scan signals to the scan lines S1 through Sn in sequence. Further, the scan driver 10 generates emission control signals in response to the scan control signals SCS, and supplies the emission control signals to emission control lines E1 through En in sequence.

[0007] The data driver 20 generates data signals in response to data control signals DCS transmitted from the timing controller 50, and supplies the data signals to the data lines D1 through Dm. The data driver 20 supplies the data signal corresponding to one horizontal line per horizontal period to the data lines D1 through Dm.

[0008] The timing controller 50 generates the data control signals DCS and the scan control signals SCS in response to external synchronization signals. The data control signal DCS is transmitted to the data driver 20, and the scan control signal SCS is transmitted to the scan driver 10. Further, the timing controller 50 rearranges external data Data and supplies it to the data driver 20.

[0009] The pixel portion 30 receives external first power from an external first power source line ELVDD and external second power from an external second power source line ELVSS. The first power from the first power source line ELVDD and the second power from the second power source line ELVSS are supplied to each pixel 40. Each pixel 40 receives the data signal and displays an image corresponding to the data signal. Further, the emission time of the pixels 40 is controlled by the emission control signals.

[0010] In the conventional organic light emitting display, the pixels 40 are placed in the intersection regions of the scan lines S1 through Sn and the data lines D1 through Dm. The data driver 20 includes m output lines to supply the data signals to m data lines D1 through Dm. That is, the data driver 20 of the conventional organic light emitting display should have the same number of output lines as the number of the data lines D1 through Dm. To have m output lines, the data driver 20 needs to include a plurality of data integrated circuits that increase the production cost. Particularly, as the resolution and the size of the pixel portion 30 increase, the number of output lines of the data driver 20 increases. Thus, the production cost of the organic light emitting display is increased.

[0011] Therefore, there is a need for organic light emitting displays that require fewer output lines and therefore fewer data integrated circuits in their data driver. There is also a need for an organic light emitting display that displays a stable image with high uniformity.

SUMMARY OF THE INVENTION

[0012] Accordingly, it is an aspect of the present invention to provide an organic light emitting display, in which the number of output lines provided in a data driver is decreased, and an image is displayed with uniform brightness.

[0013] The foregoing and/or other aspects of the present invention are achieved by providing an organic light emitting display including a scan driver to supply scan signals to a plurality of scan lines; a data driver to supply data signals to a plurality of output lines; a demultiplexer provided on each output line to supply the data signal to a plurality of data lines; a pixel portion coupled to the scan lines, the data lines, and pixel power source lines, and including a red pixel including a red organic light emitting diode, a green pixel including a green organic light emitting diode, and a blue pixel including a blue organic light emitting diode; a plurality of first parasitic capacitors provided in the respective data lines coupled the red pixel to charge voltage corresponding to the data signal; a plurality of second parasitic capacitors provided in the respective data lines coupled the green pixel to charge voltage corresponding to the data signal; and a plurality of third parasitic capacitors provided in the respective data lines coupled the blue pixel to charge voltage corresponding to the data signal, wherein the first through third parasitic capacitors are different in capacitance from one another.

[0014] Preferably the second parasitic capacitor has a higher capacitance than the first parasitic capacitor, and the third parasitic capacitor has a lower capacitance than the first parasitic capacitor. Preferably the organic light emitting display further comprises a power source line to supply external first power to the pixel power source line. Preferably a first overlapping area between the data line coupled to the red pixel and the power source line, a second overlapping area between the data line coupled to the green pixel and the power source line, and a third overlapping area between the data line coupled to the blue pixel and the power source line are different from one another. Preferably the first overlapping area is smaller than the second overlapping area, and larger than the third overlapping area. Preferably the data line coupled to the red pixel overlaps the power source line by a first length, and the data line coupled to the green pixel overlaps the power source line by a second length longer than the first length. Preferably the data line coupled to the blue pixel overlaps the power source line by a third length shorter than the first length. Preferably the data line coupled to the red pixel overlaps the power source line by a first width, and the data line coupled to the green pixel overlaps the power source line by a second width wider than the first width. Preferably the data line coupled to the blue pixel overlaps the power source line by a third width narrower than the first width.

Preferably the scan driver supplies the scan signal during a first period of one horizontal period, and the data driver supplies the data signals to the output lines during a second period of the one horizontal period excluding the first period. Preferably each demultiplexer comprises a plurality of transistors, each transistor being coupled to one of the plurality of data lines. Preferably the plurality of transistors are turned on in sequence, and the first capacitor, the second capacitor, and the third capacitor are charged with voltages corresponding to the data signals when the transistors are turned on. Preferably the voltages stored in the first capacitor, the second capacitor, and the third capacitor are supplied to the red pixel, the green pixel and the blue pixel for the first period.

[0015] According to another aspect of the present invention an organic light emitting display is provided, the organic light emitting display including a scan driver to supply scan signals to a plurality of scan lines; a data driver to supply data signals to a plurality of output lines; a demultiplexer provided on each output line to supply the data signal to a plurality of data lines; a first power source line to supply first power through a first side of a plurality of pixel power source lines; a pixel portion including a pixel coupled to the scan line, the data line, the pixel power source line to emit light corresponding to the data signal; and a plurality of capacitors formed to have different capacitances according to overlapping areas between the first power source line and the respective data lines, storing voltage corresponding to the data signal, and supplying the stored voltage to the pixel.

[0016] Preferably at least two data lines are different in length from each other in the overlapping area with the first power source line. Preferably the length of the overlapping areas of the data lines and the first power source line becomes shorter going from an edge portion to a center portion of the first power source line. Preferably the data lines are bent in an S-shape in the overlapping areas with the first power source line. Preferably at least two data lines are different in width from each other in the overlapping area with the first power source line. Preferably the widths of the data lines become narrower as the data lines go from an edge portion to a center portion of the first power source line. Preferably the organic light emitting display further comprises an auxiliary power source line to supply the first power through a second side of the pixel power source line. Preferably the organic light emitting display further comprises a second power source line to supply a second power different from the first power to the pixels. Preferably the scan driver supplies the scan signal for a first period of one horizontal period, and the data driver supplies a plurality of data signals to respective output lines for a second period of the one horizontal period excluding the first period.

According to still another aspect of the present invention an organic light emitting display is provided, the organic light emitting display comprising a substrate; a pad part formed on the substrate, the pad part having first pads, second pads, third pads, fourth pads, fifth pads, and sixth pads; a pixel portion formed on the substrate and including a plurality of pixels defined by a plurality of second data lines, a plurality of scan lines, and a plurality of pixel power source lines; a scan driver located on one side of the pixel portion and electrically coupled to the first pads and to the scan lines; a data

driver directly formed on the substrate or embedded as a chip on the substrate and electrically coupled to the auxiliary power source line, to the second pads, and to a first data line; a first power source line formed adjacent to all sides of the pixel portion along edges of the substrate except where the pad part is located and coupled to the third pads and to the pixel power source lines; an auxiliary power source line located on the substrate along an edge where the pad is located and coupled to the fourth pads and to the plurality of pixel power source lines; a second power source line formed on the substrate coupled to the fifth pads and to each of the pixels; and a demultiplexer block coupled to the first data line, the second data lines, and to the sixth pads. Preferably the data driver and the demultiplexer block are embedded on a flexible printed circuit coupled to the substrate and wherein the data driver and the demultiplexer block are electrically coupled to the second data lines through the pad part of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. 1 illustrates a conventional organic light emitting display.

[0018] FIG. 2 illustrates an organic light emitting display according to an embodiment of the present invention.

[0019] FIG. 3 illustrates waveforms of driving signals supplied to a scan line, a data line and the demultiplexer of FIG. 2.

[0020] FIG. 4 is a circuit diagram of a demultiplexer illustrated in FIG. 2.

[0021] FIG. 5 is a circuit diagram of a pixel illustrated in FIG. 2.

[0022] FIG. 6 is a circuit diagram illustrating coupling of the demultiplexer circuit of FIG. 4 to the pixel circuit of FIG. 5.

[0023] FIG. 7 illustrates a first layout of the organic light emitting display according to embodiments of the present invention.

[0024] FIG. 8 is an enlarged view of a first embodiment of portion "A" of the first layout shown in FIG. 7.

[0025] FIG. 9 is an enlarged view of a second embodiment of portion "A" of the first layout shown in FIG. 7.

[0026] FIG. 10 illustrates a second layout of the organic light emitting display according to embodiments of the present invention.

[0027] FIG. 11 is an enlarged view showing a first embodiment of portion "B" of the second layout shown in FIG. 10.

[0028] FIG. 12 is an enlarged view showing a second embodiment of portion "B" of the second layout shown in FIG. 10.

[0029] FIG. 13 is an enlarged view showing a third embodiment of portion "B" of the second layout shown in FIG. 10.

[0030] FIG. 14 illustrates a third layout of the organic light emitting display according to embodiments of the present invention.

DETAILED DESCRIPTION

[0031] FIG. 2 illustrates an organic light emitting display according to an embodiment of the present invention.

[0032] The organic light emitting display includes a scan driver 110, a data driver 120, a pixel portion 130, a timing controller 150, a demultiplexer block 160, a demultiplexer controller 170, and data capacitors Cdata.

[0033] The pixel portion 130 includes a plurality of pixels 140 placed adjacent to regions defined by a plurality of scan lines S1 through Sn and a plurality of second data lines DL1 through DLm. Each pixel 140 emits light corresponding to a data signal transmitted through the second data line DL. The demultiplexer block 160 includes demultiplexers 162.

[0034] FIG. 3 illustrates waveforms of driving signals supplied to the scan lines, the data lines, and the demultiplexers of FIG. 2. The figure shows scan signals SS applied to the n^{th} scan line Sn and the $(n-1)^{th}$ scan line Sn-1, emission control signals EMI applied to the emission control lines En, first, second, and third control signals CS1, CS2, CS3, and external data Data signals. The first, second, and third control signals CS1, CS2, CS3 are provided from the demultiplexer controller 170 to the pixels 140. Different parts of FIG. 3 pertain to various of the following figures and are discussed below together with the discussion of the pertinent figure. Further, the low or high position of the signals of FIG. 3 correspond to the transistor types of the circuits being driven by these signals. The circuits that are shown in the following figures may be implemented in NMOS as well as PMOS. Therefore, it is understood that driving signals of polarity opposite those shown would apply if the transistor type is changed.

[0035] The scan driver 110 generates scan signals SS in response to scan control signals SCS supplied from the timing controller 150, and supplies the scan signals SS to the scan lines S1 through Sn in sequence. The scan driver 110 supplies the scan signal SS during a predetermined period included in the one horizontal period 1H. For example, in one embodiment shown in FIG. 3, the one horizontal period 1H is divided into a scan period (first period) and a data period (second period). The scan driver 110 supplies the scan signal SS to the scan lines S1 through Sn during the scan period of the one horizontal period 1H. On the other hand, the scan driver 110 does not supply the scan signal SS during the data period of the one horizontal period 1H. The scan driver 110 also generates the emission control signals EMI in response to the scan control signals SCS, and supplies the emission control signals EMI to emission control lines E1 through En in sequence.

[0036] The data driver 120 generates the data signal in response to a data control signal DCS supplied from the timing controller 150, and supplies the data signals to a plurality of first data lines D1 through Dm/i. The data driver 120 supplies

i data signals (where i is a natural number of 2 or more) to the first data lines D1 through Dm/i that are coupled to output lines of the data driver 120 in sequence.

[0037] For example, the data driver 120 supplies data signals R, G, B to the pixels 140 in sequence during the data period of the one horizontal period 1H. The data signals R, G, B are supplied during only the data period, so that supplying the data signals R, G, B does not overlap with supplying the scan signal SS. During the scan period of the one horizontal period 1H, the data driver 120 supplies a merely dummy data signal DD.

[0038] The timing controller 150 generates the data control signals DCS and the scan control signals SCS corresponding to external synchronization signals. The data control signals DCS generated by the timing controller 150 are supplied to the data driver 120, and the scan control signals SCS generated by the timing controller 150 are supplied to the scan driver 110.

[0039] The demultiplexer block 160 includes m/i demultiplexers 162. In other words, the demultiplexer block 160 has the same number of demultiplexers 162 as the number of the first data lines D1 through Dm/i. The demultiplexers 162 are coupled to the first data lines D1 through Dm/i, respectively. The demultiplexers 162 are also coupled to i second data lines DL1 through DLm, respectively. Thus, each demultiplexer 162 supplies the i data signals R, G, B received through each first data lines D, from the data driver 120 during the data periods, to the i second data lines DL.

[0040] Accordingly, as the data signal R, G, B received through one first data line D is supplied to i second data lines DL, the number of output lines required in the data driver 120 is markedly decreased. For instance, when i is 3, the number of output lines provided in the data driver 120 is decreased to 1/3 of the number of output lines required with no demultiplexing (i of one). Thus, the number of data integrated circuits provided in the data driver 120 is decreased. Employing the demultiplexer 162 for supplying the data signal R, G, B of one first data line D to i second data lines DL, helps reduce the production cost of the organic light emitting display.

[0041] The demultiplexer controller 170 supplies i control signals to the respective demultiplexers 162 during the data period in the one horizontal period 1H, thereby splitting the data signal from one of the first data lines D into i data signals and supplying i data signals to i second data lines DL. As shown in FIG. 3, the demultiplexer controller 170 supplies the i control signals in sequence, so that the i control signals do not overlap. In the exemplary embodiment shown in FIG. 2, the demultiplexer controller 170 is separately provided outside the timing controller 150. However, the invention is not limited to this configuration and the demultiplexer controller 170 may be integrally provided inside the timing controller 150.

[0042] One data capacitor Cdata is provided in every second data line DL. The data capacitor Cdata temporarily stores the data signal R, G, B supplied to the second data line DL, and subsequently supplies the stored data signal R, G, B to the pixel 140. In one embodiment, the data capacitor Cdata is a parasitic capacitor equivalently formed by the second data line DL. In one embodiment, the capacitance of the parasitic capacitor equivalently formed by the second data line DL is larger than the capacitance of a storage capacitor Cst provided in every pixel 140 (refer to FIG. 5). This relationship between the two capacitance values causes stable storing of the data signal R, G, B in the storage capacitance Cst of the pixel 140.

[0043] FIG. 4 is a circuit diagram of the demultiplexer 162 illustrated in FIG. 2. In this figure, for the sake of convenience, i is 3 and the demultiplexer 162 is coupled to the 1st one of the first data lines D1.

[0044] Each demultiplexer 162 includes a first switching device T1, a second switching device T2, and a third switching device T3. The switching devices may be transistors.

[0045] The first switching device T1 is coupled between the 1st first data line D1 and the 1st second data line DL1. The first switching device T1 is turned on when it receives the first control signal CS1 from the demultiplexer controller 170, and supplies the data signal R, G, B from the 1st first data line D1 to the 1st second data line DL1. The data signal R, G, B supplied to the 1st second data line DL1 is temporarily stored in the first data capacitor Cdata1.

[0046] The second switching device T2 is coupled between the 1st first data line D1 and the 2nd second data line DL2. The second switching device T2 is turned on when it receives the second control signal CS2 from the demultiplexer controller 170, and supplies the data signal from the 1st first data line D1 to the 2nd second data line DL2. The data signal supplied to the 2nd second data line DL2 is temporarily stored in the second data capacitor Cdata2.

[0047] The third switching device T3 is coupled between the 1st first data line D1 and the 3rd second data line DL3. The third switching device T3 is turned on when it receives the third control signal CS3 from the demultiplexer controller 170, and supplies the data signal from the 1st first data line D1 to the 3rd second data line DL3. The data signal supplied to the 3rd second data line DL3 is temporarily stored in the third data capacitor Cdata3.

[0048] Operation of the demultiplexer 162 with the pixel 140 are described in the context of the exemplary circuit configurations of FIGs. 4 and 5.

[0049] FIG. 5 is a circuit diagram of the pixel 140 illustrated in FIG. 2. The pixel 140 of the invention is not limited to the circuit shown in FIG. 5, and may include other configurations. For example, the circuit may include at least one transistor capable of being used as a diode.

[0050] Each pixel 140 includes a pixel circuit 142 coupled to the second data line DL, the scan line Sn, the emission control line En, and an organic light emitting diode OLED. The pixel circuit 142 controls the organic light emitting diode

OLED and causes it to emit light.

[0051] The organic light emitting diode OLED includes an anode electrode coupled to the pixel circuit 142, and a cathode electrode coupled to the second power source line ELVSS. The second power source line ELVSS applies a voltage lower than the voltage of the first power source line ELVDD. For example, the second power source line ELVSS may be at ground voltage. The organic light emitting diode OLED includes fluorescent and/or phosphorescent organic material that allow it to emit light when receiving a current supplied from the pixel circuit 142.

[0052] The pixel circuit 142 includes a storage capacitor Cst and first, second, thrid, fourth, fifth, and sixth transistors M1, M2, M3, M4, M5, M6. The storage capacitor Cst and the sixth transistor M6 are coupled between the first power source line ELVDD and the $(n-1)^{th}$ scan line Sn-1. The second transistor M2 and the fourth transistor M4 are coupled together forming a first node N1 and are also coupled between the first power source line ELVDD and the second data line DL. The fifth transistor M5 is coupled between the organic light emitting diode OLED and the emission control line En. The first transistor M1 is coupled between the fifth transistor M5 and the first node N1. The third transistor M3 is coupled between gate and drain terminals of the first transistor M1. In the exemplary embodiment shown in FIG. 5, the first through sixth transistors M1 through M6 are of a p-type metal oxide semiconductor field effect transistor (PMOSFET), but the invention is not limited to this particular exemplary configuration. Alternatively, the first through sixth transistors M1 through M6 may be of an n-type metal oxide semiconductor field effect transistor (NMOSFET). As well known to those skilled in the art, in the case where the first through sixth transistors M1 through M6 are of the NMOSFET type, polarity of driving waveforms is reversed.

[0053] The first transistor M1 includes a source terminal coupled to the first node N1, the drain terminal coupled to a source terminal of the fifth transistor M5, and the gate terminal coupled to the storage capacitor Cst. Further, the first transistor M1 supplies current corresponding to voltage charged in the storage capacitor Cst to the organic light emitting diode OLED.

[0054] The third transistor M3 includes a drain terminal coupled to the gate terminal of the first transistor M1, a source terminal coupled to the drain terminal of the first transistor M1, and a gate terminal coupled to the n^{th} scan line Sn. The third transistor M3 is turned on when the scan signal SS is transmitted to the n^{th} scan line Sn, and thus causes the first transistor M1 to be coupled like a diode. That is, when the third transistor M3 is turned on, the first transistor M1 functions as a diode.

[0055] The second transistor M2 includes a source terminal coupled to the second data line DL, a drain terminal coupled to the first node N1, and a gate terminal coupled to the n^{th} scan line Sn. The second transistor M2 is turned on when the scan signal SS is transmitted to the n^{th} scan line Sn. A turned-on second transistor M2 transmits the data signal R, G, B from the second data line DL to the first node N1.

[0056] The fourth transistor M4 includes a drain terminal coupled to the first node N1, a source terminal coupled to the first power source line ELVDD, and a gate terminal coupled to the emission control line En. The fourth transistor M4 is turned on when the emission control signal EMI is not being supplied. A turned-on fourth transistor electrically couples the first power source line ELVDD with the first node N1.

[0057] The fifth transistor M5 includes the source terminal that is coupled to the drain terminal of the first transistor M1, a drain terminal coupled to the organic light emitting diode OLED, and a gate terminal coupled to the emission control line E. The fifth transistor M5 is turned on when the emission control signal EMI is not being supplied, thereby supplying current from the first transistor M1 to the organic light emitting diode OLED.

[0058] The sixth transistor M6 includes a source terminal coupled to the storage capacitor Cst, and drain and gate terminals coupled to the $(n-1)^{th}$ scan line Sn-1. Further, the sixth transistor M6 is turned on when the scan signal SS is transmitted to the $(n-1)^{th}$ scan line Sn-1, thereby initializing the storage capacitor Cst and the gate terminal of the first transistor M1.

[0059] FIG. 6 is a circuit diagram illustrating the coupling of the demultiplexer 162 of FIG. 4 to the pixel circuit 142 of FIG. 5. In the exemplary embodiment shown, one demultiplexer 162 is coupled with three pixel circuit of red (R) 142R, green (G) 142G, and blue (B) 142B, so that i is 3.

[0060] The operations of the demultiplexer 162 and the pixel 140 are described with reference to FIGs. 3 and 6. First, the scan signal SS is transmitted to the $(n-1)^{th}$ scan line Sn-1 during the scan period of the one horizontal period 1H. When the scan signal SS is transmitted to the $(n-1)^{th}$ scan line Sn-1, each sixth transistor M6 of the pixels 142R, 142G and 142B is turned on. As the sixth transistor M6 is turned on, the storage capacitor Cst and the gate terminal of the first transistor M1 are coupled to the $(n-1)^{th}$ scan line Sn-1. That is, when the scan signal SS is transmitted to the $(n-1)^{th}$ scan line Sn-1, the scan signal SS is supplied to each storage capacitor Cst and each gate terminal of the first transistor M1 provided in the pixels 142R, 142G and 142B, thereby initializing each storage capacitor Cst and each gate terminal of the first transistor M1. The scan signal SS has a voltage level lower than the data signal R, G, B.

[0061] When the scan signal SS is transmitted to the $(n-1)^{th}$ scan line Sn-1, the second transistor M2 coupled to the n^{th} scan line Sn remains turned off.

[0062] Then, the first, second, and third switching devices T1, T2, T3 are turned on in sequence by the first, second, and third control signals CS1, CS2, CS3 transmitted in sequence during the data period. When the first switching device

T1 is turned on by the first control signal CS1, the data signal R, G, B is transmitted from the 1st first data line D1 to the 1st second data line DL1. The first data capacitor Cdata1 is charged with voltage corresponding to the data signal R, G, B transmitted to the 1st second data line DL1.

[0063] When the second switching device T2 is turned on by the second control signal CS2, the data signal R, G, B is transmitted from the 1st first data line D1 to the 2nd second data line DL2. The second data capacitor Cdata2 is charged with voltage corresponding to the data signal R, G, B transmitted to the 2nd second data line DL2. When the third switching device T3 is turned on by the third control signal CS3, the data signal R, G, B is transmitted from the 1st first data line D1 to the 3rd second data line DL3. The third data capacitor Cdata3 is charged with voltage corresponding to the data signal R, G, B transmitted to the 3rd second data line DL3. As seen in FIG. 3, the first, second, and third control signals CS1, CS2, CS3 are supplied during data periods of the one horizontal period 1H. However, the scan signal SS is not supplied during the data period, and, therefore, the data signal R, G, B is not being supplied to the pixels 142R, 142G and 142B while the control signals are being supplied.

[0064] Following the data period, the scan signal SS is transmitted to the n^{th} scan line Sn. When the scan signal SS is transmitted to the n^{th} scan line Sn, each second transistor M2 and each third transistor M3 of the pixels 142R, 142G and 142B are turned on. As each second transistor M2 and each third transistor M3 of the pixels 142R, 142G and 142B turn on, voltages corresponding to the data signals R, G, B stored in the first through third data capacitor Cdata1, Cdata2, Cdata3 are supplied to the respective first nodes N1 of the pixels 142R, 142G and 142B.

[0065] When the scan signal SS transmitted to the $(n-1)^{th}$ scan line Sn-1 is set to have a voltage level lower than that of the data signal R, G, B applied to the first node N1, the first transistor M1 is turned on. The voltage applied to the gate terminal of each first transistor M1 provided in the pixels 142R, 142G and 142B is initialized by this scan signal SS transmitted to the $(n-1)^{th}$ scan line Sn-1. As the first transistor M1 is turned on, the voltage corresponding to the data signal R, G, B applied to the first node N1 is supplied to one terminal of the storage capacitor Cst via the first transistor M1 and the third transistor M3. As a result, each storage capacitor Cst provided in the pixels 142R, 142G and 142B is charged with voltage corresponding to the data signal R, G, B. In addition to the voltage corresponding to the data signal R, G, B, the storage capacitors Cst are also charged with voltage corresponding to the threshold voltage of the first transistor M1. While the emission control signal EMI is not supplied through the emission control line En, the fourth and fifth transistors M4 and M5 are turned on and current corresponding to the voltage charged in the storage capacitor Cst is supplied to each organic light emitting diode OLED(R), OLED(G), OLED(B), causing them to emit light.

[0066] Thus, according to an embodiment of the present invention, the demultiplexer 162 is employed for splitting and supplying the data signal R, G, B from one of the first data lines D1 to i second data lines DL. The data capacitor Cdata1, Cdata2, Cdata3 is charged with the voltage corresponding to the data signal R, G, B during the data period, and supplies the charged voltage to the pixel 140 during the scan period. According to an embodiment of the present invention, the scan period for supplying the scan signal SS and the data period for supplying the data signal R, G, B do not overlap. As a result, the voltage applied to the gate terminal of the third transistor M3 does not fluctuate, allowing the organic light emitting display to stably display an image. Further, the voltages stored in the data capacitors Cdata1, Ddata2, Cdata3, corresponding to the data signals R, G, B, are supplied to the pixels 140 at the same time. As a result, the organic light emitting display can display an image with uniform brightness.

[0067] However, even with the same data signal R, G, B supplied, each organic light emitting display emits light with a different brightness due to material properties of the organic light emitting diodes OLED. When the same red, green, or blue data signal R, G, B is supplied to the organic light emitting display, emission efficiency varies from a high value for a green organic light emitting diode OLED(G), to lower values for a red organic light emitting diode OLED(R), and a blue organic light emitting diode OLED(B) as shown in Equation 1.

[0068]

$$G_{efficiecy} > R_{efficiency} > B_{efficiency}$$

[Equation 1]

where $G_{efficiency}$, $R_{efficiency}$, $B_{efficiency}$ denote the emission efficiencies of the organic light emitting diodes emitting green, red, and blue lights OLED(G), OLED(R), and OLED(B).

[0069] When the emission efficiency of the organic light emitting diodes OLED is different for lights of different colors, white balance is poor and it is impossible to represent a desired color. Therefore, in the organic light emitting display of the present invention, the capacitance of the data capacitor Cdata is determined taking into account the different efficiencies of emission for lights of different color. For example, the second data capacitor Cdata2 that stores the green data signal G is set to have the highest capacitance, and the third data capacitor Cdata3 that stores the blue data signal B is set to have the lowest capacitance. Then, a red pixel R, a green pixel G and a blue pixel B are properly adjusted to

achieve white balance and better picture quality.

[0070] A voltage VG applied to the gate terminal of the first transistor M1 provided in each pixel is determined by Equation 2.

[0071]

$$VG = (Cdata \times Vdata + Cst \times Vint) / (Cdata + Cst)$$

[Equation 2]

where Vdata is a voltage corresponding to the data signal R, G, B stored in the data capacitor Cdata during a current frame, and Vint is a voltage corresponding to the data signal R, G, B stored in the storage capacitor Cst during a previous frame.

[0072] Referring to Equation 2, the voltage VG applied to the gate terminal of the first transistor M1 increases as the capacitance of the data capacitor Cdata increases. For example, in the case of Cst = 1 and Vint = 1, the following Equation 3 is obtained.

[0073]

$$VG = (Cdata \times Vdata + 1) / (Cdata + 1)$$

[Equation 3]

[0074] In Equation 3, when Vdata is 10 and Cdata is 10, VG is determined as about 9.18V. Further, when Vdata is 10 and Cdata is 1000, VG is determined as about 10V. Therefore, as the capacitance of the data capacitor Cdata increases the voltage VG applied to the gate terminal of the first transistor M1 also increases. When the voltage VG applied to the gate terminal of the first transistor M1 increases, the charge stored in the storage capacitor Cst also decreases. Decrease in the charge of the storage capacitor Cst reduces the current supplied by the storage capacitor Cst to the organic light emitting diode OLED. Thus, according to an embodiment of the present invention, the capacitance of the data capacitor Cdata is set with a high value for the second data capacitor Cdata2, corresponding to the green organic light emitting diode OLED(G), a lower value for the first data capacitor Cdata1, corresponding to the red organic light emitting diode OLED(R), and even a lower value for the third data capacitor Cdata3, corresponding to the blue organic light emitting diode OLED(B). This gradation of capacitance values compensates for the differences between the emission efficiencies of the different diodes and controls the white balance.

[0075] FIG. 7 illustrates a first layout 1000 of the organic light emitting display according to embodiments of the present invention. The organic light emitting display having the first layout 1000 includes a pixel portion 130 formed on a substrate 300 and including a plurality of pixels 140 defined by a plurality of second data lines DL, a plurality of scan lines S, and a plurality of pixel power source lines VDD. The first layout 1000 also includes a first power source line 210 and an auxiliary power source line 212 coupled to the pixel power source line VDD, a data driver 120, and a demultiplexer block 160.

[0076] According to an embodiment of the present invention, the first layout 1000 of the organic light emitting display further includes a scan driver 110, a second power source line 230, and a pad part 200.

[0077] The scan driver 110 is located on one side of the pixel portion 130 and is electrically coupled to a first pad Ps of the pad part 200. The scan driver 110 supplies the scan signals SS to the scan lines S1 through Sn in sequence during the scan period of the one horizontal period 1H in response to the scan control signal SCS supplied from the first pad Ps.

[0078] The data driver 120 is electrically coupled to second pads Pd of the pad part 200 and to the first data line D. The data driver 120 generates a data signal corresponding to the data control signal DCS and the external data Data supplied from the second pads Pd, and supplies the generated data signals to the first data lines D. The data driver 120 supplies i data signals to the respective first data lines D during the data period of the one horizontal period 1H. The data driver 120 can be directly formed on the substrate 300, or embedded as a chip on the substrate 300. For example, the data driver 120 can be embedded as a chip on the substrate 300 by a chip-on glass method, a wire bonding method, a flip-chip method, a beam lead method, or the like.

[0079] The first power source line 210 is formed adjacent to all sides of the pixel portion 130 along the edges of the substrate 300 except where the pad part 200 is located. The first power source line 210 includes opposite ends coupled to a third pad Pvdd1 of the pad part 200. Further, the first power source line 210 supplies voltage received through the

third pad Pvdd1 to first ends of the pixel power source lines VDD.

[0080] The auxiliary power source line 212 is formed to be adjacent to a bottom side of the pixel portion 130. The auxiliary power source line 212 includes opposite ends electrically coupled to a fourth pad Pvdd2 of the pad part 200. The auxiliary power source line 212 supplies the voltage received through the fourth pad Pvdd2 to second ends of the pixel power source lines VDD.

[0081] The second power source line 230 is formed over the area of the pixel portion 130. The second power source line 230 commonly supplies the voltage of the second power source line ELVSS received through a fifth pad Pvss of the pad part 200 to each pixel 140.

[0082] The demultiplexer block 160 supplies i data signals received through the first data line D to i second data lines DL in response to the control signals CS1, CS2, CS3 transmitted from a sixth pad Pc of the pad part 200. Further, the data signals sequentially supplied from the demultiplexer block 160 are stored in the data capacitor Cdata equivalently formed on the second data lines DL, and then supplied to the pixels 140 at the same time.

[0083] The capacitance values of the data capacitors Cdata coupled to, or equivalently formed on, the second data line DL are set in consideration of the emission efficiency of the red organic light emitting diode OLED(R), the green organic light emitting diode OLED(G), and the blue organic light emitting diode OLED(B). As a result, the second data capacitor Cdata2, coupled to the green pixel G, has the highest capacitance, and the third data capacitor Cdata3, coupled to the blue pixel B, has the lowest capacitance. To accomplish the variation in capacitance values of the data capacitors Cdata, in one embodiment overlapping areas between the first power source line 210 and the second data line DL coupled to the red pixel R, between the first power source line 210 and the second data line DL coupled to the green pixel G, and between the first power source line 210 and the second data line DL coupled to the blue pixel B are set to be different from one another. The overlapping areas occur in portion "A" that is demarcated toward the top of the substrate 300.

[0084] FIG. 8 is an enlarged view showing a first embodiment A1 of the portion "A" shown in FIG. 7. The second data lines DL are equivalently forming the data capacitors Cdata (parasitic capacitor). The first data capacitor Cdata1 supplies a voltage corresponding to the data signal R to the red pixel R, the second data capacitor Cdata2 supplies a voltage corresponding to the data signal G to the green pixel G, and the third data capacitor Cdata3 supplies a voltage corresponding to the data signal B to the blue pixel B. The capacitance values of these three data capacitors Cdata1, Cdata2, Cdata3 are set to be different from one another.

[0085] For example, the second data lines DL1 coupled to the red pixel R overlaps the first power source line 210 by a first length h1, so that the first data capacitor Cdata1 is set to have a predetermined capacitance corresponding to the first length h1. Similarly, the second data lines DL2 coupled to the green pixel G overlaps the first power source line 210 by a second length h2. The second length h2 is longer than the first length h1, so the second data capacitor Cdata2 will have a higher capacitance than the first data capacitor Cdata1. Also, the second data lines DL3 coupled to the blue pixel B overlaps the first power source line 210 by a third length h3. The third length h3 is shorter than the first length h1, so the capacitance of the third data capacitor Cdata3 is lower than the first capacitor Cdata1.

[0086] Thus, the capacitance of the data capacitors Cdata is set in decreasing order from the second capacitor Cdata2 to the first capacitor Cdata1 to the third capacitor Cdata3 (Cdata2 (G) > Cdata1 (R) > Cdata3 (B)). This helps improve the white balance.

[0087] FIG. 9 is an enlarged view showing "A2" which is a second embodiment of the portion "A" shown in FIG. 7. The second data lines DL are equivalently forming the data capacitors Cdata. In other words, the data capacitors Cdata are parasitic capacitors forms by the second data lines DL. The first data capacitor Cdata1 supplies a voltage corresponding to the data signal R to the red pixel R, the second data capacitor Cdata2 supplies a voltage corresponding to the data signal G to the green pixel G, and the third data capacitor Cdata3 supplies a voltage corresponding to the data signal B to the blue pixel B. The three data capacitors Cdata1, Cdata2, Cdata3 are set to have capacitances that are different from one another.

[0088] For example, the second data lines DL1 coupled to the red pixel R, overlaps the first power source line 210 by a first width W1, so that the first data capacitor Cdata1 is set to have a predetermined capacitance corresponding to the first width W1. Similarly, the second data lines DL2 coupled to the green pixel G, overlaps the first power source line 210 by a second width W2. The second width W2 is wider than the first width W1, so that the second data capacitor Cdata2 is set to have a capacitance higher than the first capacitor Cdata1. Also, the second data lines DL3 coupled to the blue pixel B overlaps the first power source line 210 by a third width W3. The third width W3 is smaller than the first width W1, so that the third data capacitor Cdata3 is set to have a capacitance lower than the first capacitor Cdata1.

[0089] Thus, the capacitance of the data capacitors Cdata is set in the decreasing order from the second capacitor Cdata2 to the first capacitor Cdata1 and to the third capacitor Cdata3 (Cdata2 (G) > Cdata1 (R) > Cdata3 (B)), thereby preserving the white balance regardless of the emission efficiency of the red, green and blue organic light emitting diodes OLED.

[0090] FIG. 10 illustrates a second layout 2000 of the organic light emitting display of the present invention. The second layout 2000 has the same configuration as the first layout 1000 except for portion "B".

[0091] In the second layout 2000 of the organic light emitting display of the present invention, the data capacitors Cdata coupled to, or equivalently formed on, the second data lines DL are set differently according to overlapping areas between the second data line DL and the first power source line 210. The overlapping areas between the second data lines DL and the first power source lines 210 are varied taking into account voltage drop due to line resistance depending on the length of the first power source line 210. Thus, the data capacitors Cdata have different capacitance values according to the voltage drop in the first power source line, thereby allowing the organic light emitting display to display an image with uniform brightness.

[0092] FIG. 11 is an enlarged view showing a first embodiment "B1" of the portion "B" shown in FIG. 10. The second data lines DL are formed having the same line width, but different overlapping lengths with the first power source line 210 that result in different overlapping areas. Therefore, the consecutive second data lines DL have lengths that vary according to the location on the first power source line 210 where the second data line DL couples to the first power source line 210. The second power source lines DL becomes shorter as it goes from an edge portion of the first power source line 210 to a center portion. Thus, the overlapping areas between the first power source line 210 and the second data lines DL become smaller as the second data line DL goes from the 1^{st} second data line DL1 to the $(m/2)^{th}$ second data line DLm/2. Likewise, the overlapping areas between the first power source line 210 and the second data lines DL become larger as the second data line DL goes from the $(m/2+1)^{th}$ second data line DLm/2+1 to the m^{th} second data line DLm. The gradual decrease in the overlapping areas and the subsequent gradual increase are symmetric such that the overlapping area between the k^{th} second data line DLk and the first data line 210 is equal to that between $(m+1-k)^{th}$ second data line DLm+1-k and the first data line 210, where k is a positive integer less than m/2.

[0093] As explained above, the capacitance of the data capacitor Cdata become smaller going from the edge of the first power source line 210 to its center. This change in the capacitance values compensates for the voltage drop in the first power source line 210 from edges to center and allows the image to be displayed with uniform brightness.

[0094] FIG. 12 is an enlarged view showing a second embodiment "B2" of the portion "B" shown in FIG. 10. The second data lines DL shown in this figure also have different overlapping area with the first power source line 210. In this embodiment, the width of the overlapping areas of the consecutive second data lines DL with the first power source line 210 varies from the edges of the first power source line 210 to its center. The second data lines DL become successively narrower from an edge portion of the first power source line 210 toward its center portion.

[0095] Due to this successive narrowing of the overlapping areas, the 1^{st} second data line DL1 overlaps the first power source line 210 by a first width W1, and the 2^{nd} second data line DL2 overlaps the first power source line 210 by a second width W2 narrower than the first width W1. Similarly, the m^{th} second data line DLm overlaps the first power source line 210 by the first width W1, and the $(m-1)^{th}$ second data line DLm-1 overlaps the first power source line 210 by the second width W2. Thus, the line width of the second power source line DL becomes narrower as it goes from the edge portions of the first power source line 210 to the center portion. Consequently, the capacitance of the data capacitors Cdata decrease going from the edges of the first power source line 210 to its center. Therefore, the voltage drop from the edges to the center of the first power source line 210 is compensated by the varying capacitances of the data capacitors Cdata and an image with the uniform brightness may be displayed.

[0096] FIG. 13 is an enlarged view showing a third embodiment "B3" of the portion "B" shown in FIG. 10. In this embodiment too, the second data lines DL have different capacitances that result from their different overlapping areas with the first power source line 210. As the figure shows, the second data lines DL are bent in S-shapes to have different lengths and therefore different overlapping areas with the first power source line 210.

[0097] The S-shaped curves of the second power source lines DL become shorter in consecutive lines from an edge portion of the first power source line 210 to a center portion. Thus, the overlapping areas between the first power source line 210 and the second data lines DL become smaller as the second data lines DL go from the 1^{st} second data line DL1 to the $(m/2)^{th}$ second data line DLm/2. Similarly, the overlapping areas between the first power source line 210 and the second data lines DL become larger as the second data lines DL go from the $(m/2+1)^{th}$ second data line DLm/2+1 to the m^{th} second data line DLm. The symmetrical decrease and subsequent increase in the overlapping areas of the consecutive second data lines DL causes the overlapping area between the k^{th} second data line DLk and the first data line 210 to be equal to that between $(m+1-k)^{th}$ second data line DLm+1-k and the first data line 210, where k is a positive integer less than m/2.

[0098] Thus, the capacitance values of the data capacitors Cdata become smaller going from the edges to the center of the first power source line 210, so that the voltage drop in the first power source line 210 is compensated for and an image may be displayed with uniform brightness.

[0099] FIG. 14 illustrates a third layout 3000 of the organic light emitting display of the present invention. In FIG. 14, the organic light emitting display has the same configuration as that illustrated for the second layout in FIG. 10 except for the location of the data driver 120 and the demultiplexer block 160 that are different.

[0100] The third layout 3000 includes a data driver 120' and a demultiplexer block 160' that are embedded on a flexible printed circuit 180 coupled to a substrate 300'. Thus, the data driver 120' and the demultiplexer block 160' are electrically coupled to a second data line DL through a pad part of the substrate 300, thereby supplying a data signal. Alternatively,

the data driver 120' and the demultiplexer block 160' may be mounted on a chip on board mounted on a printed circuit board, a chip on film directly mounted on the film, a general film type connector used in a tape carrier package, or the like.

[0101] As described above, the present invention provides an organic light emitting display, in which a data signal received through one output line is split and supplied to a plurality of second data lines, thereby decreasing the number of output lines required and reducing production cost. In an embodiment, voltages corresponding to the data signals are sequentially charged in data capacitors, while the charged voltages are supplied to the pixels all at the same time. Because the voltages charged in the data capacitors are supplied to the pixels simultaneously, the organic light emitting display is allowed to display an image with uniform brightness. In an embodiment, scan periods for supplying the scan signals do not overlap with data periods for supplying the data signals. This feature yields a stable image. In an embodiment, the capacitance of a data capacitor is set depending on the emission efficiency of its corresponding organic light emitting diode, thereby keeping a proper white balance. In an embodiment, the capacitance of the data capacitor is set to compensate the voltage drop in the first power source line, thereby displaying an image with uniform brightness.

[0102] Although exemplary embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes might be made to these embodiments without departing from the principles and spirit of the invention, the scope of which is defined in the claims and their equivalents.

Claims

1. An organic light emitting display comprising:

a scan driver to supply scan signals to a plurality of scan lines;
a data driver to supply data signals to a plurality of output lines;
a demultiplexer provided on each output line to supply the data signals to a plurality of data lines;
a first power source line to supply first power through a first side of a plurality of pixel power source lines;
a pixel portion comprising a pixel coupled to the scan line, the data line, and the pixel power source line, the pixel portion being adapted to emit light corresponding to the data signal; and
at least two capacitors formed to have different capacitances corresponding to overlapping areas between the first power source line and the respective data lines, each capacitor being capable of storing voltage corresponding to a data signal and supplying stored voltage to the pixels.

2. The organic light emitting display of claim 1, wherein
the pixel portion includes a red pixel having a red organic light emitting diode, a green pixel having a green organic light emitting diode, and a blue pixel having a blue organic light emitting diode; and the organic light emitting display comprises a first capacitor provided in a data line coupled to the red pixel and being charged to a voltage corresponding to a data signal;
a second capacitor provided in a data line coupled the green pixel and being charged to a voltage corresponding to the data signal; and
a third capacitor provided in a data line coupled the blue pixel and being charged to a voltage corresponding to the data signal,
wherein the first capacitor, the second capacitor, and the third capacitor are different in capacitance from one another.

3. The organic light emitting display according to claim 1, wherein the second capacitor has higher capacitance than the first capacitor, and the third capacitor has lower capacitance than the first capacitor and/or the organic light emitting display further comprises a power source line to supply external first power to the pixel power source line.

4. The organic light emitting display according to claim 3, wherein a first overlapping area between the data line coupled to the red pixel and the power source line, a second overlapping area between the data line coupled to the green pixel and the power source line, and a third overlapping area between the data line coupled to the blue pixel and the power source line are different from one another.

5. The organic light emitting display according to claim 4, wherein the first overlapping area is smaller than the second overlapping area, and larger than the third overlapping area and/or wherein the data line coupled to the red pixel overlaps the power source line by a first width, and the data line coupled to the green pixel overlaps the power source line by a second width wider than the first width and/or wherein the data line coupled to the red pixel overlaps the power source line by a first length, and the data line coupled to the green pixel overlaps the power source line by a second length longer than the first length.

6. The organic light emitting display according to claim 5, wherein the data line coupled to the blue pixel overlaps the power source line by a third length shorter than the first length.

7. The organic light emitting display according to claim 6, wherein the data line coupled to the blue pixel overlaps the power source line by a third width narrower than the first width.

8. The organic light emitting display according to claim 1, wherein the scan driver supplies the scan signal during a first period of one horizontal period, and the data driver supplies the data signals to the output lines during a second period of the one horizontal period excluding the first period.

9. The organic light emitting display according to claim 10, wherein each demultiplexer comprises a plurality of transistors, each transistor being coupled to one of the plurality of data lines.

10. The organic light emitting display according to claim 9, wherein the plurality of transistors are turned on in sequence, and the first capacitor, the second capacitor, and the third capacitor are charged with voltages corresponding to the data signals when the transistors are turned on.

11. The organic light emitting display according to claim 10, wherein the voltages stored in the first capacitor, the second capacitor, and the third capacitor are supplied to the red pixel, the green pixel and the blue pixel for the first period.

12. The organic light emitting display according to one of the preceding claims, further comprising:

a substrate;
a pad part formed on the substrate, the pad part having first pads, second pads, third pads, fourth pads, fifth pads, and sixth pads;

wherein the scan driver is located on one side of the pixel portion and electrically coupled to the first pads and to the scan lines; and the data driver is directly formed on the substrate or embedded as a chip on the substrate and electrically coupled to an auxiliary power source line, to the second pads, and to a first data line;
the first power source line is located adjacent to all sides of the pixel portion along edges of the substrate except where the pad part is located and coupled to the third pads and to the pixel power source lines;
the auxiliary power source line is located on the substrate along an edge where the pad is located and coupled to the fourth pads and to the plurality of pixel power source lines;
a second power source line is formed on the substrate coupled to the fifth pads and to each of the pixels; and
a demultiplexer block is coupled to the first data line, the second data lines, and to the sixth pads.

13. The organic light emitting display of claim 12, wherein the data driver and the demultiplexer block are embedded on a flexible printed circuit coupled to the substrate and wherein the data driver and the demultiplexer block are electrically coupled to the second data lines through the pad part of the substrate.

FIG. 1
(PRIOR ART)

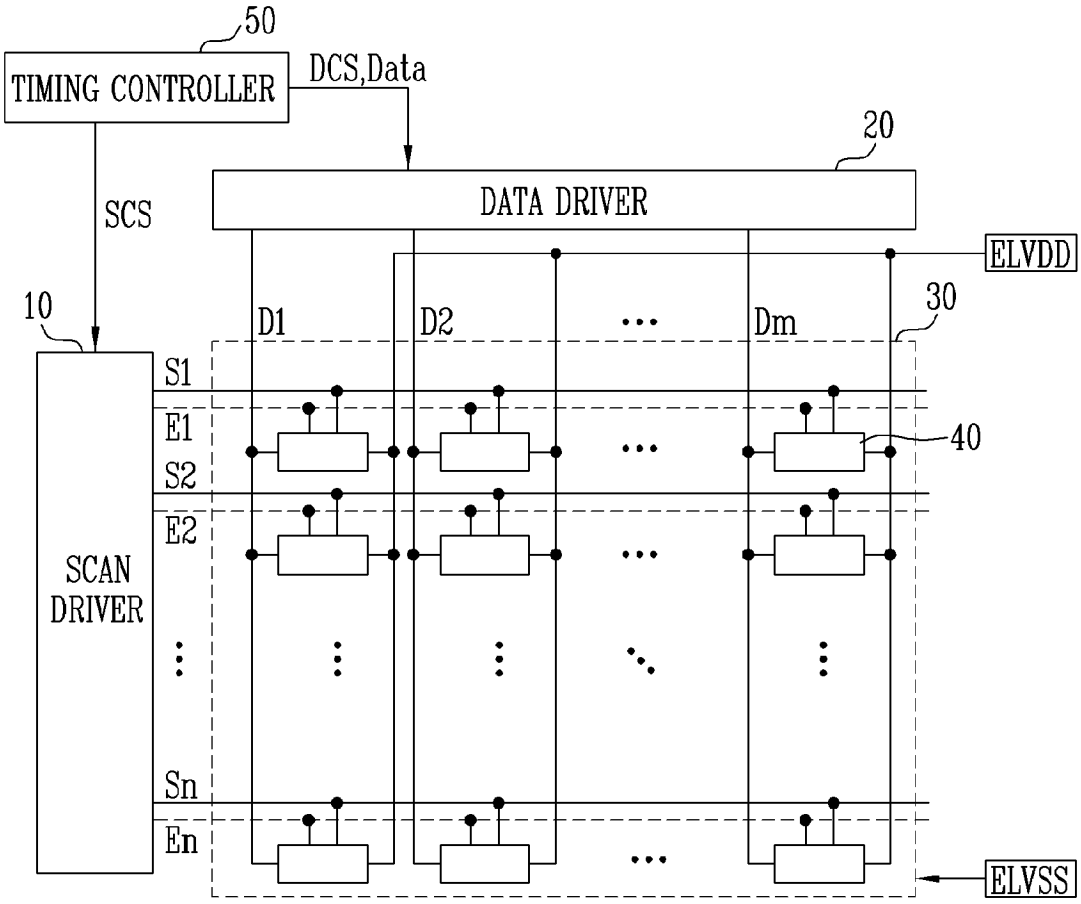


FIG. 2

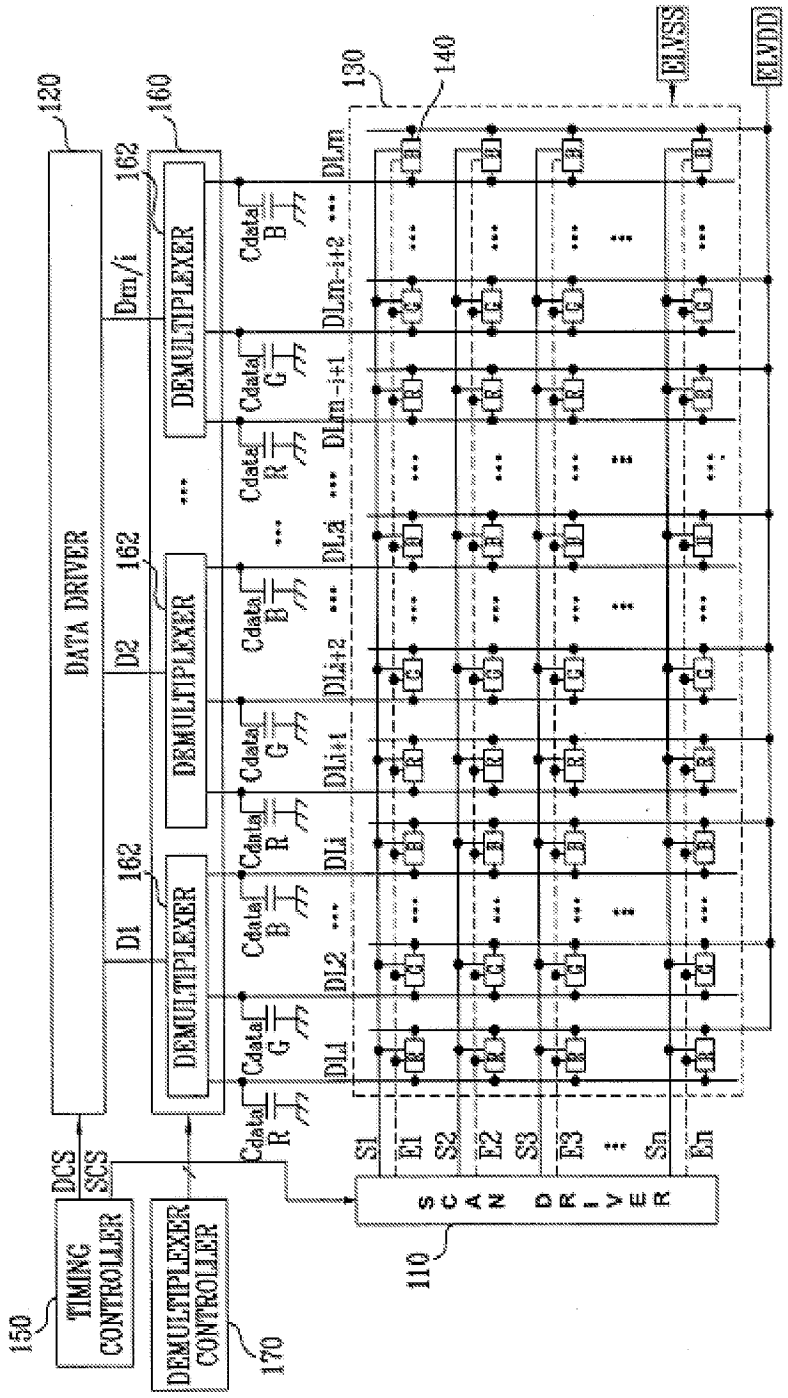

DATA DRIVER
DEMULTIPLEXER
DEMULTIPLEXER CONTROLLER
TIMING CONTROLLER
SCAN DRIVER
ELVSS
ELVDD
DCS
SCS
D1
D2
Dm/i
DL1
DL2
DLi
DLi+1
DLi+2
DLm-i+1
DLm-i+2
DLm
S1
S2
S3
Sn
E1
E2
E3
En
Cdata R
Cdata G
Cdata B
110
120
130
140
150
160
162
170

FIG. 3

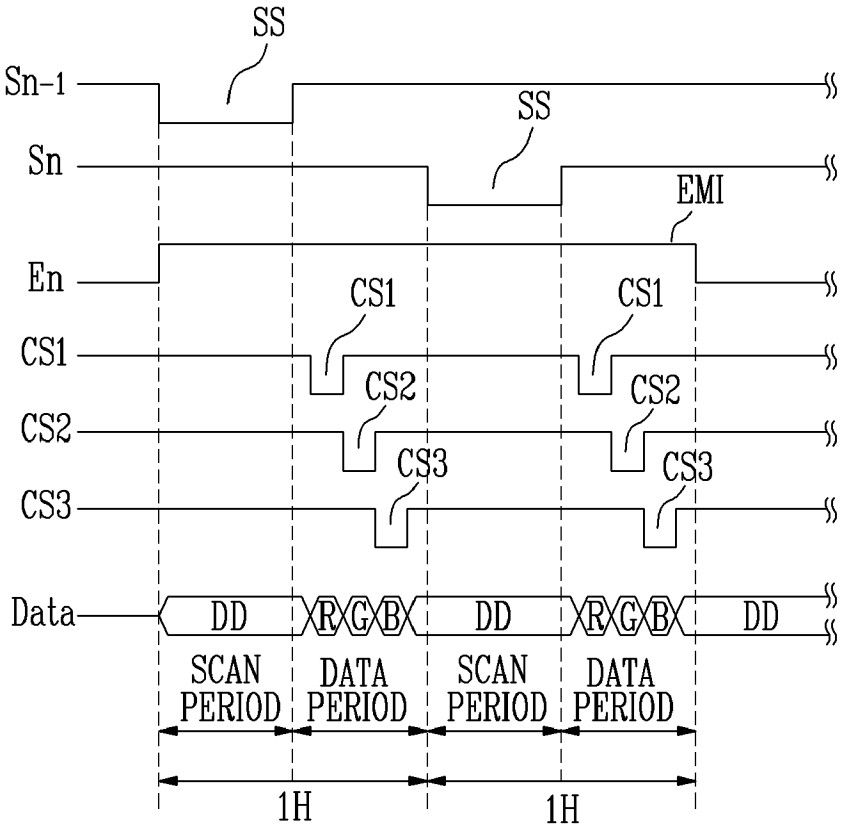

SS
Sn-1
SS
Sn
EMI
En
CS1
CS1
CS1
CS2
CS2
CS2
CS3
CS3
CS3
Data
DD
R
G
B
DD
R
G
B
DD
SCAN PERIOD
DATA PERIOD
SCAN PERIOD
DATA PERIOD
1H
1H

FIG. 4

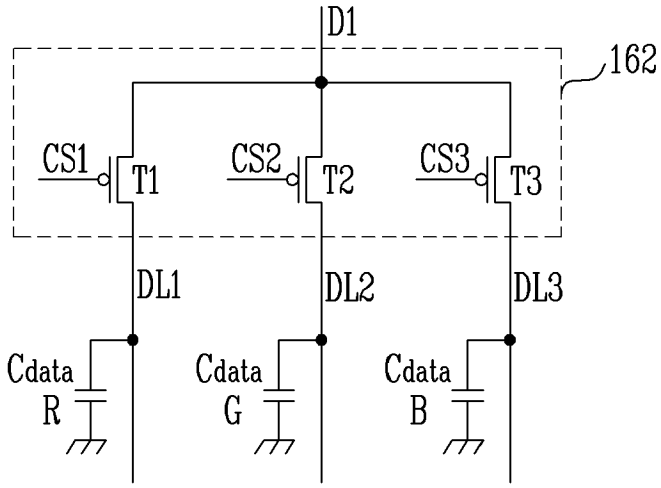

D1
162
CS1
T1
CS2
T2
CS3
T3
DL1
DL2
DL3
Cdata
R
Cdata
G
Cdata
B

FIG. 5

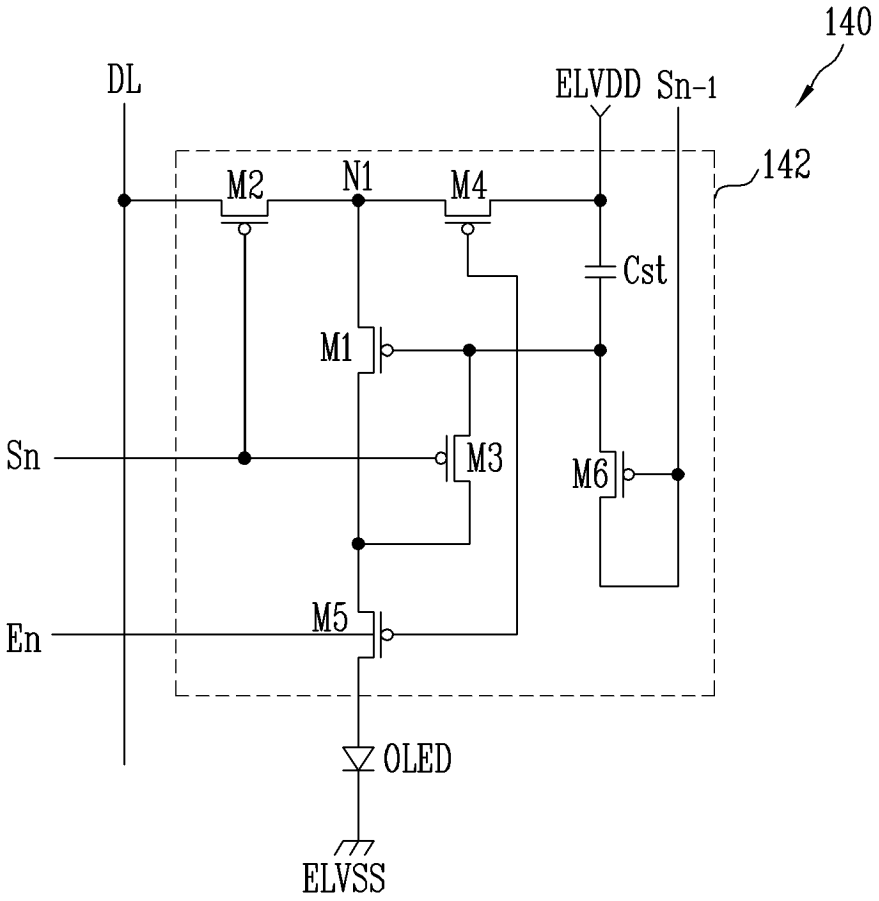


FIG. 6

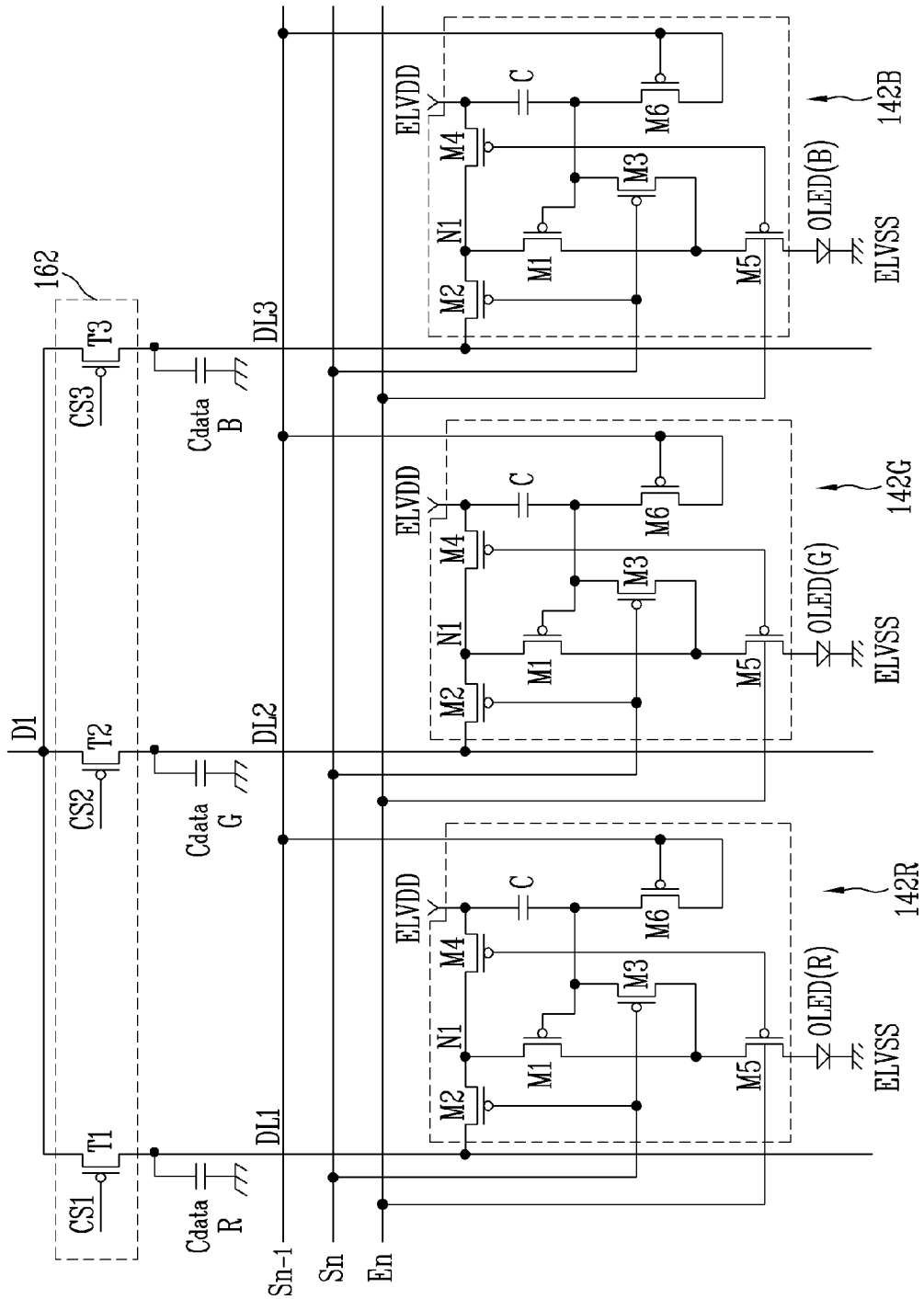

162
D1
CS1
T1
CS2
T2
CS3
T3
Cdata R
Cdata G
Cdata B
DL1
DL2
DL3
Sn-1
Sn
En
ELVDD
C
M1
M2
M3
M4
M5
M6
N1
OLED(R)
OLED(G)
OLED(B)
ELVSS
142R
142G
142B

FIG. 7

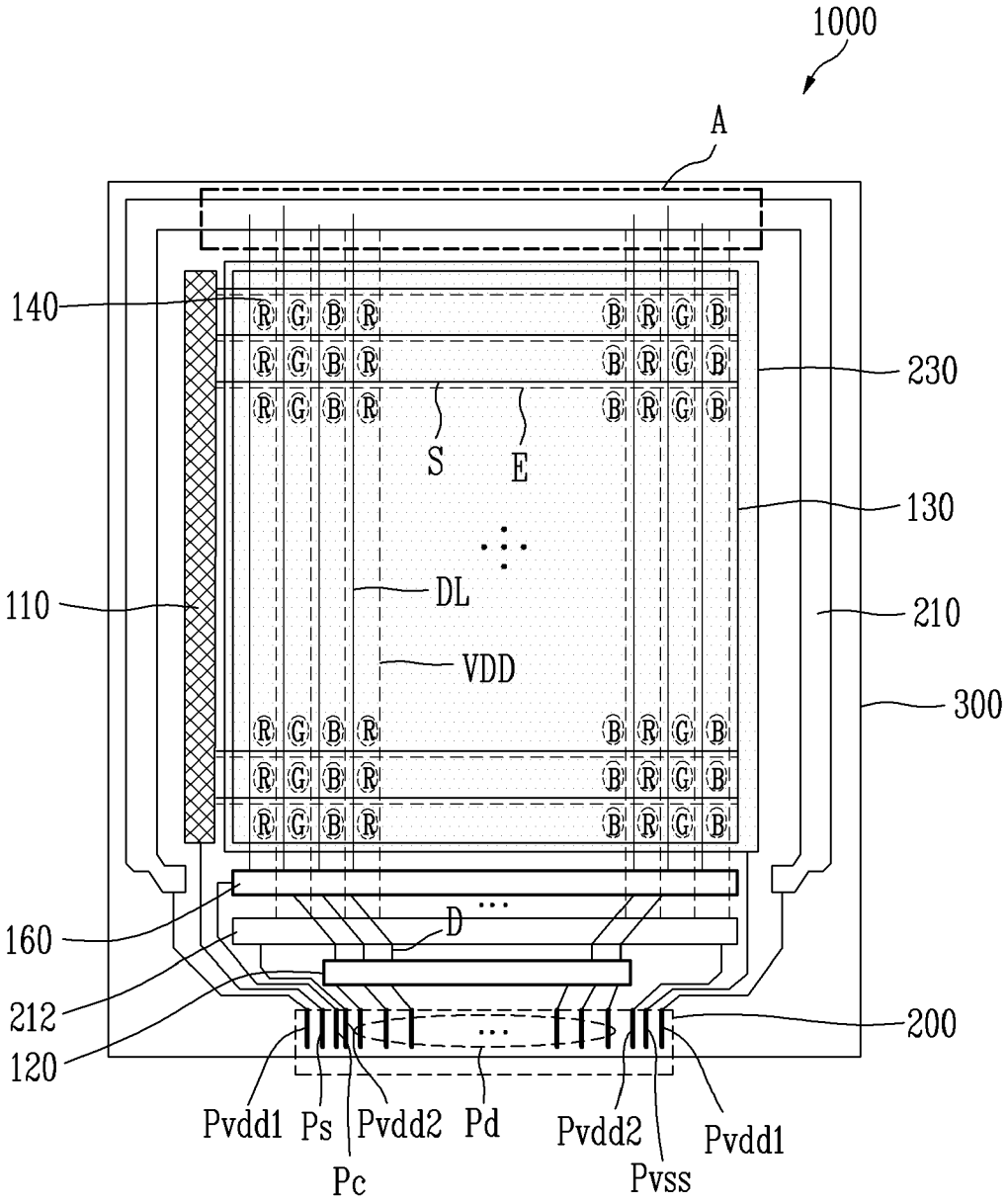

1000
A
140
230
130
110
210
300
160
212
120
200
S
E
DL
VDD
D
Pvdd1
Ps
Pvdd2
Pd
Pvdd2
Pvdd1
Pc
Pvss

FIG. 8

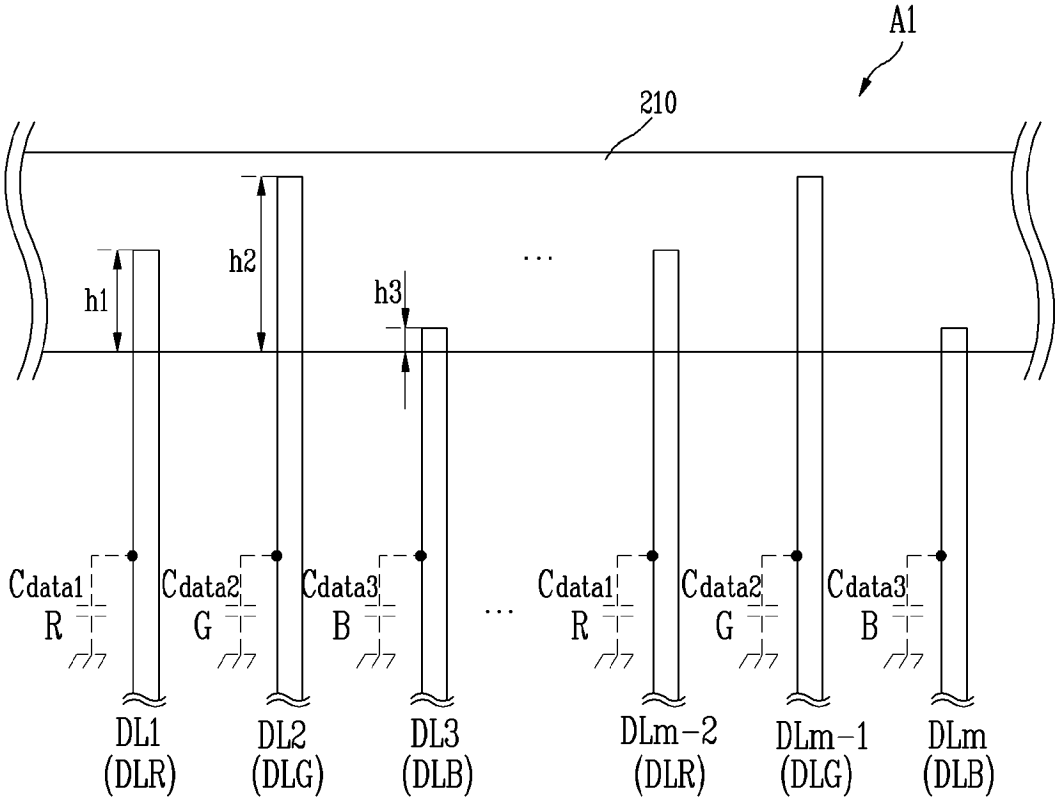

A1
210
h1
h2
h3
Cdata1
R
Cdata2
G
Cdata3
B
DL1
(DLR)
DL2
(DLG)
DL3
(DLB)
DLm-2
(DLR)
DLm-1
(DLG)
DLm
(DLB)

FIG. 9

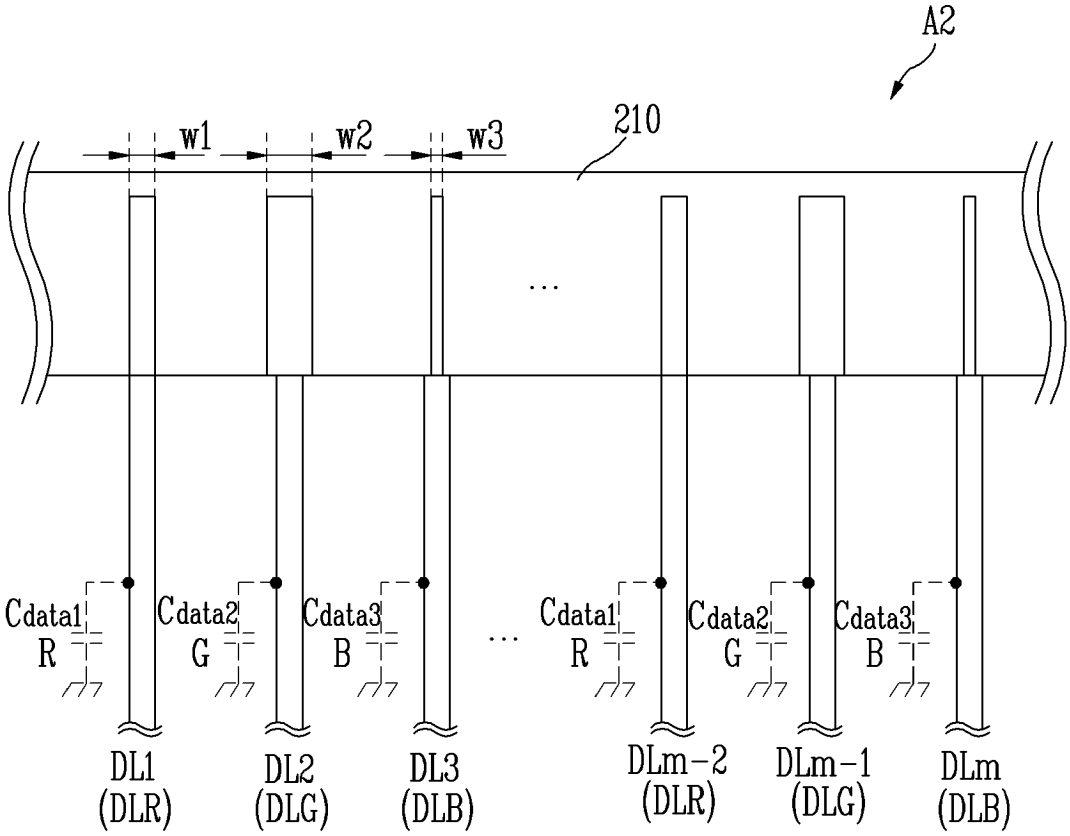

A2
w1
w2
w3
210
Cdata1
R
Cdata2
G
Cdata3
B
Cdata1
R
Cdata2
G
Cdata3
B
DL1
(DLR)
DL2
(DLG)
DL3
(DLB)
DLm-2
(DLR)
DLm-1
(DLG)
DLm
(DLB)

FIG. 10

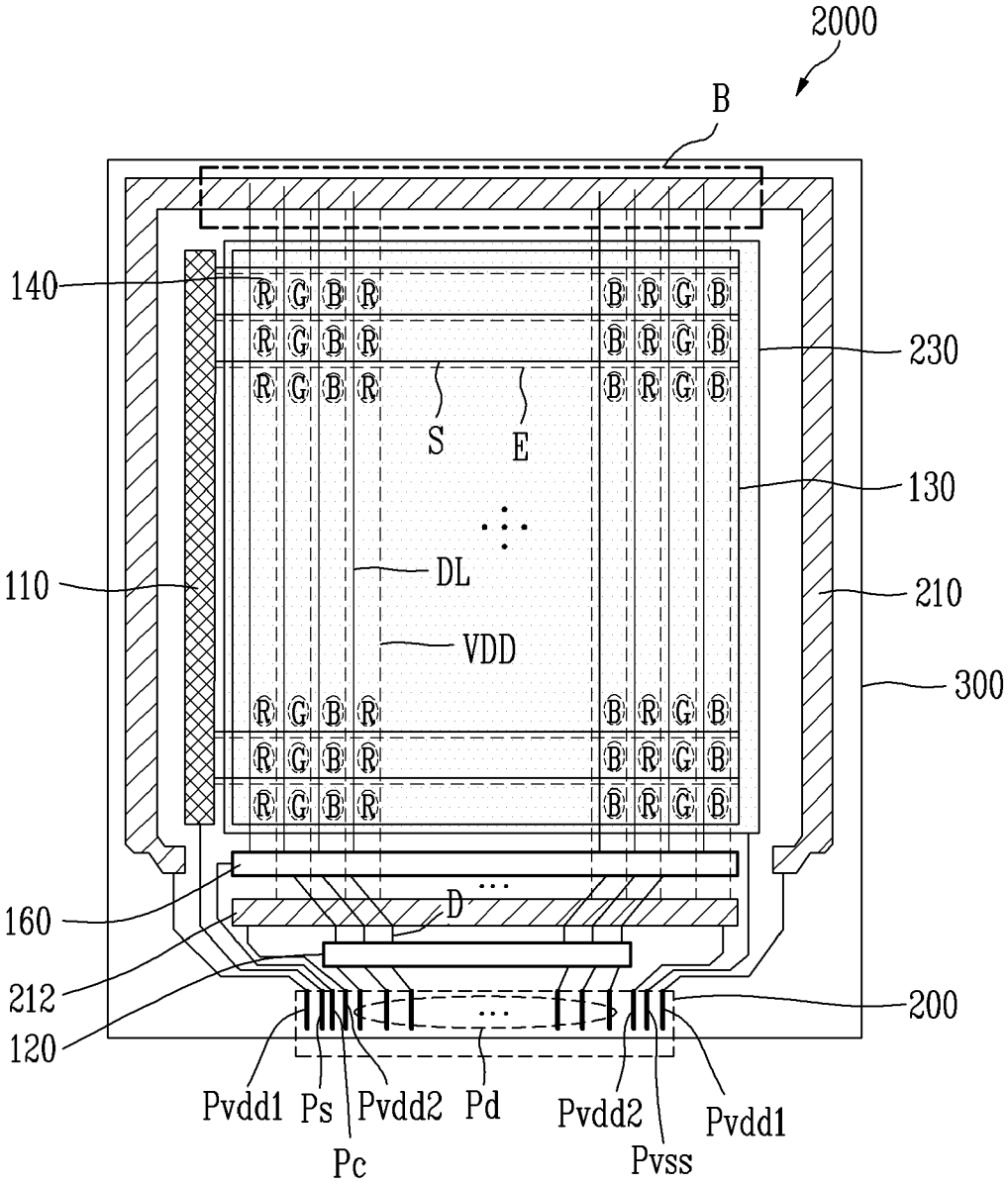

2000
B
140
230
130
110
210
300
160
212
120
200
S
E
DL
VDD
D
Pvdd1
Ps
Pvdd2
Pd
Pvdd2
Pvdd1
Pc
Pvss

FIG. 11

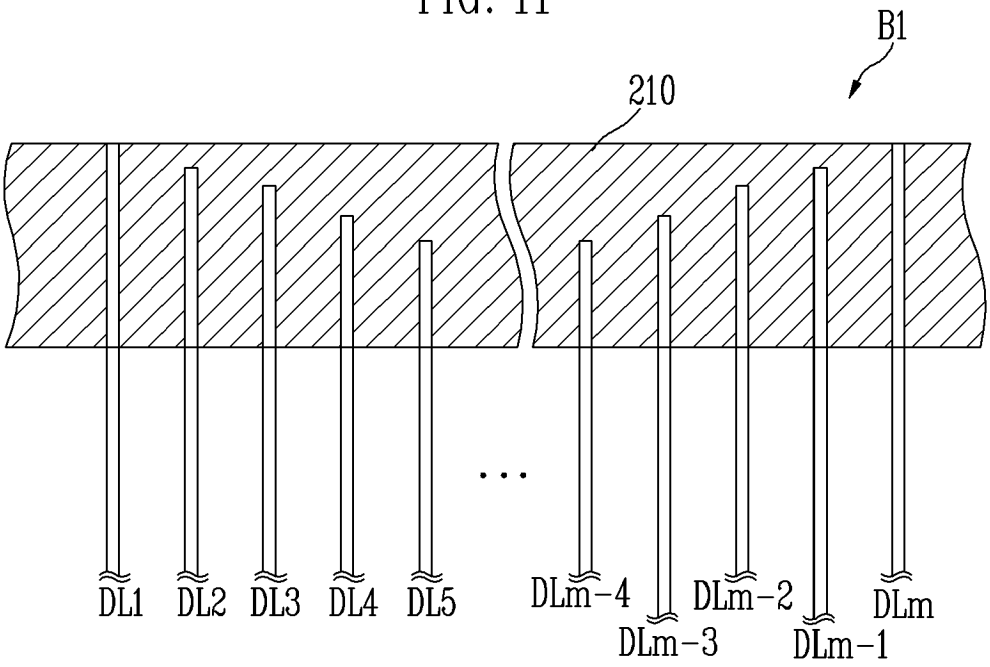

B1
210
DL1
DL2
DL3
DL4
DL5
DLm-4
DLm-3
DLm-2
DLm-1
DLm

FIG. 12

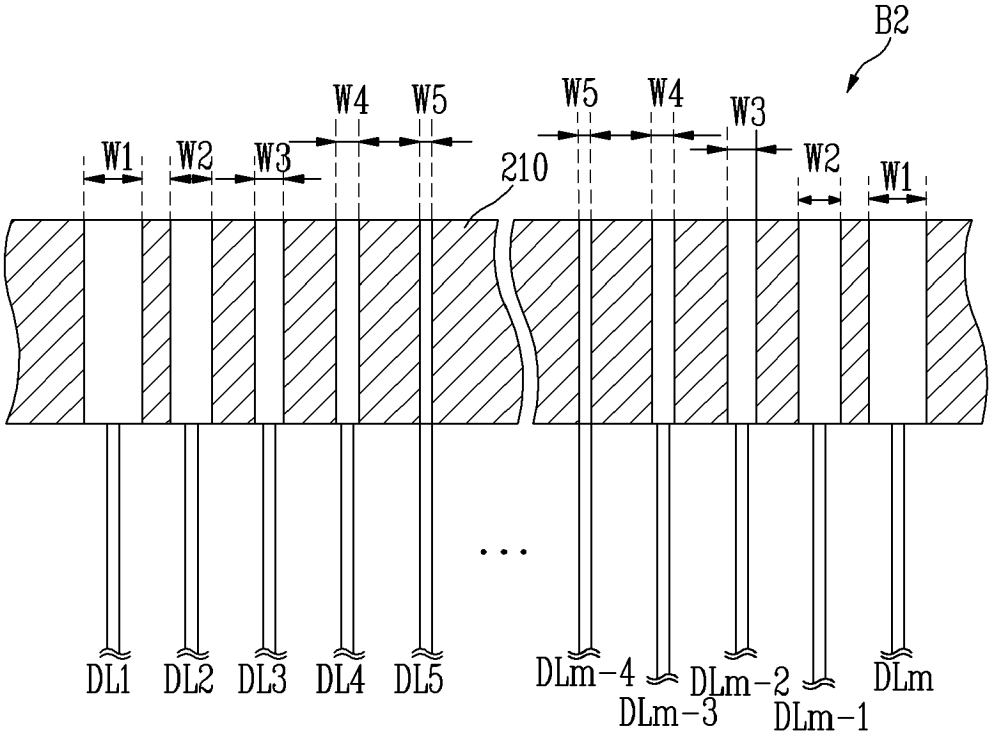

B2
W1
W2
W3
W4
W5
210
DL1
DL2
DL3
DL4
DL5
DLm-4
DLm-3
DLm-2
DLm-1
DLm

FIG. 13

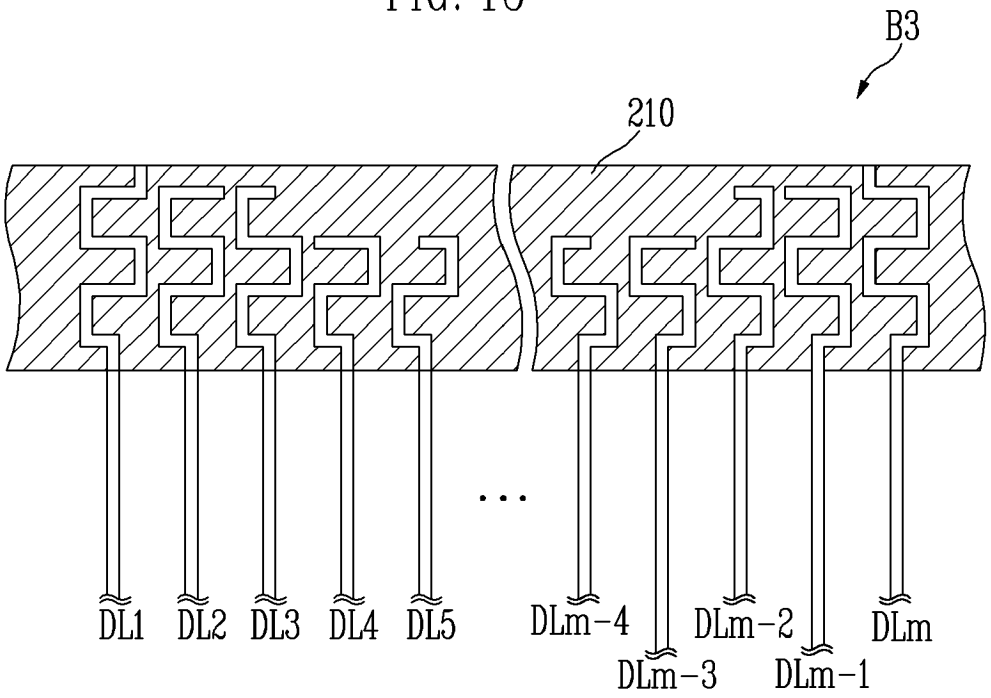
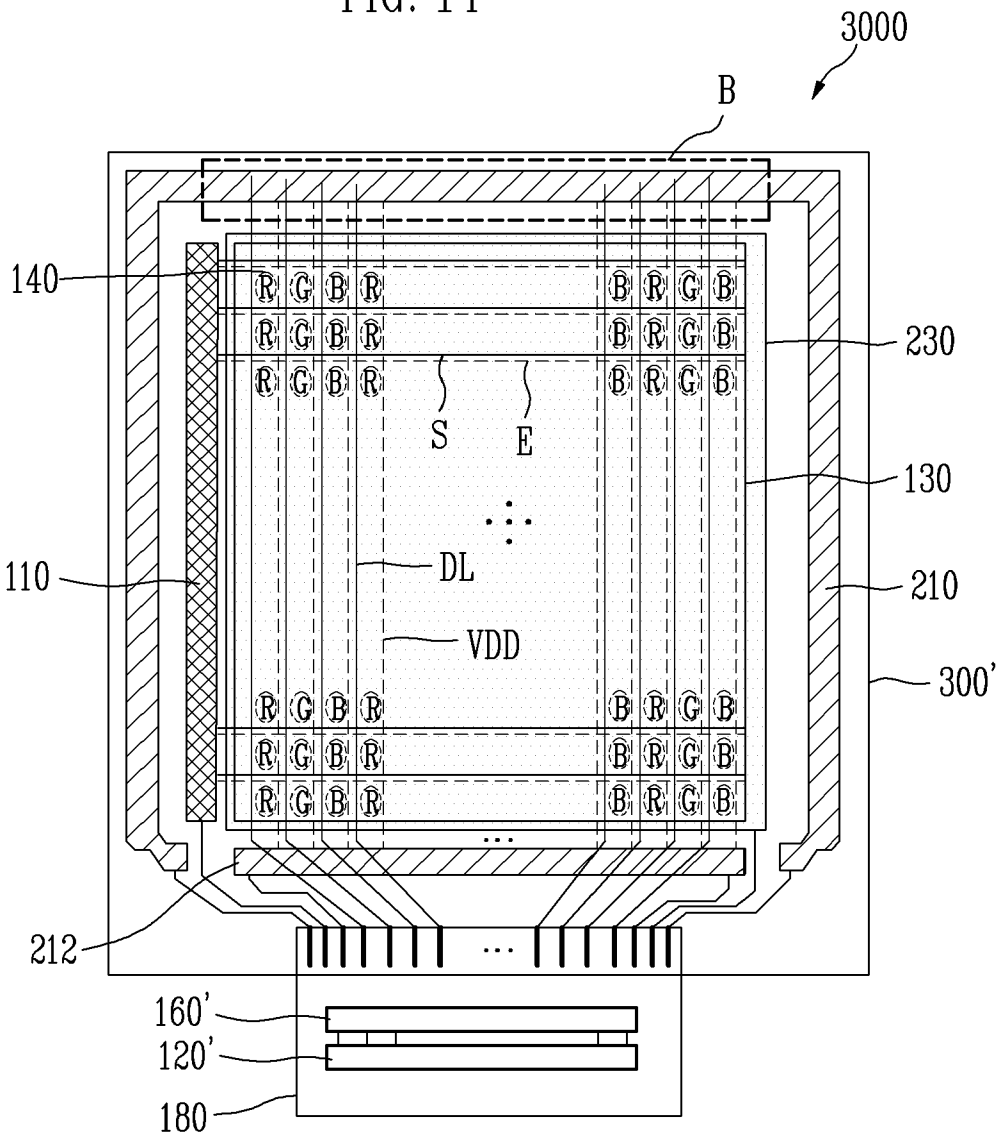


FIG. 14



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 05 10 9386

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	US 6 448 718 B1 (BATTERSBY STEPHEN J) 10 September 2002 (2002-09-10) * column 1, lines 5-7 * * column 6, lines 28-55 * * column 4, lines 50-58 * * column 6, line 56 - column 7, line 38; figure 4 *	1-7,9-13	G09G3/32
Y	US 2003/107537 A1 (OCHI HIDEO ET AL) 12 June 2003 (2003-06-12) * paragraphs [0021], [0022]; figure 4 *	1-7,9-13	
A	EP 1 347 436 A (SAMSUNG SDI CO., LTD) 24 September 2003 (2003-09-24) * paragraph [0013]; figures 4,5 *	1-13	
A	US 2003/059525 A1 (MOON SEONG-HAK) 27 March 2003 (2003-03-27) * paragraphs [0022], [0028]; figures 5,7 *	1-13	
A	US 6 583 577 B1 (CHOI WOONG-SIK ET AL) 24 June 2003 (2003-06-24) * column 3, lines 9-56; figure 4 *	1-13	TECHNICAL FIELDS SEARCHED (IPC) G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	5 December 2005	Kunze, H

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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& : member of the same patent family, corresponding document

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05-12-2005

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	有机发光显示器		
公开(公告)号	EP1647967A1	公开(公告)日	2006-04-19
申请号	EP2005109386	申请日	2005-10-10
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星SDI CO.，LTD.		
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IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G5/02 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2310/0251 G09G2310/0262 G09G2310/0297 G09G2320/0223 G09G2320/0242 G09G2320/043 H01L27/3276		
代理机构(译)	hengelhaupt，Jürgen		
优先权	1020040081812 2004-10-13 KR 1020040081811 2004-10-13 KR		
其他公开文献	EP1647967B1		
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摘要(译)

一种有机发光显示器，包括在每条数据线上的解复用器，其将每个数据信号分离并提供给多条数据线，从而减少所需的输出线的数量并降低生产成本。此外，对应于数据信号的电压在数据电容器中顺序充电，同时将充电电压提供给像素，允许有机发光显示器显示具有均匀亮度的图像。用于提供扫描信号的扫描周期与用于提供数据信号的数据周期不重叠，从而产生稳定的图像。此外，数据电容器的电容根据其相应的有机发光二极管的发光效率来设定，从而保持适当的白平衡。而且，数据电容器的电容被设置为补偿第一电源线中的电压降，从而显示具有均匀亮度的图像。

FIG. 6