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(54) **SRAM core cell for light-emitting display**

SRAM Speicherzelle für eine lichtemittierende Anzeige

Cellule de mémoire SRAM pour un afficheur luminescent

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Description

BACKGROUND OF THE INVENTION

(a) Field of the Invention

[0001] The present invention relates to a static RAM (SRAM) core cell. More specifically, the present invention relates to a SRAM core cell for a light-emitting display, and is applicable to a data driver of an organic electroluminescence (EL) light-emitting display device.

(b) Description of the Related Art

[0002] The organic EL light-emitting display is a device for displaying an image by controlling a current flowing to an organic material that emits light when the current flows to it. In the organic EL light-emitting display, the organic material is divided by pixels and arranged in a matrix form. The organic EL light-emitting display is promising as a next-generation display device because of its advantages such as low-voltage driving requirement, light weight, slim design, wide viewing angle, rapid response, etc.

[0003] FIG. 1 illustrates the principle of light emission of a typical organic EL.

[0004] In general, an organic EL light-emitting display, which is a display device that electrically excites a fluorescent organic compound to emit light, drives N × M organic light-emitting cells by voltage or current to represent an image. The organic light-emitting cell has a structure of FIG. 1 that includes an ITO (Indium Tin Oxide) pixel electrode, an organic thin film, and a metal layer. The organic thin film is a multi-layer structure that includes a light-emitting layer (EML), an electron transport layer (ETL), and a hole transport layer (HTL) to keep electrons and holes in good balance and enhance the light-emitting efficiency. The organic thin film may also include an electron injecting layer (EIL) and a hole injecting layer (HIL).

[0005] There are typically two driving methods for the organic light-emitting cells: the passive matrix method and the active matrix method using TFTs. The passive matrix method involves selectively driving anode and cathode lines arranged orthogonally to each other, while the active matrix method involves coupling TFTs and capacitors to the respective pixel electrodes and sustaining a voltage according to a capacitor capacity.

[0006] FIG. 2 is a schematic block diagram of a typical organic EL display device.

[0007] Referring to FIG. 2, the organic EL display device includes a video controller 210, a panel controller 220, a power module 230, a scan driver 240, a data driver 250, and an organic EL panel 260. The scan driver 240 and the data driver 250 supply various signals to the organic EL panel 260 in the column and row directions via analog and digital interfaces, respectively.

[0008] More specifically, various analog signals such as R, G, and B signals and sync signals are fed into the video controller 210 and converted into digital signals. The panel controller 220 controls the converted digital signals and supplies them to the scan driver 240 and the data driver 250 in sequence. The organic EL panel 260 drives N × M organic light-emitting cells by voltage or current using the signals supplied from the scan driver 240 and the data driver 250, and the power supplied from the power module 230 to represent an image.

[0009] FIG. 3 shows a general active matrix organic EL display panel using TFTs.

[0010] Referring to FIG. 3, the organic EL display device includes an organic EL display panel 310, a data driver 320, and a scan driver 330.

[0011] The organic EL display panel 310 includes m data lines D1, D2, ..., Dm arranged in columns; n scan lines S1, S2, ..., Sn arranged in rows; and n × m pixel circuits. The m data lines D1, D2, ..., Dm transfer data signals representing image signals to the pixel circuits, and the n scan lines S1, S2, ..., Sn transfer selection signals to the pixel circuits. Each pixel circuit is formed in one pixel area 310-1 defined by two adjacent ones of the m data lines D1, D2, ..., Dm, and two adjacent ones of the n scan lines S1, S2, ..., Sn. The pixel circuit includes, for example, transistors 311 and 312, a capacitor 313, and an organic EL diode 314. Here, reference numeral 315 denotes a power voltage Vdd.

[0012] More specifically, each pixel circuit 310-1 includes the organic EL diode (OLED) 314, two transistors 311 and 312, and the capacitor 313. For example, the two transistors 311 and 312 may be PMOS transistors.

[0013] The driving transistor 312 has its source coupled to the power voltage V_{dd}, and the capacitor 313 coupled between its gate and source. The capacitor 313 sustains the gate-source voltage of the driving transistor 312 for a predetermined time period, and the switching transistor 311 transfers a data voltage from the data line Dm to the driving transistor 312 in response to the selection signal from the current scan line Sn.

[0014] The organic EL diode 314 has its cathode coupled to a reference voltage V_{ss}, and emits a light corresponding to a current applied through the driving transistor 312. Here, the power V_{ss} coupled to the cathode of the organic EL diode 314 is lower than the power V_{dd} and can be a ground voltage.

[0015] The scan driver 330 sequentially applies the selection signal to the n scan lines S1, S2, ..., Sn, while the data driver 320 sequentially applies a data voltage corresponding to the image signal to the m data lines D1, D2, ..., Dm.

[0016] The scan driver 330 and/or the data driver 320 may be coupled to the organic EL display panel 310, or mounted as a chip in a tape carrier package (TCP) soldered and coupled to the organic EL display panel 310. Alternatively, the scan driver 330 and/or the data driver 320 may be mounted as a chip in a flexible printed circuit (FPC) or a film soldered and coupled to the display panel 310.

[0017] Moreover, the scan driver 330 and/or the data driver 320 may be directly mounted on a glass substrate of the organic EL display panel 310, or substituted by driver circuitry including the same layers of the scan lines, the data lines, and the TFTs on the glass substrate.

[0018] FIG. 4 is a circuit diagram of a CMOS SRAM core cell according to prior art.

[0019] The CMOS SRAM core cell according to prior art is used with the data driver 320 to implement the organic EL display device as an SOP (System On Package), and is designed as a SRAM having six TFTs. The SRAM stores the data to be displayed on the organic EL panel 260.

[0020] Referring to FIG. 4, symbols "MP1" and "MP2" denote pull-up transistors, symbols "MN1" and "MN2" denote pull-down transistors, and symbols "MP3" and "MP4" denote pass transistors for a data access. Here, MP1 to MP4 are PMOS transistors, and MN1 and MN2 are NMOS transistors. The MP1 and the MN1, and the MP2 and the MN2 are implemented as CMOS transistors and arranged in a latch configuration.

[0021] In the CMOS RAM core cell according to prior art, a plurality of NMOS and PMOS transistors must be formed with a predetermined width and a predetermined length, with a restriction on a design of the layout, allowing no flexibility of design and causing defects in the fabrication process.

[0022] US 4688030 and US 5526303 disclose static RAM core cells according to the prior art. They show six transistor cells having oblique channels and a word line on each side of the cell.

SUMMARY OF THE INVENTION

[0023] In one embodiment, the present invention is a SRAM core cell as claimed in claim 1 for a light-emitting display that has an enhanced integration level of a defined layout space by forming the gate channel of a thin film transistor (TFT) constituting the SRAM core cell in an oblique direction.

[0024] In one embodiment, the present invention is a SRAM core cell for a light-emitting display that secures a process margin to prevent defects in the fabrication process by enhancing the efficiency of a defined layout space.

[0025] Here, the oblique direction is a clockwise direction or a counterclockwise direction with respect to the first or second direction.

[0026] The switching transistors or the data memory transistors arranged in an oblique direction include a polysilicon layer deposited in an oblique direction on a substrate.

[0027] The channels of the transistors formed on the active region and arranged in an oblique direction are preferably arranged in sequence. The transistors arranged in an oblique direction on the active region include a polysilicon layer deposited in an oblique direction with respect to a vertical direction on the substrate.

[0028] In one embodiment, the present invention arranges transistors in sequence so as to form a polysilicon layer or channels forming the transistors in an oblique direction in a defined region in designing a SRAM for a data driver of a light-emitting display, thereby enhancing the layout efficiency of the core cell and implementing a light-emitting display device of a high integration level.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention, and, together with the description, serve to explain the principles of the invention.

[0030] FIG. 1 illustrates the principle of light emission of an organic EL display device.

[0031] FIG. 2 is a schematic block diagram of an organic EL display device.

[0032] FIG. 3 shows a general active matrix organic EL display panel using TFTs.

[0033] FIG. 4 is a circuit diagram of a CMOS SRAM core cell for an EL display device.

[0034] FIG. 5 shows a layout of a CMOS RAM core cell for a light-emitting display according to an embodiment of the present invention.

[0035] FIG. 6 is a circuit diagram showing the layout part taken in an oblique direction in the CMOS RAM core cell shown of FIG. 5.

[0036] FIG. 7 is a diagram specifically showing the layout taken in an oblique direction in the CMOS RAM core cell according to an embodiment of the present invention in an oblique direction.

DETAILED DESCRIPTION

[0037] Hereinafter, a SRAM core cell for a light-emitting display according to an embodiment of the present invention will be described in detail with reference to the accompanying drawings.

[0038] Referring to FIG. 4, a SRAM core cell includes two flip-flop circuits for memory (e.g., MP1 and MN1, and MP2 and MN2), and two switches (e.g., MP3 and MP4). By applying pulses to word lines to turn a cell transistor on, data transfer is activated between a bit line pair ("Bit" and "Bitb") and flip-flops. When writing data, a high voltage is applied to one side of the bit line pair, a low voltage being applied to the other side. This is transferred to a memory node (a common source/drain node of MP1 and NM1, and a common source/drain node of MP2 and MN2) to memorize binary information. When reading data, a voltage sustained at the bit line pair is detected in correspondence to the voltage of nodes and transferred to the exterior. Unlike the DRAM, the SRAM stores data without a refresh operation, i.e., statically by the flip-flop feedback, as long as the power is on. However, the SRAM is relatively expensive because a large number of elements are used to construct one cell, with a memory capacity

being about 1/4 of the DRAM with the same area.

[0039] FIG. 5 shows a layout of a CMOS RAM core cell for light-emitting display according to an embodiment of the present invention.

[0040] Referring to FIG. 5, the CMOS RAM core cell for a light-emitting display according to an embodiment of the present invention is a data memory device for the data driver of a light-emitting device that includes six thin film transistors (MP1 to MP4, and MN1 and MN2) each having a gate, a source, and a drain. In the figure, reference numerals 511 to 520 denote contact holes respectively. Also, reference numeral 532 denotes a metal line coupled to a power voltage VDD, reference numeral 531 denotes a metal line coupled to a ground voltage VSS, reference numerals 534 and 535 denote a pair of bit lines, and reference numeral 533 denotes a word line. Also, reference numerals 541 to 544 denote metal lines, and reference numerals 551 and 554 denote poly lines, respectively.

[0041] Among the six thin film transistors (MP1 to MP4, and MN1 and MN2), the first switching transistor MP3 has a gate coupled to a word line 533, and a source/drain coupled to the first bit line 534 to select an input to the first bit line 534 according to the input signal of the word line 533.

[0042] For example, the word line 533 has a role in a gate poly of the first switching transistor MP3, and a metal line across the contact hole 517 and the contact hole 515 has a role in the source/drain of the first switching transistor MP3. The layouts of the five transistors (MP1, MP2, MP4, MN1 and MN2) are formed in the same manner.

[0043] The second switching transistor MP4 has a gate coupled to the word line 533, and a source/drain coupled to a second bit line 535, so as to select an input to the second bit line 535 according to the input signal to the word line 533.

[0044] The first to fourth data memory transistors (MP1 and MN1, and MP2 and MN2) that form a flip-flop as described above are coupled to a power voltage (VDD) or a ground voltage (VSS), so as to enable reading or writing of data under the control of the first and second switching transistors MP3 and MP4.

[0045] As illustrated in the figure, the channels of the first and second switching transistors MP3 and MP4, or the first to fourth data memory transistors (MP1 and MN1, and MP2 and MN2) are formed in an oblique direction. When the direction of the bit lines is a first direction, and that of the word line is a second direction, the channels of the switching transistors and the data memory transistors are formed in an oblique direction with respect to the first and second directions, respectively. The oblique direction may be a clockwise direction or a counterclockwise direction with respect to the first or second direction. In addition, the first and second switching transistors MP3 and MP4, or the first to fourth data memory transistors (MP1 and MN1, and MP2 and MN2) may be arranged in sequence at the same angle on a defined layout space.

[0046] FIG. 6 is a circuit diagram showing the layout part taken in an oblique direction in the CMOS RAM core cell of FIG. 5.

[0047] The SRAM core cell for a light-emitting display according to an embodiment of the present invention includes a plurality of thin film transistors each having a gate, a source, and a drain. The thin film transistors include four PMOS transistors 611 to 614, and two NMOS transistors 621 and 622, so as to enable writing or reading of data under the control of bit lines and word lines. As described previously, among the six transistors, MP1 and MP2 611 and 612 are pull-up transistors, MN1 and MN2 621 and 622 are pull-down transistors, and MP3 and MP4 613 and 614 are switching transistors for an access. Here, the MP1 to MP4 611 to 614 are PMOS transistors, and the MN1 and MN2 621 and 622 are NMOS transistors. In one embodiment, these transistors are arranged in sequence at an angle of 45° on a defined layout space.

[0048] FIG. 7 is a diagram specifically showing the layout taken in an oblique direction in the CMOS RAM core cell according to one embodiment of the present invention.

[0049] The CMOS SRAM core cell, according to the embodiment of the present invention as shown in FIG. 7, has a defined layout of 22 μm $\times$ 20 μm (22 μm in width and 20 μm in length) and includes six thin film transistors as stated above.

[0050] In the figure, reference numeral 532 denotes a metal line coupled to a power voltage VDD, reference numeral 531 denotes a metal line coupled to a ground voltage VSS, reference numerals 534 and 535 denote a pair of bit lines, and reference numeral 533 denotes a word line.

[0051] Referring to FIG. 7, the CMOS RAM core cell includes six transistors, i.e., four PMOS transistors 611 to 614 and two NMOS transistors 621 and 622, and its data write/read is under the control of the bit line pair and the word line. As stated above, the six transistors are arranged in sequence, for example, at an angle of 45° on a defined layout space.

[0052] The switching transistors or the data memory transistors arranged in an oblique direction may include a polysilicon layer deposited in an oblique direction on a substrate. Namely, an active region is formed on a polysilicon layer deposited in an oblique direction, and a gate, a source, and a drain are formed in the active region for the above-stated oblique arrangement of the channels.

[0053] Furthermore, a semiconductor device having a plurality of transistors formed in an oblique direction on a layout space of a predetermined area can also be implemented according to an embodiment of the present invention. The semiconductor includes a plurality of transistors each having a gate and a source/drain formed on a substrate or on an active region deposited on the substrate. The channels of the transistors on the active region are arranged in an oblique direction on the layout space of a predetermined area. Here, the channels of the transistors formed in an oblique direction on the active region are arranged in sequence and include a polysili-

con layer deposited in an oblique direction with respect to the vertical direction on the substrate.

[0054] Consequently, the CMOS SRAM core cell for a light-emitting display according to the embodiments of the present invention can have enhanced integration efficiency by forming the channels or the polysilicon layer in an oblique direction.

[0055] While this invention has been described in connection with what is presently considered to be the most practical and exemplary embodiment, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

[0056] As described above, the present invention arranges transistors in sequence so as to form a polysilicon layer or channels forming the transistors in an oblique direction in a defined region in designing a SRAM for a data driver of a light-emitting display, thereby enhancing the layout efficiency of the core cell and implementing a light-emitting display device of a high integration level.

Claims

1. A static RAM (SRAM) core cell for a light-emitting display including a plurality of thin film transistors (MN1, MN2, MP1, MP2, MP3, MP4) each having a gate, a source and a drain as a data memory for a data driver of the light-emitting display, the SRAM core cell comprising:

a bit line (Bit, BitB);
a word line (Word);
a switching transistor (MP3, MP4) coupled to the bit line and the word line, to select writing or reading of data; and
a data memory transistor (MN1, MP1, MN2, MP2) coupled to a power voltage Vdd or a ground voltage Vss, to enable writing or reading of data,
wherein the bit line and the word line being formed in first and second directions, respectively, and
wherein channels of the switching transistor and the data memory transistor being formed in an oblique direction with respect to the first and second directions, respectively;
characterized in that said word line consists of a single word line in the static RAM core cell.

2. The SRAM core cell as claimed in claim 1, wherein the oblique direction is one or more of the group consisting of a clockwise direction and a counterclockwise direction, with respect to the first or second direction.

3. The SRAM core cell as claimed in claim 1, wherein the switching transistor or the data memory transistor is arranged in sequence on a defined layout space.

4. The SRAM core cell as claimed in claim 1, wherein the switching transistor or the data memory transistor arranged in an oblique direction includes a polysilicon layer deposited in an oblique direction on a substrate.

5. A static RAM (SRAM) core cell as claimed in claim 1 further comprising:

a first thin film switching transistor having a gate coupled to the word line, and a source/drain coupled to a first bit line, to select an input to the first bit line according to an input signal to the word line;
a second thin film switching transistor having a gate coupled to the word line, and a source/drain coupled to a second bit line, to select an input to the second bit line according to an input signal to the word line; and
four thin film data memory transistors coupled to a power voltage or a ground voltage, to enable writing or reading of data under the control of the first and second switching transistors,
wherein the bit lines and the word line being formed in first and second directions, respectively, and
wherein channels of the first and second switching transistors and the four data memory transistors being formed in an oblique direction with respect to the first and second directions, respectively.

6. The SRAM core cell as claimed in claim 5, wherein the first and second switching transistors and the four data memory transistors are arranged in sequence on a layout space of a predetermined area.

7. The SRAM core cell as claimed in claim 5, wherein each of the transistors arranged in an oblique direction include a polysilicon layer deposited in an oblique direction on a substrate.

8. A semiconductor device comprising:

a static RAM core cell as claimed in claim 1;
a substrate including said bit line and said single word line formed in first and second directions, respectively; and
a said plurality of transistors each having a gate and a source/drain formed on an active region deposited on the substrate,
wherein channels of the transistors formed on the active region being formed in an oblique direction with respect to the first and second directions.

9. The semiconductor device as claimed in claim 8, wherein the oblique direction is one or more of the group consisting of a clockwise direction and a counterclockwise direction with respect to the first and second directions.

10. The semiconductor device as claimed in claim 8, wherein each of the transistors arranged in an oblique direction on the active region include a polysilicon layer deposited in an oblique direction with respect to the first and second directions.

11. The semiconductor device as claimed in claim 8, further comprising a line driver and a scan driver for controlling an organic EL panel.

12. The semiconductor device as claimed in claim 11, further comprising a video controller and a panel controller for controlling the line driver and the scan driver.

13. A light emitting display driver comprising:

a static RAM according to claim 5;
an organic EL panel; and
a line driver and a scan driver for controlling the organic EL panel.

14. The light emitting display driver as claimed in claim 13, further comprising a video controller and a panel controller for controlling the line driver and the scan driver.

Patentansprüche

1. Statische RAM (SRAM)-Speicherzelle für eine lichtemittierende Anzeige, aufweisend eine Vielzahl von Dünnfilmtransistoren (MN1, MN2, MP1, MP2, MP3, MP4), von denen jeder ein Gate, eine Source und ein Drain als Datenspeicher für einen Datentreiber der lichtemittierenden Anzeige aufweist, wobei die SRAM-Speicherzelle aufweist:

eine Bitleitung (Bit, BitB);
eine Wortleitung (Word);
einen Schalttransistor (MP3, MP4), der an die Bitleitung und die Wortleitung gekoppelt ist, so dass das Schreiben oder Lesen von Daten ausgewählt wird; und
einen Datenspeichertransistor (MN1, MP1, MN2, MP2), der an eine Versorgungsspannung Vdd oder ein Massepotential Vss gekoppelt ist, so dass das Schreiben oder Lesen von Daten ermöglicht wird,
wobei die Bitleitung und die Wortleitung jeweils in eine erste und zweite Richtung ausgebildet sind, und
wobei Kanäle des Schalttransistors und des Datenspeichertransistors jeweils in eine schräge Richtung bezüglich der ersten und zweiten Richtung ausgebildet sind;
dadurch gekennzeichnet, dass die besagte Wortleitung aus einer einzelnen Wortleitung in der statischen RAM-Speicherzelle besteht.

2. SRAM-Speicherzelle nach Anspruch 1, wobei die schräge Richtung eine oder mehrere aus der Gruppe bestehend aus einer Richtung im Uhrzeigersinn und einer Richtung gegen den Uhrzeigersinn bezüglich der ersten oder zweiten Richtung ist.

3. SRAM-Speicherzelle nach Anspruch 1, wobei der Schalttransistor oder der Datenspeichertransistor aufeinanderfolgend in einem definierten Anordnungsfreiraum angeordnet ist.

4. SRAM-Speicherzelle nach Anspruch 1, wobei der in eine schräge Richtung angeordnete Schalttransistor oder Datenspeichertransistor eine Polysiliziumschicht aufweist, die in eine schräge Richtung auf einem Substrat abgeschieden wird.

5. Statische RAM (SRAM)-Speicherzelle nach Anspruch 1, weiterhin aufweisend:

einen ersten Dünnfilm-Schalttransistor, der ein an die Wortleitung gekoppeltes Gate und ein(e) an eine erste Bitleitung gekoppelte(s) Source/Drain aufweist, so dass ein Eingang in die erste Bitleitung gemäß einem Eingangssignal in die Wortleitung ausgewählt wird;
einen zweiten Dünnfilm-Schalttransistor, der ein an die Wortleitung gekoppeltes Gate und ein(e) an eine zweite Bitleitung gekoppelte(s) Source/Drain aufweist, so dass ein Eingang in die zweite Bitleitung gemäß einem Eingangssignal in die Wortleitung ausgewählt wird; und
vier Dünnfilm-Datenspeichertransistoren, die an eine Versorgungsspannung oder ein Massepotential gekoppelt sind, so dass das Schreiben oder Lesen von Daten unter der Steuerung des ersten und zweiten Schalttransistors ermöglicht wird,
wobei die Bitleitungen und die Wortleitung jeweils in eine erste und zweite Richtung ausgebildet sind, und
wobei Kanäle des ersten und zweiten Schalttransistors und der vier Datenspeichertransistoren jeweils in eine schräge Richtung bezüglich der ersten und zweiten Richtung ausgebildet sind.

6. SRAM-Speicherzelle nach Anspruch 5, wobei der erste und zweite Schalttransistor und die vier Datenspeichertransistoren aufeinanderfolgend in einem

Anordnungsfreiraum eines vorbestimmten Bereichs angeordnet sind.

7. SRAM-Speicherzelle nach Anspruch 5, wobei jeder der in eine schräge Richtung angeordneten Transistoren eine Polysiliziumschicht aufweist, die in einer schrägen Richtung auf einem Substrat angeordnet ist.

8. Halbleitervorrichtung, aufweisend:

eine statische RAM-Speicherzelle nach Anspruch 1;
ein Substrat, das die besagte Bitleitung und die besagte einzelne Wortleitung aufweist, die jeweils in eine erste und zweite Richtung ausgebildet sind; und
die besagte Vielzahl von Transistoren, von denen jeder ein Gate und ein(e) Source/Drain aufweist, die in einer auf dem Substrat abgeschiedenen aktiven Region ausgebildet sind,
wobei Kanäle der Transistoren, die in der aktiven Region ausgebildet sind, in eine schräge Richtung bezüglich der ersten und zweiten Richtung ausgebildet sind.

9. Halbleitervorrichtung nach Anspruch 8, wobei die schräge Richtung eine oder mehrere aus der Gruppe bestehend aus einer Richtung im Uhrzeigersinn und einer Richtung gegen den Uhrzeigersinn bezüglich der ersten und zweiten Richtung ist.

10. Halbleitervorrichtung nach Anspruch 8, wobei jeder der in eine schräge Richtung angeordneten Transistoren in der aktiven Region eine Polysiliziumschicht aufweist, die in eine schräge Richtung bezüglich der ersten und zweiten Richtung ausgebildet ist.

11. Halbleitervorrichtung nach Anspruch 8, weiterhin aufweisend einen Leitungstreiber und einen Ansteuertreiber zur Steuerung eines organischen elektrolumineszenten Panels.

12. Halbleitervorrichtung nach Anspruch 11, weiterhin aufweisend eine Videosteuervorrichtung und eine Panelsteuervorrichtung zur Steuerung des Leitungstreibers und des Ansteuertreibers.

13. Treiber einer lichtemittierenden Anzeige, aufweisend:

ein statisches RAM nach Anspruch 5;
ein organisches elektrolumineszentes Panel; und
einen Leitungstreiber und einen Ansteuertreiber zur Steuerung des organischen elektrolumineszenten Panels.

14. Treiber einer lichtemittierenden Anzeige nach Anspruch 13, weiterhin aufweisend eine Videosteuerungsvorrichtung und eine Panelsteuerungsvorrichtung zur Steuerung des Leitungstreibers und des Ansteuertreibers.

Revendications

1. Cellule de coeur de mémoire vive (RAM pour "Random Access Memory") statique (SRAM pour "Static RAM") pour un écran à émission de lumière incluant une pluralité de transistors (MN1, MN2, MP1, MP2, MP3, MP4) à couches minces ayant chacun une grille, une source et un drain en tant que mémoire de donnée pour un circuit d'attaque de données de l'écran à émission de lumière, la cellule de coeur de SRAM comprenant :

une ligne de bit (Bit, BitB) ;
une ligne de mot (Word) ;
un transistor (MP3, MP4) de commutation raccordé à la ligne de bit et à la ligne de mot, pour choisir d'écrire ou de lire une donnée ;
un transistor (MN1, MP1, MN2, MP2) de mémoire de donnée raccordé à une tension Vdd d'alimentation et à une tension Vss de masse, pour permettre l'écriture ou la lecture d'une donnée, dans laquelle la ligne de bit et la ligne de mot sont formées respectivement dans des première et seconde directions, et
dans laquelle les canaux du transistor de commutation et du transistor de mémoire de donnée sont formés dans une direction oblique par rapport aux première et seconde directions, respectivement ;
caractérisée en ce que ladite ligne de mot est constituée d'une unique ligne de mot dans la cellule de coeur de RAM statique.

2. Cellule de coeur de SRAM selon la revendication 1, dans laquelle la direction oblique est une ou plusieurs du groupe constitué d'une direction dans le sens des aiguilles d'une montre et d'une direction dans le sens contraire des aiguilles d'une montre, par rapport à la première ou à la seconde direction.

3. Cellule de coeur de SRAM selon la revendication 1, dans laquelle le transistor de commutation ou le transistor de mémoire de donnée est agencé en séquence sur un espace défini d'implantation.

4. Cellule de coeur de SRAM selon la revendication 1, dans laquelle le transistor de commutation ou le transistor de mémoire de donnée agencé dans une direction oblique inclut une couche de silicium polycristallin déposée dans une direction oblique sur un substrat.

5. Cellule de coeur de RAM statique (SRAM) selon la revendication 1, comprenant en outre :

un premier transistor de commutation à couches minces ayant une grille raccordée à la ligne de mot, et une source/drain raccordée à une première ligne de bit, pour choisir une entrée sur la première ligne de bit en fonction d'un signal d'entrée sur la ligne de mot ;
un second transistor de commutation à couches minces ayant une grille raccordée à la ligne de mot, et une source/drain raccordée à une seconde ligne de bit, pour choisir une entrée sur la seconde ligne de bit en fonction d'un signal d'entrée sur la ligne de mot ; et
quatre transistors de mémoire de donnée à couches minces raccordés à une tension d'alimentation ou à une tension de masse, pour permettre l'écriture ou la lecture de données sur ordre des premier et second transistors de commutation,
dans laquelle les lignes de bit et la ligne de mot sont formées respectivement dans des première et seconde directions, et
dans laquelle les canaux des premier et second transistors de commutation et des quatre transistors de mémoire de donnée sont formés dans une direction oblique par rapport aux première et seconde directions, respectivement.

6. Cellule de coeur de SRAM selon la revendication 5, dans laquelle les premier et second transistors de commutation et les quatre transistors de mémoire de donnée sont agencés en séquence sur un espace d'implantation d'une surface prédéterminée.

7. Cellule de coeur de SRAM selon la revendication 5, dans laquelle chacun des transistors agencés dans une direction oblique inclut une couche de silicium polycristallin déposée dans une direction oblique sur un substrat.

8. Dispositif à semi-conducteurs comprenant :

une cellule de coeur de RAM statique selon la revendication 1 ;
un substrat incluant ladite ligne de bit et ladite unique ligne de mot formées respectivement dans des première et seconde directions ; et
ladite pluralité de transistors ayant chacun une grille et une source/drain formée sur une région active déposée sur le substrat,
dans lequel les canaux des transistors formés sur la région active sont formés dans une direction oblique par rapport aux première et seconde directions.

9. Dispositif à semi-conducteurs selon la revendication 8, dans lequel la direction oblique est une ou plusieurs du groupe constitué d'une direction dans le sens des aiguilles d'une montre et d'une direction dans le sens contraire des aiguilles d'une montre, par rapport aux première et seconde directions.

10. Dispositif à semi-conducteurs selon la revendication 8, dans lequel chacun des transistors agencés dans une direction oblique sur la région active inclut une couche de silicium polycristallin déposée dans une direction oblique par rapport aux première et seconde directions.

11. Dispositif à semi-conducteurs selon la revendication 8, comprenant en outre un circuit d'attaque de ligne et un circuit d'attaque de balayage destinés à commander un écran électroluminescent organique.

12. Dispositif à semi-conducteurs selon la revendication 11, comprenant en outre un régisseur de vidéo et un régisseur d'écran destinés à commander le circuit d'attaque de ligne et le circuit d'attaque de balayage.

13. Circuit d'attaque d'écran à émission de lumière comprenant :

une RAM statique selon la revendication 5 ;
un écran électroluminescent organique ; et
un circuit d'attaque de ligne et un circuit d'attaque de balayage destinés à commander l'écran électroluminescent organique.

14. Circuit d'attaque d'écran à émission de lumière selon la revendication 13, comprenant en outre un régisseur de vidéo et un régisseur d'écran destinés à commander le circuit d'attaque de ligne et le circuit d'attaque de balayage.

FIG.1
Prior Art

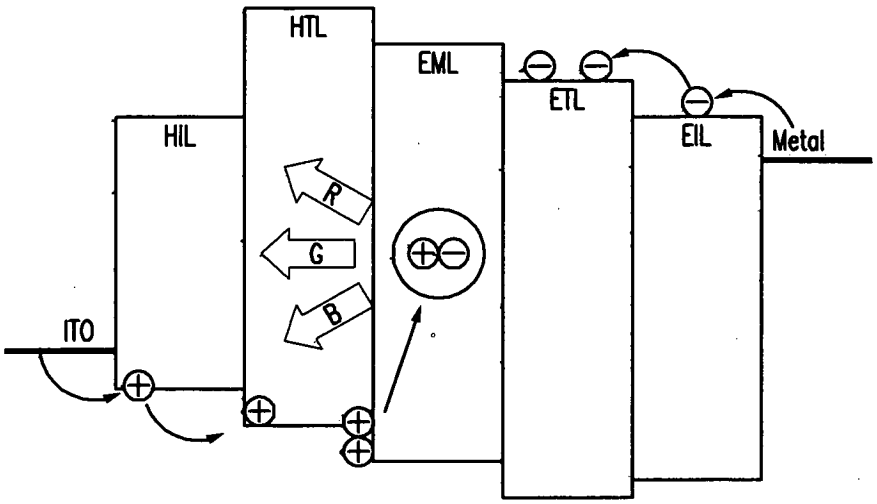


FIG.2,
Prior Art

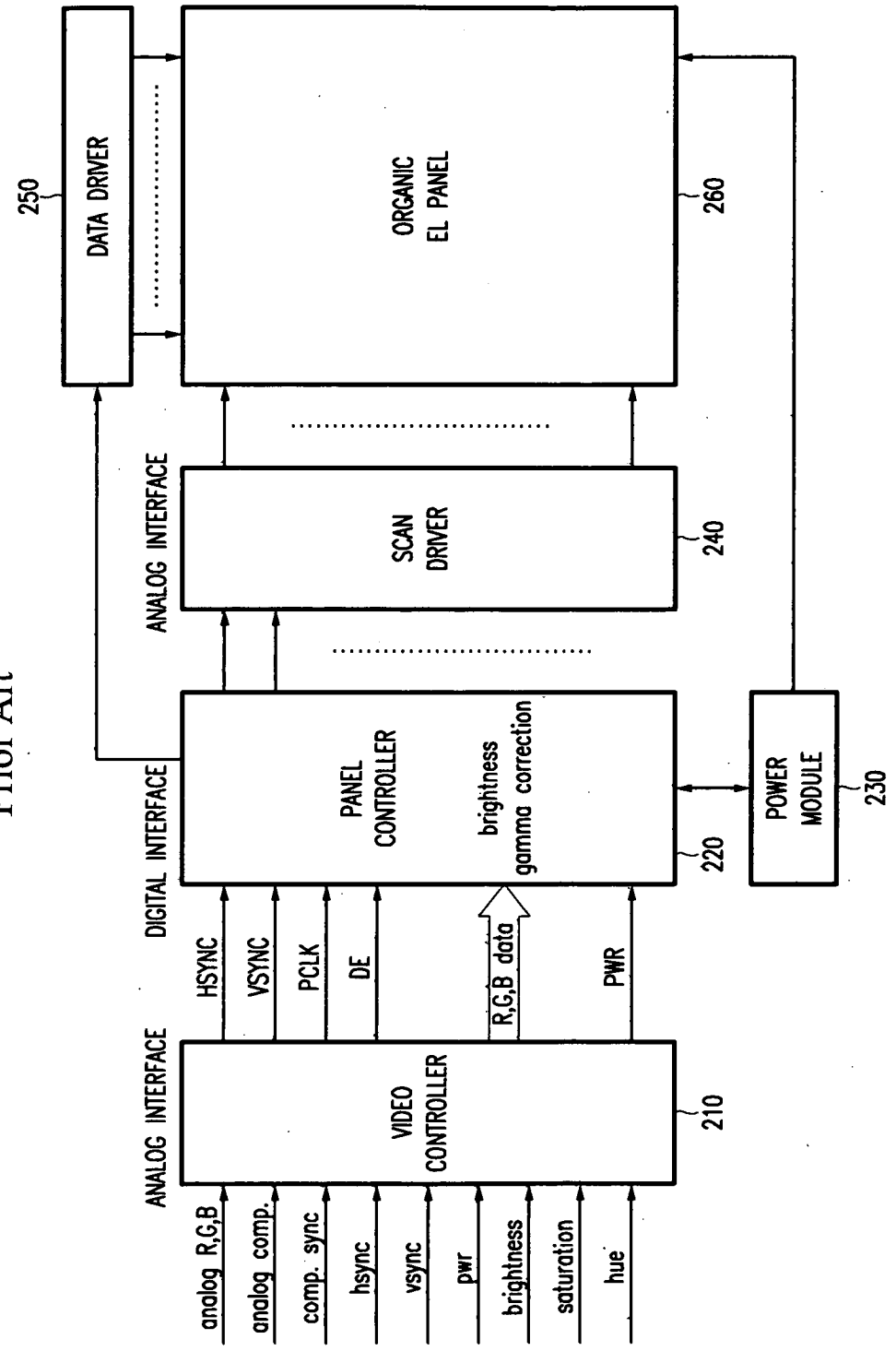


FIG.3
Prior Art

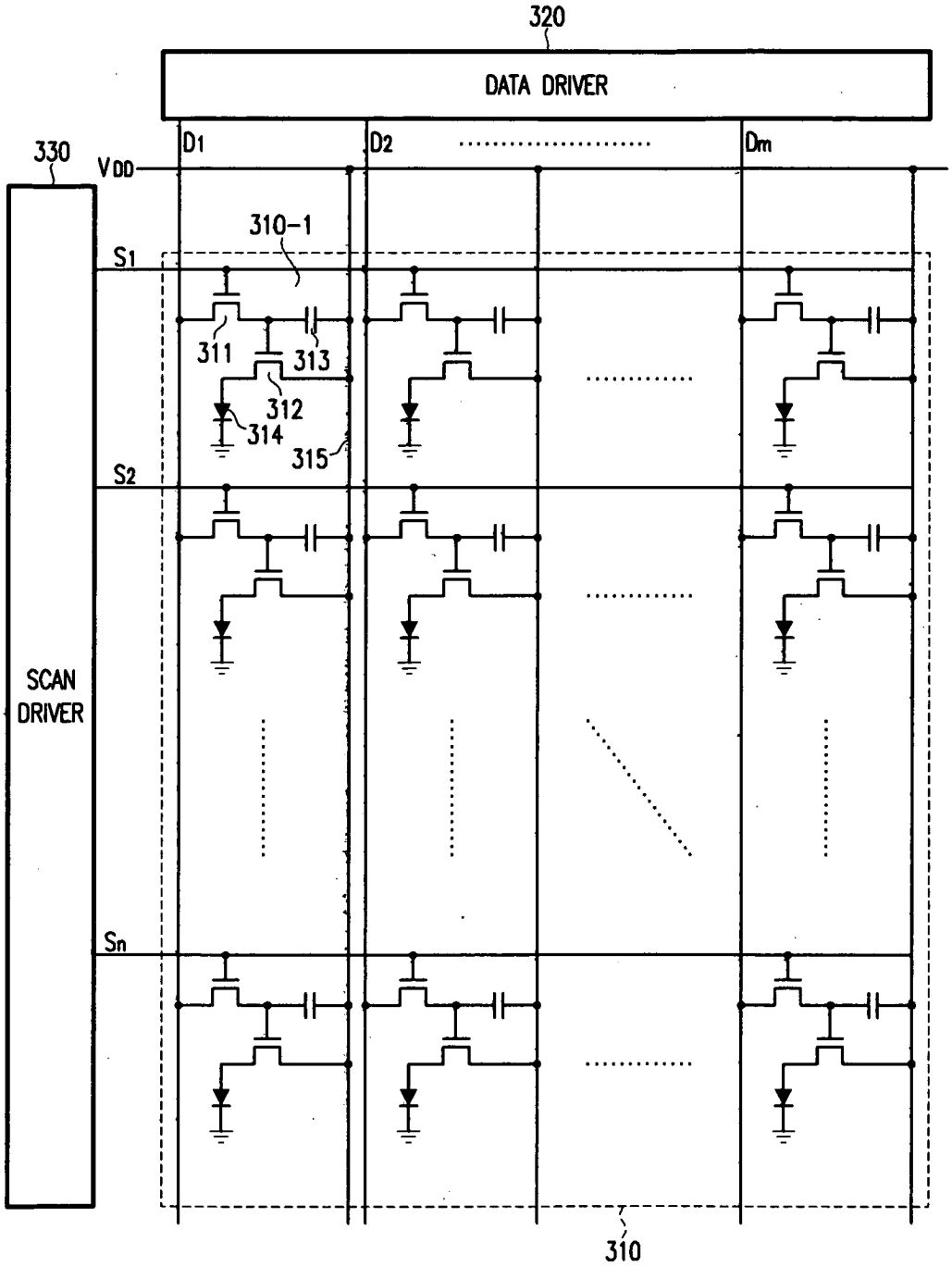


FIG.4
Prior Art

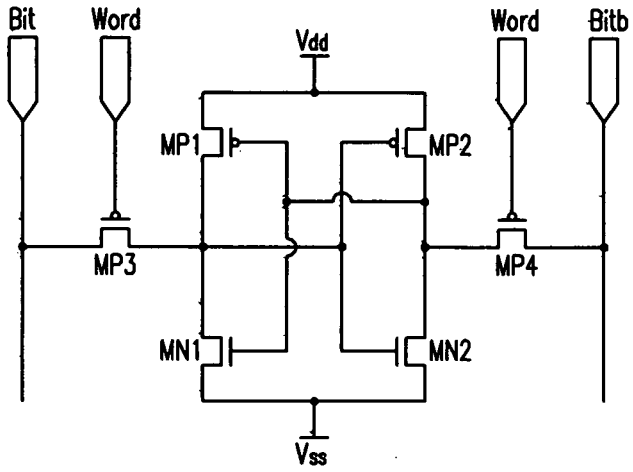


FIG.5

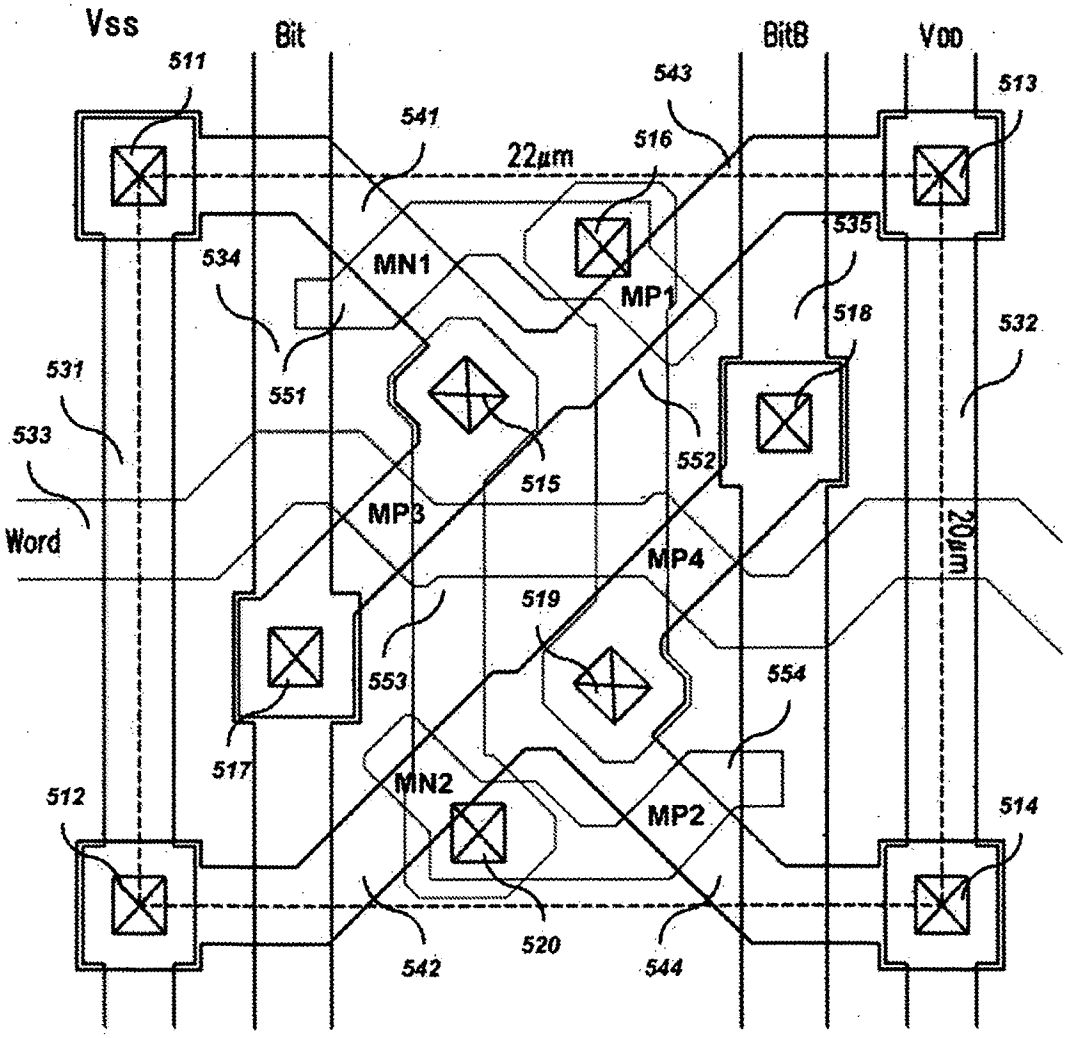

Vss
Bit
BitB
Vdd
511
513
541
543
22μm
516
535
534
MN1
MP1
518
532
531
551
552
533
515
MP3
Word
MP4
20μm
519
553
554
517
MN2
512
MP2
514
542
520
544

FIG.6

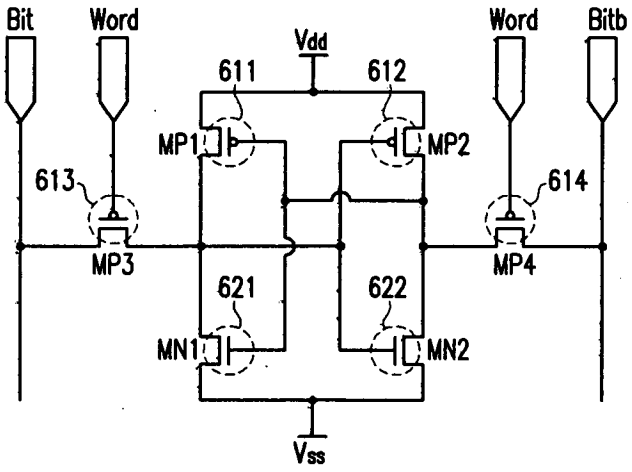
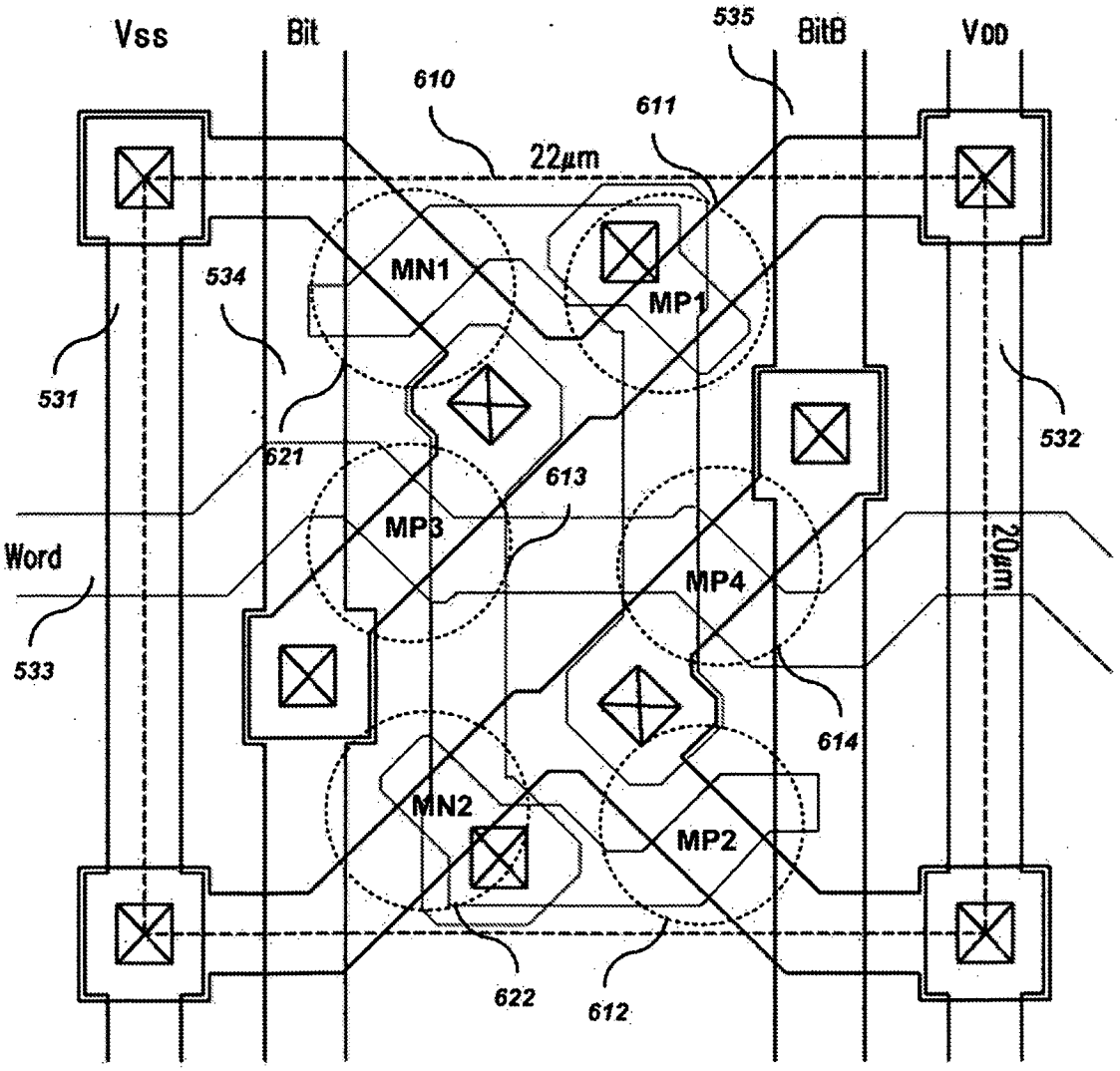

Bit
Word
Vdd
Word
Bitb
611
612
MP1
MP2
613
614
MP3
MP4
621
622
MN1
MN2
Vss

FIG.7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Bit
535
BitB
VDD
610
611
22μm
MN1
MP1
534
531
621
532
613
MP3
MP4
20μm
Word
533
614
MN2
MP2
622
612

REFERENCES CITED IN THE DESCRIPTION

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- US 5526303 A **[0022]**

专利名称(译)	用于发光显示器的SRAM核心单元		
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[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
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CPC分类号	G09G3/3225 G09G3/3275 G11C11/412 H01L27/0207 H01L27/11 H01L27/1108 F24F13/24 F24F2013/245		
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摘要(译)

用于有机电致发光发光显示装置的数据驱动器的发光显示器的SRAM核心单元包括薄膜晶体管作为用于发光显示器的数据驱动器的数据存储器。 SRAM核心单元还包括开关晶体管和数据存储晶体管。开关晶体管耦合到位线和字线以选择数据写入或读取。数据存储晶体管耦合到电源电压或地电压以实现数据写入和读取。位线和字线沿第一和第二方向形成。开关晶体管和数据存储晶体管的沟道相对于第一和第二方向在倾斜方向上形成。

FIG.1
Prior Art