(19) **日本国特許庁(JP)**

(12)公表特許公報(A)

(11)特許出願公表番号

特表2004-510999 (P2004-510999A)

(43) 公表日 平成16年4月8日 (2004. 4.8)

(51) Int.C1.		FΙ			テーマコー	ド (参考)
GO9G	3/30	G09G	3/30	J	3K007	
GO9F	9/30	GO9F	9/30	338	5C080	
GO9G	3/20	GO9F	9/30	365Z	5CO94	
H O 1L	33/00	G09G	3/20	624B	5FO41	
H 05 B	33/14	G09G	3/20	670J		
		審査請求 未請	求 予	備審査請求 未請求	(全 45 頁)	最終頁に続く

(21) 出願番号 特願2001-519495 (P2001-519495) (86) (22) 出願日 平成12年8月2日 (2000.8.2) (85) 翻訳文提出日 平成13年4月19日 (2001.4.19) (86) 国際出願番号 PCT/EP2000/007520 (87) 国際公開番号 W02001/015232 (87) 国際公開日 平成13年3月1日 (2001.3.1) (31) 優先権主張番号 9919536.4 (32) 優先日 平成11年8月19日 (1999.8.19)

(33) 優先権主張国 イギリス (GB)

(81) 指定国 EP (AT, BE, CH, CY, DE, DK, ES, FI, FR,

GB, GR, IE, IT, LU, MC, NL, PT, SE), JP, KR

(71) 出願人 590000248

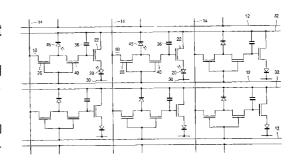
コーニンクレッカ フィリップス エレクトロニクス エヌ ヴィ
Koninklijke Philips Electronics N. V.
オランダ国 5621 ベーアー アインドーフェン フルーネヴァウツウェッハ 1
Groenewoudseweg 1,5621 BA Eindhoven, The Netherlands (74)代理人 100072051

最終頁に続く

(54) 【発明の名称】アクティブマトリクス電界発光表示装置

(57)【要約】

アクティブマトリックス電界発光表示装置は、各々が電流駆動電界発光表示素子(20)を含む表示画素(10)のアレイを具え、前記表示素子に、前のアドレス周期において印加されたデータ信号によって決定されるキャパシタンス(36)において蓄積される電圧にしたがって、駆動周期において前記表示素子を流れる電流を制御する駆動装置(22)を接続した。前記表示素子におけるエージングの影響を補償するために、前記キャパシタンスに蓄積された電圧をアクセス周期中のその表示素子の光出力に応じて調節する電気光学手段(45,40)を前記画素に含めた。



弁理士 杉村 興作

【特許請求の範囲】

【請求項1】

各々が電界発光表示素子及び駆動装置を具える表示画素のアレイを具え、前記駆動装置が、前記表示素子を流れる電流を、アドレス周期中に前記画素に印加され、前記駆動装置に接続された蓄積キャパシタンスにおいて電圧として蓄積された駆動信号に基づいて制御する、アクティブマトリックス電界発光表示装置において、各々の画素が、アドレス中に前記表示素子によって発生された光に応答し、前記アドレス周期中に、前記アドレス周期中に前記キャパシタンスにおいて蓄積された電圧信号を、前記表示素子の光出力レベルにしたがって調節するように配置された電気光学手段を含むことを特徴とするアクティブマトリックス電界発光表示装置。

【請求項2】

請求項1に記載のアクティブマトリックス電界発光表示装置において、前記電気光学手段が、前記画素において前記アドレス周期中に流れる電流を、印加されたデータ信号に従って調節し、この電流に、前記アドレス周期後に前記キャパシタンスにおいて蓄積された電圧が依存することを特徴とするアクティブマトリックス電界発光表示装置。

【請求項3】

請求項1又は2に記載のアクティブマトリックス電界発光表示装置において、前記電気光学手段が、前記蓄積キャパシタンスをアドレス周期中に流れる電流を前記表示素子光出力に従ってシャントするように配置された光電装置を具えることを特徴とするアクティブマトリックス電界発光表示装置。

【請求項4】

請求項3に記載のアクティブマトリックス電界発光表示装置において、前記光電装置を、前記蓄積キャパシタンスにスイッチ装置を介して接続し、前記スイッチ装置が、画素アドレス周期中に、前記光電装置を前記蓄積キャパシタンスと並列に接続するように動作することを特徴とするアクティブマトリックス電界発光表示装置。

【請求項5】

請求項3又は4に記載のアクティブマトリックス電界発光表示装置において、前記光電装置がフォトダイオードを具えることを特徴とするアクティブマトリックス電界発光表示装置。

【請求項6】

請求項1ないし5のいずれか1項に記載のアクティブマトリックス電界発光表示装置において、前記駆動装置が薄膜トランジスタを具えることを特徴とするアクティブマトリックス電界発光表示装置。

【発明の詳細な説明】

[0001]

本発明は、電界発光表示画素のアレイを具えるアクティブマトリックス電界発光表示装置に関する。さらに特に、本発明は、表示画素のアレイを具え、前記表示画素の各々が、電界発光表示画素と、前記表示画素を通る電流を、アドレス周期中に印加され、該表示装置に接続された蓄積キャパシタンスにおける電圧として蓄積される駆動信号に基づいて制御する駆動装置とを具える、アクティブマトリックス電界発光表示装置に関する。

[0 0 0 2]

電界発光表示素子を用いるマトリックス表示装置は、よく知られている。前記表示素子は、例えば、ポリマ材料を使用する有機薄膜電界発光素子、又は、慣例的なIII・V半導体混合物を使用する発光ダイオード(LED)を具えてもよい。有機電界発光材料、特にポリマ材料における最近の発展は、特にビデオ表示装置にこれらが使用される能力を論証した。これらの材料は、代表的に、1対の電極間に挟まれた電界発光材料、例えば半導電複合ポリマの1つ以上の層を具え、前記電極の一方が透明で、他方がホール又は電子を前記ポリマ層に注入するのに適した材料のものである。前記ポリマ材料を、CVDプロセス、又は単純に、溶解可能複合ポリマの溶液を使用する印刷又はスピンコーティング技術によって形成することができる。

10

20

30

40

20

30

40

50

[0003]

有機電界発光材料は、ダイオード様I - V特性を示し、表示機能及びスイッチング機能の 双方を与えることができ、したがって、パッシブ型ディスプレイにおいて使用することが できる。

[0004]

しかしながら、本発明は、各々の画素が表示素子を通る電流を制御するスイッチング装置とを具えるアクティブマトリックス電界発光ディスプレイの例は、欧州特許出願公開明細書第0653741号及、第0717446号において記載されている。表示素子が容量性であり、したがあるまとができるアクティブマトリックス液晶表示装置と異なり、前記電界発光表示素子とができるアクティブマトリックス液晶表示装置と異なり、下FT(薄膜トランジを発生するために連続的に電流を通す必要がある。通常、TFT(薄膜トランジを異える画素の駆動装置は、前記表示素で流れる電流を制御する原因である。前記表示表子の輝度は、該表示素子を流れる電流を制御する原因である。前記表示素子を流れる電圧又は一次である。前記表示素子を通る電圧又は電流信号の形態における駆動(データ)信号し、からの必要な出力を決定する電圧又は電流信号の形態における駆動(データ)活表示素子を通る電流を供給するまで、フィールド周期に対応する周期中に前記表示素子を通る電流を供給するように保持するように作用する。

[0005]

既知の有機電界発光材料、特にポリマ材料に関する問題は、これらがエージングの影響を受け、それによって、所定の駆動電流に対する光出力が動作時間の間に減少することである。特定の用途において、このようなエージングの影響が重要でないかもしれないが、画素化ディスプレイにおける重要性は、画素からの出力変化におけるどのようなわずかな変化も見る人によって容易に知覚されるため、重大である。

[0006]

本発明の目的は、この問題を少なくともある程度まで克服したアクティブマトリックス電 界発光ディスプレイを提供することである。

[0 0 0 7]

本発明によれば、電界発光表示素子及び駆動装置を各々が具える画素のアレイを具え、前記駆動装置が、前記表示素子を流れる電流を、アドレス周期中に画素に印加され、前記駆動装置に接続された蓄積キャパシタンスに蓄積された駆動信号に基づいて制御する、アクティブマトリックス電界発光表示装置において、各画素が、アドレス中に前記表示素子によって発生される光に応答すると共に、前記アドレス周期において、前記キャパシタンスに蓄積された電圧信号を、前記表示素子の光出力レベルに従って調節するように配置された電気光学調節手段を含むことを特徴とするアクティブマトリックス電界発光表示装置が提供される。

[0008]

このように、前記電気光学調節手段によって、アドレスに続く駆動(表示)周期における前記表示素子の光出力レベルを決定する蓄積された信号電圧は、前記表示素子の光出力特性に従って調節され、フィードバック変数を供給し、これによって、前記画素に設定された駆動レベルが、前記表示素子のエージングの影響に関して補償され、所定の印加駆動信号に対する表示素子からの所望の光出力レベルが、前記アレイにおける個々の表示素子の駆動電流レベル/光出力レベル特性における可能な変化に係わりなく、実際的に保持されるようにすることができる。

[0009]

アクティブマトリックス電界発光表示装置において一般的なように、画素の駆動装置がTFT(薄膜トランジスタ)を具える場合、本発明は他の重要な利点を提供する。表示素子に関する駆動電流を、前記キャパシタンスにおいて蓄積された電圧に対応する前記TFTのゲートに印加される電圧によって決定する。したがって、この駆動電流は、前記TFT

の特性と、例えば、製造プロセスによる前記アレイにおける画素の個々のTFTのしきい値電圧、モビリティ及び寸法における変化とに強く依存し、前記表示素子電流と、したがって、発生される光レベルとにおける望ましくない変化を生じ、前記表示出力における非一様性を招くおそれがある。前記蓄積された電圧信号の制御における前記電気光学調節手段の影響も、TFT特性におけるこのような変化を補償する。

[0010]

本発明は、ポリマLED材料を使用する装置において特に有利であるが、もちろん、電界発光材料が同様にエージングの影響を受け、結果として、動作の時間周期に渡って所定の駆動電流に対してより低い光出力レベルを生じるどのような電界発光装置における利点に適用することができる。

[0011]

特に、前記電気光学手段は、前記アドレス周期中に画素を流れる電流を印加されたデータ信号に応じて調節し、前記アドレス周期後の前記キャパシタンスに蓄積された電圧がこの電流に依存する。

[0012]

好適実施形態において、前記電気光学手段は、スイッチ装置、例えば他のTFTを経て前記蓄積キャパシタンスに接続された光電装置を具え、前記スイッチ装置を、前記アドレス周期中に前記光電装置を前記蓄積キャパシタンスと並列に接続するように、前記アドレス周期中に閉じるように配置した。前記駆動周期中、前記同地は、前記蓄積キャパシタンスから電気的に切り離される。前記アドレス周期において、電流信号から成るデータ信号に関して、前記装置は、前記キャパシタンスからの電流を、前記表示素子の光出力に応じて、平衡状態に達し、前記キャパシタンス電圧と、前記駆動TFTのゲート電圧とが安定するまで、シャントするように作用する。

[0013]

前記光電装置は、好適には、フォトダイオードを具えるが、フォトレジスタ又はフォトトランジスタを代わりに用いることもできる。

[0014]

ここで、本発明によるアクティブマトリックス電界発光表示装置の一実施形態を、添付した図面の参照と共に、例として説明する。

[0015]

図面は単に図式的なものである。同じ参照符を、図面を通して、同じ又は同様の部分を示すために使用した。

[0016]

図1を参照し、アクティブマトリックス電界発光表示装置は、ブロック10によって示し、各々が電界発光表示素子と、前記表示素子を通る電流を制御する関連する駆動装置とを具える規則的に間隔を置き、行(選択)導体すなわちライン12及び列(データ)導体すなわちライン14の交差する組間の交点において位置する画素の行及び列マトリックスアレイを有するパネルを具える。簡単にするため、いくつかの画素のみをここに示す。画素10を、前記個々の組の終端において接続された行走査駆動回路16及び列データ駆動回路18を具える周辺駆動回路によって、アドレス導体の組を経てアドレスする。

[0 0 1 7]

画素の各行を、回路16によって個々の行導体12に印加される選択信号によってアドレスし、各行の画素に、回路18によって前記列導体に並列に供給される個々のデータ信号に従って、これらの個々の表示出力を決定する個々の駆動信号をロードするようにする。各行がアドレスされると、適切なデータ信号が回路18によって適切な同期において供給される。

[0018]

図 2 は、既知の装置におけるいくつかの代表的な画素の回路を示す。この特定の装置において、前記データ信号は電圧信号から成る。各々の画素 1 0 は、ここではダイオード素子 (LED)として表し、間に1つ以上の有機電界発光材料の活性層を挟んだ1対の電極を 10

20

30

40

50

具える発光有機電界発光表示素子20を具える。この特定の実施形態において、前記材料 はポリマLED材料から成るが、低分子量物質のような他の有機電界発光材料を使用する こともできる。前記アレイの表示素子を、関連するアクティブマトリックス回路網と一緒 に 、 絶 縁 支 持 部 の 一 方 の 側 に 搭 載 す る 。 前 記 表 示 素 子 の カ ソ ー ド 又 は ア ノ ー ド の い ず れ か を、透明導電材料によって形成する。前記指示部を、ガラスのような透明材料のものとし 、前記基板に最も近い個々の表示素子20の電極を、ITOのような透明導電材料によっ て構成し、前記電界発光層によって発生された光が、これらの電極及び指示部を通過し、 前記指示部の他方の側における観察者に見えるようにすることができる。代わりに、前記 光出力を、この場合において前記アレイにおけるすべての表示素子に共通の供給ラインを 構 成 す る 連 続 I T O 層 の 部 分 を 具 え る 前 記 パ ネ ル 及 び 表 示 素 子 ア ノ ー ド の 上 か ら 見 る こ と もできる。前記表示素子のカソードは、カルシウム又はマグネシウム銀合金のような低仕 事関数を有する金属を具える。使用できる好適な有機結合ポリマ材料は、WO96/36 9 5 6 において記載されている。他の低分子量有機材料の例は、欧州特許出願公開明細書 第 0 7 1 7 4 4 6 号において記載されており、この欧州特許出願公開明細書は、アクティ ブマトリックス電界発光装置の構成及び動作の例も記載されており、これらにおいて開示 されている内容は、参照によってここに含まれる。

[0019]

各々の画素 1 0 は、表示素子 2 0 の動作を該画素に印加されるアナログデータ信号電圧に基づいて制御するTFT 2 2 の形態における駆動装置を含む。ある画素に関する前記駆動電圧を、各列の画素間で供給される列導体 1 4 を経て印加する。列導体 1 4 を、電流制御駆動トランジスタのゲートにアドレスTFT 2 6 を経て結合する。ある行の画素のアドレスTFT 2 6 に関するゲートを、一緒に共通行導体 1 2 に結合する。

[0020]

各行の画素 1 0 は、通常はすべての画素に共通の連続電極として設けられる共通電圧供給ライン 3 0 と、個々の共通電流ライン 3 2 とを共有する。表示素子 2 0 及び駆動装置 2 2 を、電圧供給ライン 3 0 と、供給ライン 3 0 に対して正電位であり、表示素子 2 0 を通って流れる電流に関する電流源として作用する共通電流ライン 3 2 との間に直列に接続する。表示素子 2 0 を通って流れる電流を、スイッチング装置 2 2 によって制御し、この電流は、列導体 1 4 に供給される前記データ信号によって決定される蓄積された制御信号に依存するトランジスタ 2 2 におけるゲート電圧の関数である。

[0021]

ある行の画素を、個々の行の画素に関するアドレスTFT26をオンに切り替える選択パルスを行導体12に印加する行駆動回路16によって選択する。前記ビデオ情報から得られる電圧レベルを、駆動回路18によって列導体14に印加し、アドレスTFT26によって駆動トランジスタ22のゲートに伝送する。ある行の画素が行導体12を経てアドレスされていない期間中、アドレストランジスタ26はターンオフするが、駆動トランジスタ22のゲートと共通電流ライン32との間に接続された画素蓄積キャパシタ36によって保持される。駆動トランジスタ22のゲートと共通電流ライン32との間の電圧は、画素10の表示素子20を通過する電流を決定する。したがって、前記表示素子を流れる電流は、駆動トランジスタ22のゲート・ソース電圧の関数である(トランジスタ22のソースは共通電流ライン32に接続され、トランジスタ22のドレインは表示素子20に接続されている)。この電流は、前記画素の光出カレベル(グレイスケール)を制御する。

[0022]

スイッチングトランジスタ22を、飽和状態において、ゲート・ソース電圧が前記トランジスタを流れる電流をドレイン・ソース電圧にかかわりなく管理するように動作するように配置する。その結果、前記ドレイン電圧のわずかな変化は、表示素子20を流れる電流に影響を与えない。したがって、電流供給ライン30における電圧は、前記画素の正確な動作に対して重要ではない。

[0023]

50

40

10

20

30

10

20

30

40

50

画素の各行を、個々の行アドレス周期において、各々の行の画素にこれらの駆動信号を順次に与え、前記画素を、駆動(フィールド)周期の間、これらが次にアドレスされるまで 所望の光出力を与えるようにセットするようにアドレスする。

[0024]

この既知の画素回路に関して、キャパシタ36に蓄積された電圧が、前記印加されたデータ信号によってほぼ決定され、この電圧が、駆動トランジスタ22及び表示素子20を流れる電流を制御し、結果として生じる前記表示素子の光出力レベルが常に前記表示素子のこのとき存在する電流 / 光出力レベル特性に依存することは認識されるであろう。前記表示素子の電界発光材料は、所定の駆動電流レベルに対する光出力レベルの減少を結果として生じるエージングの影響を招く動作期間中の劣化を受けるおそれがある。したがって、より長く(より激しく)駆動されたこれらの画素は、低下した輝度を示し、表示の非一様性を生じるであろう。ポリマLED材料に関して、このようなエージングの影響は、重大であるかもしれない。

[0 0 2 5]

本発明において、ある画素にアドレス段階中に蓄積された駆動信号を、該画素におけるフィードバック装置として作動する電気光学手段によって、前記表示素子の発光特性にしたがって、これらのようなエージングの影響に関して少なくともある程度補償し、前記表示素子の必要な光出力レベルがその後にアドレスしたときに発生することを保証するように自動的に調節する。

[0026]

図3を参照し、本発明による、エージングの問題を少なくともある程度克服することを目的とする表示装置の一実施形態における画素の等価回路を示す。各々の画素10において、表示素子20を、再び、ここではすべての画素によって共有される共通電極層によって構成したように示す電流ライン32と電圧供給ライン30との間の駆動トランジスタ22に直列に接続し、アドレストランジスタ26のゲート及びソースを、関連する行及び列導体12及び14に各々接続する。また、蓄積キャパシタ36を、再び、駆動トランジスタ22のゲートと電流ライン32との間に接続する。

[0027]

前記画素は、さらに、再びTFTの形態における追加のスイッチ装置40を含み、このスイッチ装置40を、アドレスTFT26と、蓄積キャパシタ36と駆動トランジスタ22のゲートとの間のノードとの間に接続し、スイッチ装置40のゲート端子をアドレスTFT26のゲートと同じ行導体12に接続し、行導体12に印加される(ゲート)パルス選択信号の印加によって、アドレスTFT26と同期して動作させるようにする。

[0 0 2 8]

フォトダイオード 4 5 を、前記画素に関係する電流ライン 3 2 と、TFT 2 6 及び 4 0 間のノードとの間に接続する。前記画素を、フォトダイオード 4 5 が該画素の表示素子 2 0 によって放射された光に曝されるように構成する。これらの構成部品間のこのような光学的結合の目的は、以下のこの画素の動作の説明から明らかになるであろう。

[0029]

この装置において、前記画素に列導体14を経て印加される前記データ信号は、電圧信号でなくアナログ電流信号から成る。電圧でなく電流データ信号を使用するアクティブマトリックス電界発光装置は、既知であり、例えば、WO99/65012に記載されているようなものである。

[0030]

既知の画素回路に関して、この画素回路は、2つの状態、前記画素を所望の表示出力状態に設定するアドレス状態と、前記表示素子をその後、前記設定状態にしたがって、前記画素がその後のフィールドにおいて再びアドレスされるまで駆動する駆動状態とを有する。前記アドレス状態において、行駆動回路16は、選択パルス信号を行導体12に個々の行アドレス周期において印加し、行導体12はTFT26及び40をターンオンする。キャパシタ36は、ここで、例えば、このときに完全に放電されるとする。前記アドレス段階

20

30

40

50

において、電流は、関連する列導体14に、前記印加されたデータ信号にしたがってシン クされる。充電経路は、電流ライン32から、並列の蓄積キャパシタ36及びフォトダイ オード45を通るものである。前記フォトダイオードが逆バイアスされているため、この 初期期間において高いインピーダンスを有する。その結果、蓄積キャパシタ36は、 T 2 6 及 び 4 0 を 経 て 充 電 を 開 始 し 、 駆 動 T F T 2 2 の ソ ー ス 及 び ゲ ー ト 間 の 電 圧 は 上 昇 する。TFT22のしきい値レベルに達すると、TFT22は、導通を開始し、表示素子 20を流れる電流を生じ、光を発生し、それによって光出力を発生する。表示素子20及 びフォトダイオード45の互いに関する適切な物理的配置の結果として、導通している表 示素子20によって放射される光のいくらかはフォトダイオード45に当たり、フォトダ イオード45にフォト電流を導通し始めさせる。フォト電流の程度は、それによって逆バ イアスされても、受けた光レベル(光子の量/秒)に比例する。次に、フォトダイオード 45は、キャパシタ36からの電流をシャントする。依然として行アドレス周期内である 短い時間の後、列導体14によってシンクされている電流がすべて前記フォトダイオード のみによってシャントされ、駆動TFT22のゲート電圧が安定する平衡状態に達する。 このように、表示素子20からの光を、フォトダイオード45を経てアドレス中の前記画 その設定におけるフィードバック変数として使用する。

[0031]

次に、前記画素回路を、前記行選択パルスの停止に応じてTFT26及び40をターンオフし、TFT22のゲートと蓄積キャパシタ36との間のノードを、フォトダイオード45及び列導体14から絶縁することによって、その駆動状態に切り替える。ここで、キャパシタ36は、TFT22のゲート・ソース電圧を、前記駆動(表示)段階における前記表示素子の電流駆動レベルを決定する調節された駆動信号レベルとして、前記画素が次にアドレスされるまで蓄積する。これは結果として、この駆動期間を通じて表示素子20を流れる安定電流を生じる。前記表示素子からの光を前記画素の設定におけるフィードバック変数として使用するため、前記駆動段階中の1秒当たりの光出力(光子)は、所望の出力光レベルにしたがって固定され、前記入力電流に比例する。

[0 0 3 2]

アドレス中、このように前記表示素子からの光出力を使用することによって、前記画素の設定は、関連する表示素子の特性を発生する瞬時の光出力と、キャパシタ36に蓄積された駆動信号電圧とに依存するようになり、TFT22によって決定される前記表示素子を流れる電流の結果として生じるレベルは、前記表示素子におけるエージングの影響を補償するように自動的に適宜に調節される。ある表示素子における所定の駆動電流に対する光出力レベルがエージングのために低下した場合、前記調節された蓄積された駆動信号は、前記表示素子を、適切により高い電流レベルにおいて駆動させ、所望の表示効果を保持する。

[0033]

前記キャパシタが、前記アドレス段階の開始時において、完全に放電されているのではなく、充電されており、前記アドレス電流(データ信号)がゼロの場合、フォトダイオード45におけるフォト電流は、キャパシタ36を、この段階中に表示素子20からの光出力がなくなるまで放電させ、駆動段階において光は放出されない。

[0 0 3 4]

これらのような影響の補償を外れて、前記画素回路は、前記アレイにおける異なった画素のTFT22の、例えば、これらのしきい値電圧、寸法及びTFTを形成するのに使用した薄膜製造プロセスの性質によるモビリティにおける変化から生じる動作特性における変化を自動的に補償するのにも有効である。結果として、前記アレイにおける表示素子からの光出力の一様性におけるさらなる改善が達成される。

[0035]

上記画素回路の実施形態において使用したTFTは、すべてpチャネルMOSFETから成る。しかしながら、nチャネルMOSFETを代わりに使用することもでき、表示素子20及びフォトダイオード45の極性と、印加される駆動電圧とを反対にする。好適には

、ポリシリコンTFTを使用するが、代わりに、アモルファスシリコンTFTを用いることもできる。

[0036]

フォトダイオード 4 5 を、(ダイオード接続された)フォトトランジスタや、フォトレジスタ、又は、他の適切な光電装置と交換してもよい。

[0037]

フォトダイオード 4 5 を、表示素子 2 0 によって放射された光に曝されるように配置したが、好適には、前記装置に当たる周囲光から完全に遮蔽し、動作において、前記表示素子からの光のみに応じるようにする。

[0038]

上記実施形態における電流ラインは、行方向において延在し、個々の行の画素によって共有されるが、これらは、代わりに、列方向において延在し、各々の電流ラインを、個々の列の画素によって共有してもよい。

[0 0 3 9]

要約において、したがって、各々が電流駆動電界発光表示素子を含む画素のアレイを具え、前記表示素子に、前のアドレス周期において印加されたデータ信号によって決定されるキャパシタンスにおいて蓄積される電圧にしたがって、駆動周期において前記表示素子を流れる電流を制御する駆動装置を接続した、アクティブマトリックス電界発光表示装置を開示した。前記表示素子におけるエージングの影響を補償するために、前記キャパシタンスに蓄積された電圧をアクセス周期中のその表示素子の光出力に応じて調節する電気光学手段を前記画素に含めた。

[0040]

本開示を読むことによって、他の変形が当業者には明らかであろう。これらのような変形は、アクティブマトリックス電界発光表示装置及びその構成部品の分野において既知であり、既にここで説明した特徴の代わり又はそれらに追加して使用することができる他の特徴を含んでもよい。

【図面の簡単な説明】

【図1】画素のアレイを具える既知のアクティブマトリックス電界発光表示装置の単純化 した概要図である。

【図2】図1の既知のアクティブマトリックス電界発光表示装置のいくつかの代表的な画素の等価回路を示す。

【図3】本発明によるアクティブマトリックス電界発光表示装置の一実施形態におけるいくつかの代表的な画素の等価回路を示す。

10

20

30

【国際公開パンフレット】

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization International Bureau



(43) International Publication Date 1 March 2001 (01.03.2001)

PCT

(10) International Publication Number WO 01/15232 A1

(51) International Patent Classification7: H01L 27/00, (72) Inventor: HUNTER, Iain, M.; Prof. Holstlaan 6, G09G 3/32 NL-5656 AA Eindhoven (NL).

(21) International Application Number: PCT/EP00/07520 (74) Agent: WILLIAMSON, Paul, L.: International Octoolbureau B.V., Prof. Holstlaan 6. NL-5656 AA Eindhoven (NL).

(22) International Filing Date: 2 August 2000 (02.08.2000)

(81) Designated States (national): JP, KR. English

(25) Filing Language:

English

(26) Publication Language:

(84) Designated States (regional): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

A1

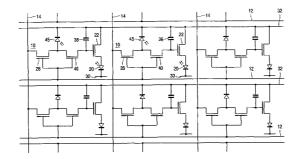
19 August 1999 (19.08.1999) GB Published:

With international search report.

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]: Groenewoudseweg 1, NL-5621 BA
Eindhoven (NL).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ACTIVE MATRIX ELECTROLUMINESCENT DISPLAY DEVICE



(57) Abstract: An active matrix electroluminescent display device comprises an array of display pixels (10) which each include a current-driven electroluminescent display element (20) connected to a driving device (22) controlling the current flowing through the display element in a drive period according to a voltage stored on a capacitance (36) determined by a data signal applied in a preceding address period. In order to compensate for ageing effects in the display element, electro-optic means (45, 40) are included in the pixel for adjusting the woltage stored on the capacitance in dependence on light output of its display element during the address period.

PCT/EP00/07520

1

DESCRIPTION

ACTIVE MATRIX ELECTROLUMINESCENT DISPLAY DEVICE

This invention relates to active matrix electroluminescent display devices comprising an array of electroluminescent display pixels. More particularly, the invention concerns an active matrix electroluminescent display device comprising an array of display pixels each comprising an electroluminescent display element and a driving device for controlling the current through the display element based on a drive signal applied to the pixel during an address period and stored as a voltage on a storage capacitance connected to the driving device.

Matrix display devices employing electroluminescent, light-emitting, display elements are well known. The display elements may comprise organic thin film electroluminescent elements, for example using polymer materials, or else light emitting diodes (LEDs) using traditional III-V semiconductor compounds. Recent developments in organic electroluminescent materials, particularly polymer materials, have demonstrated their ability to be used practically for video display devices. These materials typically comprise one or more layers of an electroluminescent material, for example a semiconducting conjugated polymer, sandwiched between a pair of electrodes, one of which is transparent and the other of which is of a material suitable for injecting holes or electrons into the polymer layer. The polymer material can be fabricated using a CVD process, or simply by printing or a spin coating technique using a solution of a soluble conjugated polymer.

Organic electroluminescent materials exhibit diode-like I-V properties, so that they are capable of providing both a display function and a switching function, and can therefore be used in passive type displays.

PCT/EP00/07520

2

However, the invention is concerned with active matrix display devices, with each pixel comprising a display element and a switching device for controlling the current through the display elements. Examples of an active matrix electroluminescent display are described in EP-A-0653741 and EP-A-0717446. Unlike active matrix liquid crystal display devices in which the display elements are capacitive and therefore take virtually no current and allow a drive signal voltage to be stored on the capacitance for the whole field period, the electroluminescent display elements need to continuously pass current to generate light. A driving device of a pixel, usually comprising a TFT (thin film transistor), is responsible for controlling the current through the display element. The brightness of the display element is proportional to the current flowing through it. During an address period for a pixel, a drive (data) signal in the form of a voltage or current signal determining the required output from the display element is applied to the pixel and stored as a corresponding voltage level on a storage capacitance which is connected to, and controls the operation of, the current controlling drive device with the voltage stored on the capacitance serving to maintain operation of the switching device in supplying current through the display element during the period, corresponding to a field period, until the pixel is addressed again.

A problem with known organic electroluminescent materials, particularly polymer materials, is that they suffer ageing effects whereby the light output for a given drive current is reduced over a period of time of operation. While in certain applications such ageing effects may not be critical, the consequences in a pixellated display can be serious as any slight variations in light output from pixels can easily be perceived by a viewer.

It is an object of the present invention to provide an active matrix electroluminescent display device in which this problem is overcome at least to an extent.

According to the present invention there is provided an active matrix electroluminescent display device comprising an array of display pixels each comprising an electroluminescent display element and a driving device for

PCT/EP00/07520

3

controlling the current through the display element based on a drive signal applied to the pixel during an address period and stored as a voltage on a storage capacitance connected to the driving device, which is characterised in that each pixel includes electro-optic adjustment means which is responsive to light produced by the display element during addressing and arranged to adjust in the address period the voltage signal stored on the capacitance in accordance with the light output level of the display element.

Thus, by means of the electro-optic adjustment means, the stored signal voltage for determining the light output level of the display element in the drive (display) period following addressing is adjusted according to the light output characteristic of the display element, providing a feedback variable, whereby the drive level set on the pixel can compensate for the effects of ageing of the display elements so that a desired light output level from a display element for a given applied drive signal is substantially maintained regardless of possible variations in the drive current level / light output level characteristics of individual display elements in the array.

In the case where the drive device of a pixel comprises a TFT (thin film transistor) as is usual in active matrix electroluminescent display devices, the invention offers a further important advantage. The drive current for a display element is determined by the voltage applied to the gate of the TFT, corresponding to the voltage stored in the capacitance. This drive current therefore depends strongly on the characteristics of the TFT and variations in the threshold voltage, mobility and dimensions of the individual TFTs of pixels over the array, for example due to manufacturing processes, can produce unwanted variations in the display element currents and hence light levels produced, leading to non-uniformity in the display output. The effect of the electro-optic adjustment means in controlling the stored voltage signal will also compensate for such variations in TFT characteristics.

Although the invention is particularly beneficial in devices using polymer 30 LED materials, it can of course be applied to advantage in any electroluminescent device in which the electroluminescent material similarly

PCT/EP00/07520

4

suffers ageing effects resulting in lower light output levels for a given drive current over a period of time of operation.

Preferably the electro-optic means regulates a current flowing in the pixel during the address period according to an applied data signal upon which current the voltage stored on the capacitance following the address period is dependent.

In a preferred embodiment, the electro-optic means comprises a photoelectric device connected to the storage capacitance via a switch device, for example another TFT, which is arranged to be closed during the address period so as to connect the photoelectric device in parallel with the storage capacitance during the address period. During the driving period, the device is effectively disconnected from the storage capacitance and plays no part in the operation of the pixel. In the address period, and with the data signal comprising a current signal, the device serves to shunt current from the capacitance in dependence upon the display element's light output until an equilibrium state is reached and the capacitance voltage, and the gate voltage of the drive TFT, stabilises.

The photoelectric device preferably comprises a photodiode, although a photoresistor or phototransistor could alternatively be employed.

20

An embodiment of an active matrix electroluminescent display device in accordance with the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a simplified schematic diagram of a known active matrix electroluminescent display device comprising an array of pixels;

Figure 2 shows the equivalent circuit of a few typical pixels of the known active matrix electroluminescent display device of Figure 1; and

Figure 3 shows the equivalent circuit of a few typical pixels in an embodiment of active matrix electroluminescent display device according to the invention.

The Figures are merely schematic. The same reference numbers are used throughout the Figures to denote the same or similar parts.

WO 01/15232 PCT/EP00/07520

5

Referring to Figure 1, the active matrix electroluminescent display device comprises a panel having a row and column matrix array of regularly-spaced pixels, denoted by the blocks 10, each comprising an electroluminescent display element and an associated driving device controlling the current through the display element, and which are located at the intersections between crossing sets of row (selection) and column (data) address conductors, or lines, 12 and 14. Only a few pixels are shown here for simplicity. The pixels 10 are addressed via the sets of address conductors by a peripheral drive circuit comprising a row, scanning, driver circuit 16 and a column, data, driver circuit 18 connected to the ends of the respective sets.

Each row of pixels is addressed in turn by means of a selection signal applied by the circuit 16 to the relevant row conductor 12 so as to load the pixels of the row with respective drive signals, determining their individual display outputs, according to the respective data signals supplied in parallel by the circuit 18 to the column conductors. As each row is addressed, the appropriate data signals are supplied by the circuit 18 in appropriate synchronisation.

Figure 2 illustrates the circuit of a few, typical, pixels in this known device. In this particular device, the data signals comprise voltage signals. Each pixel, 10, includes a light emitting organic electroluminescent display element 20, represented here as a diode element (LED), and comprising a pair of electrodes between which one or more active layers of organic electroluminescent material is sandwiched. In this particular embodiment the material comprises a polymer LED material, although other organic electroluminescent materials, such as low molecular weight materials, could be used. The display elements of the array are carried together with the associated active matrix circuitry on one side of an insulating support. Either the cathodes or the anodes of the display elements are formed of transparent conductive material. The support is of transparent material such as glass and the electrodes of the individual display elements 20 closest to the substrate can consist of a transparent conductive material such as ITO so that light

PCT/EP00/07520

6

generated by the electroluminescent layer is transmitted through these electrodes and the support so as to be visible to a viewer at the other side of the support. Alternatively, the light output could be viewed from above the panel and the display element anodes in this case would comprise parts of a continuous ITO layer constituting a supply line common to all display elements in the array. The cathodes of the display elements comprise a metal having a low work-function such as calcium or magnesium silver alloy. Examples of suitable organic conjugated polymer materials which can be used are described in WO 96/36959. Examples of other, low molecular weight, organic materials are described in EP-A-0717446, which also describes examples of the construction and operation of an active matrix electroluminescent device and whose disclosure in these respects is incorporated herein by reference.

Each pixel 10 includes a drive device in the form of a TFT 22 which controls the operation of the display element 20 based on an analogue data signal voltage applied to the pixel. The signal voltage for a pixel is supplied via a column conductor 14 which is shared between a respective column of pixels. The column conductor 14 is coupled to the gate of the current-controlling drive transistor 22 through an address TFT 26. The gates for the address TFTs 26 of a row of pixels are coupled together to a common row conductor 12.

Each row of pixels 10 also shares a common voltage supply line 30, usually provided as a continuous electrode common to all pixels, and a respective common current line 32. The display element 20 and the drive device 22 are connected in series between the voltage supply line 30 and the common current line 32, which is at a positive potential with respect to the supply line 30 and acts as a current source for the current flowing through the display element 20. The current flowing through the display element 20 is controlled by the switching device 22 and is a function of the gate voltage on the transistor 22, which is dependent upon a stored control signal determined by the data signal supplied to the column conductor 14.

A row of pixels is selected by the row driver circuit 16 applying a selection pulse to the row conductor 12 which switches on the address TFTs 26 for the respective row of pixels. A voltage level derived from the video

PCT/EP00/07520

7

information is applied to the column conductor 14 by the driver circuit 18 and is transferred by the address TFT 26 to the gate of the drive transistor 22. During the periods when a row of pixels is not being addressed via the row conductor 12 the address transistor 26 is turned off, but the voltage on the gate of the drive transistor 22 is maintained by a pixel storage capacitor 36 which is connected between the gate of the drive transistor 22 and the common current line 32. The voltage between the gate of the drive transistor 22 and the common current line 32 determines the current passing through the display element 20 of the pixel 10. Thus, the current flowing through the display element is a function of the gate-source voltage of the drive transistor 22 (the source of the transistor 22 being connected to the common current line 32, and the drain of the transistor 22 being connected to the display element 20). This current in turn controls the light output level (grey-scale) of the pixel.

The switching transistor 22 is arranged to operate in saturation, so that the gate-source voltage governs the current flowing through the transistor, irrespectively of the drain-source voltage. Consequently, slight variations of the drain voltage do not affect the current flowing through the display element 20. The voltage on the voltage supply line 30 is therefore not critical to the correct operation of the pixels.

Each row of pixels is addressed in turn in this manner in respective row address periods so as to load the pixels of each row in sequence with their drive signals and set the pixels to provide desired display outputs for the drive (field) period until they are next addressed.

With this known pixel circuit, it will be appreciated that the voltage stored on the capacitor 36 is substantially determined by the applied data signal voltage and that as this voltage in turn controls the drive transistor 22 and the current through the display element 20 then the resulting light output level of the display element at any time will be dependent on the then existing current/light output level characteristic of the display element. The electroluminescent material of the display element can suffer degradation over a period time of operation leading to ageing effects which result in a reduction of the light output level for a given drive current level. Those pixels which

PCT/EP00/07520

WO 01/15232

10

have, therefore, been driven longer (or harder) will exhibit reduced brightness and cause display non-uniformities. With polymer LED materials the effects of such ageing can be significant.

In the present invention, the drive signal stored in a pixel during the 5 addressing phase is automatically adjusted through electro-optical means in the pixel, acting as a feedback arrangement, according to the light emission characteristic of the display element so as to compensate at least to some extent for such ageing effects and ensure that the required light output level of the display element is produced following addressing.

Referring to Figure 3, there is shown the equivalent circuit of a pixel in an embodiment of display device according to the invention and intended to overcome, at least to some extent, the problem of ageing. In each pixel 10 the display element 20 is again connected in series with the drive transistor 22 between the current line 32 and a voltage supply line 30, here shown 15 constituted by a common electrode layer shared by all the pixels, and the gate and source of address transistor 26 are connected to the associated row and column conductors 12 and 14 respectively. Also the storage capacitor 36 is again connected between the gate of the drive transistor 22 and the current line 32.

The pixel further includes an additional switch device 40, again in the form of a TFT, which is connected between the address TFT 26 and the node between the storage capacitor 36 and the gate of the drive transistor 22 with its gate terminal connected to the same row conductor 12 as the gate of the address TFT 26 so as to be operated simultaneously with that TFT by the application of a (gating) pulse selection signal applied to the row conductor 12.

A photodiode 45 is connected between the current line 32 associated with the pixel and the node between the TFTs 26 and 40. The pixel is constructed in such a way that the photodiode 45 is exposed to light emitted by the display element 20 of the pixel. The purpose of such optical coupling 30 between these components will become apparent from the following description of the operation of this pixel.

WO 01/15232 PCT/EP00/07520

9

In this device, the data signals applied to the pixels via the column conductors 14 comprise analogue current signals rather than voltage signals. Active matrix electroluminescent devices using current rather than voltage data signals are known, an example of such being described in WO99/65012 (PHB 34253)

As with the known pixel circuit, this pixel circuit has two states, an addressing state in which the pixel is set to the desired display output condition and a driving state in which the display element is thereafter driven according to the set condition until the pixel is again addressed in the 10 subsequent field. In the addressing state, the row driver circuit 16 applies a selection pulse signal to the row conductor 12 in a respective row address period which turns on the TFTs 26 and 40. The capacitor 36 is assumed here for example to be fully discharged at this time. In the addressing phase, a current is sunk in the associated column conductor 14 according to the applied data signal. The charge path is from the current line 32 through the storage capacitor 36 and the photodiode 45 in parallel. As the photodiode is reversed biased it has a high impedance in this initial period. Consequently, the storage capacitor 36 starts to charge through the TFTs 26 and 40 and the voltage between the source and gate of the drive TFT 22 increases. When the threshold level of the TFT 22 is reached the TFT 22 begins to conduct resulting in a current flow through the display element 20 and generation of light thereby to produce a display output. Some of the light emitted by the conducting display element 20 falls upon the photodiode 45, as a result the appropriate physical arrangement of these two components with respect to each other, which causes the photodiode 45 to start to conduct a photocurrent. The extent of photocurrent is proportional to the light level (quantity of photons/second) received thereby even though it is reverse biased. The photodiode 45 then shunts current from the capacitor 36. After a short time, still within the row address period, an equilibrium state is achieved in which the 30 current being sunk by the column conductor 14 is all shunted by the photodiode alone and the gate voltage of the drive TFT 22 stabilises. Thus,

15

25

PCT/EP00/07520

10

the light from the display element 20 is used as a feedback variable, via the photodiode 45, in the setting of the pixel during addressing.

The pixel circuit is then switched to its drive state by the turning off of the TFTs 26 and 40, upon termination of the row selection pulse, to isolate electrically the node between the gate of the TFT 22 and the storage capacitor 36 from the photodiode 45 and column conductor 14. The capacitor 36 now acts to store the gate-source voltage of the TFT 22 as an adjusted drive signal level determining the current drive level of the display element in the drive (display) phase until the pixel is next addressed. This results in a steady current flowing through the display element 20 throughout this drive period. As light from the display element is used as a feedback variable in the setting of the pixel, the light output (photons) per second during the drive phase is fixed according to a desired output light level, and is proportional to the input current.

By using the light output from the display element in this manner during addressing, the setting of the pixel is made dependent on the instantaneous light output generating characteristic of the associated display element and the drive signal voltage stored on the capacitor 36, and the consequential level of current through the display element determined by the TFT 22, is automatically adjusted accordingly so as to compensate for the effects of ageing in the display element. If the light output level for a given drive current in a display element is reduced due to ageing, then the adjusted stored drive signal will cause the display element to be driven at a appropriately higher current level to maintain the desired display effect.

If the capacitor is charged at the start of the addressing phase rather than being fully discharged, and the addressing current (data signal) is zero, the photocurrent in the photodiode 45 will discharge the capacitor 36 until there is no light output from the display element 20 during this phase, and no light would be emitted in the driving phase.

Besides compensating for such effects, the pixel circuit is also effective to compensate automatically for variations in the operational characteristics of the TFTs 22 of different pixels in the array resulting, for example, from

20

PCT/EP00/07520

variations in their threshold voltages, dimensions, and mobilities due to the nature of the thin film fabrication processes used to form the TFTs. As a result, further improvement in the uniformity of light output from the display elements over the array is achieved

The TFTs used in the above embodiment of pixel circuit all comprise pchannel MOS TFTs. However, n-channel MOS TFTS could be used instead, with the polarity of the display element 20 and photodiode 45, and the applied drive voltages being reversed. Preferably, polysilicon TFTs are used, although alternatively amorphous silicon TFTs could be employed.

The photodiode 45 may be replaced by a phototransistor (diodeconnected) or possibly a photoresistor or other suitable photo-electric device.

Although the photodiode 45 is arranged so that it is exposed to light emitted by the display element 20, it is preferably shielded from ambient light falling on the device so that it is responsive in operation solely to light from the display element.

While the current lines in the above embodiment extend in the row direction and are shared by respective rows of pixels, they may instead extend in the column direction with each current line then being shared by a respective column of pixels.

In summary, therefore, there has been disclosed an active matrix electroluminescent display device which comprises an array of display pixels which each include a current-driven electroluminescent display element connected to a driving device controlling the current flowing through the display element in a drive period according to a voltage stored on a 25 capacitance determined by a data signal applied in a preceding address period. In order to compensate for ageing effects in the display element, electro-optic means are included in the pixel for adjusting the voltage stored on the capacitance in dependence on light output of its display element during the

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the field of active matrix

PCT/EP00/07520

12

electroluminescent display devices and component parts thereof and which may be used instead of or in addition to features already described herein.

20

PCT/EP00/07520

13

CLAIMS

- 1. An active matrix electroluminescent display device comprising an array of display pixels each comprising an electroluminescent display element and a driving device for controlling the current through the display element based on a drive signal applied to the pixel during an address period and stored as a voltage on a storage capacitance connected to the driving device, characterised in that each pixel includes electro-optic adjustment means which is responsive to light produced by the display element during addressing and arranged to adjust in the address period the voltage signal stored on the capacitance in the address period in accordance with the light output level of the display element.
 - An active matrix electroluminescent display device according to Claim 1, characterised in that the electro-optic means regulates a current flowing in the pixel during the address period according to an applied data signal upon which current the voltage stored on the capacitance following the address period is dependent.
- An active matrix electroluminescent display device according to Claim 1, or Claim 2, characterised in that the electro-optic means comprises a photoelectric device arranged to shunt an electrical current flowing through the storage capacitance during addressing according to the display element light output.
 - 4. An active matrix electroluminescent display device according to Claim 3, characterised in that the electro-optic device is connected to the storage capacitance via a switch device which is operated during a pixel address period so as to connect the electro-optic device in parallel with the storage capacitance.

PCT/EP00/67520

WO 01/15232

1/

- 5. An active matrix electroluminescent display device according to Claim 3 or 4, characterised in that the electro-optic device comprises a photodiode.
- 6. An active matrix electroluminescent display device according to anyone of the preceding claims, characterised in that the driving device comprises a thin film transistor.

【国際公開パンフレット(コレクトバージョン)】

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

CORRECTED VERSION

(19) World Intellectual Property Organization International Bureau



(43) International Publication Date 1 March 2001 (01,03,2001)

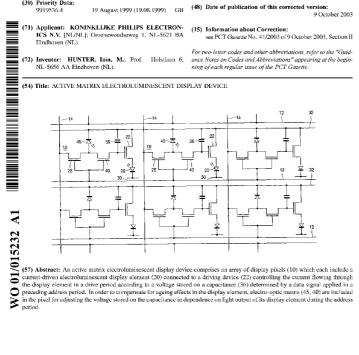
PCT

WO 01/015232 A1

(51) International Patent Classification ⁷ : H01L 27/00 G09G 3/32	, (74) Agent: WILLIAMSON, Paul, L.; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Bindhoven (NL).
(21) International Application Number: PCT/EP00/07520	(81) Designated States (national): JP, KR.
(22) International Filing Date: 2 August 2000 (02.08.2000	(84) Designated States (regional): European patent (A1, BE,
(25) Filing Language: English	CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).
(26) Publication Language: English	Published: with international search report
(30) Priority Data: 9919536.4 19 August 1999 (19.08.1999) GF	(48) Date of publication of this corrected version: 9 October 2003
(71) Applicant: KONINKLIJKE PHILIPS ELECTRON ICS N.V. [NL/NL]; Groenewoodseweg 1, NL-5621 BA	

nΠ

(72) Inventor: HUNTER, Iain, M.; Prof. Holsilaan 6, NL-5656 ΔΛ Eindhoven (NL).
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.



PCT/EP00/07520

DESCRIPTION

ACTIVE MATRIX ELECTROLUMINESCENT DISPLAY DEVICE

1

This invention relates to active matrix electroluminescent display devices comprising an array of electroluminescent display pixels. More particularly, the invention concerns an active matrix electroluminescent display device comprising an array of display pixels each comprising an electroluminescent display element and a driving device for controlling the current through the display element based on a drive signal applied to the pixel during an address period and stored as a voltage on a storage capacitance connected to the driving device.

Matrix display devices employing electroluminescent, light-emitting, display elements are well known. The display elements may comprise organic thin film electroluminescent elements, for example using polymer materials, or else light emitting diodes (LEDs) using traditional III-V semiconductor compounds. Recent developments in organic electroluminescent materials, particularly polymer materials, have demonstrated their ability to be used practically for video display devices. These materials typically comprise one or more layers of an electroluminescent material, for example a semiconducting conjugated polymer, sandwiched between a pair of electrodes, one of which is transparent and the other of which is of a material suitable for injecting holes or electrons into the polymer layer. The polymer material can be fabricated using a CVD process, or simply by printing or a spin coating technique using a solution of a soluble conjugated polymer.

Organic electroluminescent materials exhibit diode-like I-V properties, so that they are capable of providing both a display function and a switching function, and can therefore be used in passive type displays.

PCT/EP00/07520

2

However, the invention is concerned with active matrix display devices, with each pixel comprising a display element and a switching device for controlling the current through the display elements. Examples of an active matrix electroluminescent display are described in EP-A-0653741 and EP-A-0717446. Unlike active matrix liquid crystal display devices in which the display elements are capacitive and therefore take virtually no current and allow a drive signal voltage to be stored on the capacitance for the whole field period, the electroluminescent display elements need to continuously pass current to generate light. A driving device of a pixel, usually comprising a TFT (thin film transistor), is responsible for controlling the current through the display element. The brightness of the display element is proportional to the current flowing through it. During an address period for a pixel, a drive (data) signal in the form of a voltage or current signal determining the required output from the display element is applied to the pixel and stored as a corresponding voltage level on a storage capacitance which is connected to, and controls the operation of, the current controlling drive device with the voltage stored on the capacitance serving to maintain operation of the switching device in supplying current through the display element during the period, corresponding to a field period, until the pixel is addressed again.

A problem with known organic electroluminescent materials, particularly polymer materials, is that they suffer ageing effects whereby the light output for a given drive current is reduced over a period of time of operation. While in certain applications such ageing effects may not be critical, the consequences in a pixellated display can be serious as any slight variations in light output from pixels can easily be perceived by a viewer.

It is an object of the present invention to provide an active matrix electroluminescent display device in which this problem is overcome at least to an extent

According to the present invention there is provided an active matrix electroluminescent display device comprising an array of display pixels each comprising an electroluminescent display element and a driving device for

PCT/EP00/07520

3

controlling the current through the display element based on a drive signal applied to the pixel during an address period and stored as a voltage on a storage capacitance connected to the driving device, which is characterised in that each pixel includes electro-optic adjustment means which is responsive to light produced by the display element during addressing and arranged to adjust in the address period the voltage signal stored on the capacitance in accordance with the light output level of the display element.

Thus, by means of the electro-optic adjustment means, the stored signal voltage for determining the light output level of the display element in the drive (display) period following addressing is adjusted according to the light output characteristic of the display element, providing a feedback variable, whereby the drive level set on the pixel can compensate for the effects of ageing of the display elements so that a desired light output level from a display element for a given applied drive signal is substantially maintained regardless of possible variations in the drive current level / light output level characteristics of individual display elements in the array.

In the case where the drive device of a pixel comprises a TFT (thin film transistor) as is usual in active matrix electroluminescent display devices, the invention offers a further important advantage. The drive current for a display element is determined by the voltage applied to the gate of the TFT, corresponding to the voltage stored in the capacitance. This drive current therefore depends strongly on the characteristics of the TFT and variations in the threshold voltage, mobility and dimensions of the individual TFTs of pixels over the array, for example due to manufacturing processes, can produce unwanted variations in the display element currents and hence light levels produced, leading to non-uniformity in the display output. The effect of the electro-optic adjustment means in controlling the stored voltage signal will also compensate for such variations in TFT characteristics.

Although the invention is particularly beneficial in devices using polymer 30 LED materials, it can of course be applied to advantage in any electroluminescent device in which the electroluminescent material similarly

PCT/EP00/07520

4

suffers ageing effects resulting in lower light output levels for a given drive current over a period of time of operation.

Preferably the electro-optic means regulates a current flowing in the pixel during the address period according to an applied data signal upon which current the voltage stored on the capacitance following the address period is dependent.

In a preferred embodiment, the electro-optic means comprises a photoelectric device connected to the storage capacitance via a switch device, for example another TFT, which is arranged to be closed during the address period so as to connect the photoelectric device in parallel with the storage capacitance during the address period. During the driving period, the device is effectively disconnected from the storage capacitance and plays no part in the operation of the pixel. In the address period, and with the data signal comprising a current signal, the device serves to shunt current from the capacitance in dependence upon the display element's light output until an equilibrium state is reached and the capacitance voltage, and the gate voltage of the drive TFT, stabilises.

The photoelectric device preferably comprises a photodiode, although a photoresistor or phototransistor could alternatively be employed.

20

An embodiment of an active matrix electroluminescent display device in accordance with the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a simplified schematic diagram of a known active matrix electroluminescent display device comprising an array of pixels;

Figure 2 shows the equivalent circuit of a few typical pixels of the known active matrix electroluminescent display device of Figure 1; and

Figure 3 shows the equivalent circuit of a few typical pixels in an embodiment of active matrix electroluminescent display device according to the invention.

The Figures are merely schematic. The same reference numbers are used throughout the Figures to denote the same or similar parts.

PCT/EP00/07520

5

Referring to Figure 1, the active matrix electroluminescent display device comprises a panel having a row and column matrix array of regularly-spaced pixels, denoted by the blocks 10, each comprising an electroluminescent display element and an associated driving device controlling the current through the display element, and which are located at the intersections between crossing sets of row (selection) and column (data) address conductors, or lines, 12 and 14. Only a few pixels are shown here for simplicity. The pixels 10 are addressed via the sets of address conductors by a peripheral drive circuit comprising a row, scanning, driver circuit 16 and a column, data, driver circuit 18 connected to the ends of the respective sets.

Each row of pixels is addressed in turn by means of a selection signal applied by the circuit 16 to the relevant row conductor 12 so as to load the pixels of the row with respective drive signals, determining their individual display outputs, according to the respective data signals supplied in parallel by the circuit 18 to the column conductors. As each row is addressed, the appropriate data signals are supplied by the circuit 18 in appropriate synchronisation.

Figure 2 illustrates the circuit of a few, typical, pixels in this known device. In this particular device, the data signals comprise voltage signals. Each pixel, 10, includes a light emitting organic electroluminescent display element 20, represented here as a diode element (LED), and comprising a pair of electrodes between which one or more active layers of organic electroluminescent material is sandwiched. In this particular embodiment the material comprises a polymer LED material, although other organic electroluminescent materials, such as low molecular weight materials, could be used. The display elements of the array are carried together with the associated active matrix circuitry on one side of an insulating support. Either the cathodes or the anodes of the display elements are formed of transparent conductive material. The support is of transparent material such as glass and the electrodes of the individual display elements 20 closest to the substrate can consist of a transparent conductive material such as ITO so that light

PCT/EP00/07520

6

generated by the electroluminescent layer is transmitted through these electrodes and the support so as to be visible to a viewer at the other side of the support. Alternatively, the light output could be viewed from above the panel and the display element anodes in this case would comprise parts of a continuous ITO layer constituting a supply line common to all display elements in the array. The cathodes of the display elements comprise a metal having a low work-function such as calcium or magnesium silver alloy. Examples of suitable organic conjugated polymer materials which can be used are described in WO 96/36959. Examples of other, low molecular weight, organic materials are described in EP-A-0717446, which also describes examples of the construction and operation of an active matrix electroluminescent device and whose disclosure in these respects is incorporated herein by reference.

Each pixel 10 includes a drive device in the form of a TFT 22 which controls the operation of the display element 20 based on an analogue data signal voltage applied to the pixel. The signal voltage for a pixel is supplied via a column conductor 14 which is shared between a respective column of pixels. The column conductor 14 is coupled to the gate of the current-controlling drive transistor 22 through an address TFT 26. The gates for the address TFTs 26 of a row of pixels are coupled together to a common row conductor 12.

Each row of pixels 10 also shares a common voltage supply line 30, usually provided as a continuous electrode common to all pixels, and a respective common current line 32. The display element 20 and the drive device 22 are connected in series between the voltage supply line 30 and the common current line 32, which is at a positive potential with respect to the supply line 30 and acts as a current source for the current flowing through the display element 20. The current flowing through the display element 20 is controlled by the switching device 22 and is a function of the gate voltage on the transistor 22, which is dependent upon a stored control signal determined by the data signal supplied to the column conductor 14.

A row of pixels is selected by the row driver circuit 16 applying a selection pulse to the row conductor 12 which switches on the address TFTs 26 for the respective row of pixels. A voltage level derived from the video

PCT/EP00/07520

WO 01/015232

20

7

information is applied to the column conductor 14 by the driver circuit 18 and is transferred by the address TFT 26 to the gate of the drive transistor 22. During the periods when a row of pixels is not being addressed via the row conductor 12 the address transistor 26 is turned off, but the voltage on the gate of the drive transistor 22 is maintained by a pixel storage capacitor 36 which is connected between the gate of the drive transistor 22 and the common current line 32. The voltage between the gate of the drive transistor 22 and the common current line 32 determines the current passing through the display element 20 of the pixel 10. Thus, the current flowing through the display element is a function of the gate-source voltage of the drive transistor 22 (the source of the transistor 22 being connected to the display element 20. This current in turn controls the light output level (grev-scale) of the pixel.

The switching transistor 22 is arranged to operate in saturation, so that the gate-source voltage governs the current flowing through the transistor, irrespectively of the drain-source voltage. Consequently, slight variations of the drain voltage do not affect the current flowing through the display element 20. The voltage on the voltage supply line 30 is therefore not critical to the correct operation of the pixels.

Each row of pixels is addressed in turn in this manner in respective row address periods so as to load the pixels of each row in sequence with their drive signals and set the pixels to provide desired display outputs for the drive (field) period until they are next addressed.

With this known pixel circuit, it will be appreciated that the voltage

stored on the capacitor 36 is substantially determined by the applied data
signal voltage and that as this voltage in turn controls the drive transistor 22
and the current through the display element 20 then the resulting light output
level of the display element at any time will be dependent on the then existing
current/light output level characteristic of the display element. The
electroluminescent material of the display element can suffer degradation over
a period time of operation leading to ageing effects which result in a reduction
of the light output level for a given drive current level. Those pixels which

PCT/EP00/07520

8

have, therefore, been driven longer (or harder) will exhibit reduced brightness and cause display non-uniformities. With polymer LED materials the effects of such ageing can be significant.

In the present invention, the drive signal stored in a pixel during the addressing phase is automatically adjusted through electro-optical means in the pixel, acting as a feedback arrangement, according to the light emission characteristic of the display element so as to compensate at least to some extent for such ageing effects and ensure that the required light output level of the display element is produced following addressing.

Referring to Figure 3, there is shown the equivalent circuit of a pixel in an embodiment of display device according to the invention and intended to overcome, at least to some extent, the problem of ageing. In each pixel 10 the display element 20 is again connected in series with the drive transistor 22 between the current line 32 and a voltage supply line 30, here shown constituted by a common electrode layer shared by all the pixels, and the gate and source of address transistor 26 are connected to the associated row and column conductors 12 and 14 respectively. Also the storage capacitor 36 is again connected between the gate of the drive transistor 22 and the current line 32.

The pixel further includes an additional switch device 40, again in the form of a TFT, which is connected between the address TFT 26 and the node between the storage capacitor 36 and the gate of the drive transistor 22 with its gate terminal connected to the same row conductor 12 as the gate of the address TFT 26 so as to be operated simultaneously with that TFT by the application of a (gating) pulse selection signal applied to the row conductor 12.

A photodiode 45 is connected between the current line 32 associated with the pixel and the node between the TFTs 26 and 40. The pixel is constructed in such a way that the photodiode 45 is exposed to light emitted by the display element 20 of the pixel. The purpose of such optical coupling between these components will become apparent from the following description of the operation of this pixel.

PCT/EP00/07520

9

In this device, the data signals applied to the pixels via the column conductors 14 comprise analogue current signals rather than voltage signals. Active matrix electroluminescent devices using current rather than voltage data signals are known, an example of such being described in WO99/65012 (PHB 34253).

As with the known pixel circuit, this pixel circuit has two states, an addressing state in which the pixel is set to the desired display output condition and a driving state in which the display element is thereafter driven according to the set condition until the pixel is again addressed in the subsequent field. In the addressing state, the row driver circuit 16 applies a selection pulse signal to the row conductor 12 in a respective row address period which turns on the TFTs 26 and 40. The capacitor 36 is assumed here for example to be fully discharged at this time. In the addressing phase, a current is sunk in the associated column conductor 14 according to the applied data signal. The charge path is from the current line 32 through the storage capacitor 36 and the photodiode 45 in parallel. As the photodiode is reversed biased it has a high impedance in this initial period. Consequently, the storage capacitor 36 starts to charge through the TFTs 26 and 40 and the voltage between the source and gate of the drive TFT 22 increases. When the 20 threshold level of the TFT 22 is reached the TFT 22 begins to conduct resulting in a current flow through the display element 20 and generation of light thereby to produce a display output. Some of the light emitted by the conducting display element 20 falls upon the photodiode 45, as a result the appropriate physical arrangement of these two components with respect to each other, which causes the photodiode 45 to start to conduct a photocurrent. The extent of photocurrent is proportional to the light level (quantity of photons/second) received thereby even though it is reverse biased. The photodiode 45 then shunts current from the capacitor 36. After a short time, still within the row address period, an equilibrium state is achieved in which the current being sunk by the column conductor 14 is all shunted by the photodiode alone and the gate voltage of the drive TFT 22 stabilises. Thus,

15

25

PCT/EP00/07520

10

the light from the display element 20 is used as a feedback variable, via the photodiode 45, in the setting of the pixel during addressing.

The pixel circuit is then switched to its drive state by the turning off of the TFTs 26 and 40, upon termination of the row selection pulse, to isolate electrically the node between the gate of the TFT 22 and the storage capacitor 36 from the photodiode 45 and column conductor 14. The capacitor 36 now acts to store the gate-source voltage of the TFT 22 as an adjusted drive signal level determining the current drive level of the display element in the drive (display) phase until the pixel is next addressed. This results in a steady current flowing through the display element 20 throughout this drive period. As light from the display element is used as a feedback variable in the setting of the pixel, the light output (photons) per second during the drive phase is fixed according to a desired output light level, and is proportional to the input current.

By using the light output from the display element in this manner during addressing, the setting of the pixel is made dependent on the instantaneous light output generating characteristic of the associated display element and the drive signal voltage stored on the capacitor 36, and the consequential level of current through the display element determined by the TFT 22, is automatically adjusted accordingly so as to compensate for the effects of ageing in the display element. If the light output level for a given drive current in a display element is reduced due to ageing, then the adjusted stored drive signal will cause the display element to be driven at a appropriately higher current level to maintain the desired display effect.

If the capacitor is charged at the start of the addressing phase rather than being fully discharged, and the addressing current (data signal) is zero, the photocurrent in the photodiode 45 will discharge the capacitor 36 until there is no light output from the display element 20 during this phase, and no light would be emitted in the driving phase.

Besides compensating for such effects, the pixel circuit is also effective to compensate automatically for variations in the operational characteristics of the TFTs 22 of different pixels in the array resulting, for example, from

PCT/EP00/07520

11

variations in their threshold voltages, dimensions, and mobilities due to the nature of the thin film fabrication processes used to form the TFTs. As a result, further improvement in the uniformity of light output from the display elements over the array is achieved.

The TFTs used in the above embodiment of pixel circuit all comprise pchannel MOS TFTs. However, n-channel MOS TFTS could be used instead, with the polarity of the display element 20 and photodiode 45, and the applied drive voltages being reversed. Preferably, polysilicon TFTs are used, although alternatively amorphous silicon TFTs could be employed.

The photodiode 45 may be replaced by a phototransistor (diodeconnected) or possibly a photoresistor or other suitable photo-electric device.

Although the photodiode 45 is arranged so that it is exposed to light emitted by the display element 20, it is preferably shielded from ambient light falling on the device so that it is responsive in operation solely to light from the display element.

While the current lines in the above embodiment extend in the row direction and are shared by respective rows of pixels, they may instead extend in the column direction with each current line then being shared by a respective column of pixels.

In summary, therefore, there has been disclosed an active matrix electroluminescent display device which comprises an array of display pixels which each include a current-driven electroluminescent display element connected to a driving device controlling the current flowing through the display element in a drive period according to a voltage stored on a capacitance determined by a data signal applied in a preceding address period. In order to compensate for ageing effects in the display element, electro-optic means are included in the pixel for adjusting the voltage stored on the capacitance in dependence on light output of its display element during the address period.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the field of active matrix

WO 01/015232 PCT/EP00/07520

12

electroluminescent display devices and component parts thereof and which may be used instead of or in addition to features already described herein.

PCT/EP00/07520

13

CLAIMS

20

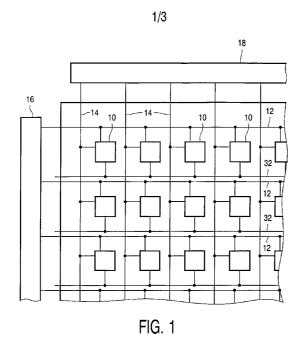
- 1. An active matrix electroluminescent display device comprising an array of display pixels each comprising an electroluminescent display element and a driving device for controlling the current through the display element based on a drive signal applied to the pixel during an address period and stored as a voltage on a storage capacitance connected to the driving device, characterised in that each pixel includes electro-optic adjustment means which is responsive to light produced by the display element during addressing and arranged to adjust in the address period the voltage signal stored on the capacitance in the address period in accordance with the light output level of the display element.
- 2. An active matrix electroluminescent display device according to Claim 1, characterised in that the electro-optic means regulates a current flowing in the pixel during the address period according to an applied data signal upon which current the voltage stored on the capacitance following the address period is dependent.
- An active matrix electroluminescent display device according to Claim 1, or Claim 2, characterised in that the electro-optic means comprises a photoelectric device arranged to shunt an electrical current flowing through the storage capacitance during addressing according to the display element light output.
- 4. An active matrix electroluminescent display device according to Claim 3, characterised in that the electro-optic device is connected to the storage capacitance via a switch device which is operated during a pixel address period so as to connect the electro-optic device in parallel with the storage capacitance.

PCT/EP00/07520

14

- An active matrix electroluminescent display device according to Claim 3 or 4, characterised in that the electro-optic device comprises a photodiode.
- An active matrix electroluminescent display device according to anyone of the preceding claims, characterised in that the driving device comprises a thin film transistor.

PCT/EP00/07520



.

WO 01/015232 PCT/EP00/07520

2/3

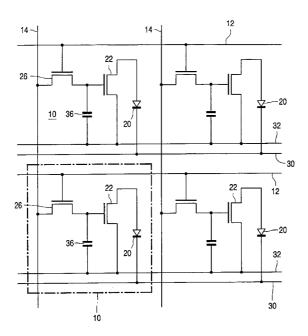
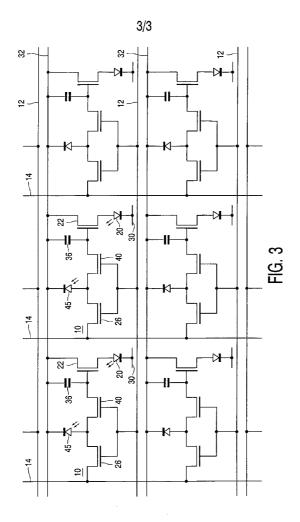


FIG. 2

PCT/EP00/07520



【国際調査報告】

	INTERNATIONAL SEARCH I	PEPORT _		
	INTERNATIONAL SEARCH	CLI ONI	Internati-	Application No
			PCT/EP	00/07520
A. CLASSI IPC 7	FICATION OF SUBJECT MATTER H01L27/00 G09G3/32			
According to	o International Patent Classification (IPC) on to both national classifica	tion and IPC		
B. FIELDS	SEARCHED			
Minimum do	ocumentation searched. (classification system followed by classification HOTL G09G	in symbols)		
Documenta	tion searched other than minimum documentation to the extent that so	uch documents are incl	ided in the fle	elds searched
Electronic d	ata base consulted during the international search (name of data bas	se and, where practical	search terms	used)
INSPEC	, EPO-Internal, PAJ			
C. DOCUM	ENTS CONSIDERED TO BE RELEVANT			
Category °	Citation of document, with indication, where appropriate, of the rele	ovant passages		Relevant to claim No.
χ	EP 0 923 067 A (SEIKO EPSON CORP)			1-3,5,6
γ	16 June 1999 (1999-06-16) paragraphs '0081!-'0098!			4
P,Y	WO 99 65012 A (PHILIPS ELECTRONIC	S NV;		4
	PHILIPS AB) 16 December 1999 (199 cited in the application the whole document			
А	WO 99 40559 A (PHILIPS ELECTRONIC PHILIPS AB) 12 August 1999 (1999- the whole document			1
A	EP 0 845 812 A (CASIO COMPUTER CO 3 June 1998 (1998-06-03) page 7, 11ne 2-35	LTD)		1
		./		
		′		
X Fun	ther documents are listed in the continuation of box C.	X Patent family	members are	Hsted in annex.
'A' docum consi E' aartier filing 'L' docum which citatie 'O' docum	ent defining the general state of the lad which is not detect to be of particular relevance document but published on or after the international date ent which may throw doubts on priority claim(s) or	The late document justicities of the flux international filing date are notified as also not no central until this application but clied to understand the principle or theory underlying the invention. **Z document of particular relevance; the claimed invention cannot be considered not exceeded to the claim of the control and considered notification to considered notification and the observation and the observation are relevance in the claimed invention. **Z document of particular relevance; the claimed invention of the claimed invention to the control of the claimed invention to the control of the claimed invention to the claimed inven		
latert		in the art. *&* document member of the same patent family Date of mailing of the international search report		
	actual completion of the international search December 2000	12/12/2		іві зевісні гэрогі
	mailing address of the ISA	Authorized efficer		
	European Patent Office, P.S. 5818 Patentisan 2 NL – 2280 HV Piswrijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl. Fax: (+31–70) 340–3016	van der Linden, J.E.		

Tel. (+31-70), 340-2040, 1 Fac: (+31-70), 340-3016 Form PCT/ISA/210 (second sheet) (July 1992)

page 1 of 2

	INTERNATIONAL SEARCH REPORT		
	INTERNATIONAL SEARCH REPORT		cation No
		PCT/EP 00/	07520
	(Ion) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication,where appropriate, of the relevant passages	ĮF	Relevant to claim No.
A	EP 0 180 642 A (JAPAN TRAFFIC MANAG ET AL) 14 May 1986 (1986-05-14) the whole document		1
A	PATENT ABSTRACTS OF JAPAN vol. 013, no. 567 (M-908), 15 December 1989 (1989-12-15) & JP 01 238962 A (NIPPON SHEET GLASS CO), 25 September 1989 (1989-09-25) abstract		1

page 2 of 2

INTERNATIONAL SEARCH REPORT

	In.	nation on patent family members			Internat!	Application No	
		,			PCT/EP	00/07520	
Patent document cited in search report		Publication date		Patent family member(s)		Publication date	
EP 0923067	Α	16-06-1999	WO	984087	71 A	17-09-1998	
WO 9965012	A	16-12-1999	EΡ	103452	29 A	13-09-2000	
WO 9940559	A	12-08-1999	EP US	097414 614416		26-01-2000 07-11-2000	
EP 0845812	A	03-06-1998	JP JP US	1016156 1016295 607245	58 A	19-06-1998 19-06-1998 06-06-2000	
EP 0180642	A	14-05-1986	JP JP JP WO KR	202278 702398 6017739 850379 890518	37 B 95 A 95 A	26-02-1996 15-03-1995 11-09-1985 29-08-1985 16-12-1989	
JP 01238962	A	25-09-1989	JP DE DE EP EP US US	25770: 689290: 689290: 03355! 09172: 09172: 54519: 58148:	71 D 71 T 53 A 12 A 13 A 77 A	29-01-1997 21-10-1999 03-02-2000 04-10-1989 19-05-1999 19-05-1999 19-09-1995 29-09-1998	

フロントページの続き

(51) Int.CI.⁷ F I テーマコード (参考)

H 0 1 L 33/00 J H 0 5 B 33/14 A

(72)発明者 イアイン エム ハンター

オランダ国 5656 アーアー アインドーフェン プロフ ホルストラーン 6

F ターム(参考) 3K007 AB02 AB17 DB03 GA04

5C080 AA06 BB05 CC03 DD04 DD05 DD29 EE28 FF11 HH11

5C094 AA03 AA53 AA55 BA03 BA27 CA19 GA10

5F041 BB24 BB26 BB27 BB33 BB34 CA34 FF06



专利名称(译)	有源矩阵电致发光显示装置						
公开(公告)号	JP2004510999A	公开(公告)日	2004-04-08				
申请号	JP2001519495	申请日	2000-08-02				
[标]申请(专利权)人(译)	皇家飞利浦电子股份有限公司						
申请(专利权)人(译)	皇家飞利浦电子股份有限公司的Vie						
[标]发明人	イアインエムハンター						
发明人	イアイン エム ハンター						
IPC分类号	H01L51/50 G09F9/30 G09G3/20 G09G3/30 G09G3/32 H01L27/32 H01L33/00 H05B33/14						
CPC分类号	G09G3/32 G09G3/3233 G09G2300/0809 G09G2300/0819 G09G2300/0842 G09G2300/088 G09G2320 /043 G09G2320/045 G09G2360/148 H01L27/3269						
FI分类号	G09G3/30.J G09F9/30.338 G09F9/30.365.Z G09G3/20.624.B G09G3/20.670.J H01L33/00.J H05B33 /14.A						
F-TERM分类号	3K007/AB02 3K007/AB17 3K007/DB03 3K007/GA04 5C080/AA06 5C080/BB05 5C080/CC03 5C080 /DD04 5C080/DD05 5C080/DD29 5C080/EE28 5C080/FF11 5C080/HH11 5C094/AA03 5C094/AA53 5C094/AA55 5C094/BA03 5C094/BA27 5C094/CA19 5C094/GA10 5F041/BB24 5F041/BB26 5F041 /BB27 5F041/BB33 5F041/BB34 5F041/CA34 5F041/FF06						
优先权	1999019536 1999-08-19 GB						
其他公开文献	JP4393740B2						
外部链接	<u>Espacenet</u>						

摘要(译

有源矩阵发光显示器件中,每个包括包含电流驱动发光显示装置(20)显示像素的阵列(10),所述显示装置是由在前面的地址期间施加的数据信号来确定根据电容(36)中累积的电压,驱动周长用于控制流过显示元件的电流的驱动装置(22)在该时段中连接。光学装置(45,40),用于在访问期间根据显示元件的光输出调节电容中累积的电压,以补偿显示元件中老化的影响。

