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(54) **LIQUID CRYSTAL DISPLAY DEVICE**

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(57) **ABSTRACT**

A liquid crystal display device includes a first substrate, a gate line and a first data line disposed on the first substrate and insulated from each other, a first thin film transistor connected to the gate line and the first data line, a lower pixel electrode connected to the first thin film transistor, an interlayer insulating layer disposed on the lower pixel electrode, an upper pixel electrode disposed on the interlayer insulating layer and connected to the first thin film transistor and the lower pixel electrode, a second substrate facing the first substrate, a common electrode disposed on the second substrate, and a liquid crystal layer disposed between the first substrate and the second substrate. The upper pixel electrode includes a plurality of minute branches. A ratio of an interval between the minute branches with respect to a thickness of the liquid crystal layer is 2.7 to 5.0.

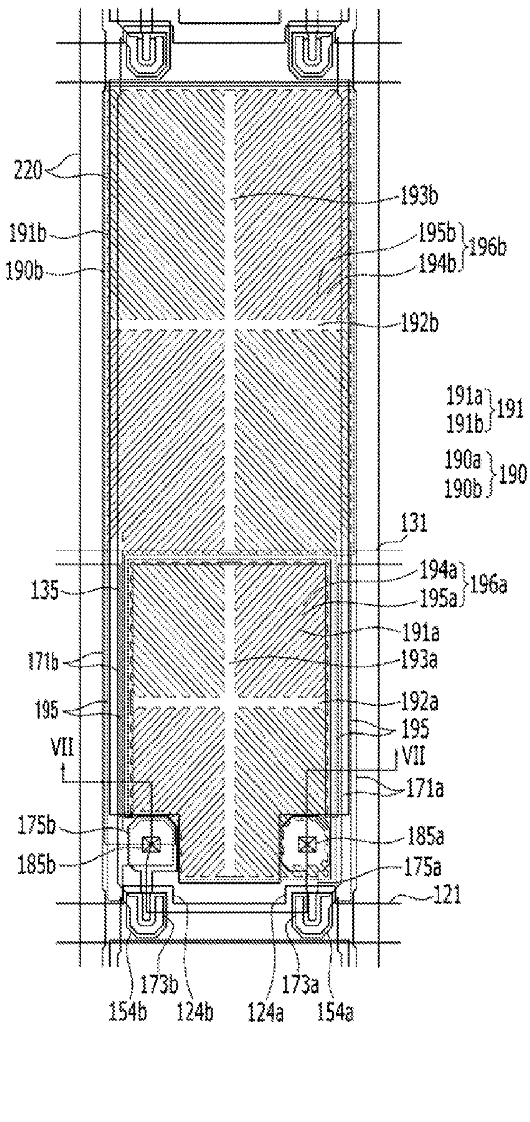


FIG. 1

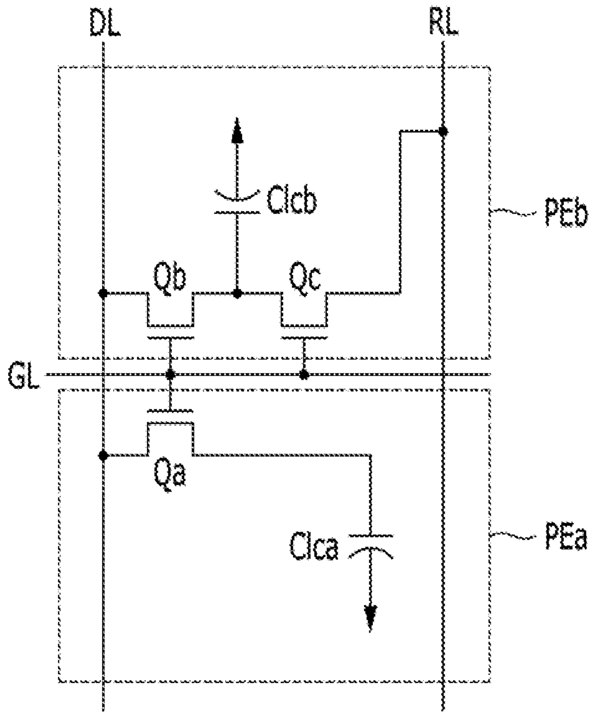
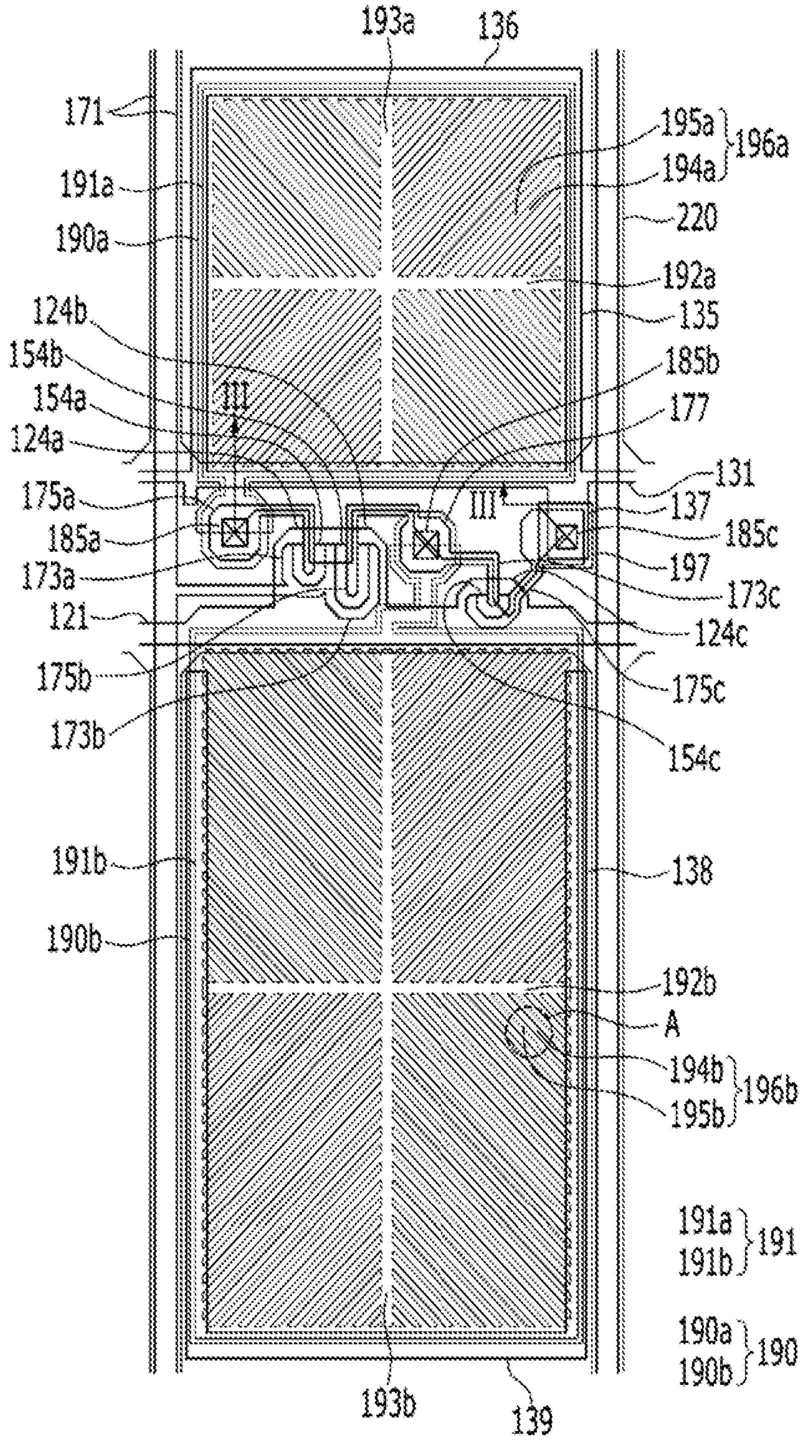


FIG. 2


193a
136
171
195a
194a
196a
191a
190a
220
192a
135
124b
154b
185b
154a
177
III
124a
131
175a
137
III'
185c
185a
197
173a
173c
121
124c
175b
175c
173b
154c
191b
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191b
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190b
190
193b
139

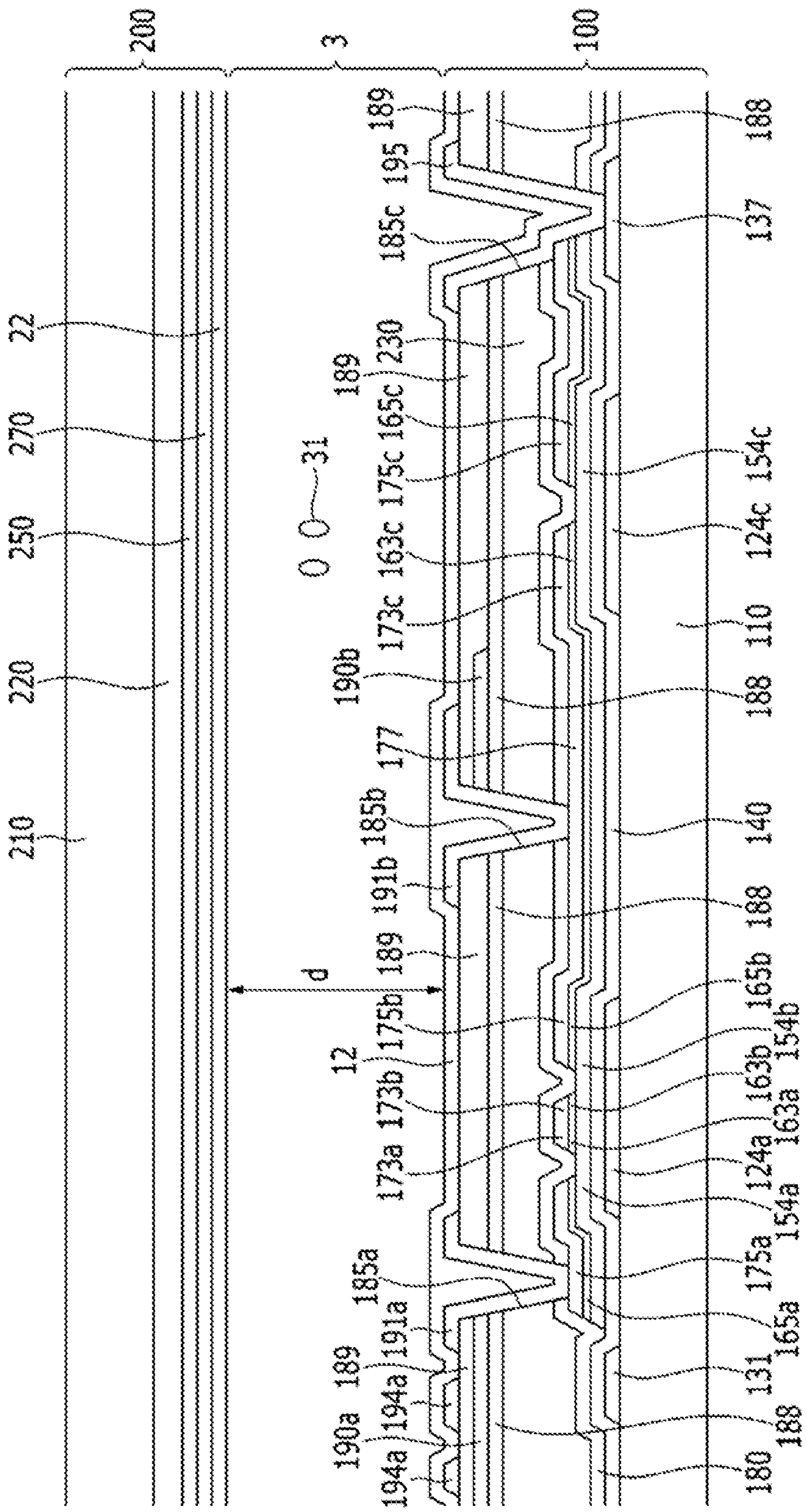

200
3
100
22
270
250
220
210
31
d
12
189
195
185c
230
165c
175c
163c
173c
190b
177
185b
191b
175b
173b
173a
185a
191a
194a
190a
188
137
154c
124c
110
140
165b
154b
163b
163a
124a
154a
175a
165a
131
180

FIG. 3

FIG. 4

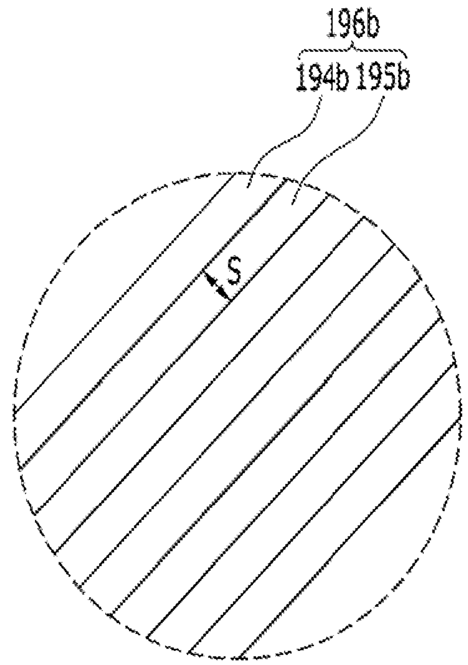


FIG. 5

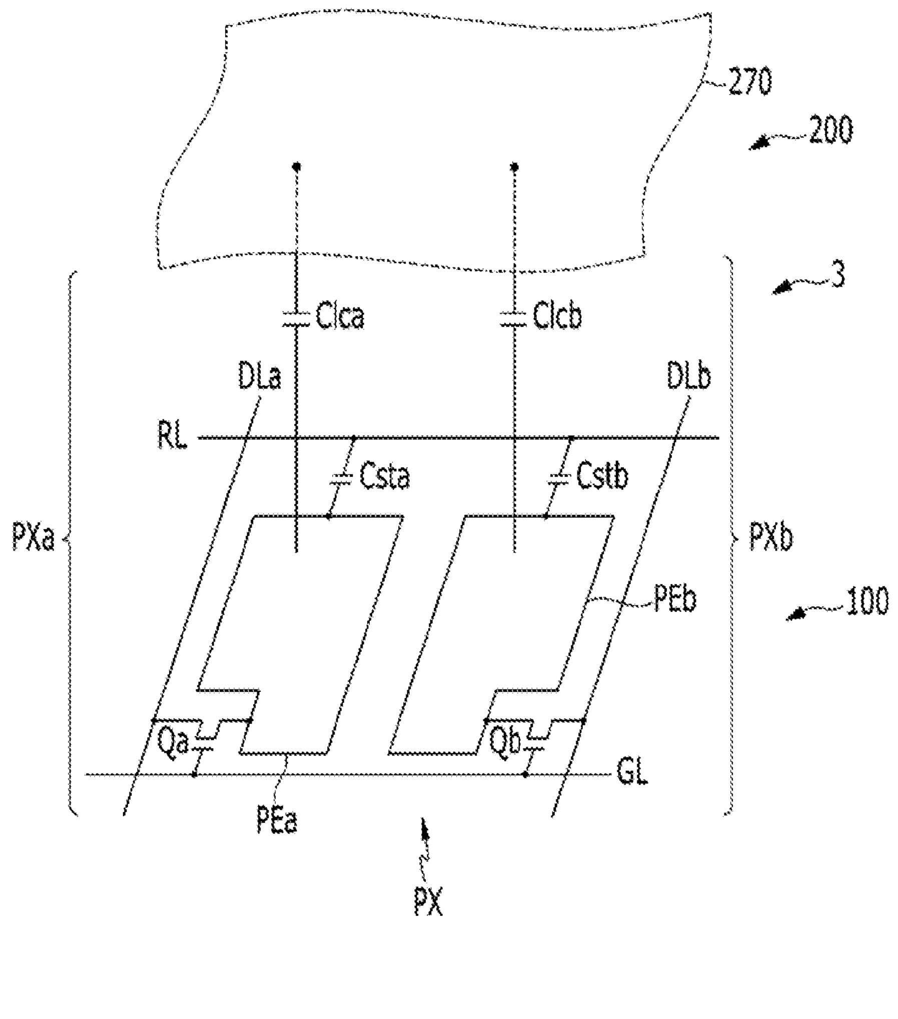
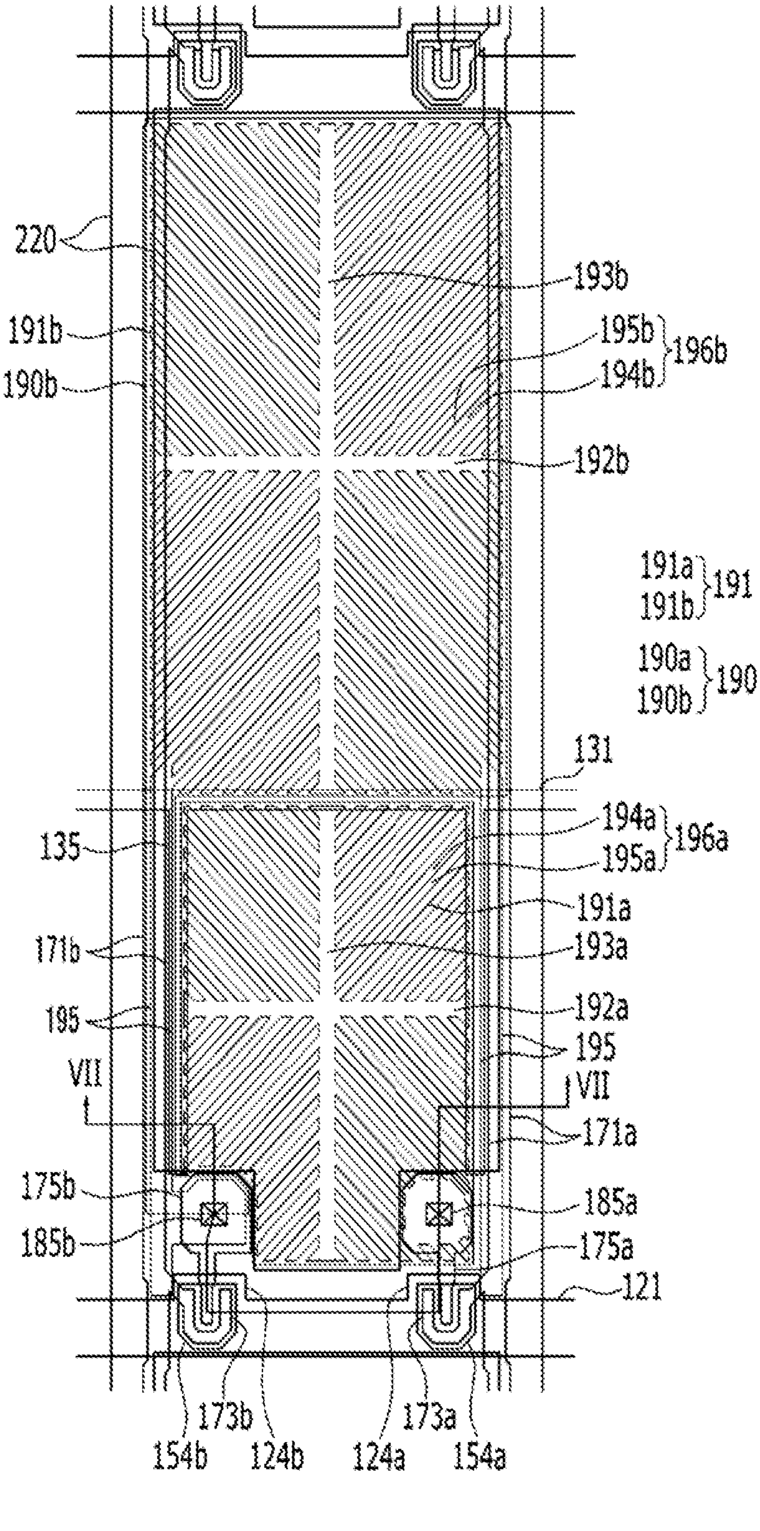

270
200
3
Clca
Clcb
DLa
DLb
RL
Csta
Cstb
PXa
PXb
PEb
100
Qa
Qb
GL
PEa
PX

FIG. 6



220
191b
190b
193b
195b
194b
196b
192b
191a
191b
191
190a
190b
190
131
135
194a
195a
196a
191a
193a
171b
195
192a
195
VII
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185b
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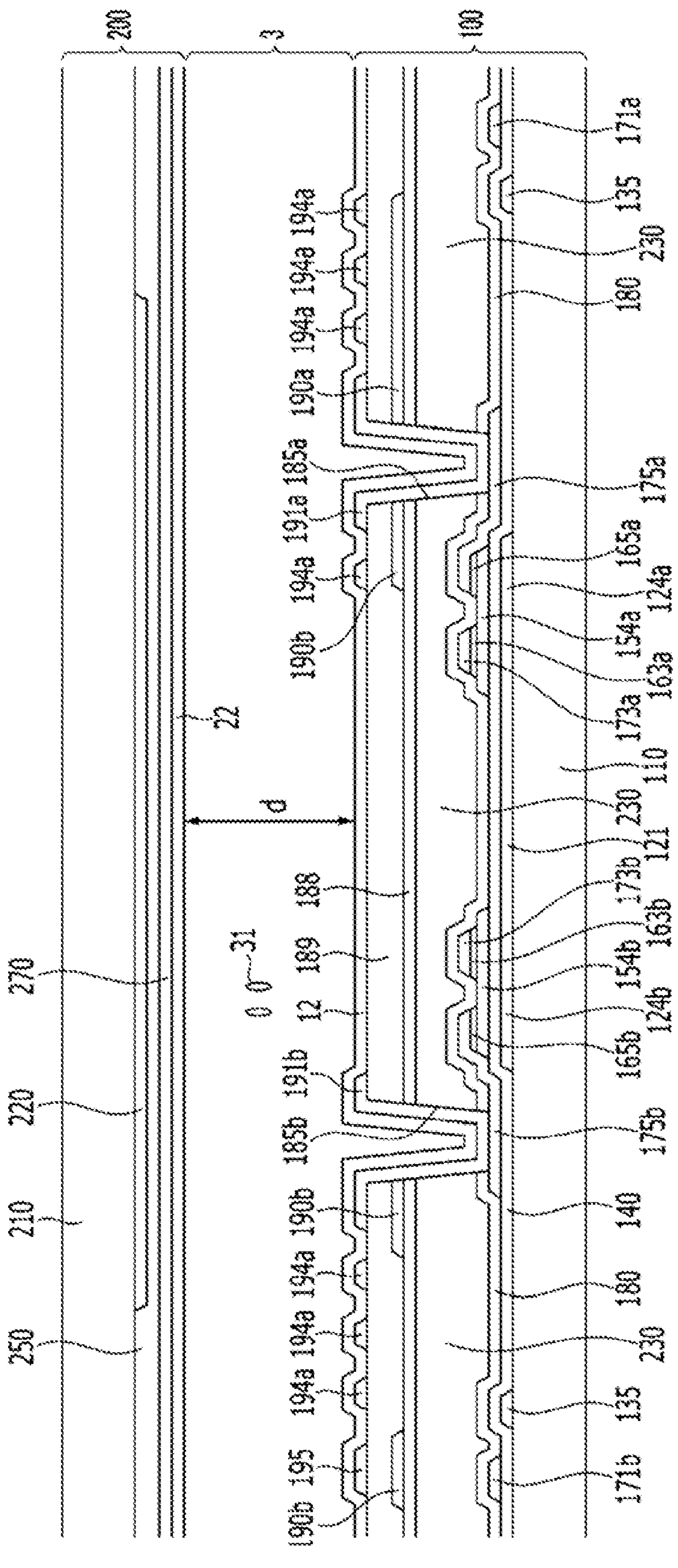
121
173b
173a
154b
124b
124a
154a

FIG. 7


200
3
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220
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250
22
d
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12
189
188
190b
195
194a
190a
185a
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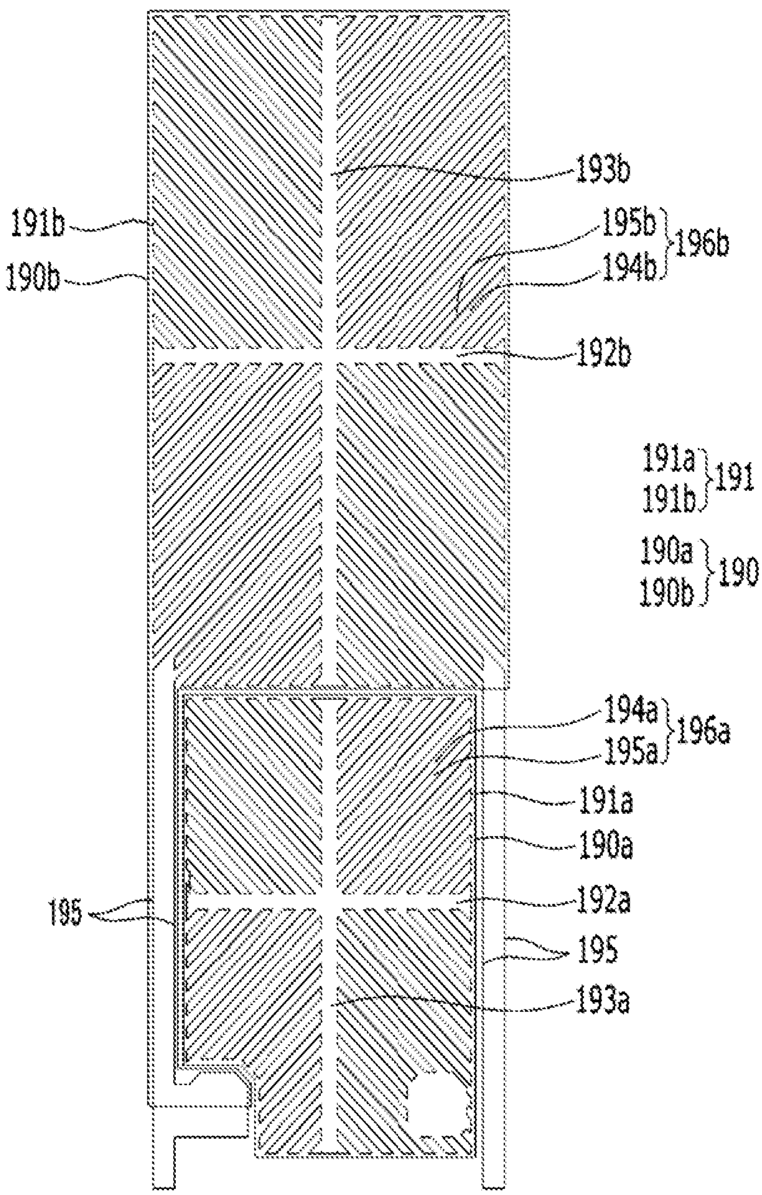
191b
185b
171a
135
230
180
175a
165a
124a
154a
163a
173a
110
121
173b
163b
154b
124b
165b
175b
140
171b

FIG. 8


193b
191b
195b
196b
190b
194b
192b
191a
191b
191
190a
190b
190
194a
196a
195a
191a
190a
195
192a
195
193a

LIQUID CRYSTAL DISPLAY DEVICE

CLAIM OF PRIORITY

[0001] This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. §119 from an application earlier filed in the Korean Intellectual Property Office on 16 Jan. 2015 and there duly assigned Serial No. 10-2015-0008147.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display device.

[0004] 2. Description of the Related Art

[0005] A liquid crystal display device is one of the flat panel displays which are most widely used in recent years and includes two display panels in which a field generating electrode such as a pixel electrode and a common electrode is formed and a liquid crystal layer interposed between the display panels.

[0006] A voltage is applied to the field generating electrode to generate an electric field in the liquid crystal layer, and an orientation of liquid crystal molecules of the liquid crystal layer is determined therethrough, and polarization of incident light is controlled to display an image.

[0007] Among the liquid crystal displays, a vertically aligned (VA) mode liquid crystal display in which a major axis of the liquid crystal molecule is arranged to be vertical to upper and lower display panels in a state where no electric field is applied is getting the spotlight because it has a high contrast ratio and easily achieves a wide reference viewing angle.

[0008] In order to achieve a wide viewing angle in such a vertically aligned (VA) mode liquid crystal display, a plurality of domains having different liquid crystal alignment directions may be formed in one pixel.

[0009] As described above, in order to firm the plurality of domains, a method of forming a cutout such as a minute slit in the field generating electrode or a method of forming, a protrusion on the field generating electrode is used. According to this method, the liquid crystals are aligned to be vertical to the fringe field which is formed between an edge of the cutout or the protrusion and the field generating electrode, which faces the edge, thereby forming a plurality of domains.

[0010] In the meantime, when the plurality of slits is formed in the field generating electrode, transmittance in a portion where the slit is formed is undesirably lowered.

[0011] The above information disclosed in this Background section is only for enhancement of understanding of the background of the invention and therefore it may contain information that does not farm the prior art that is already known in this country to a person of ordinary skill in the art.

SUMMARY OF THE INVENTION

[0012] The present invention has been made in an effort to improve the quality of as liquid crystal display device.

[0013] An object of the present invention is to improve transmittance of a liquid crystal display device in which a plurality of minute slits is formed in a field generating electrode.

[0014] A liquid crystal display device according to an exemplary embodiment of the present invention includes a first substrate, a gate line, and a first data line which are disposed on the first substrate and are insulated from each other, a first thin film transistor which is connected to the gate line and the first data line, a lower pixel electrode which is connected to the first thin film transistor, an interlayer insulating layer which is disposed on the lower pixel electrode, an upper pixel electrode which is disposed on the interlayer insulating layer and is connected to the first thin film transistor and the lower pixel electrode, a second substrate which faces the first substrate, a common electrode which is disposed on the second substrate, and a liquid crystal layer which is disposed between the first substrate and the second substrate, and the lower pixel electrode and the upper pixel electrode overlap each other, the upper pixel electrode includes a plurality of minute branches, the lower pixel electrode has a whole plate shape in plan view, and a ratio of an interval between the minute branches with respect to a thickness of the liquid crystal layer is 2.7 to 5.0.

[0015] The liquid crystal layer may include liquid crystal molecules having a negative dielectric anisotropy.

[0016] The lower pixel electrode may include a first lower subpixel electrode and a second lower subpixel electrode which are separated from each other, and the upper pixel electrode may include a first upper subpixel electrode and a second upper subpixel electrode which are separated from each other.

[0017] The first lower subpixel electrode and the first upper subpixel electrode may overlap each other and the second lower subpixel electrode and the second upper subpixel electrode may overlap each other.

[0018] Each of the first upper subpixel electrode and the second upper subpixel electrode may include as cross-shaped stein portion which is formed of a horizontal stem portion and a vertical stem portion that intersects the horizontal stem portion and the minute branch may extend from the cross-shaped stem portion.

[0019] The liquid, crystal display according to the exemplary embodiment of the present invention may further include as second thin film transistor which is connected to the gate line and the first data line and as third thin film transistor which is connected to an output terminal of the second thin film transistor.

[0020] The first lower subpixel electrode and the first upper subpixel electrode may be connected to the first thin film transistor and the second lower subpixel electrode and the second upper subpixel electrode may be connected to the second thin film transistor.

[0021] The liquid crystal display according to the exemplary embodiment of the present invention may further include a reference voltage, line which is connected to an output terminal of the third thin film transistor.

[0022] The liquid crystal display according to the exemplary embodiment of the present invention may further include a second data line which intersects the gate line and a second thin film transistor which is connected to the gate line and the second data line.

[0023] The first lower subpixel electrode, and the first upper subpixel electrode may be connected to the first thin film transistor and the second lower subpixel electrode and the second upper subpixel electrode may be connected to the second thin film transistor.

[0024] According to the present invention, transmittance may be improved by adjusting a thickness of the liquid crystal layer, a dielectric anisotropy of the liquid crystal, and a pitch of the minute branch portions.

[0025] Further, the transmittance may be improved by adjusting the width of the minute branches and the minute slits which form the minute branch portion.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

[0027] FIG. **1** is an equivalent circuit diagram of one pixel of a liquid, crystal display according to an exemplary embodiment of the present invention.

[0028] FIG. **2** is a layout view of one pixel of a liquid crystal display according to an exemplary embodiment of the present invention.

[0029] FIG. **3** is a cross-sectional view of the liquid crystal display taken along the line III-III of FIG. **2**.

[0030] FIG. **4** is an enlarged view of a portion A of FIG. **2**.

[0031] FIG. **5** is an equivalent circuit diagram of one pixel of a liquid crystal display according to another exemplary embodiment of the present invention.

[0032] FIG. **6** is a layout view of one pixel of a liquid crystal display according to another exemplary embodiment of the present invention.

[0033] FIG. **7** is a cross-sectional view of the liquid crystal display taken along the line VII-VII of FIG. **6**.

[0034] FIG. **8** is a top plan view illustrating a pixel electrode of the liquid crystal display of FIG. **6**.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0035] Hereinafter, the present invention will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention.

[0036] Accordingly, the drawings and description are to be regarded as illustrative in nature and not restrictive. Like reference numerals designate like elements throughout the specification.

[0037] The size and thickness of the components shown the drawings are optionally determined for better understanding and ease of description, and the present invention is not limited to the examples shown in the drawings.

[0038] In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. In addition, in the drawings, for understanding and ease of description, the thicknesses of some layers and areas are exaggerated. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

[0039] Further, unless explicitly described to the contrary, the word "comprise" and variations such as "comprises" or "comprising", will be understood to imply the inclusion of stated elements but not the exclusion of any other elements. In addition, throughout the specification, "on" implies being positioned above or below a target element and does not imply being necessarily positioned on the top on the basis of a gravity direction.

[0040] First, a liquid crystal display device according to an exemplary embodiment of the present invention will be described with reference to FIGS. **1** to **4**.

[0041] FIG. **1** is an equivalent circuit diagram of one pixel of a liquid crystal display device according to an exemplary embodiment of the present invention.

[0042] Referring to FIG. **1**, one pixel PX of a liquid crystal display device according to the present exemplary embodiment includes a plurality of signal lines including a gate line GL which transmits a gate signal, a data line DL which transmits a data signal, and a reference voltage line RL which transmits a divided reference voltage, first, second, and third switching elements Qa, Qb, and Qc which are connected to the plurality of signal lines and first and second liquid crystal capacitors Clca and Clcb.

[0043] The first and second switching elements Qa and Qb are connected to the gate line GL and the data line DL, and the third switching element Qc is connected to an output terminal of the second switching element Qb and the reference voltage line RL.

[0044] The first switching element Qa and the second switching element Qb are three terminal elements such as a thin film transistor. A control terminal thereof is connected to the gate line GL, an input terminal thereof is connected to the data line DL, an output terminal of the first switching element Qa is connected to the first liquid crystal capacitor Clca, and an output terminal of the second switching element Qb is connected to the second liquid crystal capacitor Clcb and an input terminal of the third switching element Qc.

[0045] The third switching element Qc is also a three terminal element such as a thin film transistor in which a control terminal is connected to the gate line GL, an input terminal is connected to the second liquid crystal capacitor Clcb, and an output terminal is connected to the reference voltage line RL.

[0046] When a gate on signal is applied to the gate line GL, the first switching element Qa, the second switching element Qb, and the third switching element Qc which are connected to the gate line GL are turned on. Therefore, a data voltage which is applied to the data line DL is applied to a first subpixel electrode PEa and a second subpixel electrode PEb through the turned-on first switching element Qa and second switching, element Qb, respectively. In this case, the data voltages which are applied to the first subpixel electrode PEa and the second subpixel electrode PEb are equal to each other, and the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb are charged with a value which is equal to a difference between a common voltage and the data voltage. Simultaneously to this, the voltage which is charged into the second liquid crystal capacitor Clcb is divided by the turned on third switching element Qc. By doing this, the voltage which is charged into the second liquid crystal capacitor Clcb is lowered by a difference between the common voltage and the divided reference voltage. That is, the voltage which is charged into the first liquid crystal capacitor Clca is higher than the voltage which is charged into the second liquid crystal capacitor Clcb.

[0047] As described above, the voltage which is charged into the first liquid crystal capacitor Clca is different from the voltage which is charged into the second liquid crystal capacitor Clcb. Since the voltage which is charged into the first liquid crystal capacitor Clca is different from the voltage which is charged into the second liquid crystal capacitor Clcb, inclined angles of the liquid crystal molecules in the first subpixel and the second subpixel are different from each other, so that the luminances of two subpixels are different from each other. Therefore, when the voltage of the first liquid crystal capacitor Clca and the voltage of the second liquid crystal capacitor Clcb are appropriately adjusted, an image which is seen from the side is closer to an image which is seen from the front as much as possible, thereby improving a side visibility.

[0048] In the illustrated exemplary embodiment, in order to make the voltage which is charged into the first liquid crystal capacitor Clca be different from the voltage which is charged into the second liquid crystal capacitor Clcb, a third switching element Qc which is connected to the second liquid crystal capacitor Clcb and the reference voltage line RL is provided. However, in the liquid crystal display according to another exemplary embodiment of the present invention, the second liquid crystal capacitor Clcb may be connected to a step-down capacitor. Specifically, a third switching element including as first terminal which is connected to a step down gate line, a second terminal which is connected to a second liquid crystal capacitor Clcb, and a third terminal which is connected to the step down capacitor is provided so that a part of as quantity of charges charged into the second liquid crystal capacitor Clcb is charged into the step-down capacitor, thereby setting charged voltages between the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb to be different from each other.

[0049] In addition, the charged voltage between the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb may be set to be different from each other using various methods.

[0050] Now, a structure of the liquid crystal display according to the exemplary embodiment illustrated in FIG. **1** will be described in brief with reference to FIGS. **2** to **4**.

[0051] FIG. **2** is a layout, view of one pixel of a liquid crystal display according to an exemplary embodiment of the present invention. FIG. **3** is a cross-sectional view of the liquid crystal display taken along the line III-III of FIG. **2**. FIG. **4** is an enlarged view of a portion A of FIG. **2**.

[0052] Referring to FIG. **2** to FIG. **4**, a liquid crystal display according to the present exemplary embodiment includes a first display panel for substrate) **100**, a second display panel (or substrate) **200** which faces the first display panel **100**, and a liquid crystal layer **3** interposed between the first and second display panels **100** and **200**.

[0053] Hereinafter, the first display and **100** will be described.

[0054] A gate line **121** and a reference voltage line **131** are disposed on a first insulation substrate **110** which is formed of a transparent glass or plastic.

[0055] The gate line **121** mainly extends in a horizontal direction, transmits a gate signal, and includes a first gate electrode **124***a* a second gate electrode **124***b* and a third gate electrode **124***c*. The gate line **121** further includes a wide end portion not illustrated) to be connected with other layer or an external driving circuit.

[0056] The reference voltage line **131** mainly extends in to horizontal direction, transmits a predetermined voltage such as a reference voltage, and includes a first vertical storage electrode **135**, a first horizontal storage electrode **136**, and a reference electrode **137**. The first vertical and horizontal storage electrodes **135** and **136** enclose a first upper subpixel electrode **191***a* which will be described below and the reference electrode **137** protrudes toward the gate line **121**. Further, the reference voltage line **131** includes a second vertical storage electrode **138**, a second horizontal storage electrode **139** which enclose a second upper subpixel electrode **191***b* which will be described below. Even though not illustrated in FIG. **1**, the first horizontal storage electrode **136** may be connected with the second horizontal storage electrode **139** of a previous pixel by an integrated wiring line.

[0057] A gate insulating layer **140** is disposed on the gate line **121** and the reference voltage line **131** and a first semiconductor **154***a*, a second semiconductor **154***b*, and a third semiconductor **154***c* which are formed of an amorphous or polysilicon are disposed on the gate insulating layer **140**. Further, the first semiconductor **154***a*, the second semiconductor **154***b*, and the third semiconductor **154***c* may be formed of oxide semiconductors.

[0058] A plurality of pairs of ohmic contacts **163***a*, **165***a*, **163***b*, **165***b*, **163***c*, and **165***c* are disposed on the first semiconductor **154***a*, the second semiconductor **154***b*, and the third semiconductor **154***c*, respectively. The ohmic contacts **163***a*, **165***a*, **163***b*, **165***b*, **163***c*, and **165***c* may be formed of suicide or n+ hydrogenated amorphous silicon doped with an n-type impurity at a high concentration. Further, when the first semiconductor **154***a*, the second semiconductor **154***b*, and the third semiconductor **154***c* are formed of the oxide semiconductors, the ohmic contacts **163***a*, **165***a*, **163***b*, **165***b*, **163***c*, and **165***c* may be omitted.

[0059] Data conductors **171**, **173***a*, **173***b*, **173***c*, **175***a*, **175***b*. and **175***c* including a plurality of data lines **171** including a first source electrode **173***a* and as second source electrode **173***b*, a first drain electrode **175***a*, a second drain electrode **175***b*, a third source electrode **173***c*, and a third drain electrode **175***c* are disposed on the ohmic contacts **163***a*, **165***a*, **163***b*, **165***b*, **163***c*, and **165***c* and the gate insulating layer **140**.

[0060] The data lines **171** transmit data signals and mainly extend in a vertical direction to intersect the gate line **121** and the reference voltage line **131**. The first source electrode **173***a* and the second drain electrode **175***b* overlap the first semiconductor **154***a*, the second source electrode **173***b* and the second drain electrode **175***b* overlap the second semiconductor **154***b*, and the third source electrode **173***c* and the third drain electrode **175***c* overlap the third semiconductor **154***c*. The first source electrode **173***a* and the first drain electrode **175***a* are opposite to each other with the first gate electrode **124***a* therebetween, the second source electrode **173***b* and the second drain electrode **175***b* are opposite to each other with the second gate electrode **124***b* therebetween, and the third source electrode **173***c* and the third drain electrode **175***c* are opposite to each other with the third gate electrode **124***c* therebetween. The second drain electrode **175***b* is connected with the third source electrode **173***c* and includes an expansion **177** which widely expands. However, the exemplary embodiment is not limited thereto, but shapes and arrangements of the, data lines **171** including the first, second and third drain electrodes **175***a*, **175***b*, and **175***c* may vary in various ways.

[0061] Further, the data line **171** may include a wide end portion not illustrated) to be connected with other layer or an external driving circuit.

[0062] The first gate electrode **124***a*, the first source electrode **173***a*, the first drain electrode **175***a* and the first semiconductor **154***a* form a first thin film transistor (TFT) Qa, and a channel of the first thin film transistor Qa is formed in the first semiconductor **154***a* between the first source electrode **173***a* and the first drain electrode **175***a*. Similarly, the second gate electrode **124***b*, the second source electrode **173***b*, the second drain electrode **175***b* and the second semiconductor **154***b* form a second thin film transistor Qb, and a channel of the second thin film transistor Qb is formed in the second semiconductor **154***b* between the second source electrode **173***b* and the second drain electrode **175***b*. Further, the third gate electrode **124***c*, the third source electrode **173***c*, the third drain electrode **175***c* and the third semiconductor **154***c* form a third thin film transistor Qc, and a channel of the third thin film transistor Qc is formed in the third semiconductor **154***c* between the third source electrode **173***c* and the third drain electrode **175***c*.

[0063] A passivation layer **180** is disposed on the data conductors **171**, **173***a*, **173***b*, **173***c*, **175***a*, **175***b*, and **175***c*, and on exposed portions of the first, second, and third semiconductors **154***a*, **154***b*, and **154***c*. The passivation layer **180** may be formed of an inorganic insulating material such as silicon nitride or silicon oxide. The passivation layer **180** may prevent a pigment of a color filter **230**, which will be described below, from inflowing into exposed portions of the first, second, and third semiconductors **154***a*, **154***b*, and **154***c*.

[0064] The color filter **230** is disposed on the passivation layer **180**. The color filter **230** extends in a vertical direction along two adjacent data lines **171**.

[0065] The color filter **230** may represent one of three primary colors of red, green, and blue. However, the color which is represented by the color filter is not limited to three primary colors of red, green, and blue, but may be one of cyan, magenta, yellow, and white.

[0066] An overcoat **188** is disposed on the color filter **230**.

[0067] The overcoat **188** may be formed of an inorganic insulating material such as silicon nitride or silicon oxide. The overcoat **188** prevents the color filter **230** from being loosen, and suppresses the contamination of the liquid crystal layer **3** by an organic material such as a solvent which inflows from the color filter **230**, thereby preventing faulty such as an image lag caused when a screen is driven.

[0068] A lower pixel electrode **190** is disposed on the overcoat **188**.

[0069] The lower pixel electrode **190** includes a first lower subpixel electrode **190***a* and a second lower subpixel electrode **190***b* which are separated from each other with the gate line **121** therebetween and adjacent to each other in a column direction with respect to the gate line **121**. The first lower subpixel electrode **190***a* and the second lower subpixel electrode **190***b* are located in a first subpixel area and a second subpixel area, respectively. The first subpixel area and the second subpixel area form one pixel area.

[0070] The first lower subpixel electrode **190***a* and the second lower subpixel electrode **190***b* have a planar shape having a whole plate shape over the first subpixel area and the second subpixel area. Here, the whole plate means a plate shape which is not split as one body.

[0071] The lower pixel electrode **190** may be formed of a transparent material such as indium tin oxide (ITO) and indium zinc oxide (IZO). Further, the lower pixel electrode **190** may be also formed of a reflective metal such as aluminum, silver, chromium or an alloy thereof.

[0072] An interlayer insulating layer **189** is disposed on the overcoat **188** and the lower pixel electrode **190**. The interlayer insulating layer **189** may be formed of an inorganic insulating material such as silicon nitride or silicon oxide. Further, the interlayer insulating layer **189** may be formed of an organic insulating material.

[0073] A first contact hole **185***a* and a second contact hole **185***b* are located in the passivation layer **180**, the color filter **230**, the overcoat **188**, and the interlayer insulating layer **189** to expose the first drain electrode **175***a* and the second drain electrode **175***b*, respectively. Further, the third contact hole **185***c* is located in the passivation layer **180**, color filter **230**, the overcoat **188**, the interlayer insulating layer **189**, and the gate insulating layer **140** to expose a part of the reference electrode **137** and a part of the third drain electrode **175***c*.

[0074] Upper pixel electrodes **191** which are separated from each other and a connecting member **197** are disposed on the interlayer insulating layer **189**.

[0075] The upper pixel electrode **191** includes a first upper subpixel electrode **191***a* and a second upper subpixel electrode **191***b* which are separated from each other with the gate line **121** therebetween and adjacent to each other with respect to the gate line **121**. The first upper subpixel electrode **191***a* overlaps the first lower subpixel electrode **190***a*, and the second upper subpixel electrode **191***b* overlaps the second lower subpixel electrode **190***b*.

[0076] The upper pixel, electrode **191** and the connecting, member **197** may be formed of a transparent material such as ITO and IZO. The upper pixel electrode **191** and the connecting member **197** may be also funned of a reflective metal such as aluminum, silver, chromium or an alloy thereof.

[0077] The first upper subpixel electrode **191***a* and the second upper subpixel electrode **191***b* include cross-shaped stem portions which have a quadrangular shape as an overall shape and are formed of horizontal stem portions **192***a* and **192***b*, respectively, and vertical stem portions **193***a* and **193***b*, respectively, intersecting the horizontal stem portions.

[0078] Further, the first upper subpixel electrode **191***a* and the second upper subpixel electrode **191***b* are divided into four sub regions by the horizontal stem portions **192***a* and **192***b*, respectively, and the vertical stem portions **193***a* and **193***b*, respectively, and each sub region includes a plurality of minute branch portions **196***a* and **196***b*, respectively. Each minute branch portion **196***a* and **196***b* includes minute branches **194***a* and **194***b*, respectively, and minute slits **195***a* and **195***b*, respectively.

[0079] One of the minute branch portions **196***a* (or **196***b*) of the first upper subpixel electrode **191***a* (or of the second upper subpixel electrode **191***b*) obliquely extends from the horizontal stem portion **192***a* (or from the horizontal portion **192***b*) or from the vertical stem portion **193***a* for from the vertical stem portion **193***b*) in a left upper direction. The other minute branch portions **196***a*, for example, obliquely extends from the horizontal stem portions **192***a* or from the vertical stem portions **193***a* in a right upper direction. Further, another one of the minute branch portions **196***a*, for example, obliquely extends from the horizontal stem portions **192***a* or from the vertical stem portions **193***a* in a left lower direction, and still the other one of the minute branch portions **196***a*, for example, obliquely extends from the horizontal stem portions **192***a* or from the vertical stem portions **193***a* in a right lower direction. As shown in FIG. **2**, the same arrangements of the minute branch portions **196***a* can be applied to the minute branch portions **196***b*.

[0080] The minute branch portion **196***a* extends in a direction formed approximately 40 degrees to 45 degrees with respect to the gate line **121** or the horizontal stem portions

192*a*. The minute branch portion **196***b* extends in as direction formed approximately 40 degrees to 45 degrees with respect to the gate line **121** or the horizontal stem portion **192***b*. Particularly, the extension direction of the minute branch portion **196***a* included in the first upper subpixel electrode **191***a* may form approximately 40 degrees with respect to the horizontal stem portion **192***a*, and the extension direction of the minute branch portion **196***b* included in the second upper subpixel electrode **191***b* may form approximately 45 degrees with respect to the horizontal stem portion **192***b*. Further, minute branch portions **196***a* and **196***b* of two adjacent sub regions may be perpendicular to each other.

[0081] The first upper subpixel electrode **191***a* and the first lower subpixel electrode **190***a* are physically and electrically connected to each other through the first contact hole **185***a*. Further, the first upper subpixel electrode **191***a* is physically and electrically connected to the first drain electrode **175***a* through the first contact hole **185***a*. Accordingly, a data voltage is applied to the first upper subpixel electrode **191***a* and the first lower subpixel electrode **190***a* from the first drain electrode **175***a*.

[0082] The second upper subpixel electrode **191***b* and the second lower subpixel electrode **190***b* are physically and electrically connected to each other through the second contact hole **185***b*. Further, the second upper subpixel electrode **191***b* is physically and electrically connected to the second drain electrode **175***b* through the second contact hole **185***b*. Accordingly, the data voltage is applied to the second upper subpixel electrode **191***b* and the second lower subpixel electrode **190***b* from the second drain electrode **175***b*.

[0083] The connecting member **197** is electrically connected to the reference electrode **137** and the third drain electrode **175***c* which are exposed through the third contact hole **185***c*.

[0084] Some data voltage which is applied to the second drain electrode **175***b* is divided by the third source electrode **173***c* so that the voltage which are applied to the first upper subpixel electrode **191***a* and the first lower subpixel electrode **190***a* are higher than the voltages which are applied to the second upper subpixel electrode **191***h* and the second lower subpixel electrode **190***b*. In this case, voltages which are applied to the first upper subpixel electrode **191***a* and the first lower subpixel electrode **190***a* and the second upper subpixel electrode **191***b* and the second lower subpixel electrode **190***b* are positive (+). In contrast, when voltages which are applied to the first upper subpixel electrode **191***a* and the first lower subpixel electrode **190***a* and the second upper subpixel electrode **191***b* and the second lower subpixel electrode **190***b* are negative (−), voltages which are applied to the first upper subpixel electrode **191***a* and the first lower subpixel electrode **190***a* are lower than voltages which are applied to the second upper subpixel electrode **191***b* and the second lower subpixel electrode **190***b*.

[0085] A lower alignment layer **12** is located on the interlayer insulating layer **189**, the upper pixel electrode **191**, and the connecting member **197**.

[0086] Hereinafter, the second display panel **200** will be described.

[0087] A light blocking member **220** is formed on a second insulation substrate **210** which is formed of a transparent glass or plastic.

[0088] The light blocking, member **220** extends along the data line **171** and the gate line **121**. A width of the light blocking member **220** may be larger than a width of the data line **171** and a width of the gate line **121**. As described above, the width of the light blocking member **220** is larger than the width of the data line **171** and the width of the gate line **121** so that the light blocking member **220** may prevent the light which is incident from the outside from being reflected from a surface of the data line **171** which is formed of a metal. Accordingly, the light which is reflected from the surfaces of the data line **171** and the gate line **121** interferes with light which passes through the liquid crystal layer **3**, which may prevent the contrast ratio of the liquid crystal display from being lowered.

[0089] A plantarization layer **250** is disposed on the light blocking member **220**, a common electrode **270** is disposed on the plantarization layer **250**, and an upper alignment layer **22** is disposed on the common electrode **270**.

[0090] The lower alignment layer **12** and the upper alignment layer **22** may be formed of vertical alignment layers and may be formed of an alignment material such as polyamic acid, polysiloxane, or polyimide.

[0091] The liquid crystal layer **3** includes a plurality of liquid crystal molecule **31** having a negative dielectric anisotropy and the liquid crystal molecule **31** may be aligned such that a major axis is vertical, to the surfaces of the first and second display panels **100** and **200** in a state where no electric field is applied.

[0092] Further, the liquid crystal layer **3** may include a prepolymer such as a monomer which is cured by polymerization by light. The prepolymer may include a reactive mesogen which is polymerized by light such as ultraviolet rays.

[0093] In the meantime, the lower alignment layer **12** and the upper alignment layer **22** may include prepolymer such as a monomer which is cured by polymerization by light. In this case, the liquid crystal layer **3** does not include the prepolymer.

[0094] The first upper subpixel electrode **191***a* and the first lower subpixel electrode **190***a* and the second upper subpixel electrode **191***b* and the second lower subpixel electrode **190***b* to which the data voltages are applied generate an electric field together with the common electrode **270** of the second display panel **200**, to determine a direction of the liquid, crystal molecules **31** of the liquid crystal layer **3** between the first display panel **100** and the second display panel **200**. Luminance of the light which passes through the liquid crystal layer **3** varies depending on the direction of the liquid crystal molecules **31** determined as described above.

[0095] In the present exemplary embodiment, the plate shaped first lower subpixel electrode **190***a* and second lower subpixel electrode **190***b* are disposed to overlap the first upper subpixel electrode **191***a* and the second upper subpixel electrode **191***b*, respectively, each including minute branches **194***a* and **194***b*, thereby increasing transmittance of the liquid crystal display.

[0096] More specifically, in regions corresponding to the minute slits **195***a* and **195***b* between the minute branches **194***a* and **194***b* of the first upper subpixel electrode **191***a* and the second upper subpixel electrode **191***b*, an electric field is generated between the whole plate shaped first lower subpixel electrode **190***a* and second lower subpixel electrode **190***b* and the common electrode **270** so that the electric field is prevented from being lowered even in a region where a cutout for forming a plurality of branch electrodes is formed, thereby increasing the transmittance of the liquid crystal display.

[0097] In the meantime, in the present exemplary embodiment, an interval S (FIG. 4) between two adjacent minute branches **194***a* of the first upper subpixel electrode **191***a* is 2.7 to 5.0 times larger than a thickness d of the liquid crystal layer **3**, which is a cell gap d shown in FIG. **3**. An interval between two adjacent minute branches **194***b* of the second upper subpixel electrode **191***b* may be the same as the interval S between two adjacent minute branches **194***a*, and is 2.7 to 5.0 times larger than a thickness d of the liquid crystal layer **3**. The thickness of the liquid crystal layer **3** is the cell gap d, which is a site of the liquid crystal layer **3** along the direction between the first and second display panels **100** and **200**. The interval S between two adjacent minute branches **194***b* also can be referred to as a width S of the slit **195***b*, as shown in FIG. **4**. However, the interval between two adjacent minute branches **194***a* can be different from the interval between two adjacent minute branches **194***b*, as long as these intervals are in the range between 2.7 to 5.0 times larger than a thickness d of the liquid crystal layer **3**. In the case that the cell thickness d is not uniform over the panel, the cell thickness d can be defined as an average values over the panel.

[0098] Now, a relationship of the width S of the minute slits **195***a* and **195***b* and the cell gap d will be described with reference to Table 1.

[0099] In Table 1, as compared with a structure of a pixel electrode including the first subpixel electrode, and the second subpixel electrode having a minute branch portion including a plurality of minute slits and a plurality of minute branches, when a liquid crystal display device according to the exemplary embodiment of the present invention, the lower pixel electrode including the whole plate shaped first lower subpixel electrode and second lower subpixel electrode interposes the upper pixel electrode including the first upper subpixel electrode and the second upper subpixel electrode having the minute branch portion with the insulating layer therebetween, and the same voltage is applied to the lower pixel electrode and the upper pixel electrode, a ratio of the transmittance and a response time in a black state is measured, while changing a ratio of the width S of the minute slits **195***a* and **195***b* with respect to the cell gap d.

TABLE 1

S/d	Transmittance (%)	Ton (%)
1.3	87.6	10.1
1.7	51	3.3
2.0	53.4	82.9
2.7	104.4	1.8
3.3	104.9	1.9
4.0	104.8	2
5.0	105.2	2.2
5.3	94.1	1.9

[0100] Referring to Table 1, when a ratio of the width S of the minute slits **195***a* and **195***b* with respect to the cell gap d is 2.7 to 5.0, a ratio of the transmittance is 100% or higher than that of the structure of the pixel electrode which includes only minute branch portions. That is, it is understood that according to the liquid crystal display of the exemplary embodiment of the present invention, the transmittance of the liquid crystal display is increased.

[0101] It is also understood that when the ratio of the width S of the minute slits **195***a* and **195***b* with respect to the cell gap d is 2.7 to 5.0, a ratio of the response time in the black state is reduced by approximately 98% as compared with the structure of the pixel electrode which includes only minute branch portions. That is, it is understood that the response time in the black state of the liquid crystal display according to the exemplary embodiment of the present invention is much shorter. Therefore, it is understood that the luminance in the black state of the liquid crystal display according to the exemplary embodiment of the present invention is improved.

[0102] Now, as liquid crystal display device, according, to another exemplary embodiment of the present invention will be described with reference to FIGS. **5** to **8**.

[0103] FIG. **5** is an equivalent circuit diagram of one pixel of a liquid crystal display according to another exemplary embodiment of the present invention.

[0104] Referring to FIG. **5**, a liquid crystal display according to the present exemplary embodiment includes a first display panel (or substrate) **100**, a second display panel (or substrate) **200** which face the first display panel **100**, and a liquid crystal layer **3** interposed between the first and second display panels **100** and **200**.

[0105] The liquid crystal display device according to the present exemplary embodiment includes signal lines including a plurality of gate lines GL, a plurality of pairs of data lines DLa and DLb, and a plurality of reference voltage lines RL and a plurality of pixels PX connected to the signal lines.

[0106] Each pixel PX includes subpixels PXa and PXb. The subpixel PXa includes switching element Qa, liquid crystal capacitor Clca, and storage capacitor Csta. The subpixel PXb includes switching element Qb, liquid crystal capacitor Clcb, and storage capacitor Cstb

[0107] The switching elements Qa and Qb are three terminal elements such as a thin film transistor which is provided in a first display panel **100**. A control terminal thereof is connected to the gate line GL, an input terminal is connected to the data lines DLa and DLb, respectively, and an output terminal thereof is connected to the liquid crystal capacitors Clca and Clcb, respectively, and the storage capacitors Csta and Cstb, respectively.

[0108] The liquid crystal capacitors Clca and Clcb have subpixel electrodes PEa and PEb, respectively, and the common electrode **270** as two terminals and a portion of the liquid crystal layer **3** between the two terminals is formed of a dielectric material.

[0109] The storage capacitors Csta and Cstb which serve as auxiliary capacitors of the liquid crystal capacitors Clca and Clcb, respectively, are formed such that the reference voltage line RL and the subpixel electrodes PEa and PEb provided in the first display panel **100** overlap with an insulator therebetween and a predetermined voltage such as a common voltage Vcom is applied IS to the reference voltage line RL.

[0110] Voltages which are charged into the two liquid crystal capacitors Clca and Clcb are set to be slightly different from each other. For example, a data voltage which is applied to the liquid crystal capacitor Clca is set to be higher or lower than a data voltage which is applied to adjacent liquid crystal capacitor Clcb at all times. When the voltages of the two liquid crystal capacitors Clca and Clcb are appropriately adjusted as described above, an image which is seen from the side is closer to an image which is seen from the front, thereby improving a side visibility of the liquid crystal display.

[0111] Now, a structure of the liquid crystal display device according to the exemplary embodiment illustrated in FIG. **5** will be described in brief with reference to FIGS. **6** to **8**.

[0112] FIG. **6** is a layout view of one pixel of a liquid crystal display according to another exemplary embodiment of the present invention. FIG. **7** is a cross-sectional view of the liquid crystal display taken along the line VII-VII of FIG. **6**. FIG. **8** is a top plan view illustrating pixel electrode of the liquid crystal display of FIG. **6**.

[0113] Referring to FIG. **6** to FIG. **8**, a liquid crystal display according to the present exemplary embodiment includes as first display panel **100** and a second display panel **200** which are opposite to each other and a liquid crystal layer **3** interposed between the first and second display panels **100** and **200**.

[0114] Hereinafter, the first display panel **100** will be described.

[0115] A gate line **121** and a reference voltage line **131** are disposed on a first insulation substrate **110**.

[0116] The gate line **121** transmits a gate signal and mainly extends in a horizontal direction. The gate line **121** includes as plurality of first and second gate electrodes **124***a* and **124***b* which upwardly protrudes.

[0117] The reference voltage line **131** extends to be substantially parallel to the gate line **121** and includes a storage electrode **135** which extends from the reference voltage line **131**. Shapes and arrangements of the reference voltage line **131** and the storage electrode **135** may vary in various ways.

[0118] A gate insulating layer **140** is disposed on the gate line **121** and the reference voltage line **131** and a first semiconductor **154***a* and a second semiconductor **154***b* which are formed of an amorphous or polysilicon are disposed on the gate insulating layer **140**. Further, the first semiconductor **154***a* and the second semiconductor **154***b* may be formed of oxide semiconductors.

[0119] A plurality of pairs of ohmic contacts **163***a*, **163***b*, **165***a*, and **165***b* are disposed on the first semiconductor **154***a* and the second semiconductor **154***b*, respectively. The ohmic contacts **163***b* and **165***b* may be formed of silicide or n+ hydrogenated amorphous silicon doped with an n-type impurity at a high concentration. Further, when the first semiconductor **154***a* and the second semiconductor **154***b* **154***c* are formed of the oxide semiconductors, the ohmic contacts **163***b* and **165***b* may be omitted.

[0120] Data conductors **171***a*, **17***b*, **173***a*, **173***b*, **175***a*, and **175***b* including a first data line **171***a* including a first source electrode **173***a* and a second data line **171***b* including a second source electrode **173***b*, a first drain electrode **175***a*, and a second drain electrode **175***b* are disposed on the ohmic contacts **163***b* and **165***b* and the gate insulating layer **140**.

[0121] The first and second data lines **171***a* and **171***b* transmit data signals and mainly extend in a vertical direction to intersect the gate line **121** and the reference voltage line **131**. The first source electrode **173***a* and the second drain electrode **175***b* overlap the first semiconductor **154***a* and the second source electrode **173***b*, and the second drain electrode **175***b* overlap the second semiconductor **154***b*. The first source electrode **173***a* and the first drain electrode **175***a* are opposite to each other with the first gate electrode **124***a* therebetween, and the second source electrode **173***b* and the second drain electrode **175***b* are opposite to each other with the second gate electrode **124***b* therebetween. However, the exemplary embodiment is not limited thereto, but shapes and arrangements of the first and second data lines **171***a* and **171***b* including the first and second drain electrodes **175***a* and **175***b* may vary in various ways.

[0122] Further, the first and second data lines **171***a* and **171***b* may include a wide end portion (not illustrated) to be connected with other layer or an external driving circuit.

[0123] The first gate electrode **124***a*, the first source electrode **173***a*, the first drain electrode **175***a* and the first semiconductor **154***a* form as first thin film transistor (TFT) Qa, and a channel of the first thin film transistor Qa is formed in the first semiconductor **154***a* between the first source electrode **173***a* and the first drain electrode **175***a*. Similarly, the second gate electrode **124***b*, the second source electrode **173***b*, the second drain electrode **175***b* and the second semiconductor **154***b* form a second thin film transistor Qb, and a channel of the second thin film transistor Qb is formed in the second semiconductor **154***b* between the second source electrode **173***b* and the second drain electrode **175***b*.

[0124] A passivation layer **180** is disposed on the data conductors **171***a*, **171***b*, **173***a*, **173***b*, **175***a*, and **175***b* and on exposed portions of the first and second semiconductors **154***a* and **154***b*. The passivation layer **180** may be formed of an inorganic insulating material such as silicon nitride or silicon oxide. The passivation layer **180** may prevent a pigment of a color filter **230**, which will be described below, from inflowing into exposed portions of the first and second semiconductors **154***a* and **154***b*.

[0125] The color filter **230** is disposed on the passivation layer **180**. The color filter **230** extends in a vertical direction along the first and second data lines **171***a* and **171***b*.

[0126] The color filter **230** may represent one of three primary colors of red, green, and blue. However, the color which is represented by the color filter is not limited to three primary colors of red, green, and blue but may be one of cyan magenta, yellow, and white.

[0127] An overcoat **188** is disposed on the color filter **230**.

[0128] The overcoat **188** may be formed of an inorganic insulating material such as silicon nitride or silicon oxide. The overcoat **188** prevents the color filter **230** from being loosen and suppresses the contamination of the liquid crystal layer **3** by an organic material such as a solvent which inflows from the color filter **230**, thereby preventing faulty such as an image lag caused when a screen is driven.

[0129] A lower pixel electrode **190** is disposed on the overcoat **188**.

[0130] The lower pixel electrode **190** includes a first lower subpixel electrode **190***a* and a second lower subpixel electrode **190***b* which are separated from each other. The first lower subpixel electrode **190***a* and the second lower subpixel electrode **190***b* are located in a first subpixel area and a second subpixel area, respectively. The first subpixel area and the second subpixel area form one pixel area.

[0131] The first lower subpixel electrode **190***a* and the second lower subpixel electrode **190***b* have a planar shape having a whole plate shape over the first subpixel area and the second subpixel area.

[0132] The lower pixel electrode **190** may be formed of a transparent material such as ITO and IZO. Further, the lower pixel electrode **190** may be also formed of a reflective metal such as aluminum, silver, chromium or an alloy thereof.

[0133] An interlayer insulating layer **189** is disposed on the overcoat **188** and the lower pixel electrode **190**. The interlayer insulating layer **189** may be formed of an organic insulating material such as silicon nitride or silicon oxide. Further, the interlayer insulating layer **189** may be formed of an organic insulating material.

[0134] A first contact hole **185***a* and a second contact hole **185***b* are located in the passivation layer **180**, the color filter

230, the overcoat **188**, and the interlayer insulating layer **189** to expose the first drain electrode **175***a* and the second drain electrode **175***b*, respectively.

[0135] An upper pixel electrode **191** is disposed on the interlayer insulating layer **189**.

[0136] The upper pixel electrode **191** includes as first upper subpixel electrode **191***a* and a second upper subpixel electrode **191***b* which are separated from each other. The first upper subpixel electrode **191***a* overlaps the first lower subpixel electrode **190***a* and the second upper subpixel electrode **191***b* overlaps the second lower subpixel electrode **190***b*.

[0137] The upper pixel electrode **191** and the connecting member **197** may be formed of a transparent material such as ITO and IZO. The upper pixel electrode **191** and the connecting member **197** may be also formed of a reflective metal such as aluminum, silver, chromium or an alloy thereof.

[0138] The first upper subpixel electrode **191***a* and the second upper subpixel electrode **191***b* include cross-shaped stem portions which have a quadrangular shape as an overall shape and are formed of horizontal stem portions **192***a* and **192***b*, respectively and vertical stem portions **193***a* and **193***b*, respectively, intersecting the horizontal stem portions.

[0139] Further, the first upper subpixel electrode **191***a* and the second upper subpixel electrode **191***b* are divided into four sub regions by the horizontal stem portions **192***a* and **192***b*, respectively, and the vertical stem portions **193***a* and **193***b*, respectively, and each sub region includes a plurality of minute branch portions **196***a* and **196***b*, respectively. Each minute branch portion **196***a* and **196***b* includes minute branches **194***a* and **194***b*, respectively, and minute slits **195***a* and **195***b*, respectively.

[0140] The extension direction of each minute branch portion **196***a* forms approximately 40 degrees to 45 degrees with respect to the gate line **121** or with respect to the horizontal stem portions **192***a*. The extension direction of each minute branch portion **196***b* forms approximately 40 degrees to 45 degrees with respect to the gate line **121** or with respect to the horizontal stem portions **192***b*. Minute branch portions **196***a* and **196***b* of two adjacent sub regions may be perpendicular to each other.

[0141] The second upper subpixel electrode **191***b* includes a pair of branches **195** extending along the first and second data lines **171***a* and **171***b*. The branch **195** is located between the first upper subpixel electrode **191***a* and the first and second data lines **171***a* and **171***b*, and is connected to a lower end of the first upper subpixel electrode **191***a*.

[0142] The first upper subpixel electrode **191***a* and the first lower subpixel electrode **190***a* are physically and electrically connected to each other through the first contact hole **185***a*. Further, the first upper subpixel electrode **191***a* is physically and electrically connected to the first drain electrode **175***a* through the first contact hole **185***a*. Accordingly, a data voltage is applied to the first upper subpixel electrode **191***a* and the first lower subpixel electrode **190***a* from the first drain electrode **175***a*.

[0143] The second upper subpixel electrode **191***b* and the second lower subpixel electrode **190***b* are physically and electrically connected to each other through the second contact hole **185***b*. Further, the second upper subpixel electrode **191***b* is physically and electrically connected to the second drain electrode **175***b* through the second contact hole **185***b*. Accordingly, the data voltage is applied to the second upper subpixel electrode **191***b* and the second lower subpixel electrode **190***b* from the second drain electrode **175***b*.

[0144] Hereinafter, the second display panel **200** will be described.

[0145] A light blocking member **220** is formed on a second insulation substrate **210** which is formed of a transparent glass or plastic.

[0146] The light blocking member **220** extends along the data line **171** and the gate line **121**. A width of the light blocking, member **220** may be larger than a width of the data line **171** and a width of the gate line **121**. As described above, the width of the light blocking member **220** is larger than the width of the data line **171** and the width of the gate line **121** so that the light blocking member **220** may prevent the light which is incident from the outside from being reflected from a surface of the data line **171** which is formed of a metal. Accordingly, the light which is reflected from the surfaces of the data line **171** and the gate line **121** interferes with light which passes through the liquid crystal layer **3**, which may prevent the contrast ratio of the liquid crystal display from being lowered.

[0147] A plantarization layer **250** is disposed on the light blocking member **220**, a common electrode **270** is disposed on the plantarization layer **250**, and an upper alignment layer **22** is disposed on the common electrode **270**.

[0148] The lower alignment layer **12** and the upper alignment layer **22** may be formed of vertical alignment layers and may be formed of an alignment material such as polyamic acid, polysiloxane, or polyimide.

[0149] The liquid crystal layer **3** includes a plurality of liquid crystal molecule **31** having a negative dielectric anisotropy and the liquid crystal molecule **31** may be aligned such that a major axis is vertical to the surfaces of the first and second display panels **100** and **200** in a state where no electric field is applied.

[0150] Further, the liquid crystal layer **3** may include a prepolymer such as a monomer which is cured by polymerization by light. The prepolymer may include a reactive mesogen which is polymerized by light such as ultraviolet rays.

[0151] In the meantime, the lower alignment layer **12** and the upper alignment layer **22** may include prepolymer such as a monomer which is cured by polymerization by light. In this case, the liquid crystal layer **3** does not include the prepolymer.

[0152] The first upper subpixel electrode **191***a* and the first lower subpixel electrode **190***a* and the second upper subpixel electrode **191***b* and the second lower subpixel electrode **190***b* to which the data voltages are applied generate an electric field together with the common electrode **270** of the second display panel **200**, to determine a direction of the liquid crystal molecules **31** of the liquid crystal layer **3** between the first display panel **100** and the second display panel **200**. Luminance of the light which passes through the liquid crystal layer **3** varies depending on the direction of the liquid crystal molecules **31** determined as described above.

[0153] In the present exemplary embodiment, the plate shaped first lower subpixel electrode **190***a* and second lower subpixel electrode **190***b* are disposed to overlap the first upper subpixel electrode **191***a* and the second upper subpixel electrode **191***b* each including minute branches **194***a* and **194***b*, thereby increasing transmittance of the liquid crystal display.

[0154] More specifically, in regions corresponding to the minute slits **195***a* and **195***b* between the minute branches **194***a* and **194***b* of the first upper subpixel electrode **191***a* and the second upper subpixel electrode **191***b*, an electric field is generated between the whole plate shaped first lower subpixel electrode **190***a* and second lower subpixel electrode **190***b* and the common electrode **270** so that the electric field is prevented from being lowered even in a region where a cutout for forming a plurality of branch electrodes is formed, thereby increasing the transmittance of the liquid crystal display.

[0155] In the meantime, in the present exemplary embodiment, an interval S between the minute branches **194***a* of the first upper subpixel electrode **191***a*, and the interval S between the minute branches **194***b* of the second upper subpixel electrode **191***b*, that is a width S of the minute slits **195***a* and **195***b* (as shown in FIG. **4**) is 2.7 to 5.0 times larger than as thickness d of the liquid crystal layer **3**, that is, a cell gap d.

[0156] Now, a relationship of the width S of the minute slits **195***a* and **195***b* and the cell gap d will be described with reference to Table 2.

[0157] In Table 2, as compared with a structure of a pixel electrode including the first subpixel electrode and the second subpixel electrode having a minute branch portion including a plurality of minute slits and as plurality of minute branches, when a liquid crystal display according to the exemplary embodiment of the present invention, the lower pixel electrode including the whole plate shaped first lower subpixel electrode and second lower subpixel electrode interposes the upper pixel electrode including the first upper subpixel electrode and the second upper subpixel electrode having the minute branch portion with the insulating layer therebetween and the same voltage is applied to the lower pixel electrode and the upper pixel electrode, a ratio of the transmittance and a response time in a black state is measured, while changing a ratio of the width S of the minute slits **195***a* and **195***b* with respect to the cell gap d.

TABLE 2

S/d	Transmittance (%)	Ton (%)
1.3	85.5	10.1
1.7	49.9	3.3
2.0	52.7	82.9
2.7	102.2	1.8
3.3	102.7	1.9
4.0	102.6	2
5.0	103.0	2.2
5.3	92.3	1.9

[0158] Referring to Table 2, when a ratio of the width S of the minute slits **195***a* and **195***b* with respect to the cell gap d is 2.7 to 5.0, a ratio of the transmittance is 100% or higher than that of the structure of the pixel electrode which includes only minute branch portions. That is, it is understood that according to the liquid crystal display of the exemplary embodiment of the present invention, the transmittance of the liquid crystal display is increased.

[0159] It is also understood that when the ratio of the width S of the minute slits **195***a* and **195***b* with respect to the cell gap d is 2.7 to 5.0, a ratio of the response time in the black state is reduced by approximately 98% as compared with the structure of the pixel electrode which includes only minute branch portions. That is, it is understood that the response time in the black state of the liquid crystal display according to the exemplary embodiment of the present invention is much shorter. Therefore, it is understood that the luminance in the black state of the liquid crystal display according to the exemplary embodiment of the present invention is improved.

[0160] While this invention has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. A liquid crystal display device, comprising:

a first substrate;

a gate line and a first data line which are disposed on the first substrate and are insulated from each other;

a first thin film transistor which is connected to the gate line and the first data line;

a lower pixel electrode which is connected to the first thin film transistor;

an interlayer insulating layer which is disposed on the lower pixel electrode;

an upper pixel electrode which is disposed on the interlayer insulating layer and is connected to the first thin film transistor and the lower pixel electrode;

a second substrate which faces the first substrate;

a common electrode which is disposed on the second substrate; and

a liquid crystal layer which is disposed between the first substrate and the second substrate, wherein the lower pixel electrode and the upper pixel electrode overlap each other, the upper pixel electrode includes a plurality of minute branches, the lower pixel electrode has a whole plate shape in plan view, and a ratio of an interval between the minute branches with respect to a thickness of the liquid crystal layer is 2.7 to 5.0.

2. The liquid crystal display device of claim **1**, wherein the liquid crystal layer includes liquid crystal molecules having a negative dielectric anisotropy.

3. The liquid crystal display device of claim **2**, wherein the lower pixel electrode includes a first lower subpixel electrode and a second lower subpixel electrode which are separated from each other, and the upper pixel electrode includes a first upper subpixel electrode and a second upper subpixel electrode which are separated from each other.

4. The liquid crystal display device of claim **3**, wherein the first lower subpixel electrode and the first upper subpixel electrode overlap each other, and the second lower subpixel electrode and the second upper subpixel electrode overlap each other.

5. The liquid crystal display device of claim **4**, wherein each of the first upper subpixel electrode and the second upper subpixel electrode includes a cross-shaped stem portion which is formed of a horizontal stem portion and a vertical stem portion that intersects the horizontal stem portion, and the minute branches extend from the cross-shaped stem portion.

6. The liquid crystal display device of claim **5**, further comprising:

a second thin film transistor which is connected to the gate line and the first data line; and

a third thin film transistor which is connected to an output terminal of the second thin film transistor.

7. The liquid crystal display device of claim **6**, wherein the first lower subpixel electrode and the first upper subpixel electrode are connected to the first thin film transistor, and the second lower subpixel electrode and the second upper subpixel electrode are connected to the second thin film transistor.

8. The liquid crystal display device of claim **7**, further comprising a reference voltage line which is connected to an output terminal of the third thin film transistor.

9. The liquid crystal display device of claim **5**, further comprising:

a second data line which intersects the gate line; and

a second thin film transistor which is connected to the gate line and the second data line.

10. The liquid crystal display device of claim **9**, wherein the first lower subpixel electrode and the first upper subpixel electrode are connected to the first thin film transistor and the second lower subpixel electrode and the second upper subpixel electrode are connected to the second thin film transistor.

* * * * *

专利名称(译)	液晶显示装置		
公开(公告)号	US20160209715A1	公开(公告)日	2016-07-21
申请号	US14/958027	申请日	2015-12-03
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
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外部链接	Espacenet USPTO		

摘要(译)

一种液晶显示装置，包括第一基板，栅极线和设置在第一基板上并彼此绝缘的第一数据线，连接到栅极线和第一数据线的第一薄膜晶体管，连接的下部像素电极第一薄膜晶体管，设置在下部像素电极上的层间绝缘层，设置在层间绝缘层上并连接到第一薄膜晶体管和下部像素电极的上部像素电极，面向第一基板的第二基板，公共电极设置在第二基板上，液晶层设置在第一基板和第二基板之间。上像素电极包括多个微小分支。微小分支之间的间隔相对于液晶层厚度的比率为2.7至5.0。