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(54) **LIQUID CRYSTAL DISPLAY PANEL AND ARRAY SUBSTRATE**

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(57) **ABSTRACT**

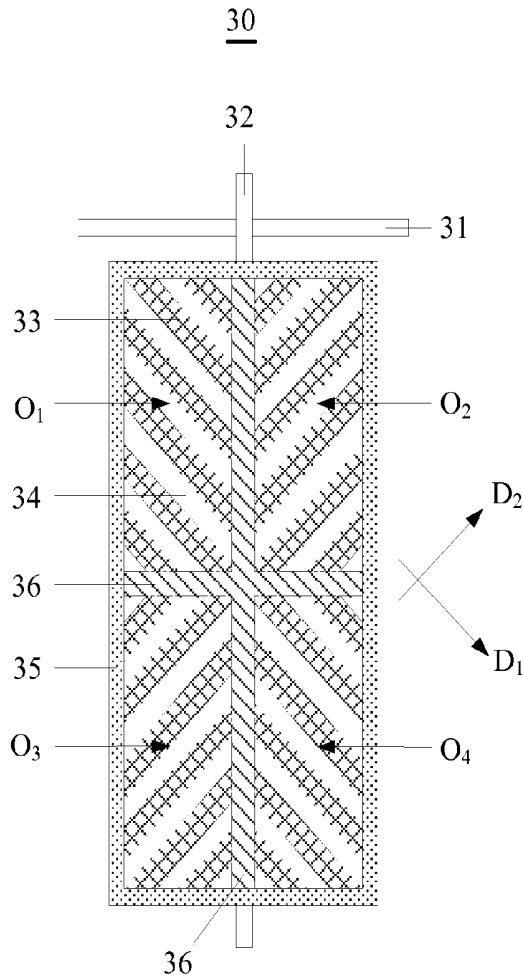
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A liquid crystal display panel and an array substrate are disclosed. A pixel electrode of each pixel unit of the array substrate is correspondingly connected with at least one data line. The pixel electrode includes multiple regions arranged as a matrix. The data line is disposed between adjacent two columns of the regions. Accordingly, the penetration ratio and the aperture ratio of the pixel unit are increased.

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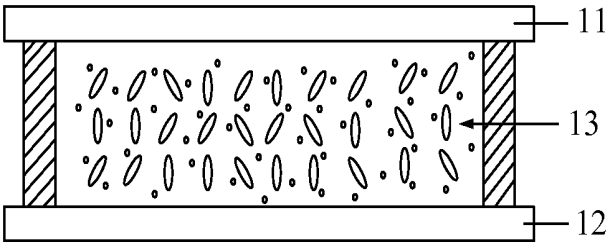


FIG. 1

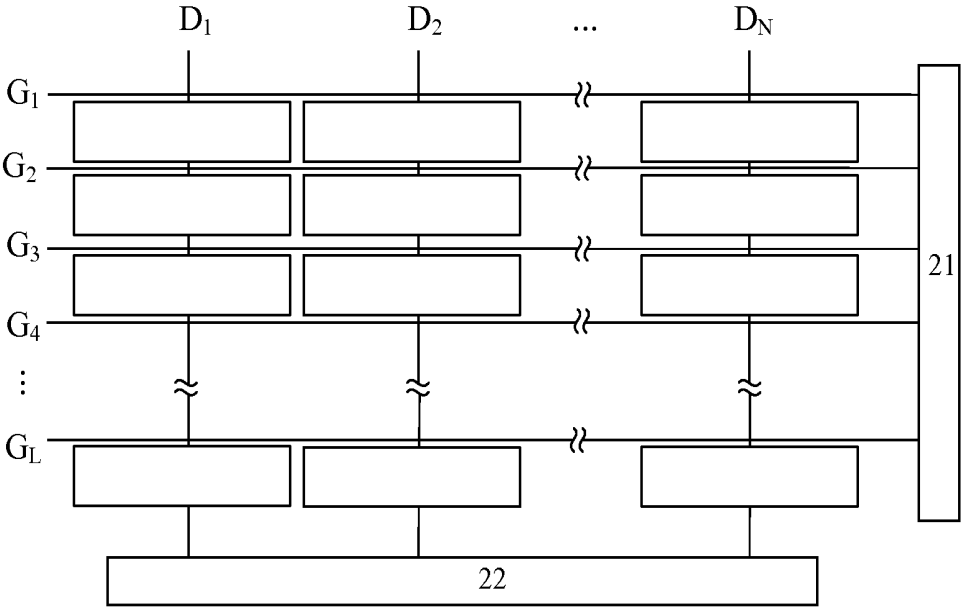


FIG. 2

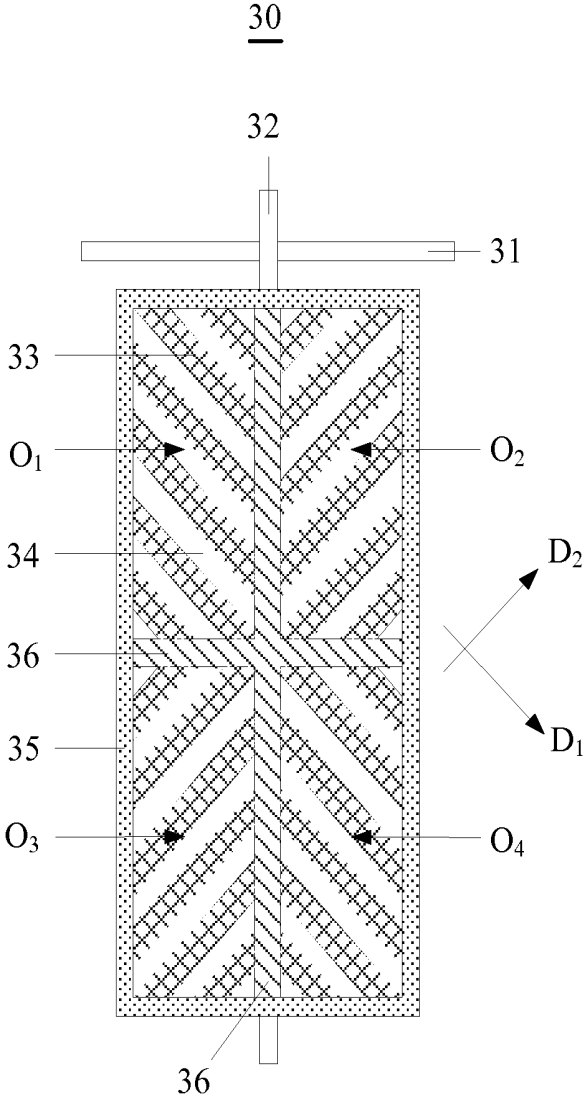


FIG. 3

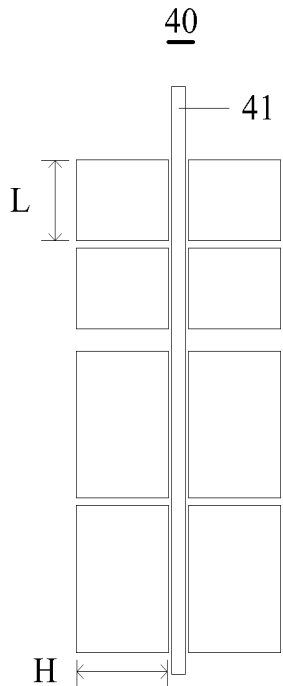


FIG. 4

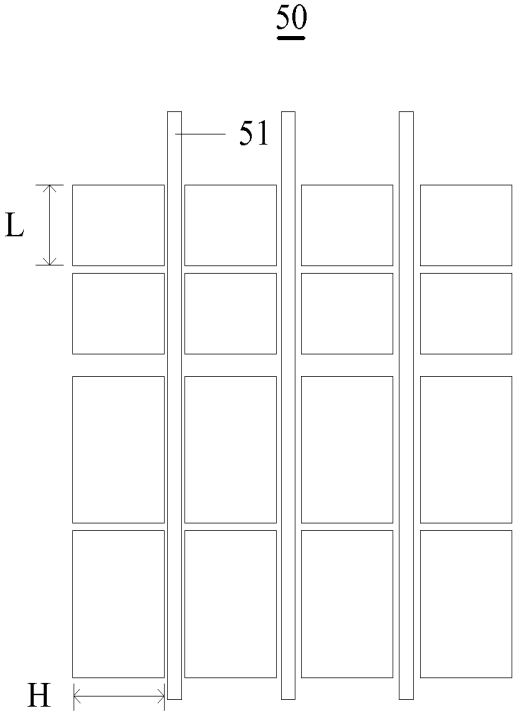


FIG. 5

## LIQUID CRYSTAL DISPLAY PANEL AND ARRAY SUBSTRATE

### BACKGROUND OF THE INVENTION

**[0001]** 1. Field of the Invention

**[0002]** The present invention relates to the liquid crystal display technology field, and more particularly to a liquid crystal display panel and an array substrate.

**[0003]** 2. Description of Related Art

**[0004]** In a pixel structure of a VA (vertical alignment) type liquid crystal display (LCD) panel, data lines on an array substrate are arranged between two adjacent pixel units and are perpendicular to scanning lines. A black matrix is disposed on the color filter substrate, and the black matrix is corresponding to the data lines and the scanning lines for preventing the light leakage. To solve the reduced aperture ratio caused by the black matrix, each of the pixel units is divided into multiple domains. However, the liquid crystal molecules which are corresponding to the multiple domains encounter different electric field strength such that dark fringes are generated when the LCD panel is displaying. As a result, the penetration ratio and the aperture ratio of the pixel unit are reduced.

### SUMMARY OF THE INVENTION

**[0005]** Accordingly, a technology problem solved by the present embodiment is to provide a liquid crystal display panel and an array substrate in order to increase the penetration ratio and the aperture ratio of the pixel unit.

**[0006]** In order to solve the above technology problem, a technology solution of the present invention is: an array substrate including multiple pixel units, wherein, each of the multiple pixel units connects with one scanning line and at least two data lines; a pixel electrode of each pixel unit includes multiple regions arranged as a matrix; and wherein, in each pixel unit, distances between two adjacent data lines are different; data lines are disposed between adjacent two columns of the regions; along a vertical direction, heights of the regions of the pixel electrode are not equal; along an extension direction which is perpendicular to the data line, widths of the regions of the pixel electrode are equal.

**[0007]** In order to solve the above technology problem, a technology solution of the present invention is: an array substrate including multiple pixel units, wherein, a pixel electrode of each multiple pixel unit connects with at least one data line; the pixel electrode of each pixel unit includes multiple regions arranged as a matrix; the at least one data line is disposed between adjacent two columns of the regions.

**[0008]** Wherein, the pixel electrode of each pixel unit connects with one data line; the pixel electrode of each pixel unit includes a first region, a second region, a third region, and a fourth region; the first region and the second region are disposed side by side; the first region and the fourth region are disposed as a diagonal arrangement; the second region and the third region are disposed as a diagonal arrangement; the one data line is disposed between the first region and the second region, and is also disposed between the third region and the fourth region.

**[0009]** Wherein, an arrangement direction of an electrode pattern of the first region and an arrangement direction of an electrode pattern of the fourth region are the same; an

arrangement direction of an electrode pattern of the second region and an arrangement direction of an electrode pattern of the third region are the same.

**[0010]** Wherein, an arrangement direction of an electrode pattern of the first region and an arrangement direction of an electrode pattern of the fourth region form a first direction; an arrangement direction of an electrode pattern of the second region and an arrangement direction of an electrode pattern of the third region form a second direction; wherein, the first direction and the second direction are perpendicular to each other.

**[0011]** Wherein, an area of the first region, an area of the second region, an area of the third region, and an area of the fourth region are the same.

**[0012]** Wherein, the pixel electrode includes multiple strip-shaped gaps, multiple first strip shape patterns, a second electrode pattern, and a third electrode pattern; the gaps and the first strip shape patterns are disposed alternately; the second electrode pattern surrounds the first region, the second region, the third region, and the fourth region; the third electrode pattern is used for defining the first region, the second region, the third region, and the fourth region.

**[0013]** Wherein, the pixel electrode of each pixel unit connects with at least two data lines; along a vertical direction, heights of the regions of the pixel electrode are not equal; along an extension direction which is perpendicular to the data line, widths of the regions of the pixel electrode are equal.

**[0014]** Wherein, in each pixel unit, distances between two adjacent data lines are different.

**[0015]** Wherein, the pixel electrode of each pixel unit connects with one scanning line.

**[0016]** In order to solve the above technology problem, a technology solution of the present invention is: a liquid crystal display (LCD) panel, comprising: a liquid crystal layer; a color filter substrate; and an array substrate; wherein, the color filter substrate and the array substrate are disposed oppositely with an interval; the liquid crystal layer is filled between color filter substrate and the array substrate; and wherein the array substrate including multiple pixel units; a pixel electrode of each multiple pixel unit connects with at least one data line; the pixel electrode of each pixel unit includes multiple regions arranged as a matrix; the at least one data line is disposed between adjacent two columns of the regions.

**[0017]** The beneficial effects of the present invention: through disposing the data lines between adjacent two columns of the regions, the opaque data lines are overlapped with the dark fringes between the multiple regions when the LCD panel is displaying. As a result, the light-shielding area corresponding to the data line is reduced, that is, the light-transparent area corresponding to the data line is increased. Accordingly, the penetration ratio and the aperture ratio of the pixel unit and the liquid crystal display panel having the pixel unit are increased.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0018]** FIG. 1 is a cross-sectional view of a liquid crystal display panel (LCD) according to a preferred embodiment of the present invention;

**[0019]** FIG. 2 is a schematic diagram of pixel units of an LCD panel according to a first embodiment of the present invention;

**[0020]** FIG. 3 is a schematic diagram of one pixel unit of an LCD panel shown in FIG. 2;

**[0021]** FIG. 4 is a schematic diagram of one pixel unit of an LCD panel according to a second embodiment of the present invention; and

**[0022]** FIG. 5 is a schematic diagram of one pixel unit of an LCD panel according to a third embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

**[0023]** FIG. 1 is a cross-sectional view of a liquid crystal display panel (LCD) according to a preferred embodiment of the present invention. FIG. 2 is a schematic diagram of pixel units of an LCD panel according to a first embodiment of the present invention. With reference to FIG. 1 and FIG. 2, the liquid crystal display (LCD) panel 10 includes a first substrate 11, a second substrate 12 and a liquid crystal layer 13 disposed between the first substrate 11 and the second substrate 12. Wherein, the first substrate 11 and the second substrate 12 are disposed oppositely with an interval. The second substrate 12 is a color filter (CF) substrate. The first substrate 11 is a thin-film-transistor array substrate. The first substrate 11 includes a transparent substrate, pixel electrodes and wirings disposed on the substrate.

**[0024]** The first substrate 11 includes multiple data lines  $D_1, D_2, \dots, D_N$ , multiple scanning lines  $G_1, G_2, \dots, G_L$  which are perpendicular to the multiple data lines, and multiple pixel units  $P_1, P_2, \dots, P_X$  which are defined by the multiple data lines  $D_1, D_2, \dots, D_N$  and the multiple scanning lines  $G_1, G_2, \dots, G_L$ . Each of the pixel units connects with a corresponding scanning line and a corresponding data line.

**[0025]** Wherein, the multiple scanning lines  $G_1, G_2, \dots, G_L$  are connected with a gate driver 21, the multiple data lines  $D_1, D_2, \dots, D_N$  are connected with a source driver 22. The gate driver 21 provides a scanning voltage to the multiple pixel units  $P_1, P_2, \dots, P_X$ . The source driver 22 provides a driving voltage to the multiple pixel units  $P_1, P_2, \dots, P_X$ .

**[0026]** FIG. 3 is a schematic diagram of one pixel unit of an LCD panel shown in FIG. 2. With reference to FIG. 3, a pixel electrode of one pixel unit 30 of the LCD panel 10 correspondingly connects with one scanning line 31 and one data line 32. The pixel electrode of the pixel unit 30 includes multiple first strip shape patterns 33, multiple strip-shaped (ITO) gaps 34, a second electrode pattern 35, and a third electrode pattern 36.

**[0027]** The second electrode pattern 35 defines an aperture area of the pixel unit 30. Third electrode pattern 36 has two strips which are perpendicular to each other and form a cross shape. The third electrode pattern 36 defines the pixel electrode of the pixel unit 30 as a first region  $O_1$ , a second region  $O_2$ , a third region  $O_3$ , and a fourth region  $O_4$  such that the pixel electrode of the pixel unit 30 is arranged as a matrix.

**[0028]** The first region  $O_1$  located at upper left side and the second region  $O_2$  located at upper right side are disposed at a same horizontal level and disposed side by side. The fourth region  $O_4$  located at lower right side and the first region  $O_1$  are disposed as a diagonal arrangement. The third region  $O_3$  located at lower left side and the second region  $O_2$  disposed as a diagonal arrangement. Preferably an area of the first region  $O_1$ , an area of the second region  $O_2$ , an area of the third region  $O_3$ , and an area of the fourth region  $O_4$  are the same.

**[0029]** Furthermore, an arrangement direction of the first electrode pattern 33 of the first region  $O_1$  and an arrangement

direction of the first electrode pattern 33 of the fourth region  $O_4$  are the same. For example, the arrangement direction is as a first direction  $D_1$  shown in FIG. 3. An arrangement direction of the first electrode pattern 33 of the second region  $O_2$  and an arrangement direction of the first electrode pattern 33 of the third region  $O_3$  are the same. For example, the arrangement direction is as a second direction  $D_2$  shown in FIG. 3. Preferably, the first direction  $D_1$  and the second direction  $D_2$  are perpendicular to each other. In this embodiment, the first direction  $D_1$  and a horizontal direction form a 45 degree angle. Correspondingly, the second direction  $D_2$  and the horizontal direction also form a 45 degree angle. Wherein, the horizontal direction means that a direction along and parallel with the scanning line 31, and from the first region  $O_1$  toward the second region  $O_2$ , or from the third region  $O_3$  toward the fourth region  $O_4$ .

**[0030]** In the pixel unit 30, the data line 32 is disposed between the first region  $O_1$  and the second region  $O_2$ , and also disposed between the third region  $O_3$  and the fourth region  $O_4$ . That is, the data line 32 is corresponding to the third pattern 36 and is insulated from and disposed below the third pattern 36.

**[0031]** In the present embodiment, for each pixel unit 30, the data line 32 is disposed between the multiple regions such that the opaque data line 32 is overlapped with the dark fringes between the multiple regions (that is, between the first region  $O_1$  and the second region  $O_2$ , and between the third region  $O_3$  and the fourth region  $O_4$ ) when the LCD panel is displaying. As a result, the light-shielding area corresponding to the data line 32 is reduced, that is, the light-transparent area corresponding to the data line 32 is increased. Accordingly, the penetration ratio and the aperture ratio of the pixel unit 30 and the liquid crystal display panel 10 having the pixel unit 30 are increased.

**[0032]** In another embodiment, as shown in FIG. 4, a pixel electrode of each pixel unit 40 has eight regions, and the pixel electrode connects with a data line 41.

**[0033]** As shown in FIG. 5, a pixel electrode of each pixel unit 50 includes sixteen regions. For the pixel structure as the present embodiment, the pixel electrode of each pixel unit 50 connects with three data lines 51. The data lines 51 are disposed along a vertical direction and among the multiple regions.

**[0034]** The distances between two adjacent data lines can be the same or not the same. Along the vertical direction, the heights  $L$  of the regions can be equal or not equal. Along an extension direction which is perpendicular to the data line, widths  $H$  of the regions can be the same or not the same. The scanning lines connected with the pixel electrode can be one or multiple. The number of the scanning lines and the electrode patterns of the regions can be determined according to the number of the thin-film transistors connected with the pixel electrode and the structure of the thin-film transistor.

**[0035]** In summary, the pixel electrode of each pixel unit connects with at least one data line, and the pixel electrode of each pixel unit includes multiple regions arranged as a matrix, and the data lines are disposed between adjacent two columns of the regions. As a result, the opaque data lines are overlapped with the dark fringes between the multiple regions when the LCD panel is displaying. As a result, the light-shielding area corresponding to the data line is reduced, that is, the light-transparent area corresponding to the data line is increased. Accordingly, the penetration ratio and the aperture

ratio of the pixel unit and the liquid crystal display panel having the pixel unit are increased.

**[0036]** The above embodiments of the present invention are not used to limit the claims of this invention. Any use of the content in the specification or in the drawings of the present invention which produces equivalent structures or equivalent processes, or directly or indirectly used in other related technical fields is still covered by the claims in the present invention.

What is claimed is:

1. An array substrate including multiple pixel units, wherein, each of the multiple pixel units connects with one scanning line and at least two data lines; a pixel electrode of each pixel unit includes multiple regions arranged as a matrix; and wherein, in each pixel unit, distances between two adjacent data lines are different; data lines are disposed between adjacent two columns of the regions; along a vertical direction, heights of the regions of the pixel electrode are not equal; along an extension direction which is perpendicular to the data line, widths of the regions of the pixel electrode are equal.
2. An array substrate including multiple pixel units, wherein, a pixel electrode of each multiple pixel unit connects with at least one data line; the pixel electrode of each pixel unit includes multiple regions arranged as a matrix; the at least one data line is disposed between adjacent two columns of the regions.
3. The array substrate according to claim 2, wherein, the pixel electrode of each pixel unit connects with one data line; the pixel electrode of each pixel unit includes a first region, a second region, a third region, and a fourth region; the first region and the second region are disposed side by side; the first region and the fourth region are disposed as a diagonal arrangement; the second region and the third region are disposed as a diagonal arrangement; the one data line is disposed between the first region and the second region, and is also disposed between the third region and the fourth region.
4. The array substrate according to claim 3, wherein, an arrangement direction of an electrode pattern of the first region and an arrangement direction of an electrode pattern of the fourth region are the same; an arrangement direction of an electrode pattern of the second region and an arrangement direction of an electrode pattern of the third region are the same.
5. The array substrate according to claim 3, wherein, an arrangement direction of an electrode pattern of the first region and an arrangement direction of an electrode pattern of the fourth region form a first direction; an arrangement direction of an electrode pattern of the second region and an arrangement direction of an electrode pattern of the third region form a second direction; wherein, the first direction and the second direction are perpendicular to each other.
6. The array substrate according to claim 3, wherein, an area of the first region, an area of the second region, an area of the third region, and an area of the fourth region are the same.
7. The array substrate according to claim 3, wherein, the pixel electrode includes multiple strip-shaped gaps, multiple first strip shape patterns, a second electrode pattern, and a third electrode pattern; the gaps and the first strip shape patterns are disposed alternately; the second electrode pattern surrounds the first region, the second region, the third region,

and the fourth region; the third electrode pattern is used for defining the first region, the second region, the third region, and the fourth region.

8. The array substrate according to claim 2, wherein, the pixel electrode of each pixel unit connects with at least two data lines; along a vertical direction, heights of the regions of the pixel electrode are not equal; along an extension direction which is perpendicular to the data line, widths of the regions of the pixel electrode are equal.

9. The array substrate according to claim 2, wherein, in each pixel unit, distances between two adjacent data lines are different.

10. The array substrate according to claim 2, wherein, the pixel electrode of each pixel unit connects with one scanning line.

11. A liquid crystal display (LCD) panel, comprising:  
a liquid crystal layer;  
a color filter substrate; and  
an array substrate;

wherein, the color filter substrate and the array substrate are disposed oppositely with an interval; the liquid crystal layer is filled between color filter substrate and the array substrate; and

wherein the array substrate including multiple pixel units; a pixel electrode of each multiple pixel unit connects with at least one data line; the pixel electrode of each pixel unit includes multiple regions arranged as a matrix; the at least one data line is disposed between adjacent two columns of the regions.

12. The LCD panel according to claim 11, wherein, the pixel electrode of each pixel unit connects with one data line; the pixel electrode of each pixel unit includes a first region, a second region, a third region, and a fourth region; the first region and the second region are disposed side by side; the first region and the fourth region are disposed as a diagonal arrangement; the second region and the third region are disposed as a diagonal arrangement; the one data line is disposed between the first region and the second region, and is also disposed between the third region and the fourth region.

13. The LCD panel according to claim 12, wherein, an arrangement direction of an electrode pattern of the first region and an arrangement direction of an electrode pattern of the fourth region are the same; an arrangement direction of an electrode pattern of the second region and an arrangement direction of an electrode pattern of the third region are the same.

14. The LCD panel according to claim 12, wherein, an arrangement direction of an electrode pattern of the first region and an arrangement direction of an electrode pattern of the fourth region form a first direction; an arrangement direction of an electrode pattern of the second region and an arrangement direction of an electrode pattern of the third region form a second direction; wherein, the first direction and the second direction are perpendicular to each other.

15. The LCD panel according to claim 12, wherein, an area of the first region, an area of the second region, an area of the third region, and an area of the fourth region are the same.

16. The LCD panel according to claim 12, wherein, the pixel electrode includes multiple strip-shaped gaps, multiple first strip shape patterns, a second electrode pattern, and a third electrode pattern; the gaps and the first strip shape patterns are disposed alternately; the second electrode pattern surrounds the first region, the second region, the third region,

and the fourth region; the third electrode pattern is used for defining the first region, the second region, the third region, and the fourth region.

**17.** The LCD panel according to claim **11**, wherein, the pixel electrode of each pixel unit connects with at least two data lines; along a vertical direction, heights of the regions of the pixel electrode are not equal; along an extension direction which is perpendicular to the data line, widths of the regions of the pixel electrode are equal.

**18.** The LCD panel according to claim **11**, wherein, in each pixel unit, distances between two adjacent data lines are different.

**19.** The LCD panel according to claim **11**, wherein, the pixel electrode of each pixel unit connects with one scanning line.

\* \* \* \* \*

专利名称(译)	液晶显示面板和阵列基板		
公开(公告)号	<a href="#">US20160139474A1</a>	公开(公告)日	2016-05-19
申请号	US14/426363	申请日	2014-11-21
[标]申请(专利权)人(译)	深圳市华星光电技术有限公司		
申请(专利权)人(译)	深圳市中国星光电科技有限公司.		
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优先权	201410659998.6 2014-11-18 CN		
外部链接	<a href="#">Espacenet</a> <a href="#">USPTO</a>		

摘要(译)

公开了一种液晶显示面板和阵列基板。阵列基板的每个像素单元的像素电极对应地与至少一条数据线连接。像素电极包括布置为矩阵的多个区域。数据线设置在相邻的两列区域之间。因此，增加了像素单元的穿透率和孔径比。

