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(54) REDUNDANCY SHIFT REGISTER CIRCUIT FOR DRIVER CIRCUIT IN ACTIVE MATRIX TYPE LIQUID CRYSTAL DISPLAY DEVICE

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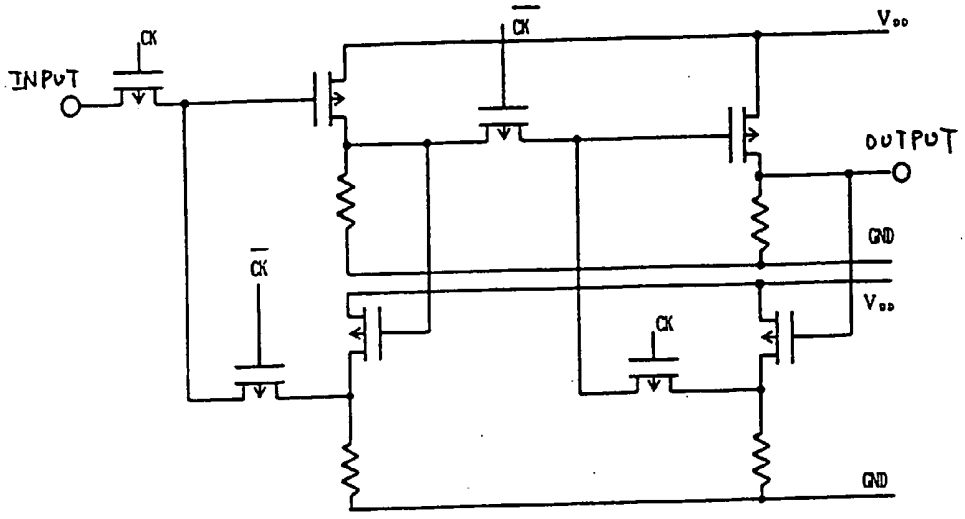
(52) **U.S. Cl.** **345/92**

(57) **ABSTRACT**

In accordance with the present invention, an active matrix display device is presented. The display device comprises a substrate having an insulating surface, a plurality of pixel electrodes arranged in a matrix form over the substrate, and a plurality of switching elements operationally connected to the pixel electrodes. Each of the switching elements further comprise a thin film transistor. The display device further includes a display medium comprising an emissive material that is capable of electrically changing luminous strength disposed at each of the pixel electrodes, and a driver circuit that includes a plurality of thin film transistors for driving the plurality of switching elements. Each of the plurality of thin film transistors comprise a crystallized semiconductor layer, a gate insulating film adjacent to the crystallized semiconductor layer and a gate electrode adjacent to the gate insulating film.



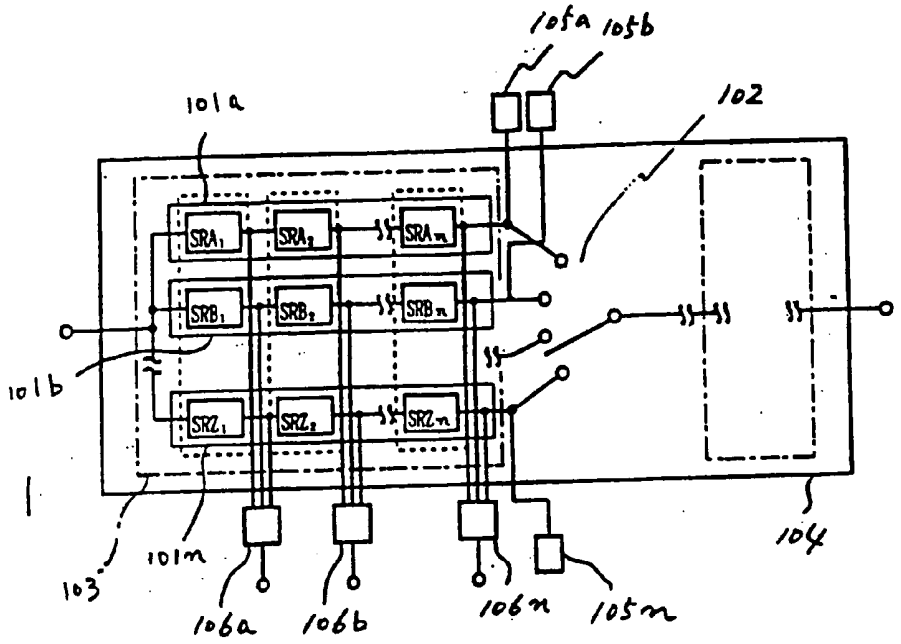


FIG. 1

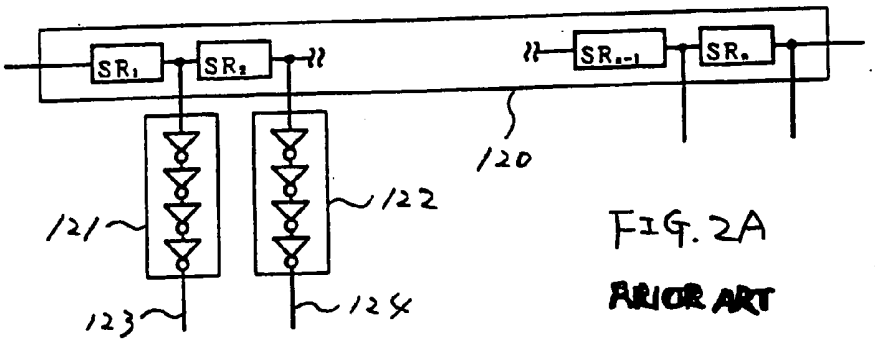


FIG. 2A

PRIOR ART

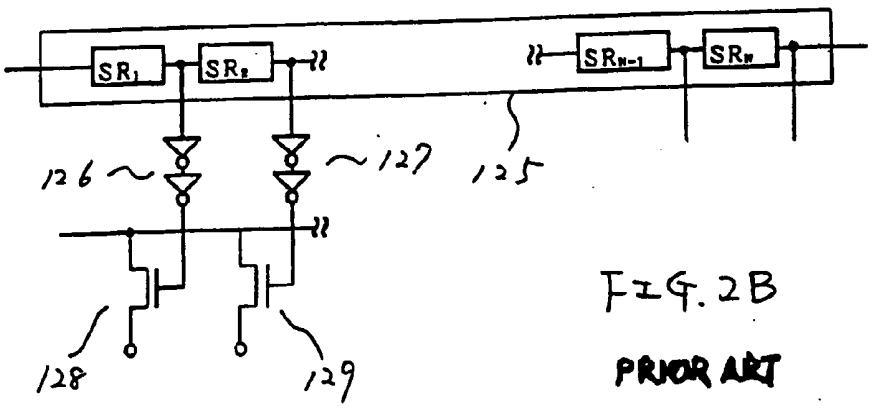


FIG. 2B

PRIOR ART

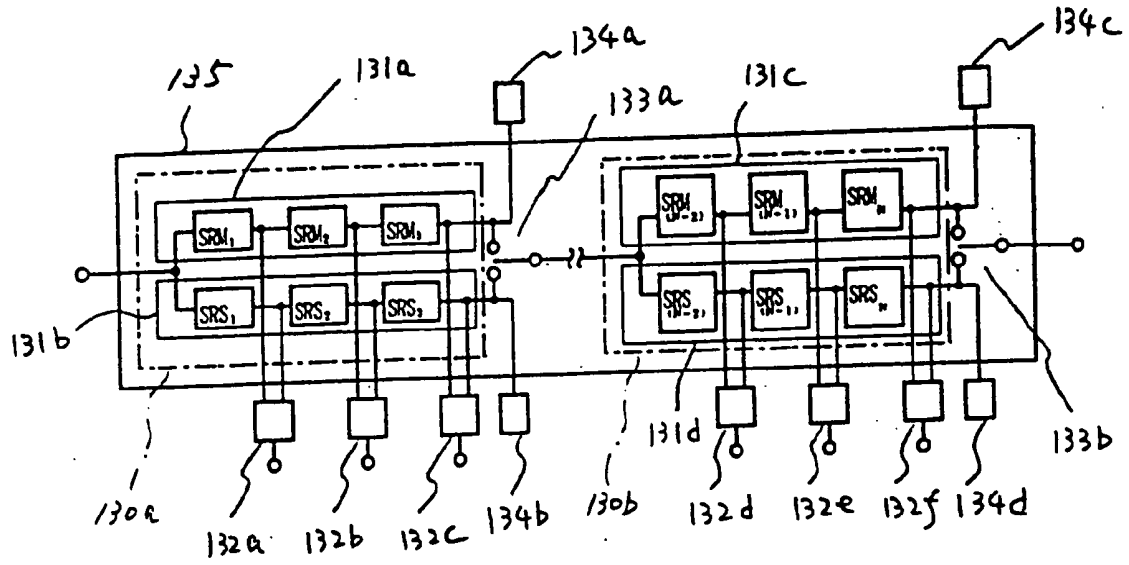

135
131a
134a
133a
131c
134c
131b
131d
133b
130a
130b
132a
132b
132c
134b
132d
132e
132f
134d

FIG. 3

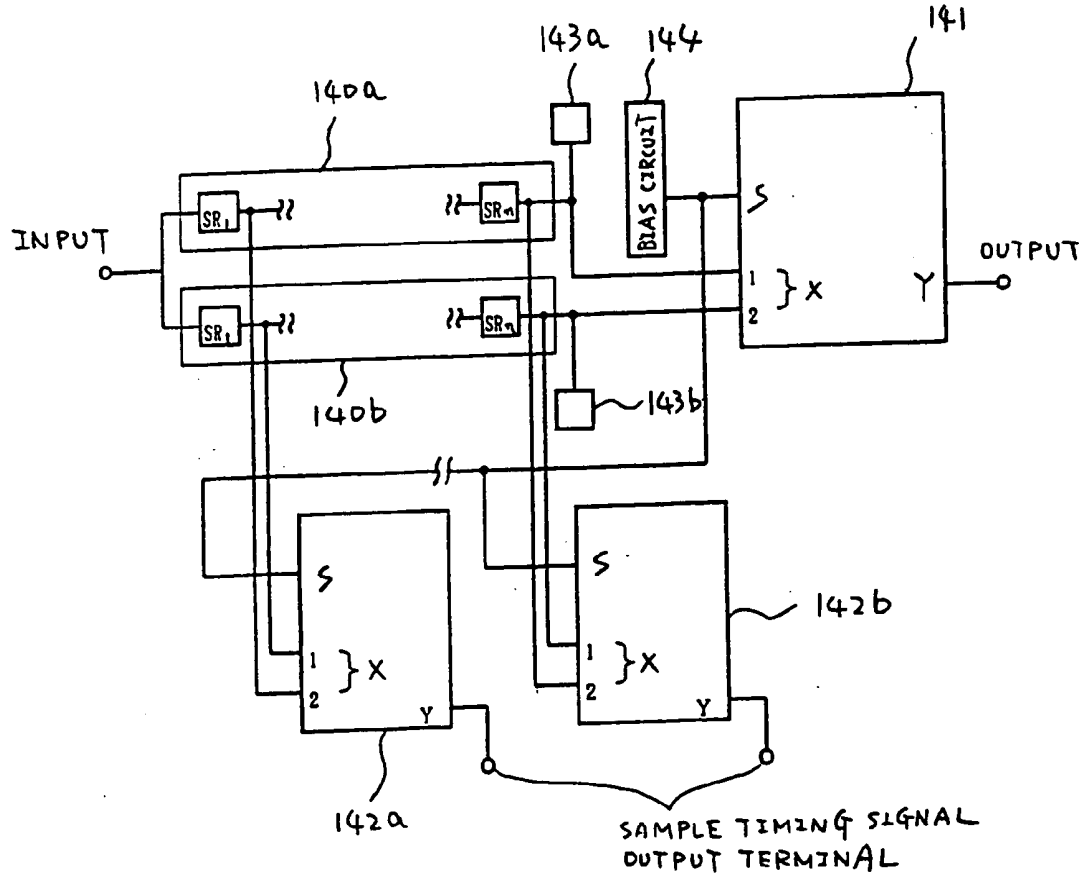

143a
144
141
140a
BIAS CIRCUIT
INPUT
OUTPUT
S
1
2
X
Y
140b
143b
142b
142a
SAMPLE TIMING SIGNAL
OUTPUT TERMINAL

FIG. 4

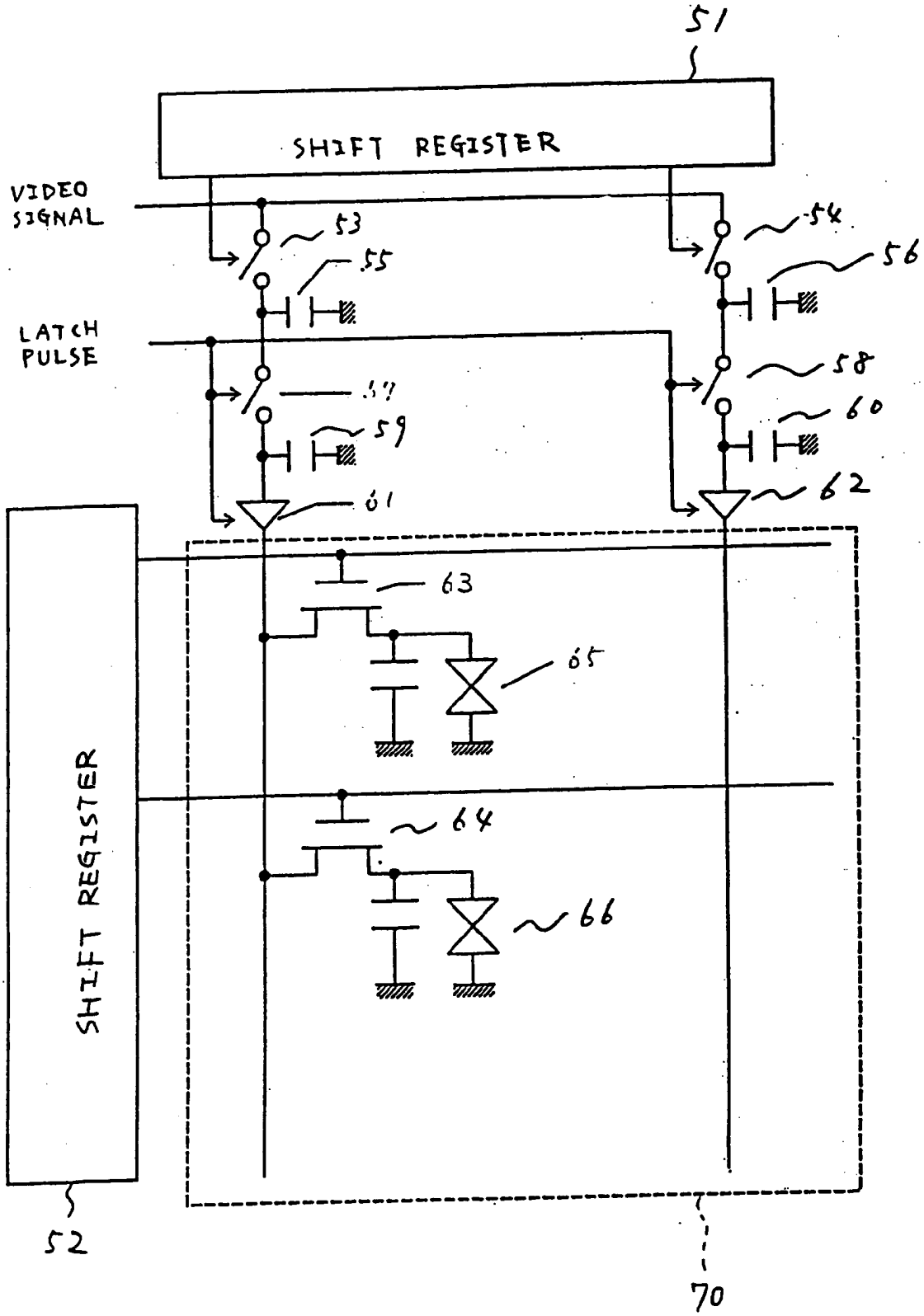


FIG. 5

PRIOR ART

Fig 6A

PRIOR ART

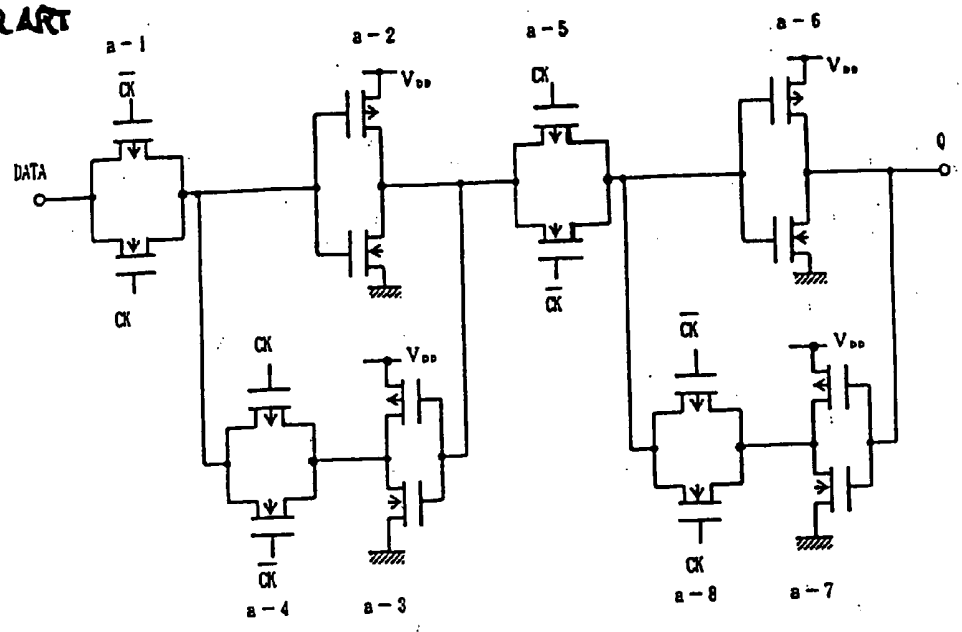


Fig 6B

PRIOR ART

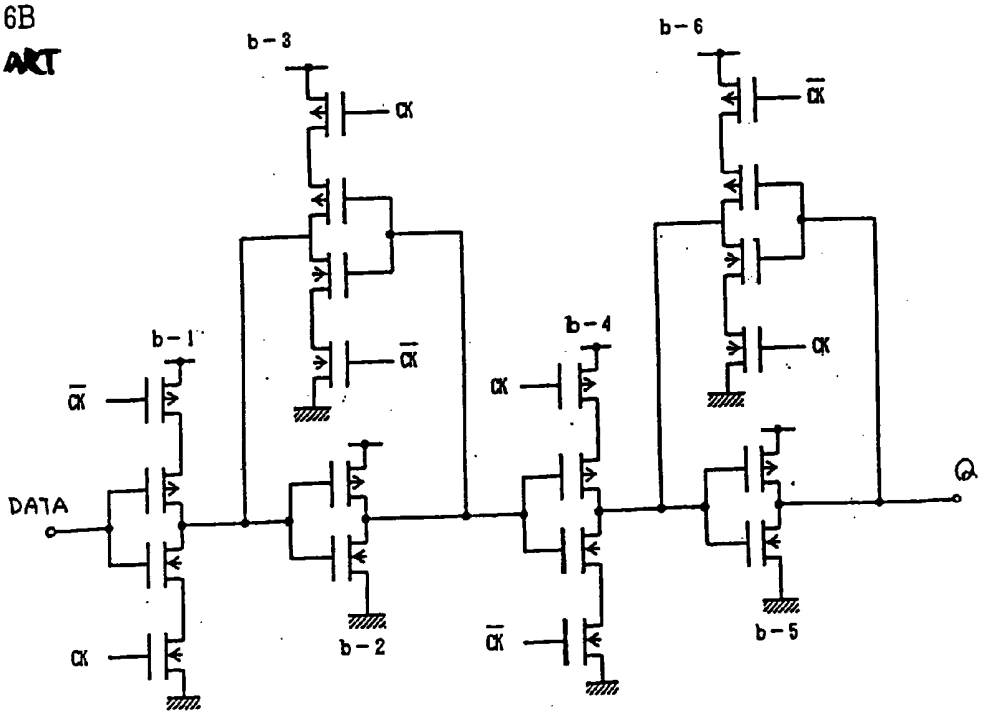


Fig 7A

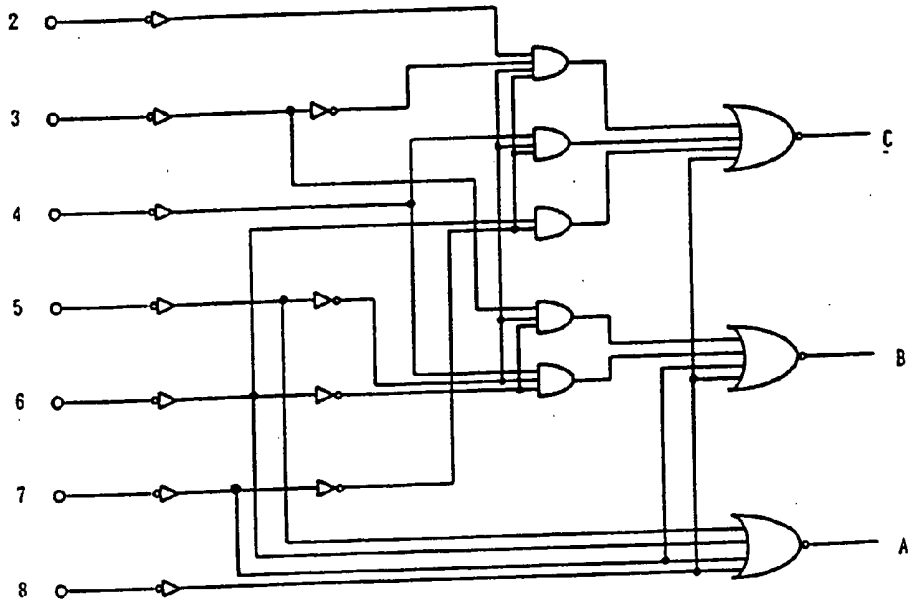
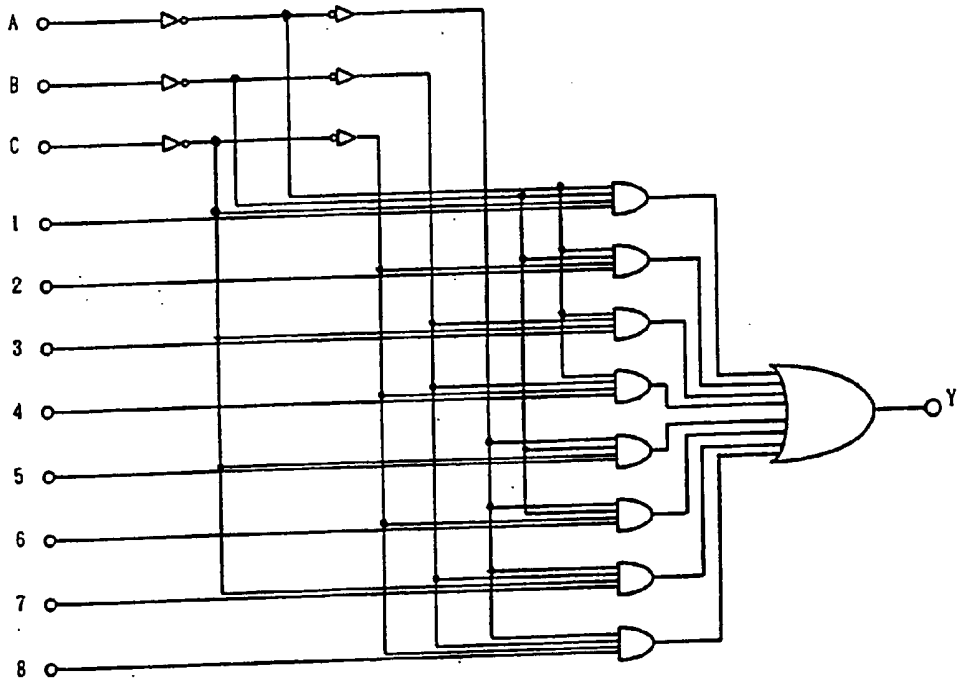


Fig 7B



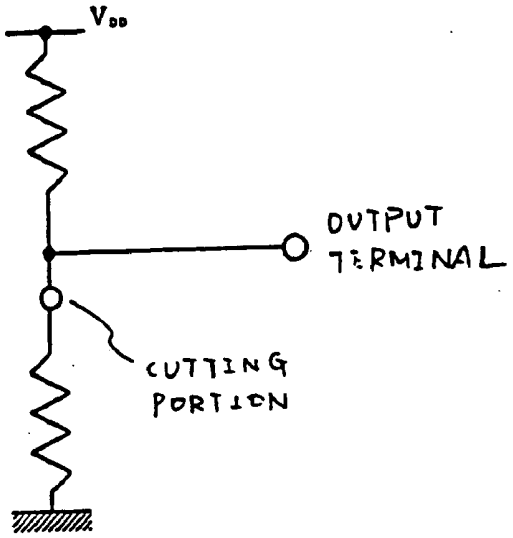


FIG. 8A

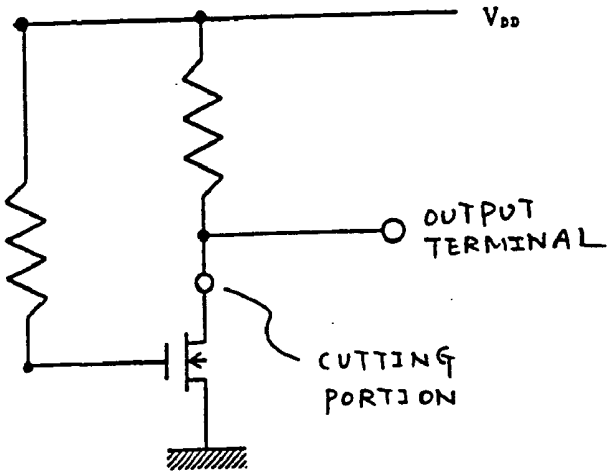


FIG. 8B

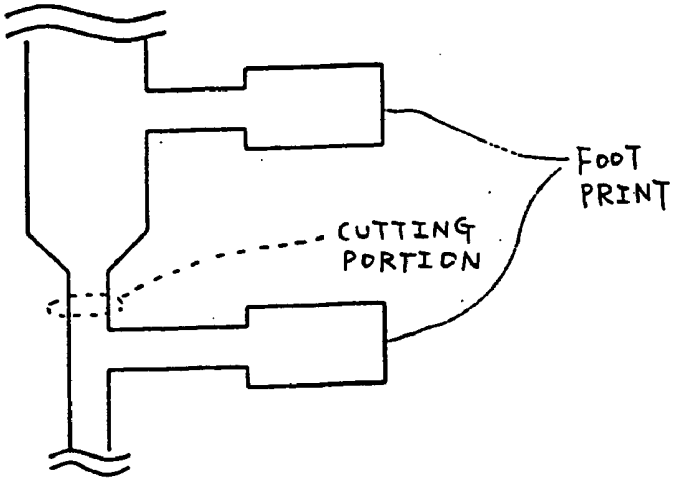


FIG. 8C

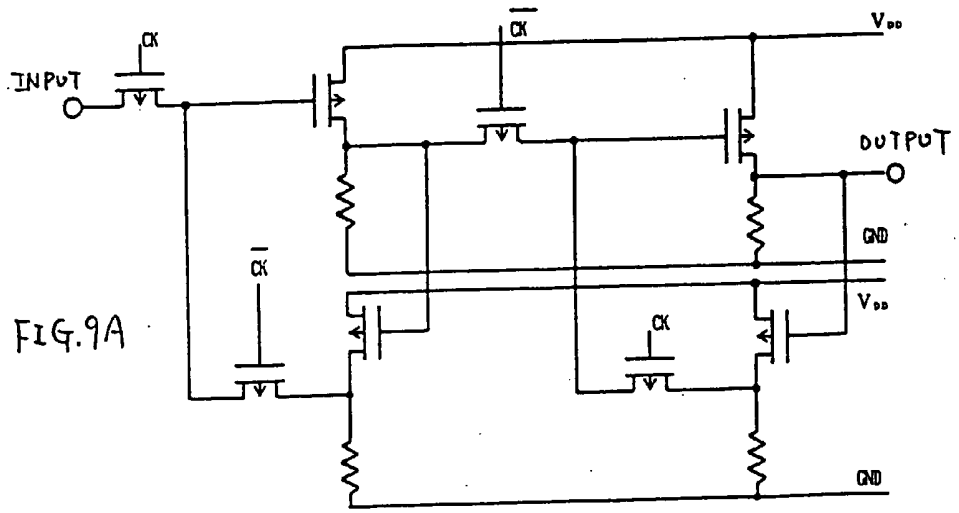


FIG.9A

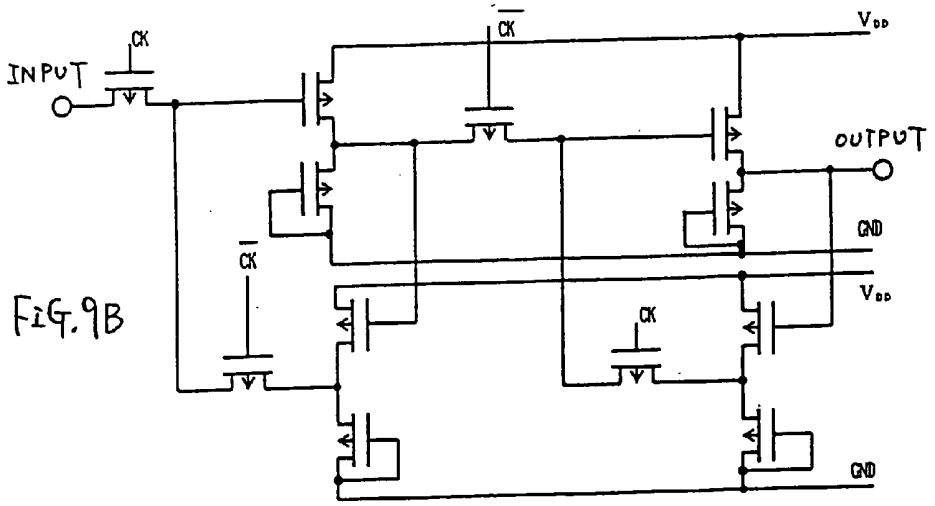


FIG.9B

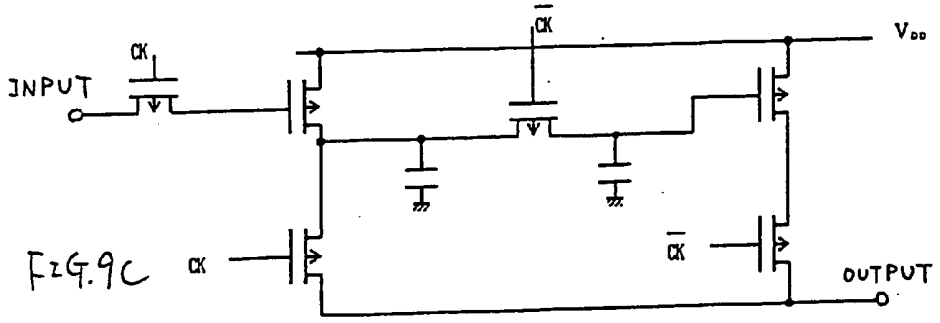


FIG.9C

Fig 10A

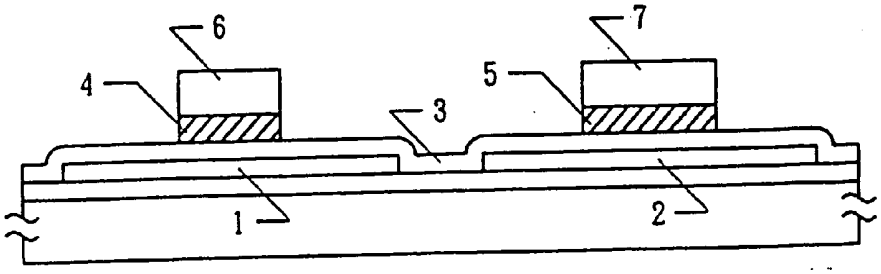


Fig 10B

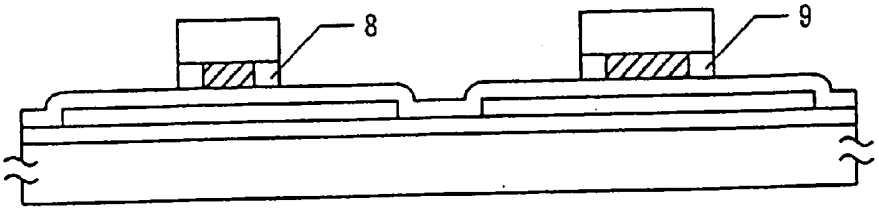


Fig 10C

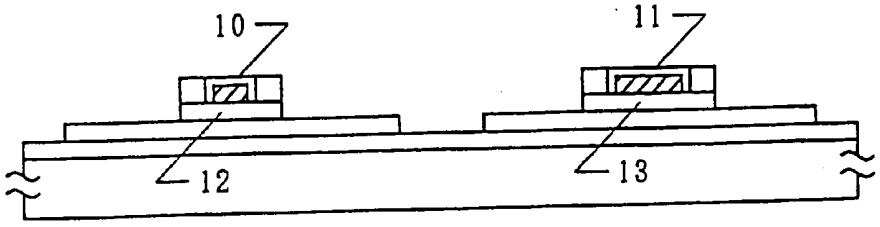


Fig 10D

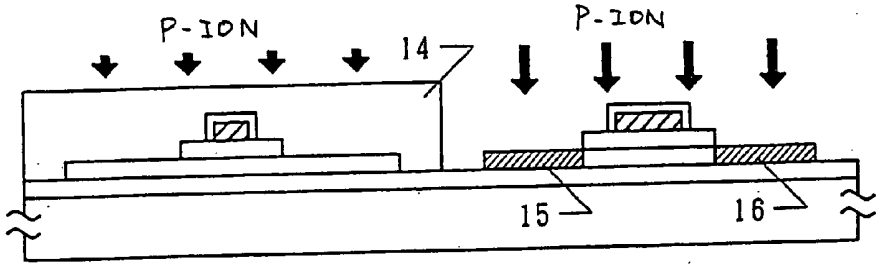


Fig 10E

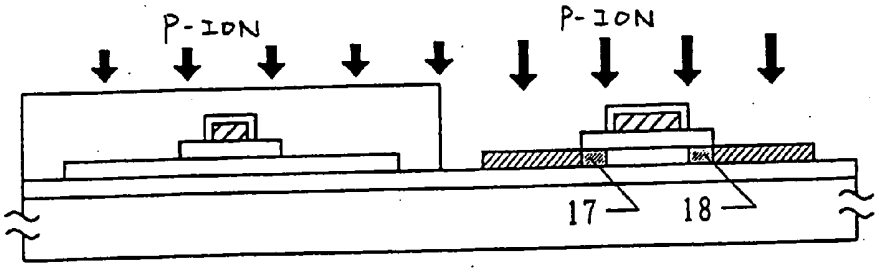


Fig 10F

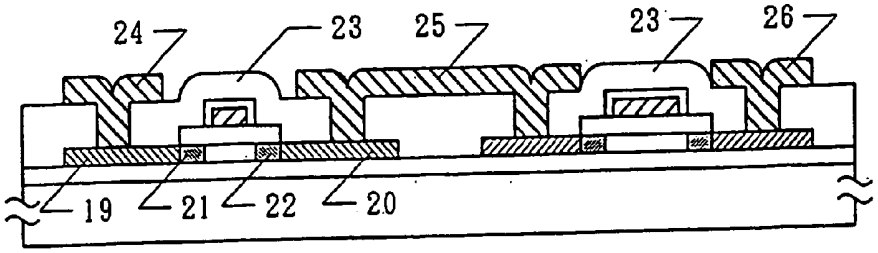


FIG. 11B

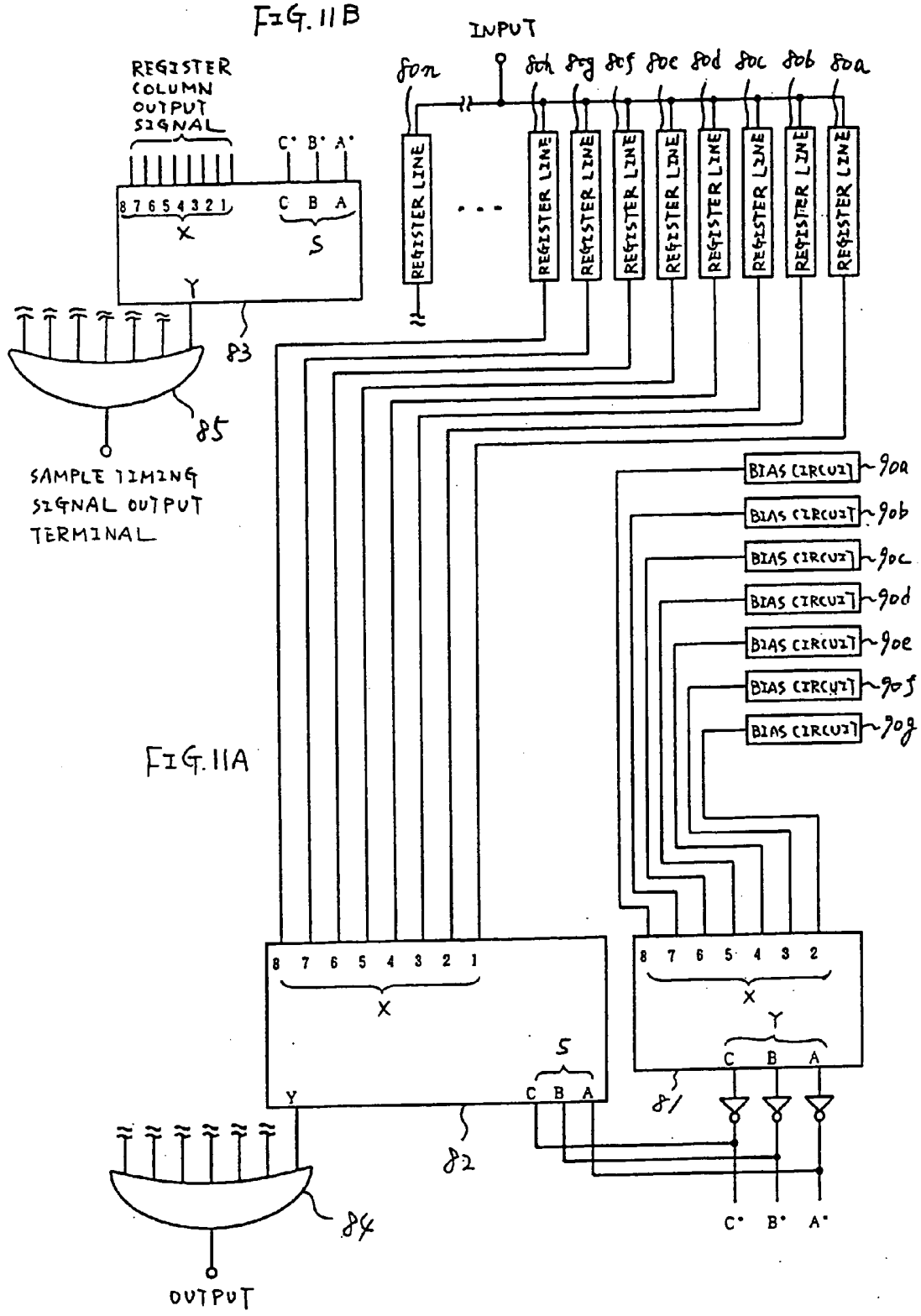


FIG. 11A

INPUT							OUTPUT		
2	3	4	5	6	7	8	A	B	C
H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	L
*	L	H	H	H	H	H	H	L	H
*	*	L	H	H	H	H	H	L	L
*	*	*	L	H	H	H	L	H	H
*	*	*	*	L	H	H	L	H	L
*	*	*	*	*	L	H	L	L	H
*	*	*	*	*	*	L	L	L	L

*:don' t care

FIG. 12

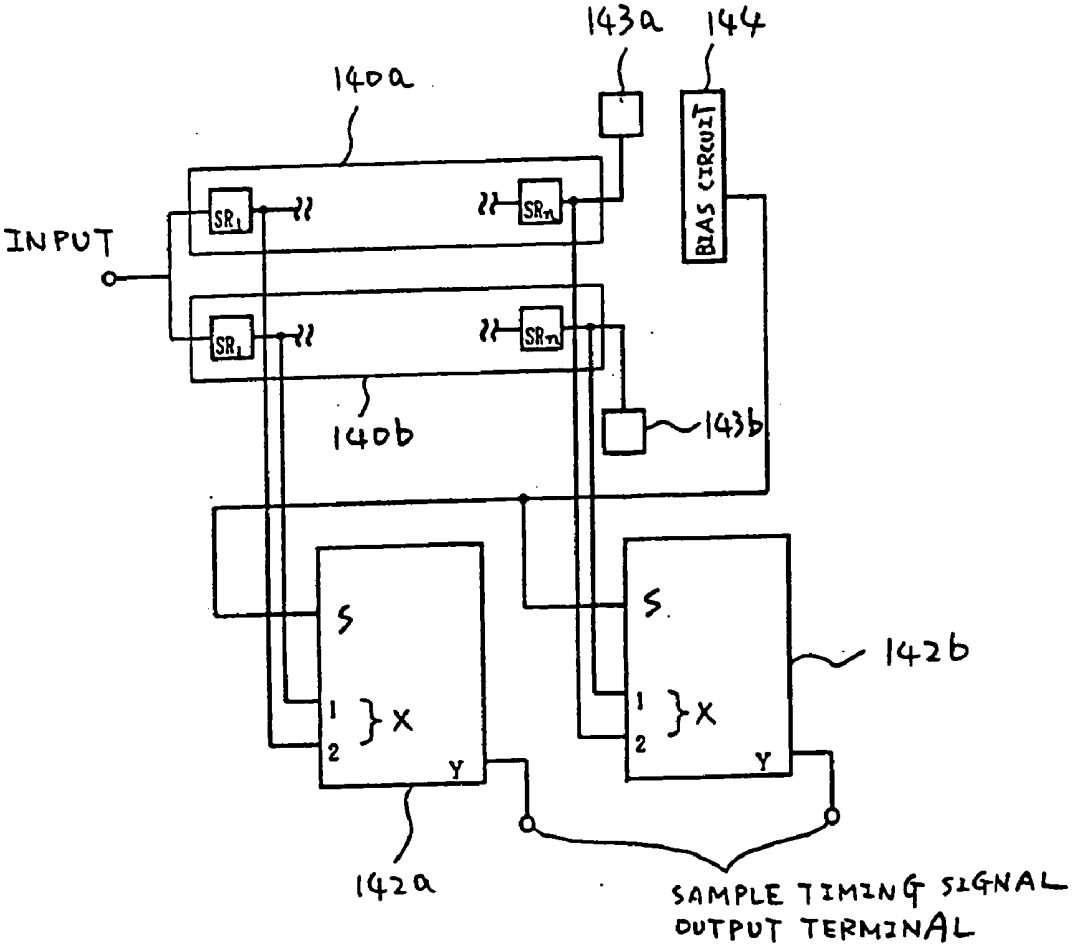

143a
144
140a
BIAS CIRCUIT
INPUT
SR1
SRn
SR1
SRn
140b
143b
S
1
2
X
Y
142b
S
1
2
X
Y
142a
SAMPLE TIMING SIGNAL
OUTPUT TERMINAL

FIG. 13

REDUNDANCY SHIFT REGISTER CIRCUIT FOR DRIVER CIRCUIT IN ACTIVE MATRIX TYPE LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a shift register circuit constructed by thin film transistor (TFTs), in particular, a redundancy shift register circuit.

[0002] A shift register circuit in which TFTs are used is utilized in a driver circuit of an image sensor or a liquid crystal display (LCD) device, in particular, recently, in a driver circuit of an active matrix type display device.

[0003] In an active matrix type display device, each pixel is arranged in a cross section portion of an active matrix circuit and connected with a switching element, and image information is controlled by on/off of the switching element. As a display media of such display device, a liquid crystal, plasma, an object (state) capable of electrically changing an optical characteristic (reflectance, refractive index, transmissivity, emission (luminous) strength) or the like are used. As a switching element, in particular, a three terminal element, that is, a field effect transistor having a gate, a source and a drain is used.

[0004] In a matrix circuit, a signal line (a gate line) which is arranged in parallel to a line is connected with gate electrodes of transistors with respect to the line, and a signal line (a source line) which is arranged in parallel to a column is connected with source (or drain) electrodes of the transistors with respect to the column. A circuit for driving the gate line is referred to as a gate driver circuit, and a circuit for driving the source line is referred to as a source driver circuit.

[0005] Since the gate driver circuit generates a vertical line scan timing signal with respect to an active matrix type display device, a shift register includes serial-connected registers (in a single line) corresponding to the number of gate lines with a vertical direction. As a result, switching of thin film transistors (TFTs) in an active matrix type display device is performed by the gate driver circuit.

[0006] Since the source driver circuit generates a horizontal line image signal of image data to be displayed on an active matrix type display device, a shift register includes serial-connected registers (in a single line) corresponding to the number of source lines with a horizontal direction. Also, by a latch pulse synchronous with a horizontal scan signal, an analog switch is turned on or off. As a result, a current is supplied from the source driver circuit to TFTs in an active matrix type display device, to control alignment of a liquid crystal cell.

[0007] Referring to **FIG. 5**, a common active matrix type display device will be described.

[0008] A horizontal line scan timing signal is generated by a shift register **51**. Analog switches **53** and **54** are turned on and then a video signal is stored in analog memories **55** and **56** in response to the horizontal line scan timing signal. Image data corresponding to the video signal stored in the analog memories **55** and **56** is stored in analog memories **59** and **60** through analog switches **57** and **58** turned on by timing of a latch pulse. The image data is supplied from the analog buffers **59** and **60** to source lines of TFTs **63** and **64** through analog buffers **61** and **62** in an active matrix circuit **70** of an active matrix type liquid crystal display device in timing of the latch pulse.

[0009] On the other hand, a vertical line scan timing signal is generated by a shift register **52** and then supplied to gate lines of the TFTs **63** and **64** in the active matrix circuit **70** of the active matrix type liquid crystal display device. Therefore, the image data (voltage) supplied to the source lines is applied to liquid crystals **65** and **66**, to determine alignment of the liquid crystals **65** and **66** connected with drain lines of the TFTs **63** and **64**, the active matrix type liquid crystal display device is operated Dy the above operation.

[0010] Generally, a shift register includes a circuit as shown in **FIGS. 6A and 6B**, in particular, a D-type flip-flop. **FIG. 6A** shows a D-type flip-flop constructed using analog switches, and **FIG. 6B** shows a D-type flip-flop constructed using clocked invertors. These operation will be described below.

[0011] In **FIG. 6A**, when an operation clock CK is a high level (H) and an input signal DATA is a high level (H), a complementary type transmission gate a-**1** is turned on and then the input signal DATA is input to a complementary type invertor circuit a-**2**. Therefore, an output of the complementary type invertor circuit a-**2** becomes a low level (L). In this state, complementary type transmission gates a-**4** and a-**5** are in a turn off state.

[0012] When the operation clock CK is changed to a low level (L) while the input signal DATA is a high level (H), the complementary transmission gate a-**1** becomes a turn off state, the complementary type transmission gates a-**4** and a-**5** become a turn on state. Therefore, an output of the complementary invertor circuit a-**2** is held to a low level (L).

[0013] Also, since the complementary type transmission gate a-**5** becomes a turn on state, an output of an complementary type invertor circuit a-**6** becomes a high level (H). In this state, a complementary type transmission gate a-**3** becomes a turn off state.

[0014] When the operation clock CK is changed to a high level (H) again, the complementary transmission gate a-**5** becomes a turn off state and the complementary type transmission gate a-**8** becomes a turn on state, so that a previous signal level is held. Therefore, an output of the complementary type invertor circuit a-**6** can be held to an input signal DATA having a high level (H) in synchronous with an operation clock CK.

[0015] As a result, a D-type flip-flop can be constructed using transmission gates. Also, when an input signal DATA is a low level (L), the above described operation is performed.

[0016] In **FIG. 6B**, when the operation clock CK is a high level (H) and the input signal DATA is a high level (H), an output of a complementary clocked invertor circuit b-**1** becomes a low level (L) and then an output of the complementary invertor circuit b-**2** becomes a high level (H). In this state, complementary clocked invertor circuits b-**3** and b-**4** are in a turn off state.

[0017] When the operation clock CK is changed to a low level (L) while the input signal DATA is a high level (H). The complementary clocked invertor circuits b-**3** and b-**4** are

turned on, so that an output of the complementary type invertor circuit b-**2** is held to a high level (H). An output of the complementary invertor circuit b-**5** becomes a high level (H). In this state, the complementary clocked invertor circuit b-**6** is a turn off state.

[**0018**] When the operation clock CK is changed to a high level again, the complementary type clocked invertor circuit becomes a turn off state, and the complementary type clocked invertor circuit becomes a turn on state. Therefore, an output of the complementary type invertor circuit can be held to an input signal DATA having a high level (H) in synchronous with an operation clock CK.

[**0019**] As a result, a D-type flip-flop is constructed by clocked invertors. Also, when an input signal DATA is a low level (L), the above described operation is performed.

[**0020**] In a shift register circuit used in gate and source driving circuits of a common active matrix type display device, as shown in **FIGS. 2A and 2B**, registers having the same number as the number of gate lines (or source lines) are connected in serial. In a gate driver circuit as shown in **FIG. 2A**, outputs of registers SR_i (i=1 to n) in a shift register circuit **120** are connected to gate lines **123** and **124** through invertor type buffer circuits **121** and **122**. In a source driver circuit as shown in **FIG. 2B**, outputs of registers SR_i (i=1 to N) in a shift register circuit **125** are connected to control terminals of sampling transmission gates **128** and **129** through invertor type buffer circuits **126** and **127**.

[**0021**] If at least one register has defect in the shift register circuit having serial-connected registers, image data and scan timing signals output from the defect register and later connected register are abnormal, an accuracy image cannot be obtained. This problem is due to a yield of a shift register.

SUMMARY OF THE INVENTION

[**0022**] The object of the present invention is to solve the above problems.

[**0023**] As shown in **FIG. 1**, a shift register circuit **104** includes at least one register group **103** and a register selecting switch **102**, the register group **103** includes register lines **101***a*, **101***b*, . . . , and **101***n* having a plurality of serial-connected registers SRAi, SRBi, . . . , and SRZi (i=1 to n), respectively. The register line selecting switch **103** selects one of the register lines.

[**0024**] In this structure, one register line is used as a main register line, and the other register lines are used as a subregister line. When a plurality of register groups are arranged in a shift register circuit, the register groups are connected with each other in serial, to use as a shift register constructing gate and source driver circuits. Defect detection terminals **105***a*, **105***b*, . . . , **105***n* are arranged with the register lines in the register group, respectively, so that whether or not each register line operates normally is detected. An output of a last register of each shift register line is connected with the register line selecting switch **103**.

[**0025**] The register line selecting switch **103** has at least one bias circuit (as described later). A voltage is always applied to the bias circuit, switching operation by the bias circuit is performed by providing one bias.

[**0026**] When one of the register lines is selected by the register line selecting switch **103**, register column selecting switches **106***a*, **106***b*, . . . , **106***n* selects registers included in the selected one of the register lines, respectively. The number of register column selecting switches coincides with the number of registers included in each register line. Each register column selecting switch selects one of a plurality of input signals as an output signal. A signal for selecting the output signal is generated by using an output signal of the bias circuit.

[**0027**] When defect is detected by examining a main register line using a defect detection terminal, one of subregister lines is examined by another defect detection terminal. When defect is not detected, the register line selecting switch **102** selects the one of the subregister lines. Simultaneously, the register column selecting switches select the registers of the selected subregister lines.

[**0028**] As a result, redundancy is performed for register lines in a register group, so that a yield for a whole shift register circuit can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[**0029**] **FIG. 1** shows a redundancy shift register circuit in a driving circuit of an active matrix type display device according to an embodiment of the present invention;

[**0030**] **FIGS. 2A and 2B** show a shift register circuit in a driving circuit of a common active matrix type display device, respectively;

[**0031**] **FIG. 3** shows a shift register circuit of an embodiment;

[**0032**] **FIG. 4** shows a shift register selecting switch of the embodiment;

[**0033**] **FIG. 5** shows a schematic view of a common active matrix type display device;

[**0034**] **FIGS. 6A and 6B** show a common register, respectively.

[**0035**] **FIGS. 7A and 7B** show a priority encoder circuit and a multiplexer circuit, respectively.

[**0036**] **FIGS. 8A** to **8**C show a bias circuit, respectively.

[**0037**] **FIGS. 9A** to **9**C show a register constructed by p-channel transistors;

[**0038**] **FIGS. 10A** to **10** show a method for forming complementary invertor circuit;

[**0039**] **FIGS. 11A and 113** show a shift register selecting circuit of the embodiment;

[**0040**] **FIG. 12** shows a truth table of a priority encoder circuit; and

[**0041**] **FIG. 13** shows a shift register selecting switch of another embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[**0042**] A thin film device (such as a complementary invertor circuit) used in the present invention will be described below.

[**0043**] A silicon oxide film having a thickness of 1000 to 3000 Å is formed as a base oxide film on a glass substrate (a low alkaline glass such as Corning 7059 or a quartz glass)

by sputtering in an atmosphere containing oxygen. To improve productivity, A film to be deposited by decomposing a tetra-ethyl-ortho-silicate (TEOS) in plasma chemical vapor deposition (CVD) may be used.

[0044] An amorphous silicon film having a thickness of 300 to 5000 Å, preferably 500 to 1000 Å is deposited by plasma CVD and low pressure CVD (LPCVD) and then placed in a reducing atmosphere at 550 to 600° C. for 4 to 48 hours to crystallize it. After this process, crystallinity may be increased (improved) by laser irradiation. The crystallized silicon film is patterned to form island regions **1** and **2**. Further, a silicon oxide film **3** having a thickness of 700 to 1500 Å is formed on the island regions **1** and **2** by sputtering.

[0045] An aluminum (containing Si of 1 weight % or Sc (scandium) of 0.1 to 0.3 weight %) film having a thickness of 1000 Å to 3 μm is formed by electron beam evaporation or sputtering. A photoresist (for example, a product of Tokyo Ohka Co. Ltd. OFPR800/30 cp) is formed by spin coating. When an aluminum oxide film having a thickness of 100 to 1000 Å is formed on a surface thereof by anodization after formation of the photoresist, adhesion to the photoresist is high. Also, by suppressing a leak current from a photoresist, it is effective on formation of a porous anodic oxide in only side surface in a later anodization process. The photoresist and the aluminum film are patterned and etched to form gate electrodes **4** and **5** and mask films **6** and **7**. **(FIG. 10A)**

[0046] The formed substrate is anodized by supplying a current in an electrolytic solution, to form an anodic oxide having a thickness of 3000 to 6000 Å, for example, 5000 Å. The anodization is performed using an acid solution containing citric acid, nitric acid, phosphoric acid, chromic acid, sulfuric acid, oxalic acid or the like of 3 to 20% by applying a voltage of 10 to 30 V to a gate electrode at a constant current. In the embodiment, the anodization is performed in an oxalic acid solution (30° C.) at 10 v for 20 to 40 minutes. A thickness of an anodic oxide is adjusted by an anodization time. **(FIG. 10B)**

[0047] After that, the mask films are removed, and then a current is supplied to the gate electrodes in an electrolytic solution (ethylene glycol solution containing tartaric acid, boric acid, nitric acid of 3 to 10%) again. In order to obtain a superior oxide film, it is preferred that a temperature of the solution is about 10° C. and lower than a room temperature. As a result, barrier type anodic oxides **10** and **11** are formed in upper and side surfaces of the gate electrodes. Thicknesses of the anodic oxides **10** and **11** are proportional to an applied voltage. For example, when an applied voltage is 150 V, an anodic oxide having a thickness of 2000 Å is formed. Thicknesses of the anodic oxides **10** and **11** are determined by a necessary offset size. Although an anodic oxide having a thickness of 300% A or more is formed by applying 250 V or higher, since this influences TFT characteristics, it is desired that an anodic oxide having a thickness of 3000 Å or less is formed. In the embodiment, a voltage is increased until 80 to 150 V and selected by necessary thicknesses of the anodic oxides **10** and **11**.

[0048] In this state, although a barrier type anodic oxide is formed by a later process, the barrier type anodic oxides **10** and **11** are formed between the porous anodic oxides **8** and **9** and the gate electrodes **4** and **5** without forming barrier type anodic oxides outside porous anodic oxides.

[0049] An insulating film **3** is etched by dry etching or wet etching. A depth of etching is arbitrary. Etching may be performed until an active layer formed under the insulating film **3** is exposed. Etching may be stopped on halfway. However, it is desired to etch the insulating film **3** until an active layer is exposed, in mass productivity, yield and uniformity. In this state, insulating films **12** and **13** covered with the anodic oxides **8** and **9** and the gate electrodes **4** and **5** remain as a gate insulating film. **(FIG. 10C)**

[0050] After that, the anodic oxides **8** and **9** are removed, it is preferred that a solution containing phosphoric acid, for example, a mixture acid containing phosphoric acid, acetic acid and nitric acid is used as an etchant. In using an etchant containing phosphoric acid, an etching rate of a porous anodic oxide is ten times or more as large as that of a barrier type anodic oxide. Therefore, since barrier type anodic oxides **10** and **11** are not etched substantially by the enchant containing phosphoric acid, the gate electrodes can be protected from etching.

[0051] In such structure, a source and a drain are formed by implanting N-type or P-type impurity ion into an active layer. In a state wherein a left TFT region is covered with a mask **14**, a phosphorus ion is irradiated (introduced) by ion doping at a relatively low speed (an accelerating voltage of 5 to 30 kV, 20 kV in the embodiment). A doping gas is phosphine (PH_3). A dose is 5×10^{14} to 5×10^{15} cm^{-2}. In this process, since a phosphorus ion cannot be transmitted through the insulating film **13**, it is implanted into only region in which a surface is exposed, so that a drain **15** and a source **16** of an N-channel type TFT are formed. **(FIG. 10D)**

[0052] Also, a phosphorus ion is irradiated by ion doping at a relatively high speed (an accelerating voltage of 60 to 120 kV, 90 kV in the embodiment). A dose is 1×10^{13} to 5×10^{14} cm^{-2}. In this process, a posphorus ion is transmitted through the insulating film **13** and reaches a region formed under the film **13**. However, since a dose is small, N-type regions **17** and **18** each having a low concentration are formed. **(FIG. 10E)**

[0053] After phosphorus doping, the mask is removed. Then, using the N-channel type TFT as a mask, as described above, a source **19**, a drain **20** and a P-type regions **21** and **22** each having a low concentration in a P-channel type TFT. A KrF excimer laser (wavelength of **248** nm and pulse width of **20** ns) is irradiated to activate an impurity ion introduced into an active layer.

[0054] A silicon oxide film having a thickness of 3000 to 6000 Å is formed as an interlayer insulator **23** on a whole surface by CVD. Also, contact holes are formed in a source and a drain of a TFT and then aluminum wiring-electrodes **24** to **26** are formed. Further, hydrogen annealing is performed at 200 to 400° C. As a result, a complementary invertor circuit using TFTs is completed. **(FIG. 10F)**

[0055] A shift register in the embodiment is formed in a basis of the above complementary invertor circuit. A shift register used in a driver circuit of an active matrix type display device and an active matrix circuit having pixel TFTs are formed on the same substrate.

[0056] Referring with **FIG. 3**, an embodiment of the present invention will be described.

[0057] In the embodiment, one main register line and one subregister line are used in each register group, and three

registers are included in each register line. Also, the number of register groups is a positive integer and a multiple of three, for example.

[0058] As shown in **FIG. 3**, a shift register circuit **135** includes register groups **130***a*, . . . , **130***b*. The register group **130***a* includes a main register line **131***a* having registers SRM_1, SRM_2 and SRM_3 and a subregister line **131***b* having registers SRS_1, SRS_2 and SRS_3. The register group **130***b* includes a main register line **131***c* having registers SRM_{N-2}, SRM_{N-1} and SRM_N and a subregister line **131***d* having registers SRS_{N-2}, SRS_{N-1} and SRS_N.

[0059] Register line selecting switches **133***a* and **133***b* are arranged to select the register lines in each register group. Defect detection terminals **134***a* and **134***b* are arranged to detect outputs of last registers of the register lines, so that whether or not each register line includes defect is detected.

[0060] Register column selecting switches **132***a* to **132***f* are arranged to select registers included in the selected register lines in each register group.

[0061] First, the main register line is examined by using the defect detection terminal in each register group. If the line is normal, the register line selecting switch is connected with the main register line. On the other hand, if the main register line has defect, the register line selecting switch is connected with the subregister line.

[0062] A conventional shift register circuit is compared with a shift register circuit according to the present invention.

[0063] In a conventional shift register circuit as shown in **FIG. 2**, when a defective rate per register is $f_n(0<f_n<1)$ and the number of registers to be serial-connected is N (a positive integer and a multiple of three), a probability An which a conventional shift register circuit as shown in **FIG. 2** is operated normally is obtained by the following equation,

$$An=(1-f_n)^N.$$

[0064] In a shift register circuit of the present invention, the same defective rate per register $f_n(0<f_n<1)$ is used. Also, the number of registers when all registers of each register group in one line are connected in serial is used as N (a positive integer and a multiple of three). Further, each register line includes three registers.

[0065] In this state, a probability Bn which one register group is not operated normally is obtained by the following equation,

$$Bn=\{1-(1-f_n)^3\}^2.$$

[0066] Therefore, since the number of register groups is N/3, a probability Cn which a whole shift register circuit is operated normally is obtained by the following equation.

$$\begin{aligned} Cn &= \left[1-\{1-(1-f_n)^3\}^2\right]^{N/3} \\ &= [1-\{1-2(1-f_n)^3+(1-f_n)^6\}]^{N/3} \\ &= [(1-f_n)3\{2-(1-f_n)3\}]^{N/3} \end{aligned}$$

[0067] If $F_n=1-f_n$ and r=N/3 (r is a positive integer),

$$An=F_n^{3r}, \text{ and}$$
$$Cn=F_n^{3r}(2-F_n^3)^r.$$

[0068] In this state, from $0<f_n<1$,

$$0<(1-f_n)=F_n<1, \text{ and}$$
$$0<F_n^3<1.$$

[0069] Therefore,

$$1<(2-F_n^3)<2, \text{ and}$$
$$1<(2-F_n^3)^r<2^r.$$

[0070] From the above relationship,

$$Cn-An=F_n^{3r}\{(2-F_n^3)^r-1\}>0.$$

[0071] As a result, An<Cn.

[0072] When the number of registers included in a source driver circuit is **480** and a defective rate of register is 0.001, a probability An' which a conventional source driver circuit is operated normally is

$$An'=(1-0.001)^{490}=0.619.$$

[0073] On the other hand, a probability Cn' which a redundancy source driver circuit according to the present invention is operated normally is

$$Cn'=[1-\{1-(1-0.001)^3\}^2]^{480/3}=0.999.$$

[0074] Therefore, it is confirmed that An'<Cn'.

[0075] As described above, redundancy of a register line increases a probability which a shift register is operated normally. If a defective rate per register is the same, this relationship is always obtained without depending on the number of registers included in one register line, the number of register lines and the number of register groups.

[0076] Structures of a register line selecting switch will be described below using **FIGS. 11A and 11B**.

[0077] The register line selecting switch includes bias circuit **90***a* to **90***g*, a priority encoder circuit **81** and a multiplexer circuit **82**.

[0078] Output terminals of register lines **80***a* to **80***h* are connected with input terminals (X) of the multiplexer **82**. The bias circuits are arranged in correspondent to register lines each having an output terminal, and the output terminals are connected with input terminals (X) of the priority encoder circuit **81**.

[0079] When outputs of the bias circuits are held, the priority encoder circuit **81** converts a bit position of L of bit string to be input into binary data and then outputs the binary data (bit string) form output terminals (Y) to input signal selecting terminals (S) of the multiplexer circuit **82** and input signal selecting terminals (S) of a multiplexer circuit **83** used as a register column selecting switch through invertor circuits.

[0080] As described above, one of the register lines is selected using a register line selecting switch constructed by a combination of the priority encoder circuit **81**, the multiplexer circuit **82** and the bias circuits **90***a* to **90***g*.

[0081] **FIG. 7A** shows an equivalent circuit of a **8** bit priority encoder circuit, and **FIG. 7B** shows an equivalent circuit of a **8** bit input multiplexer circuit. Also, **FIG. 12** shows a truth table of the priority encoder circuit of **FIG. 7A**.

[0082] **FIG. 4** shows a case wherein two register lines **140***a* and **140***b* are used in one register group. Since the

number of register lines is **2**, it is not necessary to use a priority encoder circuit as described above. Therefore, outputs of all register lines **140***a* and **140***b* are connected with input terminals (X) of a multiplexer circuit **141** for register line selection. An output terminal of a bias circuit **144** is connected with an input signal selecting terminal (S) of the multiplexer circuit **141**. Defect detection terminals **143***a* and **143***b* are used to detect a register line having defect.

[**0083**] When one of register line is normal, a low level (L) bias is supplied to the bias circuit **144** corresponding to the one of the register lines. Therefore, since a level of the input signal selecting terminal (S) of the multiplexer circuit **141** is determined, the multiplexer circuit **141** selects a normal register line, to use an output of a last register of the selected register line as an output of a register group having the selected register line.

[**0084**] A structure of a register column selecting switch will be described below using **FIG. 4**.

[**0085**] Register column selecting stitches includes multiplexer circuits **142***a*, . . . , and **142***b*, respectively. Outputs of the registers SR_1 (SR_n) constructing each column are connected with input terminals (X) of the multiplexer circuits **142***a* (**142***b*) for register column selection. To select a register in a column, an output of the bias circuit **144** is connected with input signal selecting terminals (s) of the multiplexer circuits **142***a* and **142***b*.

[**0086**] As described above, a register column selecting switch is constructed by a combination of the bias circuit **144** and the multiplexer circuits **142***a* and **142***b*.

[**0087**] A structure of a bias circuit will be described using **FIGS. 8A** to **8**C.

[**0088**] In a bias circuit as shown in **FIG. 8A**, a pull-up resistor is connected with a pull-down resistor in serial, and an output terminal and a cutting portion are provided between these resistors. A resistance value ratio between the pull-up resistor and the pull-down resistor is 100:1, and may be set in a range which a voltage level detected on the output terminal becomes a low level (L).

[**0089**] A bias circuit corresponding to a normal register line holds a low level (L), and bias circuits corresponding to register lines other than the normal register line holds a high level (H) by cutting a cutting portion of the bias circuit using a laser to obtain a pull-up state. As a result, an input signal of the multiplexer circuit can be selected.

[**0090**] In a bias circuit as shown in **FIG. 8B**, an analog switch using an N-type TFT is used. As described above, a bias circuit corresponding to a normal register line holds a low level (L), and bias circuits corresponding to register lines other than the normal register line holds a high level (H) by cutting a cutting portion of the bias circuit using a laser to obtain a pull-up state. As a result, an input signal of the multiplexer circuit can be selected.

[**0091**] **FIG. 8C** shows cutting of a cutting portion of a bias circuit. The cutting portion may be cut by applying a high voltage to two foot prints.

[**0092**] As shown in **FIGS. 11A and 11B**, in a case wherein the number of register lines is n (n>2), outputs of last registers of all register lines **80***a* to **80***n* are connect with input terminals (X) of a multiplexer circuit **82** for register line selection. Also, bias circuits **90***a* to **90***g* each having output terminals are arranged in correspondence to the register lines, and the output terminals of the bias circuits **90***a* to **90***g* are connected with input terminals (X) of the priority encoder circuit **81**. The output terminals of the priority encoder circuit **81** is connected with input signal selection terminals of the multiplexer circuit **82** through invertor circuits.

[**0093**] When a normal register line is detected, an output of a bias circuit corresponding to the register line is held to a low level (L). An output of a bias circuit corresponding to the register line is held to a low level (L). Also, an output of a bias circuit corresponding to the register line other than the normal register line is held to a high level (H). As described above, outputs of the priority encoder circuit **81** are determined by holding output levels of the output terminals of the bias circuits. Therefore, since levels of input signal selection terminals of the multiplexer circuit **62** are determined, the multiplexer circuit **82** selects a normal register line, so that an output of a last register of the selected register line is input to an input terminal of an OR circuit **84**. An output of the OR circuit **84** is used as an input of next register group in a case wherein a plurality of register groups are arranged in a shift register circuit.

[**0094**] A register column is defined at a column direction of registers of register lines. Multiplexer circuits for register column selection are arranged for each register column. The number of the multiplexer circuits for register column selection coincide with the number of registers of one register line.

[**0095**] When a normal register line is selected in one register group, an output of the priority encoder circuit **81** is input to input signal selection terminals (S) of a multiplexer circuit **83** for register column selection through invertor circuits. Therefore, registers included in the selected register line are selected in a column direction, so that sample timing signals can be output to source lines of an active matrix type display device.

[**0096**] **FIG. 13** shows a case wherein two register lines **140***a* and **140***b* are used in one register group and a shift register circuit has only one resister group. As shown in **FIG. 13**, a multiplexer circuit for register line selection can be omitted in comparison with **FIG. 4**.

[**0097**] As described above, a normal register line is selected in each register group, and a shift register circuit is constructed by connecting with each register group each other.

[**0098**] In the above embodiment, although a complementary type is used, a circuit using an N-channel type or a P-channel type may be constructed. In this state, since only one impurity doping process is performed, the number of forming processes can be decreased. **FIGS. 9A** to **9**C show shift register circuit constructed by only P-channel type. **FIG. 9A** shows an invertor circuit constructed using P-channel transistors and resistors. **FIG. 9B** shows an invertor circuit constructed using P-channel transistors. **FIG. 9C** shows a dynamic type shift register. A multiplexer circuit, a priority encoder circuit and like can be constructed using P-channel transistors and resistors.

[**0099**] In the embodiment, although only P-channel type transistor is used, a N-channel type transistor can be used.

[0100] According to the present invention, a defective rate of one register is constant and redundancy shift register circuit is used, so that a yield of a whole shift register circuit can be increased and reliability of a shift register circuit can be improved.

What is claimed is:

1. An active matrix display device comprising:

a substrate having an insulating surface;

a pixel portion comprising a pixel comprising:

a switching TFT over the substrate; and

a display element over the substrate, electrically connected to the switching TFT; and

a driver circuit comprising a shift register comprising an inverter circuit comprising:

an input terminal;

a first TFT over the substrate;

a second TFT over the substrate;

a third TFT over the substrate;

a fourth TFT over the substrate; and

an output terminal,

wherein a first terminal of the first TFT is electrically connected to the input terminal,

wherein a second terminal of the first TFT is electrically connected to a first terminal of the second TFT, and to a gate terminal of the third TFT,

wherein a first terminal of the third TFT is electrically connected to a first power source,

wherein a second terminal of the third TFT is electrically connected to a second power source, via a first resistance element,

wherein a first terminal of the fourth TFT is electrically connected to the first power source,

wherein a second terminal of the fourth TFT is electrically connected to the second power source, via a second resistance element,

wherein a second terminal of the second TFT is electrically connected to the second terminal of the fourth TFT,

wherein the output terminal is electrically connected to the second terminal of the third TFT, and to a gate terminal of the fourth TFT,

wherein a clock signal is inputted to a gate terminal of the first TFT,

wherein an inverted clock signal is inputted to a gate terminal of the second TFT, and

wherein each of the switching TFT, the first TFT, the second TFT, the third TFT and the fourth TFT comprises an active layer having a channel forming region comprising an impurity element having a same conductivity type.

2. An active matrix display device comprising:

a substrate having an insulating surface;

a pixel portion comprising a pixel comprising:

a switching TFT over the substrate; and

a display element over the substrate, electrically connected to the switching TFT; and

a driver circuit comprising a shift register comprising an inverter circuit comprising:

an input terminal;

a first TFT over the substrate;

a second TFT over the substrate;

a third TFT over the substrate;

a fourth TFT over the substrate;

a fifth TFT over the substrate;

a sixth TFT over the substrate; and

an output terminal,

wherein a first terminal of the first TFT is electrically connected to the input terminal,

wherein a second terminal of the first TFT is electrically connected to a first terminal of the second TFT, and to a gate terminal of the third TFT,

wherein a first terminal of the third TFT is electrically connected to a first power source,

wherein a second terminal of the third TFT is electrically connected to a second power source, and to a first terminal of the fifth TFT,

wherein a second terminal of the fifth TFT is electrically connected to a gate terminal of the fifth TFT, and to a second power source,

wherein a first terminal of the fourth TFT is electrically connected to the first power source,

wherein a second terminal of the fourth TFT is electrically connected to the second power source, and to a first terminal of the sixth TFT,

wherein a second terminal of the sixth TFT is electrically connected to a gate terminal of the sixth TFT, and to the second power source,

wherein a second terminal of the second TFT is electrically connected to the second terminal of the fourth TFT,

wherein the output terminal is electrically connected to the second terminal of the third TFT, and to a gate terminal of the fourth TFT,

wherein a clock signal is inputted to a gate terminal of the first TFT,

wherein an inverted clock signal is inputted to a gate terminal of the second TFT, and

wherein each of the switching TFT, the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT and the sixth TFT comprises an active layer having a

channel forming region comprising an impurity element having a same conductivity type.

3. An active matrix display device comprising:

a substrate having an insulating surface;

a pixel portion comprising a pixel comprising:

a switching TFT over the substrate; and

a display element over the substrate, electrically connected to the switching TFT; and

a driver circuit comprising a shift register comprising an inverter circuit comprising:

an input terminal;

a first TFT over the substrate;

a second TFT over the substrate;

a third TFT over the substrate;

a fourth TFT over the substrate;

a fifth TFT over the substrate;

a sixth TFT over the substrate; and

an output terminal,

wherein a first terminal of the first TFT is electrically connected to the input terminal,

wherein a gate terminal of the second TFT is electrically connected to a second terminal of the first TFT,

wherein a first terminal of the second TFT is electrically connected to a first power source,

wherein a first terminal of the fourth TFT is electrically connected to a second terminal of the second TFT, to a first terminal of the third TFT, and to a second power source via a first capacitor,

wherein a first terminal of the fifth TFT is electrically connected to the first power source,

wherein a gate terminal of the fifth TFT is electrically connected to a second terminal of the fourth TFT, and the second power source via a second capacitor,

wherein a first terminal of the sixth TFT is electrically connected to a second terminal of the fifth TFT,

wherein the output terminal is electrically connected to the second terminal of the sixth TFT, and to a second terminal of the third TFT,

wherein a clock signal is inputted to a gate terminal of the first TFT, and to a gate terminal of the third TFT,

wherein an inverted clock signal is inputted to a gate terminal of the fourth TFT, and to a gate terminal of the sixth TFT, and

wherein each of the switching TFT, the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT and the sixth TFT comprises an active layer having a channel forming region comprising an impurity element having a same conductivity type.

4. An active matrix display device comprising:

a substrate having an insulating surface;

a pixel portion comprising a pixel comprising:

a switching TFT over the substrate; and

a display element over the substrate, electrically connected to the switching TFT; and

a driver circuit comprising a shift register comprising an inverter circuit comprising:

an input terminal;

a first TFT over the substrate;

a second TFT over the substrate;

a third TFT over the substrate;

a fourth TFT over the substrate; and

an output terminal,

wherein a first terminal of the first TFT is electrically connected to the input terminal,

wherein a second terminal of the first TFT is electrically connected to a first terminal of the second TFT, and to a gate terminal of the third TFT,

wherein a first terminal of the third TFT is electrically connected to a first power source,

wherein a second terminal of the third TFT is electrically connected to a second power source, via a first resistance element,

wherein a first terminal of the fourth TFT is electrically connected to the first power source,

wherein a second terminal of the fourth TFT is electrically connected to the second power source, via a second resistance element,

wherein a second terminal of the second TFT is electrically connected to the second terminal of the fourth TFT,

wherein the output terminal is electrically connected to the second terminal of the third TFT, and to a gate terminal of the fourth TFT,

wherein a clock signal is inputted to a gate terminal of the first TFT,

wherein an inverted clock signal is inputted to a gate terminal of the second TFT,

wherein each of the switching TFT, the first TFT, the second TFT, the third TFT and the fourth TFT comprises an active layer having a channel forming region comprising an impurity element having a same conductivity type, and

wherein the active layer comprises crystallized silicon.

5. An active matrix display device comprising:

a substrate having an insulating surface;

a pixel portion comprising a pixel comprising:

a switching TFT over the substrate; and

a display element over the substrate, electrically connected to the switching TFT; and

a driver circuit comprising a shift register comprising an inverter circuit comprising:

an input terminal;

a first TFT over the substrate;

a second TFT over the substrate;

a third TFT over the substrate;

a fourth TFT over the substrate;

a fifth TFT over the substrate;

a sixth TFT over the substrate; and

an output terminal,

wherein a first terminal of the first TFT is electrically connected to the input terminal,

wherein a second terminal of the first TFT is electrically connected to a first terminal of the second TFT, and to a gate terminal of the third TFT,

wherein a first terminal of the third TFT is electrically connected to a first power source,

wherein a second terminal of the third TFT is electrically connected to a second power source, and to a first terminal of the fifth TFT,

wherein a second terminal of the fifth TFT is electrically connected to a gate terminal of the fifth TFT, and to a second power source,

wherein a first terminal of the fourth TFT is electrically connected to the first power source,

wherein a second terminal of the fourth TFT is electrically connected to the second power source, and to a first terminal of the sixth TFT,

wherein a second terminal of the sixth TFT is electrically connected to a gate terminal of the sixth TFT, and to the second power source,

wherein a second terminal of the second TFT is electrically connected to the second terminal of the fourth TFT,

wherein the output terminal is electrically connected to the second terminal of the third TFT, and to a gate terminal of the fourth TFT,

wherein a clock signal is inputted to a gate terminal of the first TFT,

wherein an inverted clock signal is inputted to a gate terminal of the second TFT,

wherein each of the switching TFT, the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT and the sixth TFT comprises an active layer having a channel forming region comprising an impurity element having a same conductivity type, and

wherein the active layer comprises crystallized silicon.

6. An active matrix display device comprising:

a substrate having an insulating surface;

a pixel portion comprising a pixel comprising:

a switching TFT over the substrate; and

a display element over the substrate, electrically connected to the switching TFT; and

a driver circuit comprising a shift register comprising an inverter circuit comprising:

an input terminal;

a first TFT over the substrate;

a second TFT over the substrate;

a third TFT over the substrate;

a fourth TFT over the substrate;

a fifth TFT over the substrate;

a sixth TFT over the substrate; and

an output terminal,

wherein a first terminal of the first TFT is electrically connected to the input terminal,

wherein a gate terminal of the second TFT is electrically connected to a second terminal of the first TFT,

wherein a first terminal of the second TFT is electrically connected to a first power source,

wherein a first terminal of the fourth TFT is electrically connected to a second terminal of the second TFT, to a first terminal of the third TFT, and to a second power source via a first capacitor,

wherein a first terminal of the fifth TFT is electrically connected to the first power source,

wherein a gate terminal of the fifth TFT is electrically connected to a second terminal of the fourth TFT, and the second power source via a second capacitor,

wherein a first terminal of the sixth TFT is electrically connected to a second terminal of the fifth TFT,

wherein the output terminal is electrically connected to the second terminal of the sixth TFT, and to a second terminal of the third TFT,

wherein a clock signal is inputted to a gate terminal of the first TFT, and to a gate terminal of the third TFT,

wherein an inverted clock signal is inputted to a gate terminal of the fourth TFT, and to a gate terminal of the sixth TFT,

wherein each of the switching TFT, the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT and the sixth TFT comprises an active layer having a channel forming region comprising an impurity element having a same conductivity type, and

wherein the active layer comprises crystallized silicon.

7. The active matrix display device, according to claim 1, wherein at least one of the first TFT, the second TFT, the third TFT and the fourth TFT has at least one lightly doped region.

8. The active matrix display device, according to claim 2, wherein at least one of the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT and the sixth TFT has at least one lightly doped region.

9. The active matrix display device, according to claim 3, wherein at least one of the first TFT, the second TFT, the

third TFT, the fourth TFT, the fifth TFT and the sixth TFT has at least one lightly doped region.

10. The active matrix display device, according to claim 4, wherein at least one of the first TFT, the second TFT, the third TFT and the fourth TFT has at least one lightly doped region.

11. The active matrix display device, according to claim 5, wherein at least one of the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT and the sixth TFT has at least one lightly doped region.

12. The active matrix display device, according to claim 6, wherein at least one of the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT and the sixth TFT has at least one lightly doped region.

13. The active matrix display device, according to claim 7,

wherein each of the first TFT, the second TFT, the third TFT and the fourth TFT has a gate electrode,

wherein the lightly doped region is formed by an ion doping method, using the gate electrode as a mask.

14. The active matrix display device, according to claim 8,

wherein each of the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT and the sixth TFT has a gate electrode,

wherein the lightly doped region is formed by an ion doping method, using the gate electrode as a mask.

15. The active matrix display device, according to claim 9,

wherein each of the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT and the sixth TFT has a gate electrode,

wherein the lightly doped region is formed by an ion doping method, using the gate electrode as a mask.

16. The active matrix display device, according to claim 10,

wherein each of the first TFT, the second TFT, the third TFT and the fourth TFT has a gate electrode,

wherein the lightly doped region is formed by an ion doping method, using the gate electrode as a mask.

17. The active matrix display device, according to claim 11,

wherein each of the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT and the sixth TFT has a gate electrode,

wherein the lightly doped region is formed by an ion doping method, using the gate electrode as a mask.

18. The active matrix display device, according to claim 12,

wherein each of the first TFT, the second TFT, the third TFT, the fourth TFT, the fifth TFT and the sixth TFT has a gate electrode,

wherein the lightly doped region is formed by an ion doping method, using the gate electrode as a mask.

19. The active matrix display device, according to claim 1, wherein the display element comprising an emissive material.

20. The active matrix display device, according to claim 2, wherein the display element comprising an emissive material.

21. The active matrix display device, according to claim 3, wherein the display element comprising an emissive material.

22. The active matrix display device, according to claim 4, wherein the display element comprising an emissive material.

23. The active matrix display device, according to claim 5, wherein the display element comprising an emissive material.

24. The active matrix display device, according to claim 6, wherein the display element comprising an emissive material.

25. The active matrix display device, according to claim 1, wherein the display element comprising a liquid crystal material.

26. The active matrix display device, according to claim 2, wherein the display element comprising a liquid crystal material.

27. The active matrix display device, according to claim 3, wherein the display element comprising a liquid crystal material.

28. The active matrix display device, according to claim 4, wherein the display element comprising a liquid crystal material.

29. The active matrix display device, according to claim 5, wherein the display element comprising a liquid crystal material.

30. The active matrix display device, according to claim 6, wherein the display element comprising a liquid crystal material.

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专利名称(译)	用于有源矩阵型液晶显示装置中的驱动电路的冗余移位寄存器电路		
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摘要(译)

根据本发明，提出了一种有源矩阵显示装置。该显示装置包括具有绝缘表面的基板，在基板上以矩阵形式布置的多个像素电极，以及可操作地连接到像素电极的多个开关元件。每个开关元件还包括薄膜晶体管。该显示装置还包括显示介质和驱动电路，该显示介质包括能够电改变设置在每个像素电极处的发光强度的发光材料，该驱动电路包括用于驱动多个开关元件的多个薄膜晶体管。多个薄膜晶体管中的每一个包括结晶半导体层，与结晶半导体层相邻的栅极绝缘膜和与栅极绝缘膜相邻的栅电极。