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(54) **LIQUID CRYSTAL DISPLAY BACKPLANE LAYOUTS AND ADDRESSING FOR NON-STANDARD SUBPIXEL ARRANGEMENTS**

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**Publication Classification**

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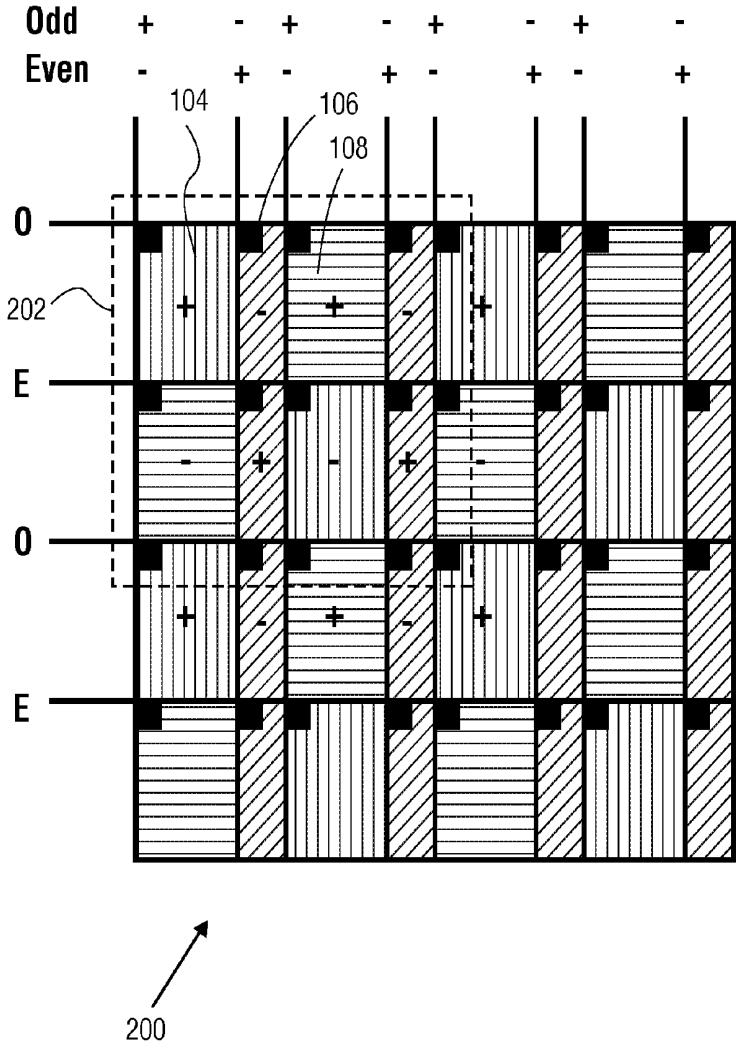
*G09G 3/36* (2006.01)

(52) **U.S. Cl.** ..... **345/88**

(57) **ABSTRACT**

Liquid crystal display backplane layouts and addressing for non-standard subpixel arrangements are disclosed. A liquid crystal display comprises a panel and a plurality of transistors. The panel substantially comprises a subpixel repeating group having an even number of subpixels in a first direction. Each thin film transistor connects one subpixel to a row and a column line at an intersection in one of a group of quadrants. The group comprises a first quadrant, a second quadrant, a third quadrant and a fourth quadrant, wherein the thin film transistors are formed in a backplane structure adjacent to intersections of the row and column lines. The thin film transistors are also substantially formed in more than one quadrant in the backplane structure.



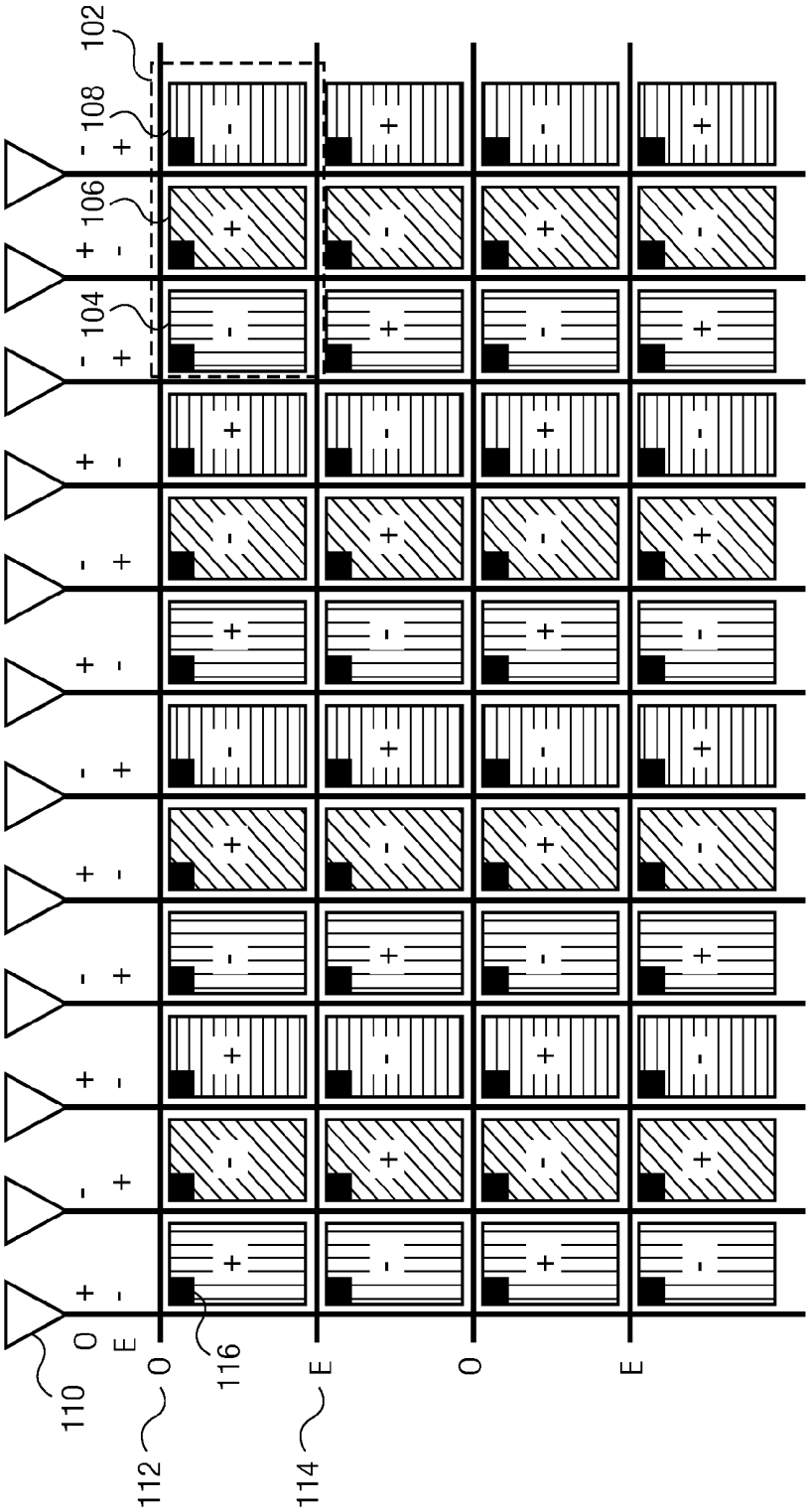



FIG. 1A
(PRIOR ART)

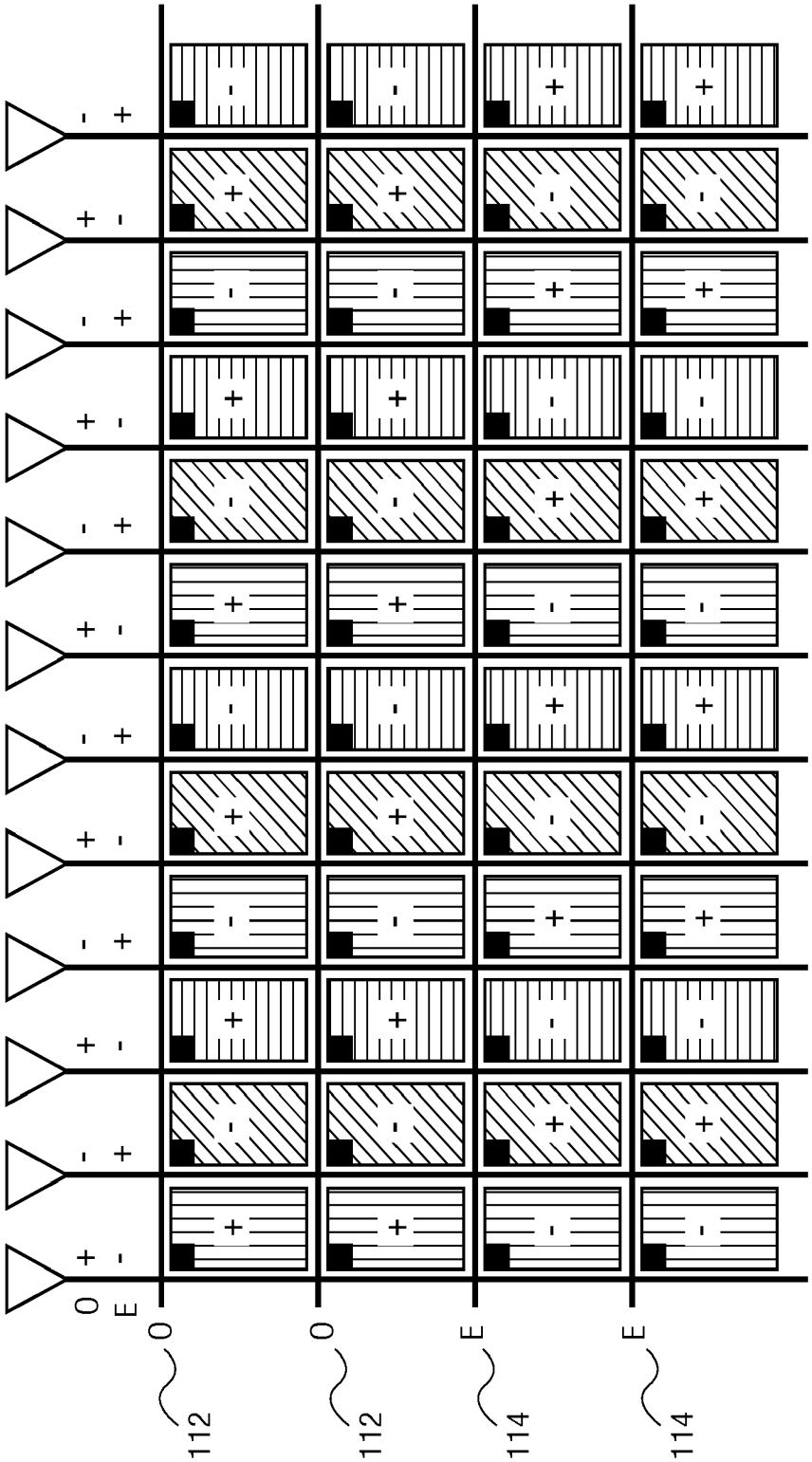



FIG. 1B
(PRIOR ART)

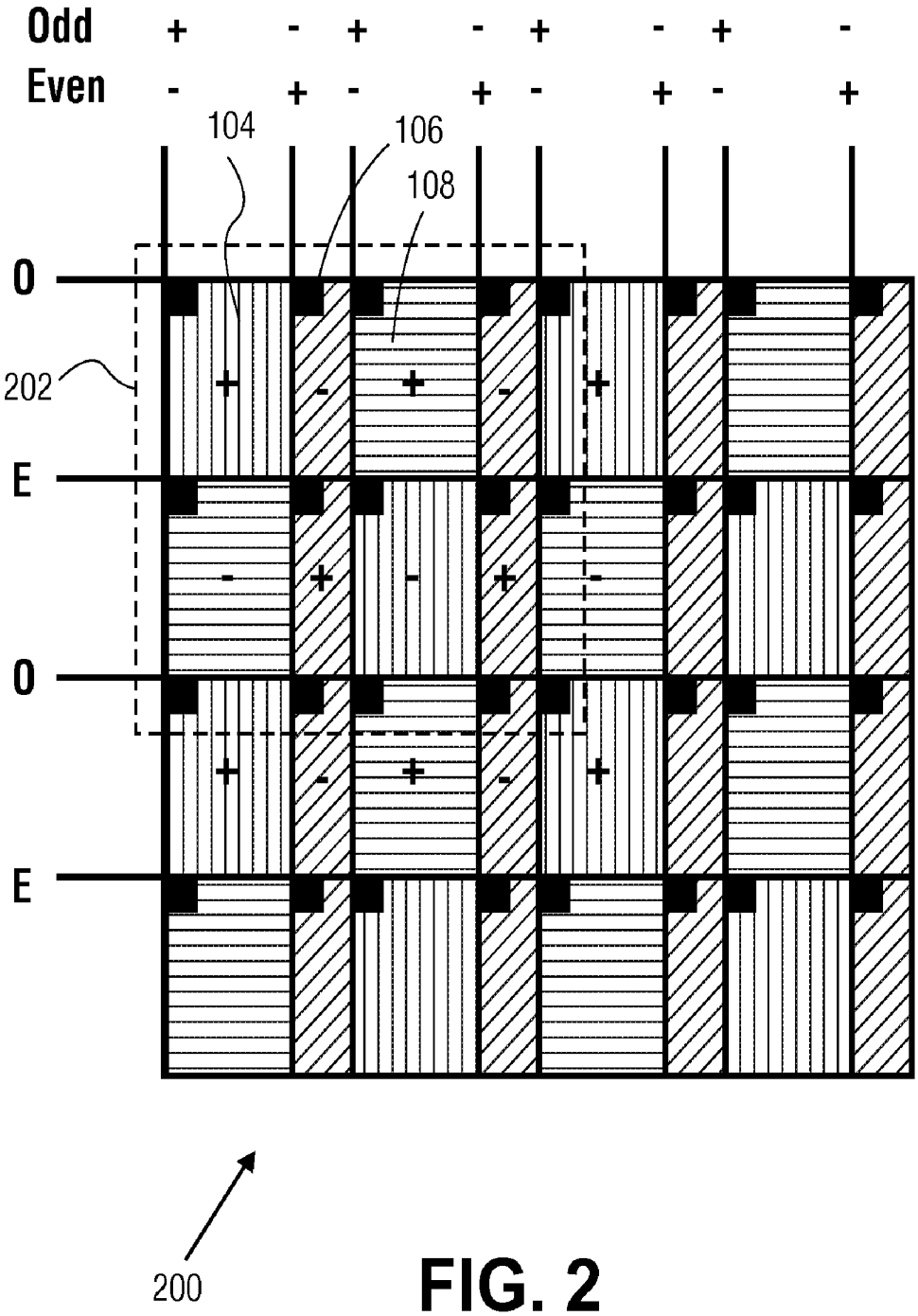



FIG. 2

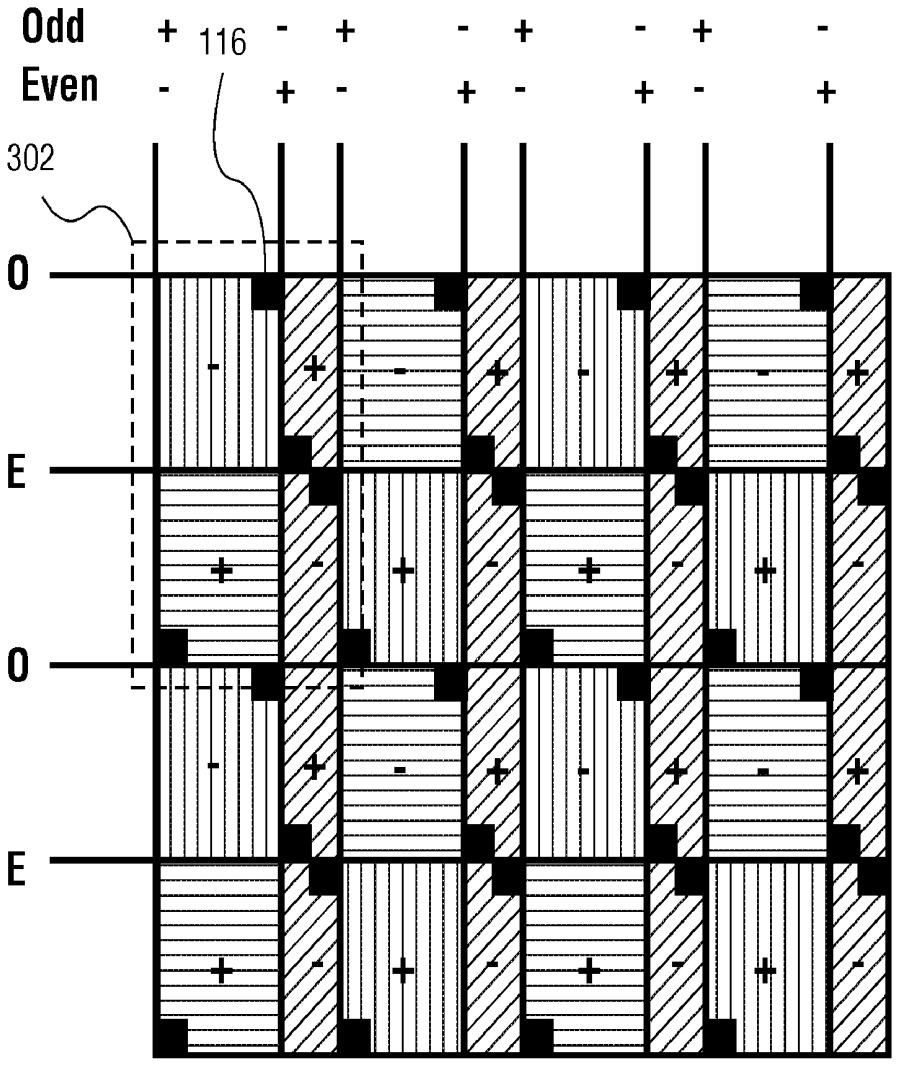



FIG. 3

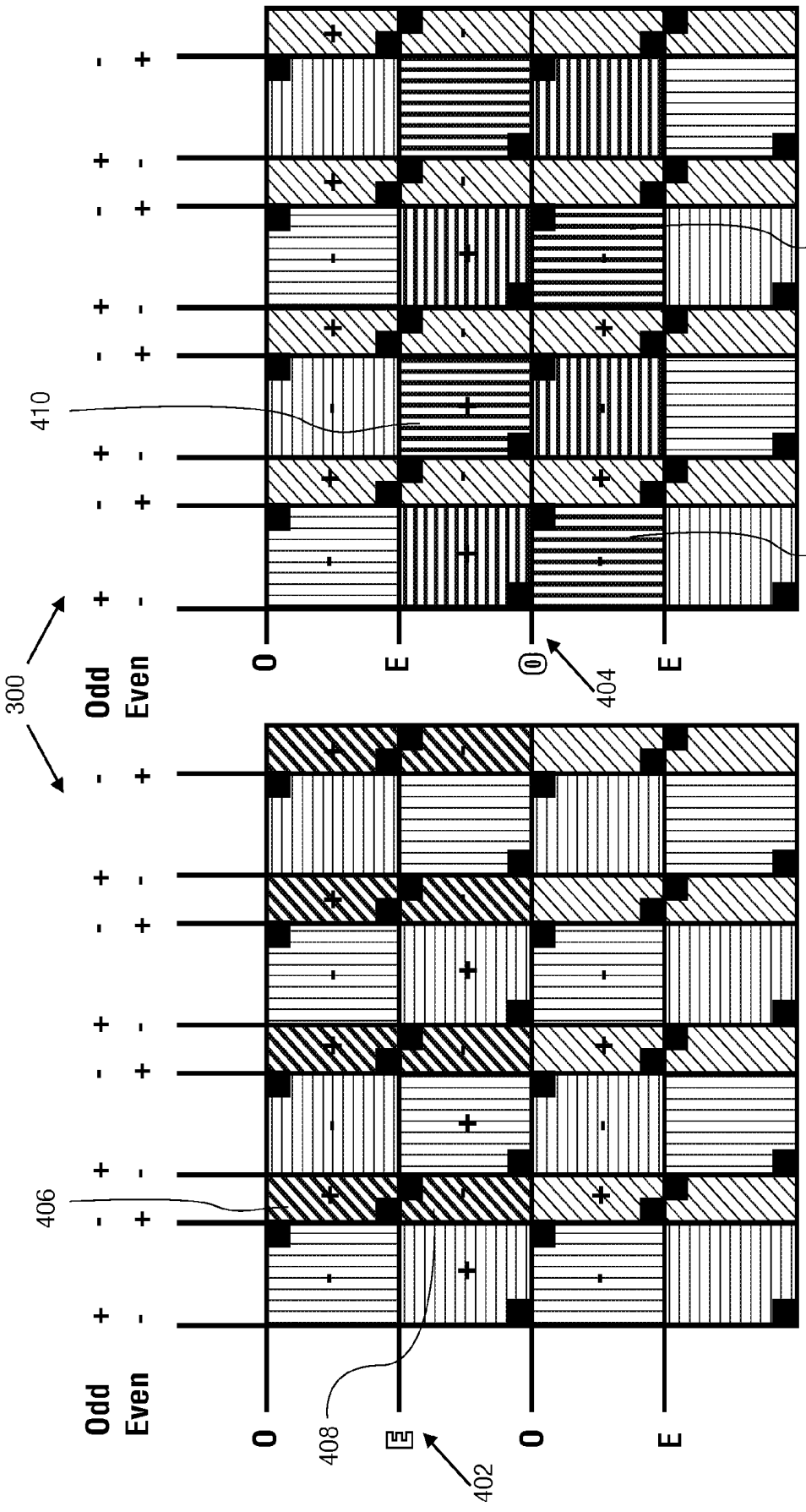



FIG. 4

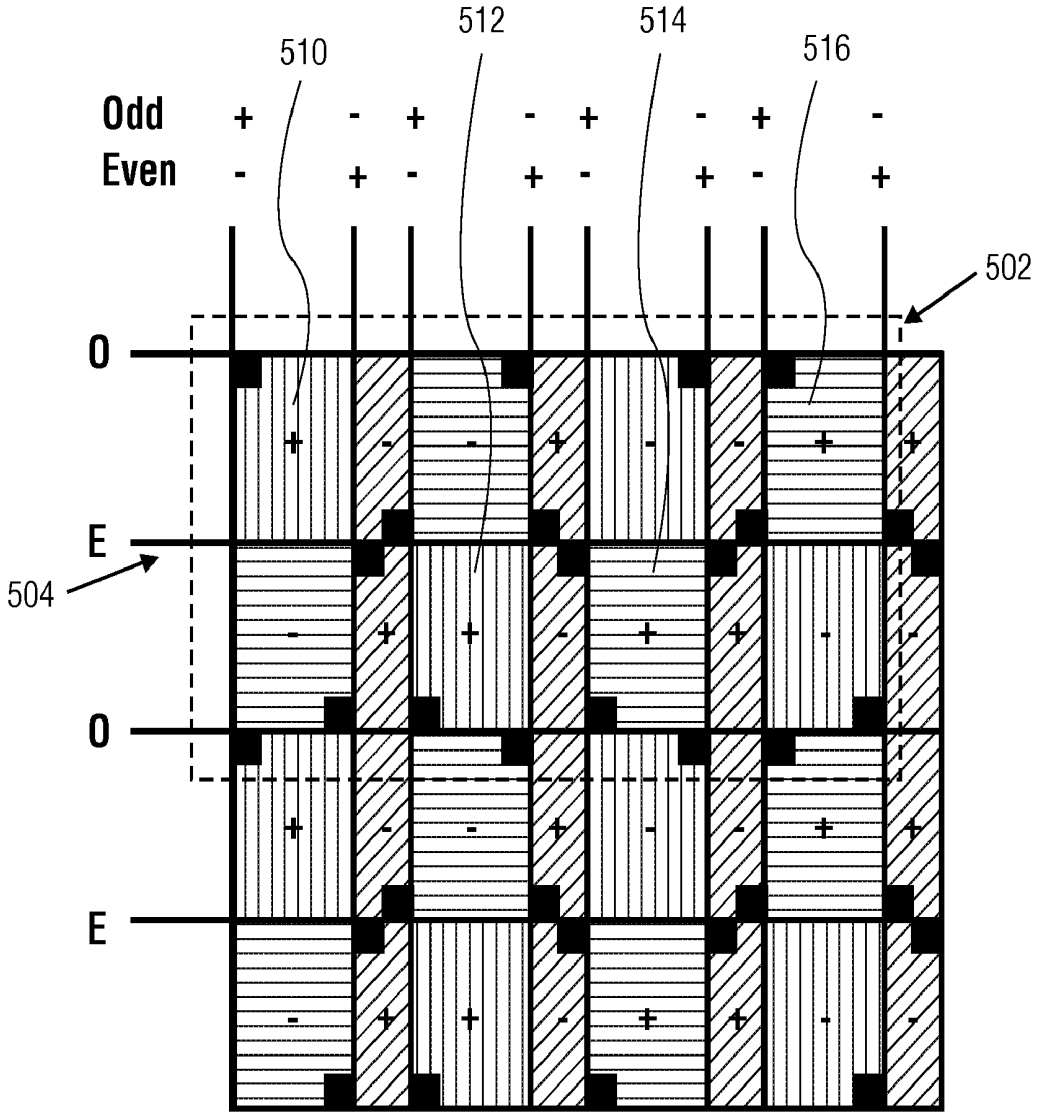



FIG. 5

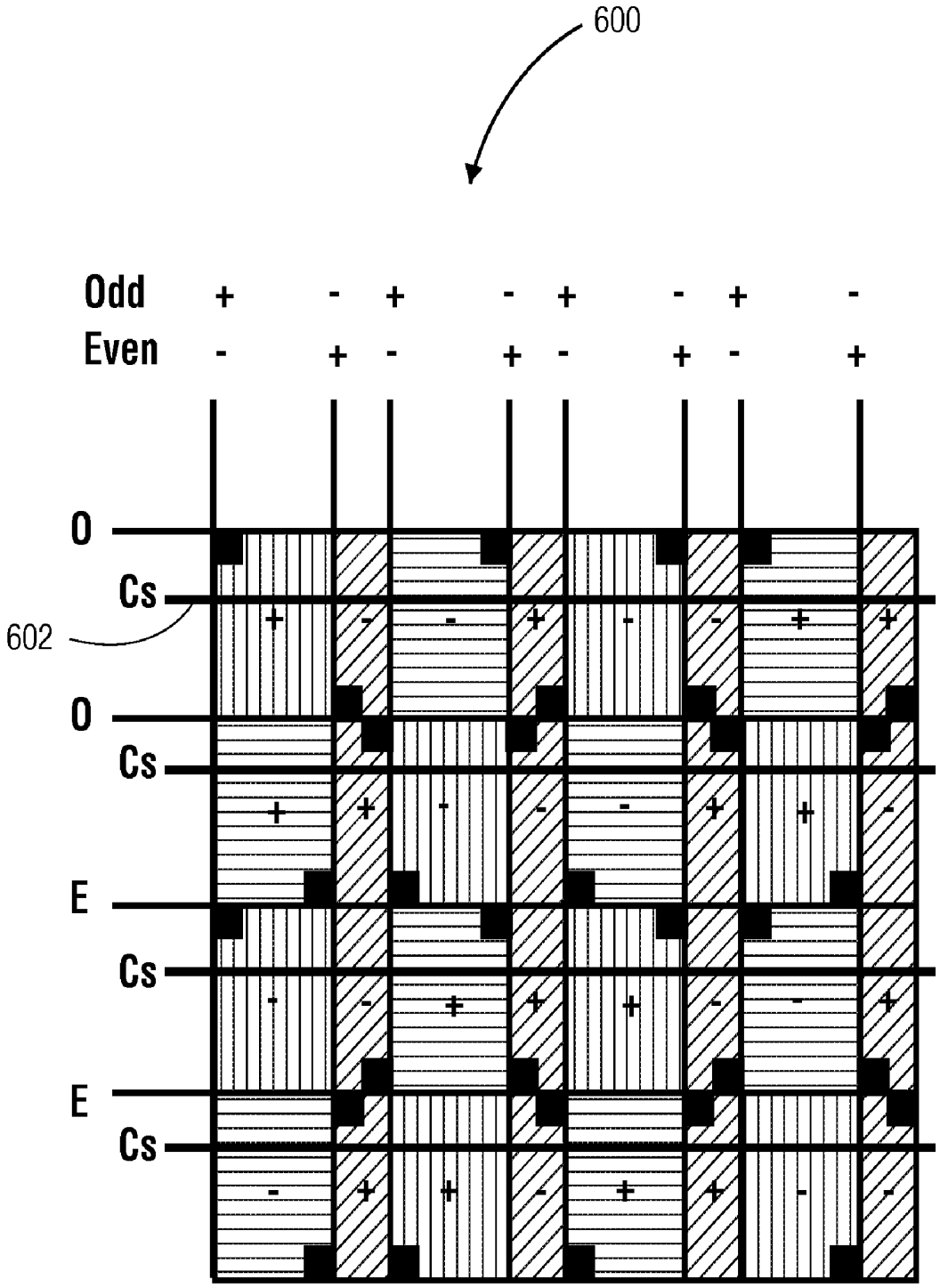



FIG. 6

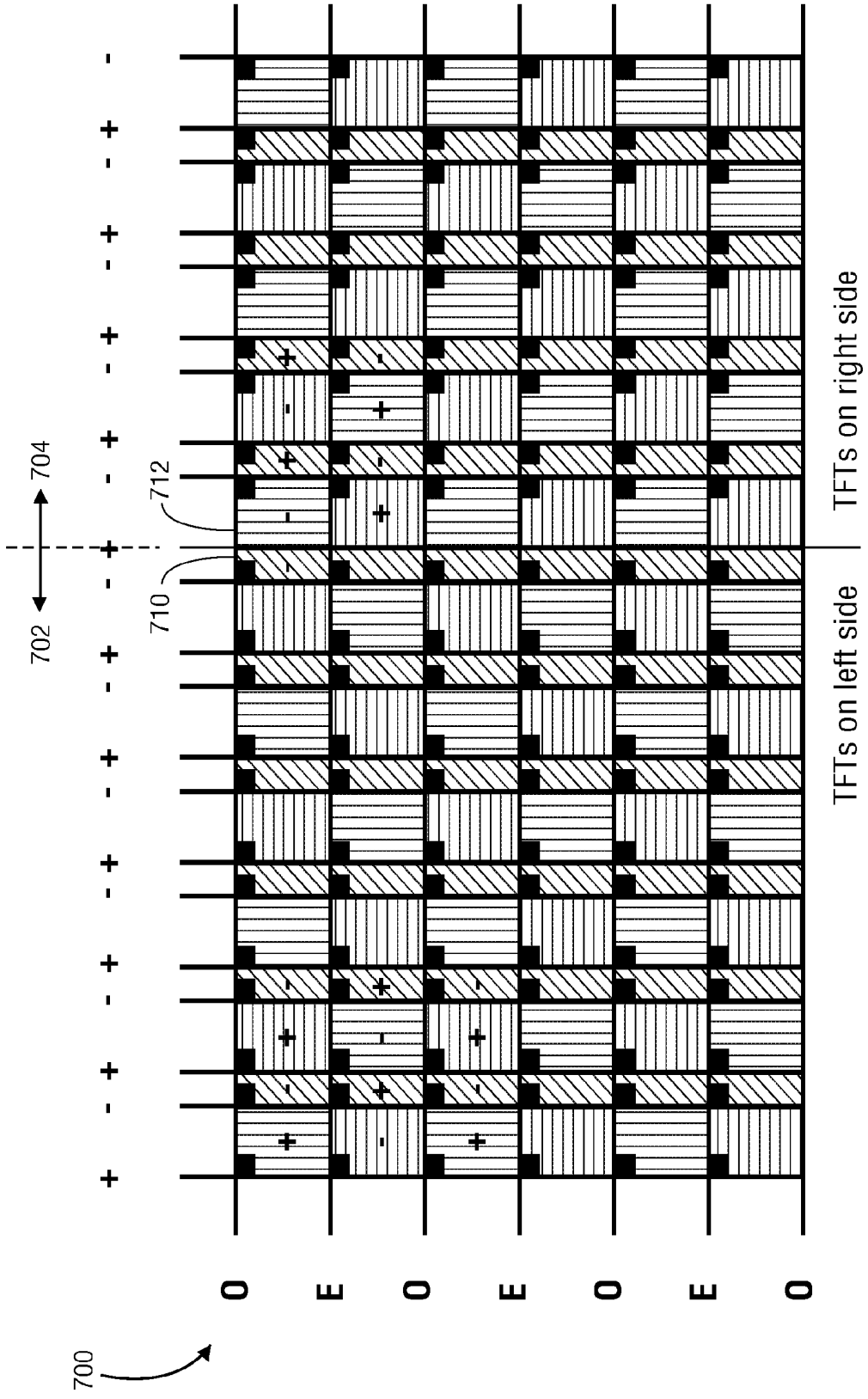

700
O E O E O E O
704
702
712
710
TFTs on left side
TFTs on right side

FIG. 7

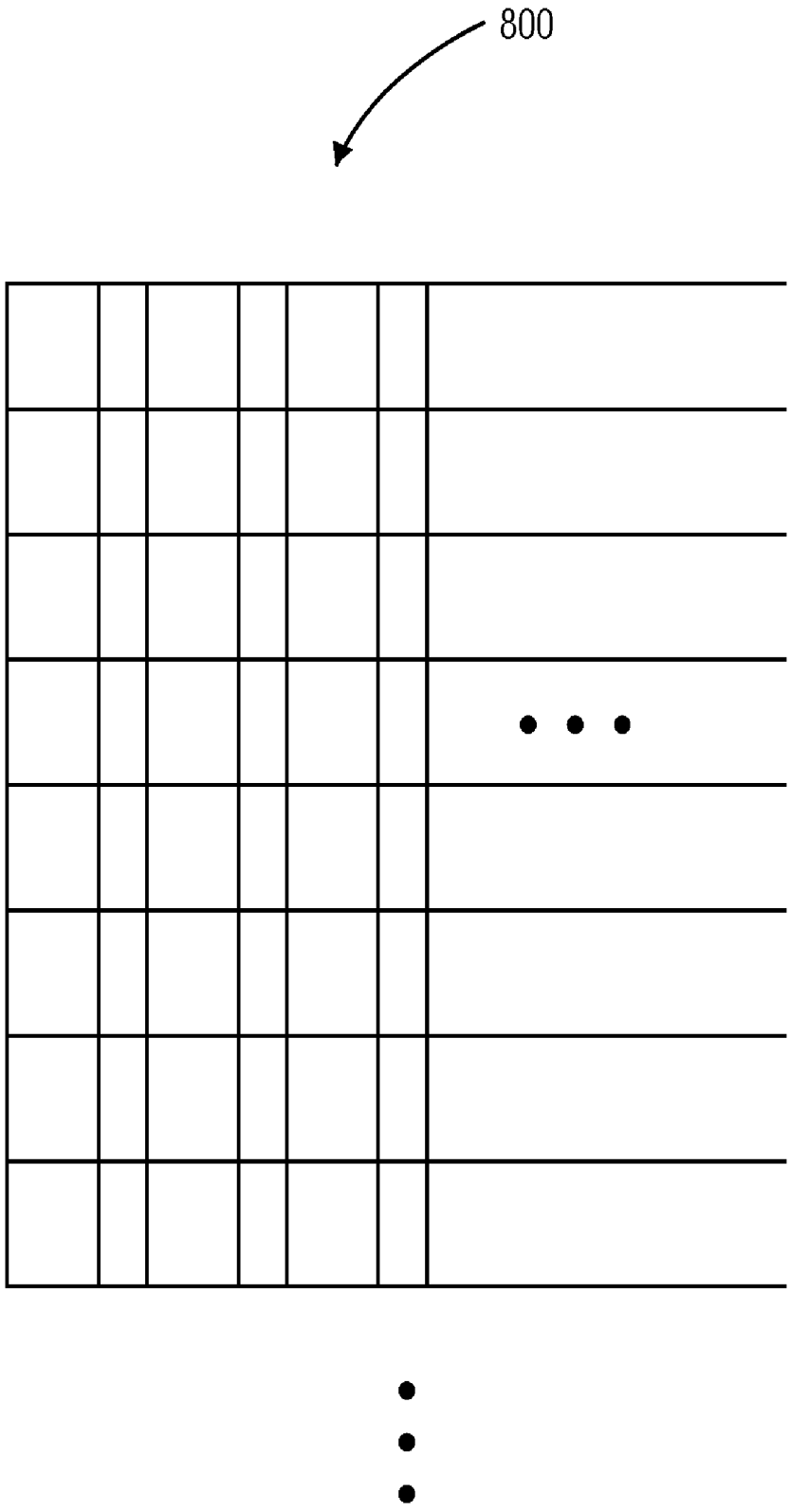



FIG. 8

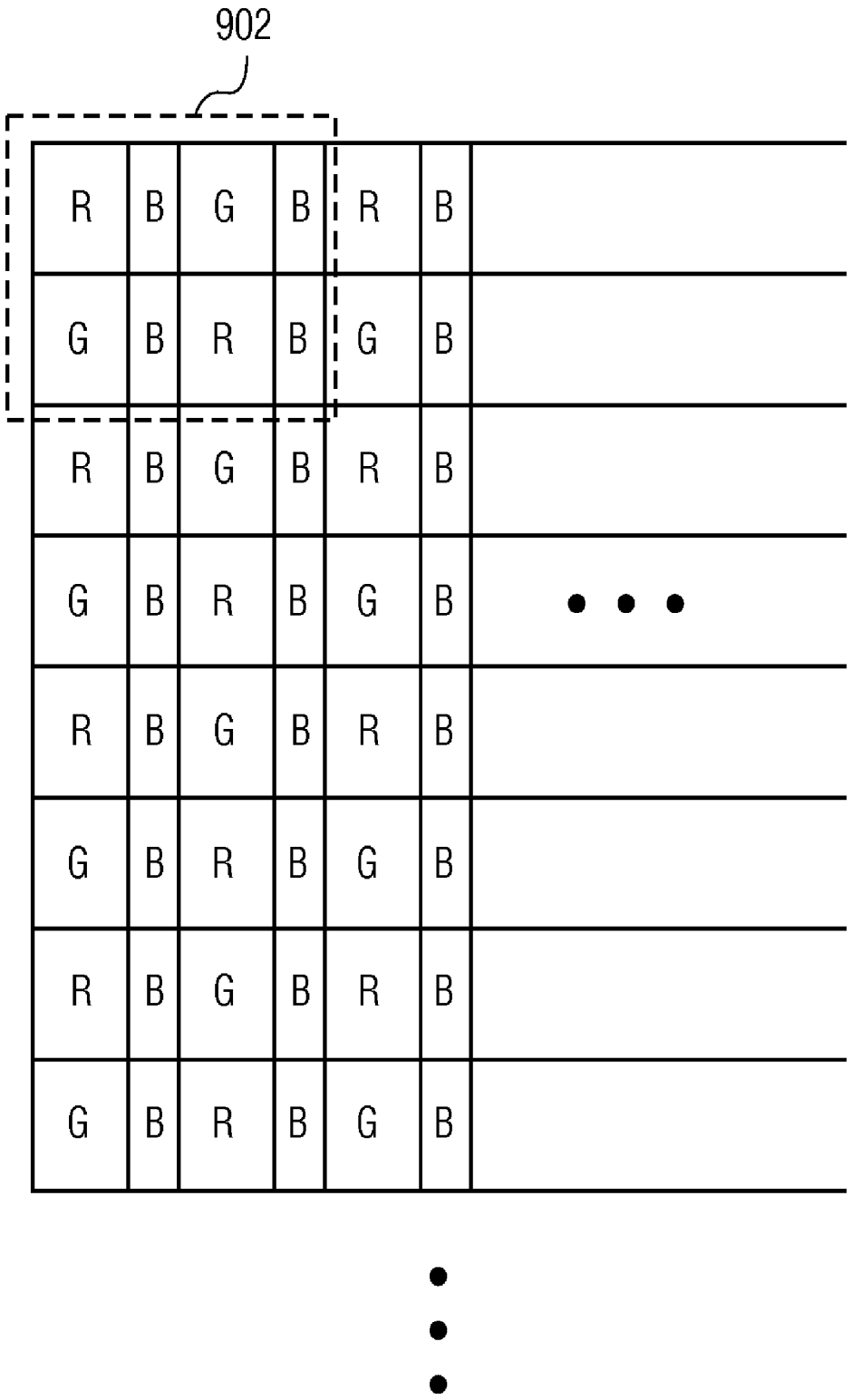

902
R B G B R B
G B R B G B
R B G B R B
G B R B G B
R B G B R B
G B R B G B
R B G B R B
G B R B G B

FIG. 9

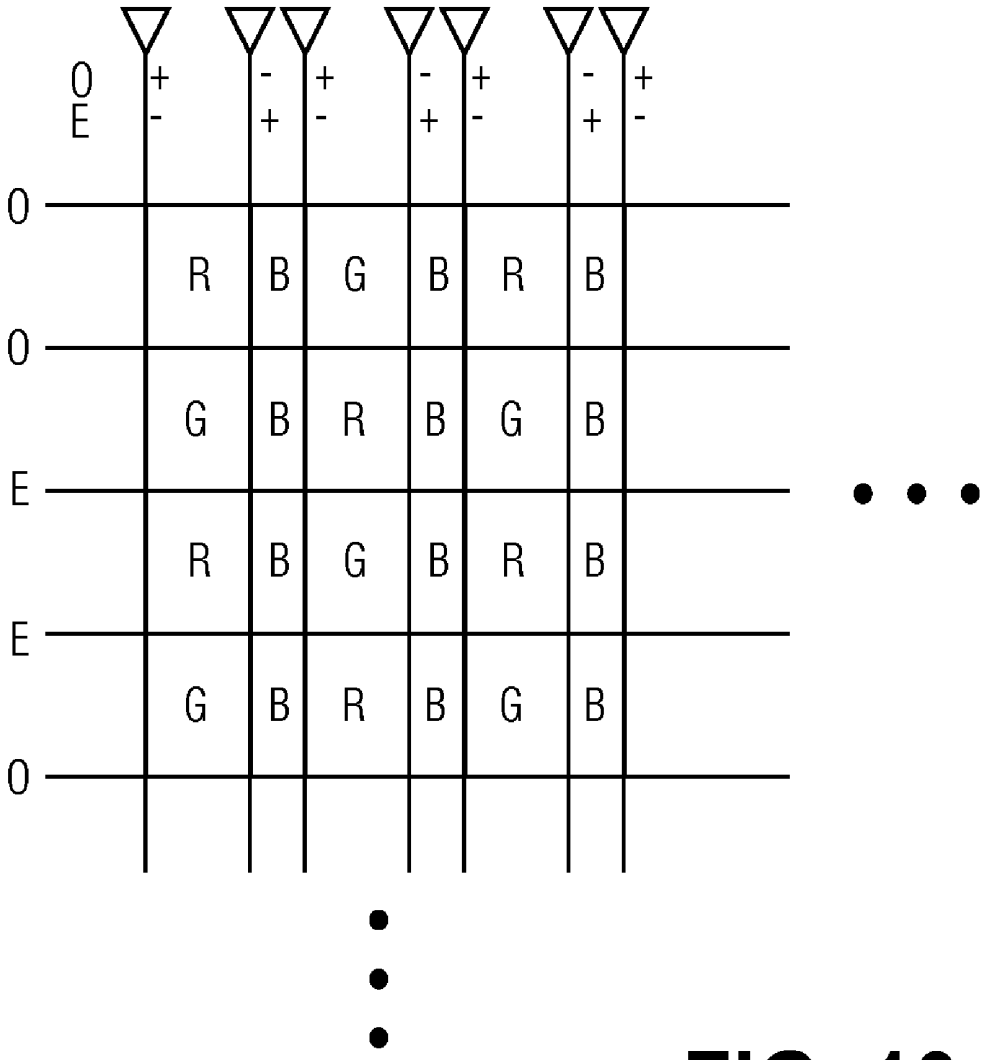



FIG. 10

| OPTION | R | G |
|---|---|---|
| 1 | + | + |
| 2 | + | - |
| 3 | - | + |
| 4 | - | - |

EXAMPLE - OPTION 1

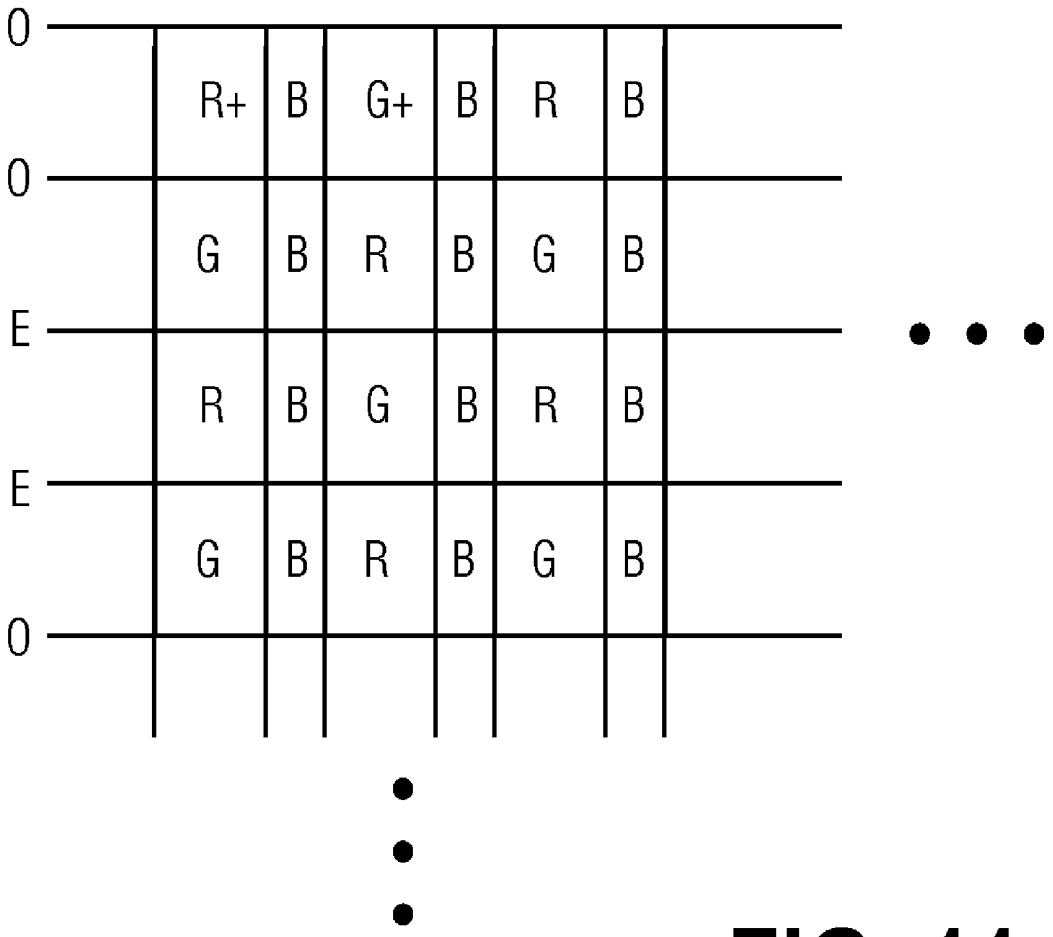



FIG. 11

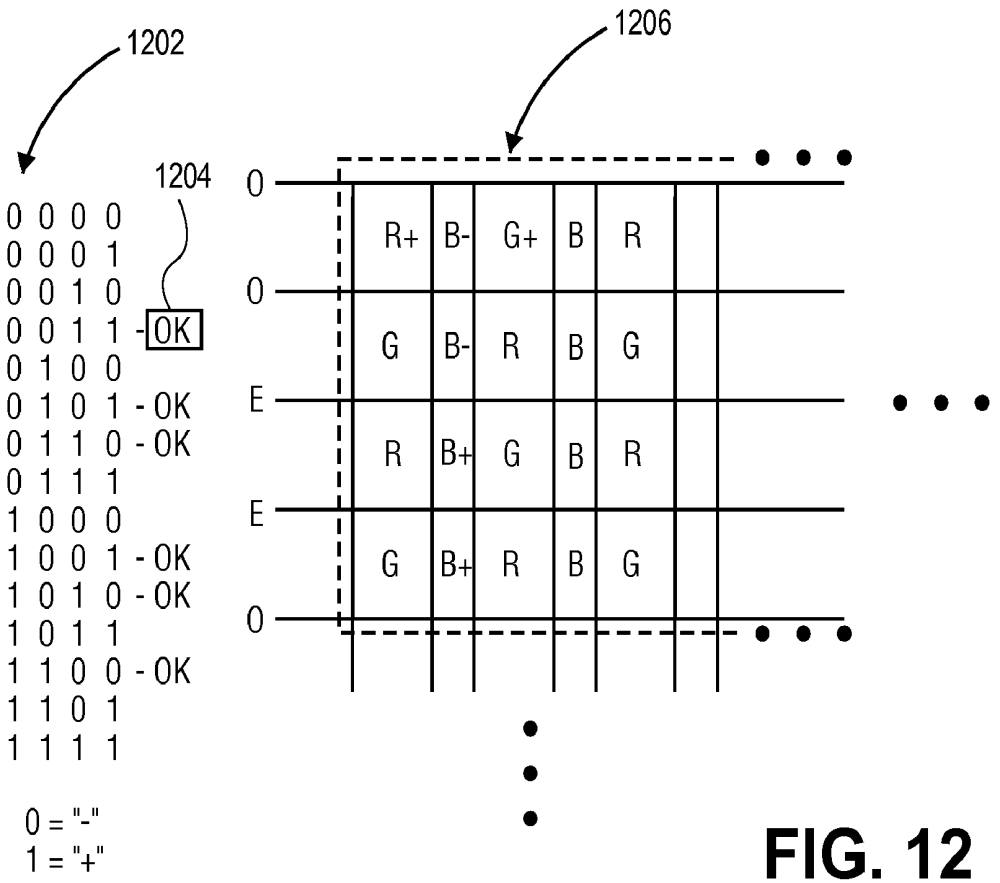

1202
1206
1204
0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1 - OK
0 1 0 0
0 1 0 1 - OK
0 1 1 0 - OK
0 1 1 1
1 0 0 0
1 0 0 1 - OK
1 0 1 0 - OK
1 0 1 1
1 1 0 0 - OK
1 1 0 1
1 1 1 1
0 = "-"
1 = "+"
0
0
E
E
0
R+ B- G+ B R
G B- R B G
R B+ G B R
G B+ R B G

FIG. 12

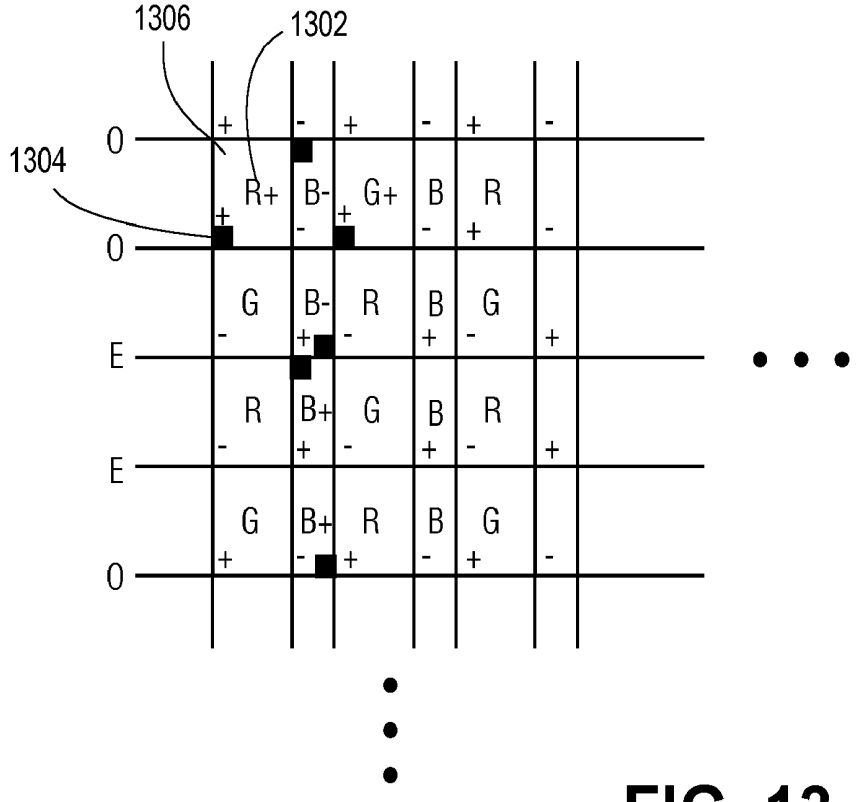

1306
1302
1304
0
0
E
E
0
R+ B- G+ B R
G B- R B G
R B+ G B R
G B+ R B G

FIG. 13

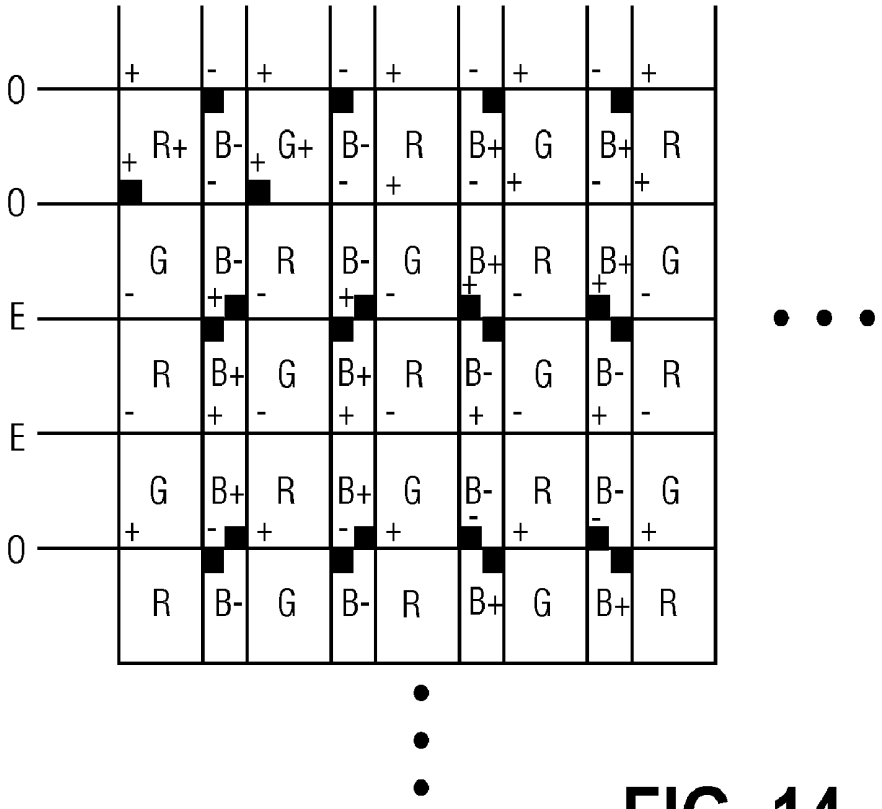

O
O
E
E
O
R+ B- G+ B- R B+ G B+ R
G B- R B- G B+ R B+ G
R B+ G B+ R B- G B- R
G B+ R B+ G B- R B- G
R B- G B- R B+ G B+ R

FIG. 14

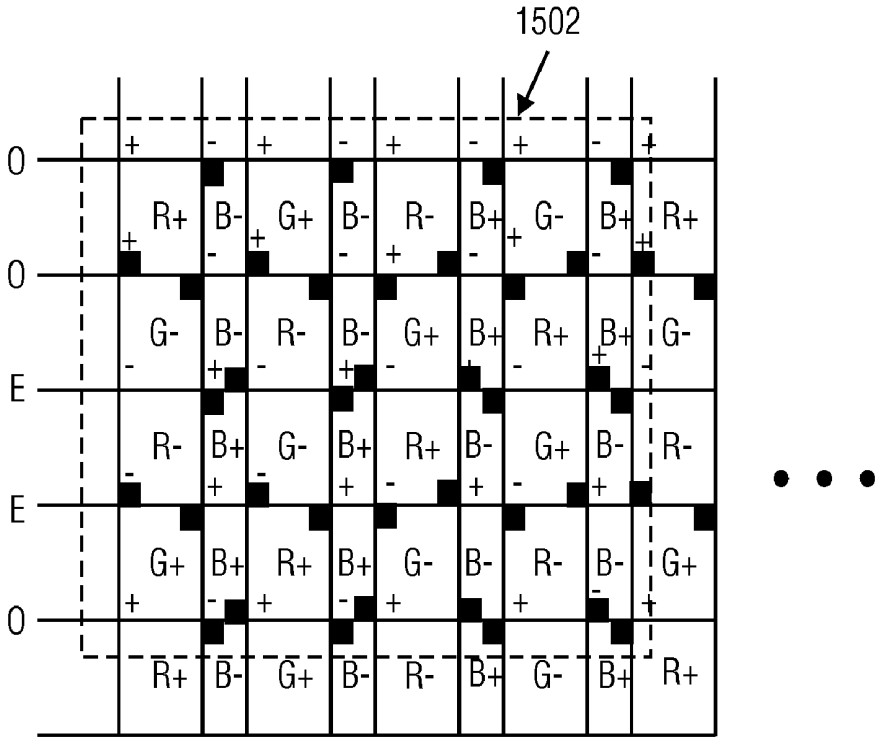

1502
O
O
E
E
O
R+ B- G+ B- R- B+ G- B+ R+
G- B- R- B- G+ B+ R+ B+ G-
R- B+ G- B+ R+ B- G+ B- R-
G+ B+ R+ B+ G- B- R- B- G+
R+ B- G+ B- R- B+ G- B+ R+

FIG. 15

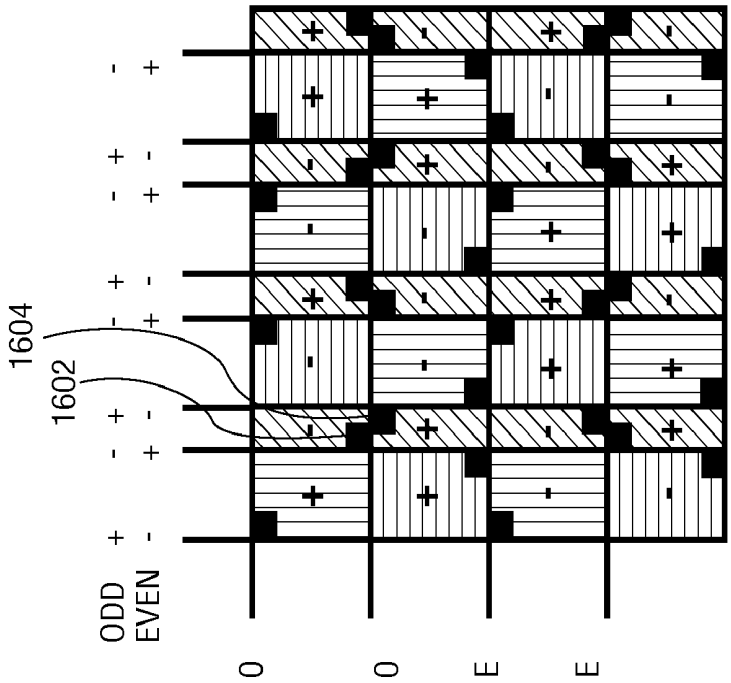



FIG. 16A

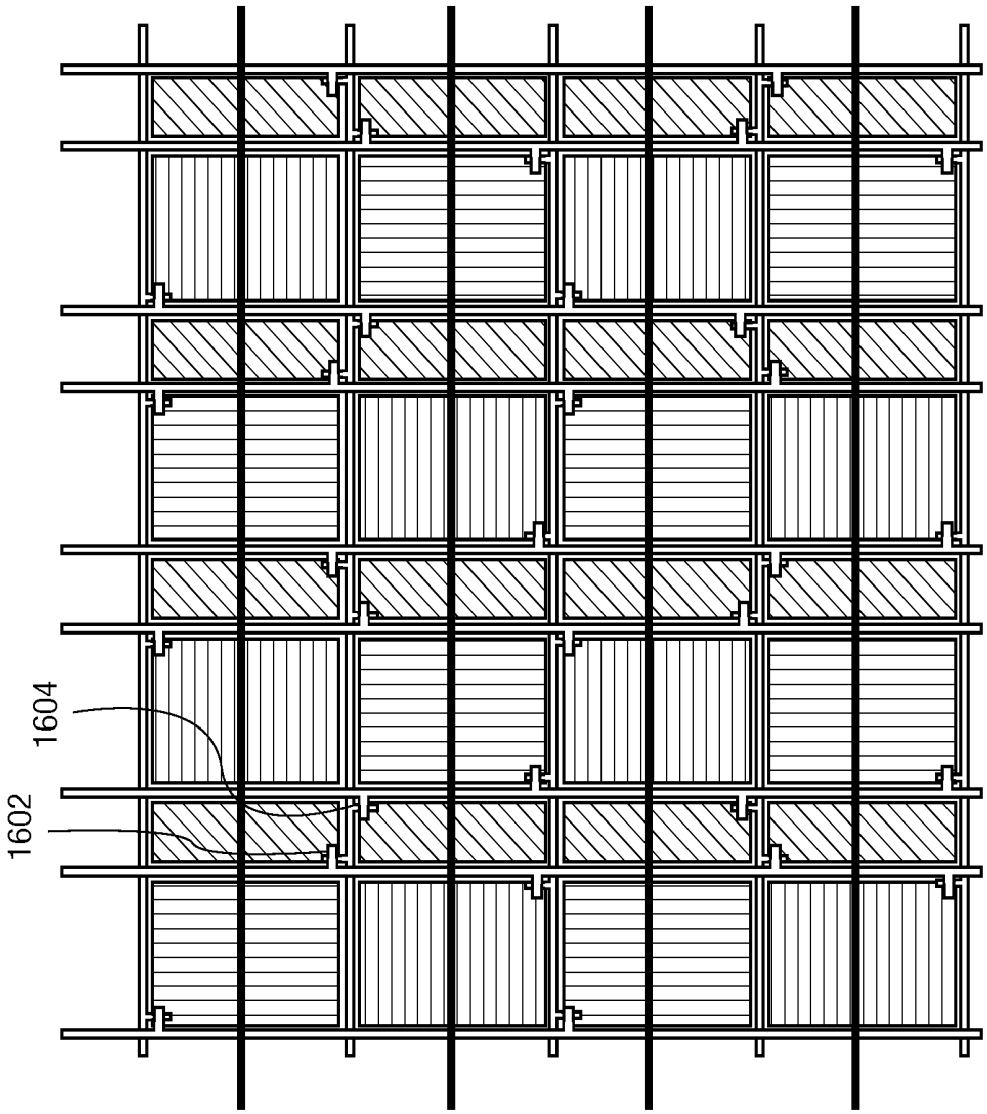



FIG. 16B

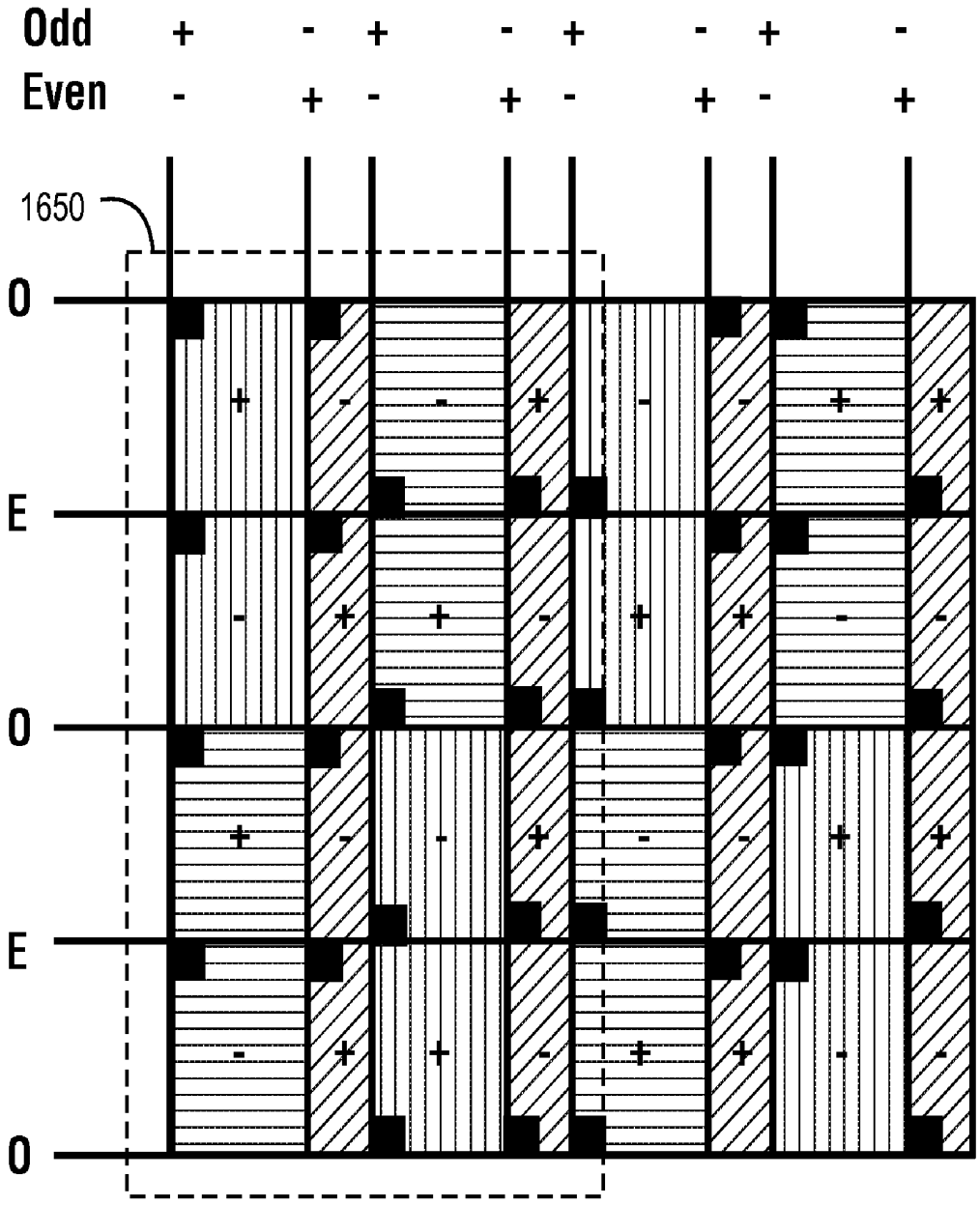



FIG. 16C

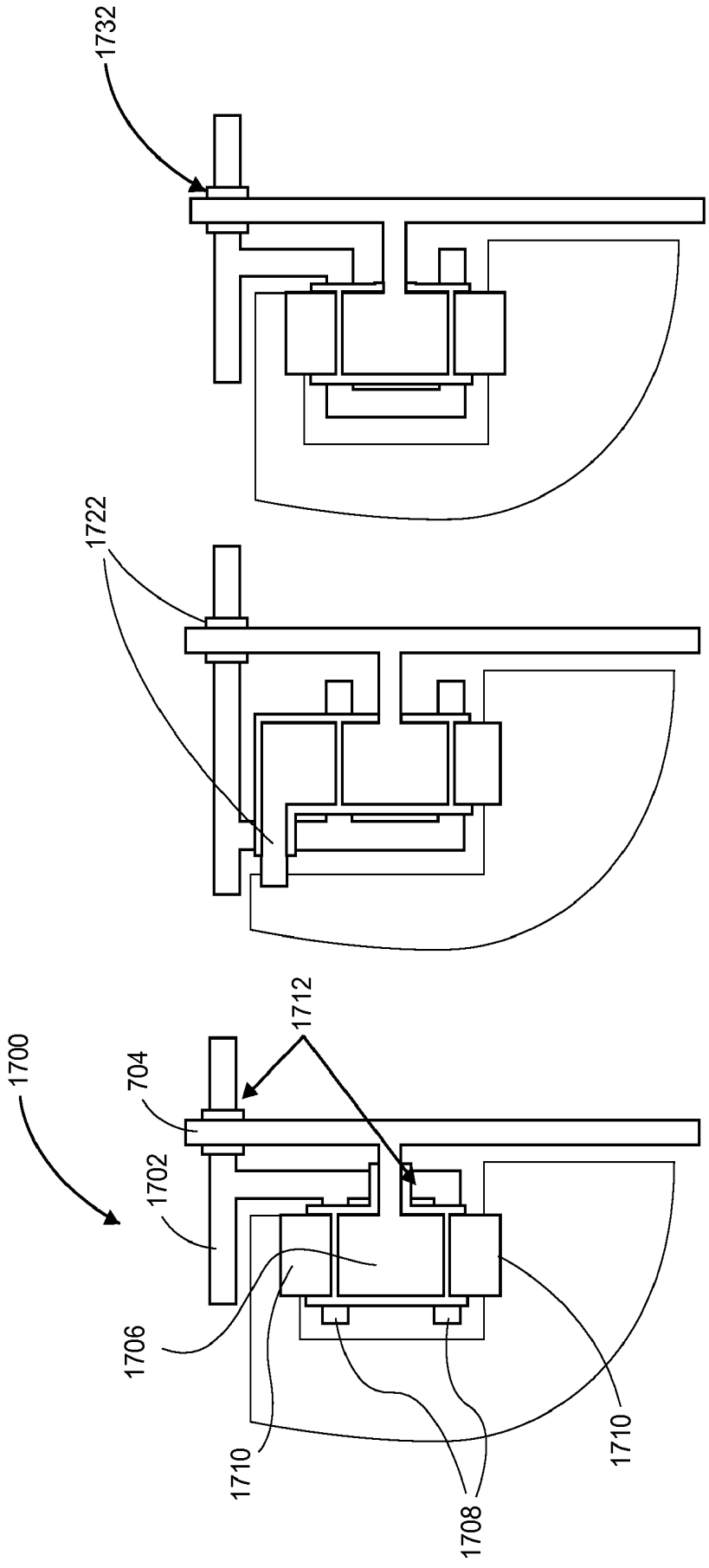



FIG. 17C

FIG. 17B

FIG. 17A
(PRIOR ART)

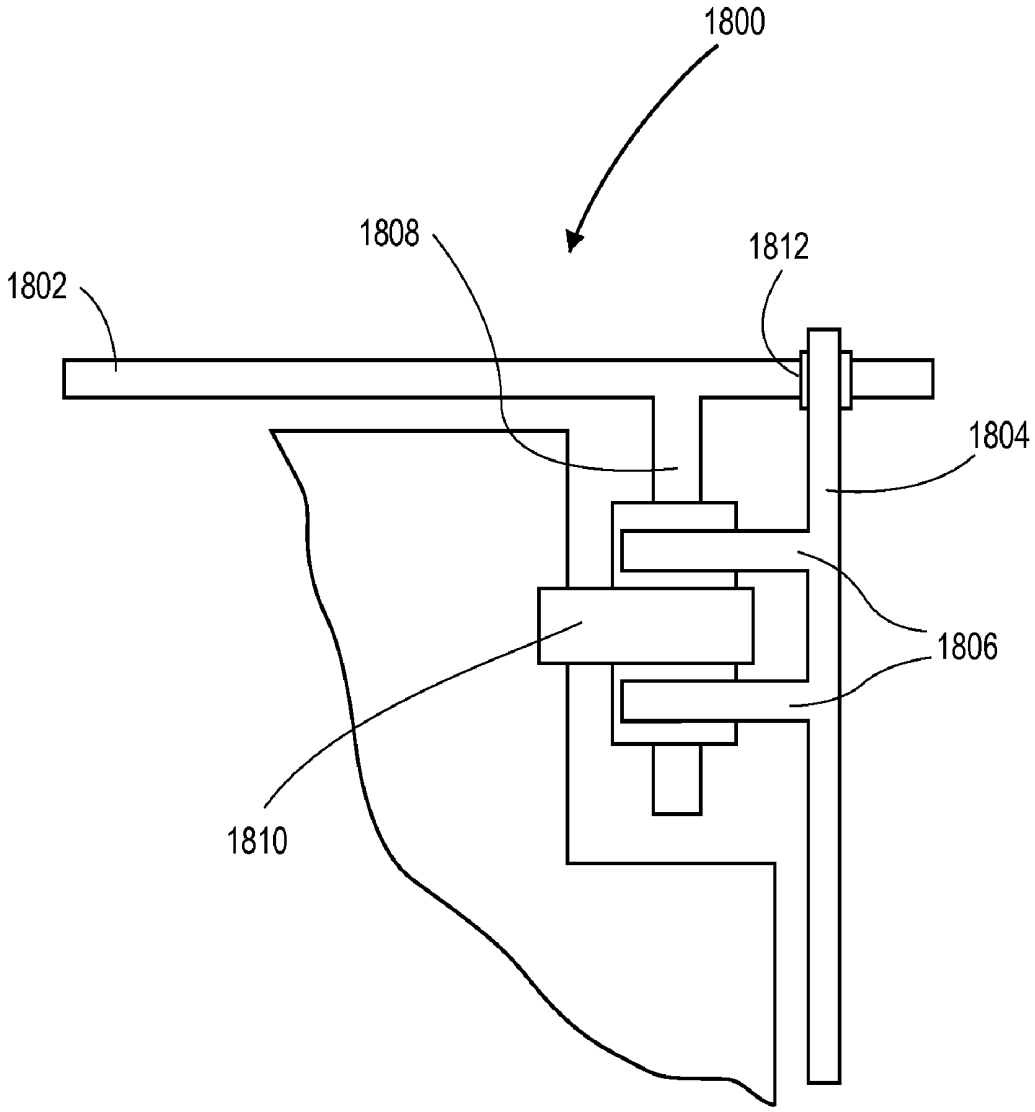



FIG. 18
(PRIOR ART)

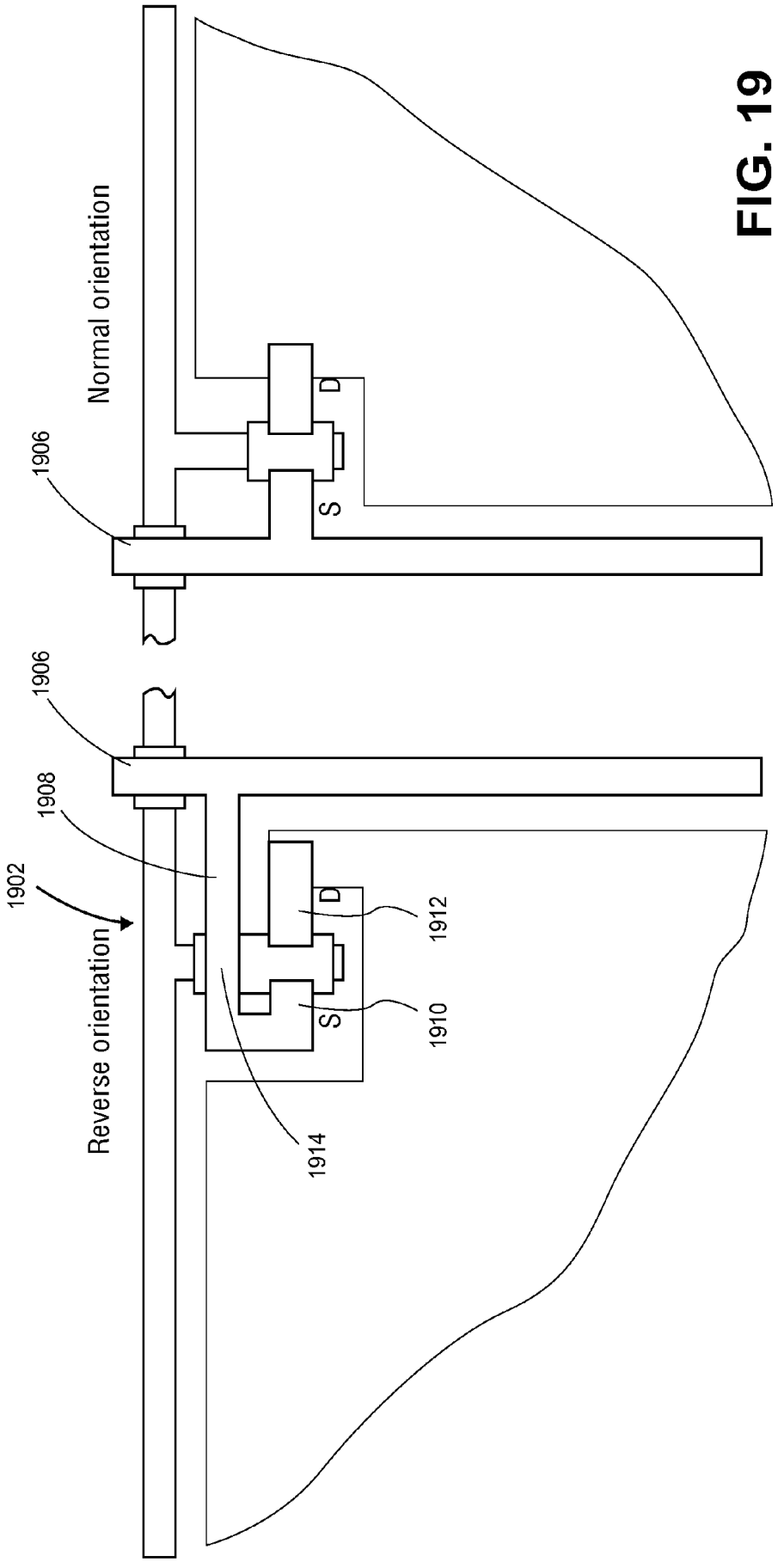

Normal orientation
1906
D
S
1906
1908
1902
Reverse orientation
D
1912
S
1910
1914

FIG. 19

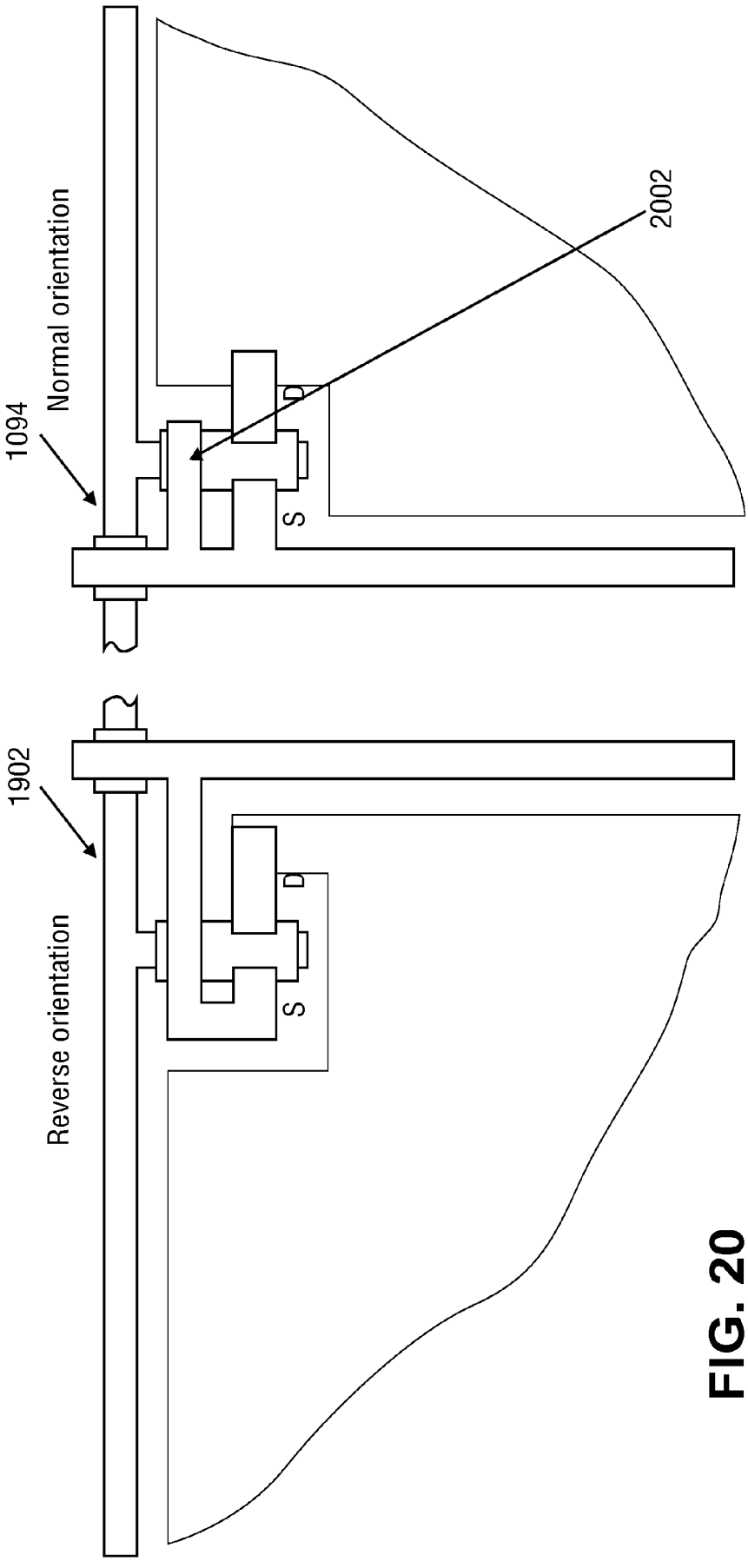

1094
Normal orientation
2002
D
S
1902
Reverse orientation
D
S

FIG. 20

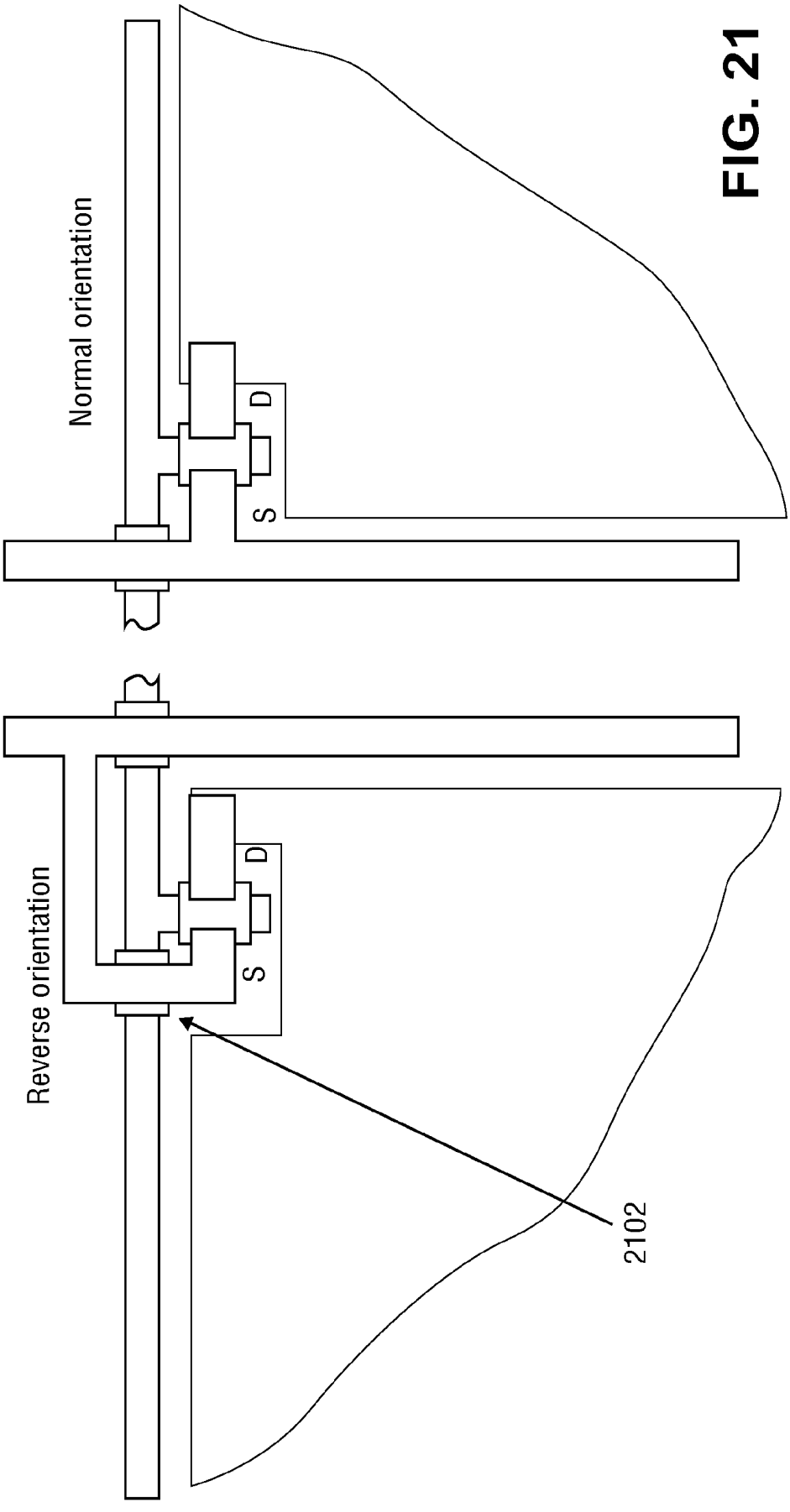



FIG. 21

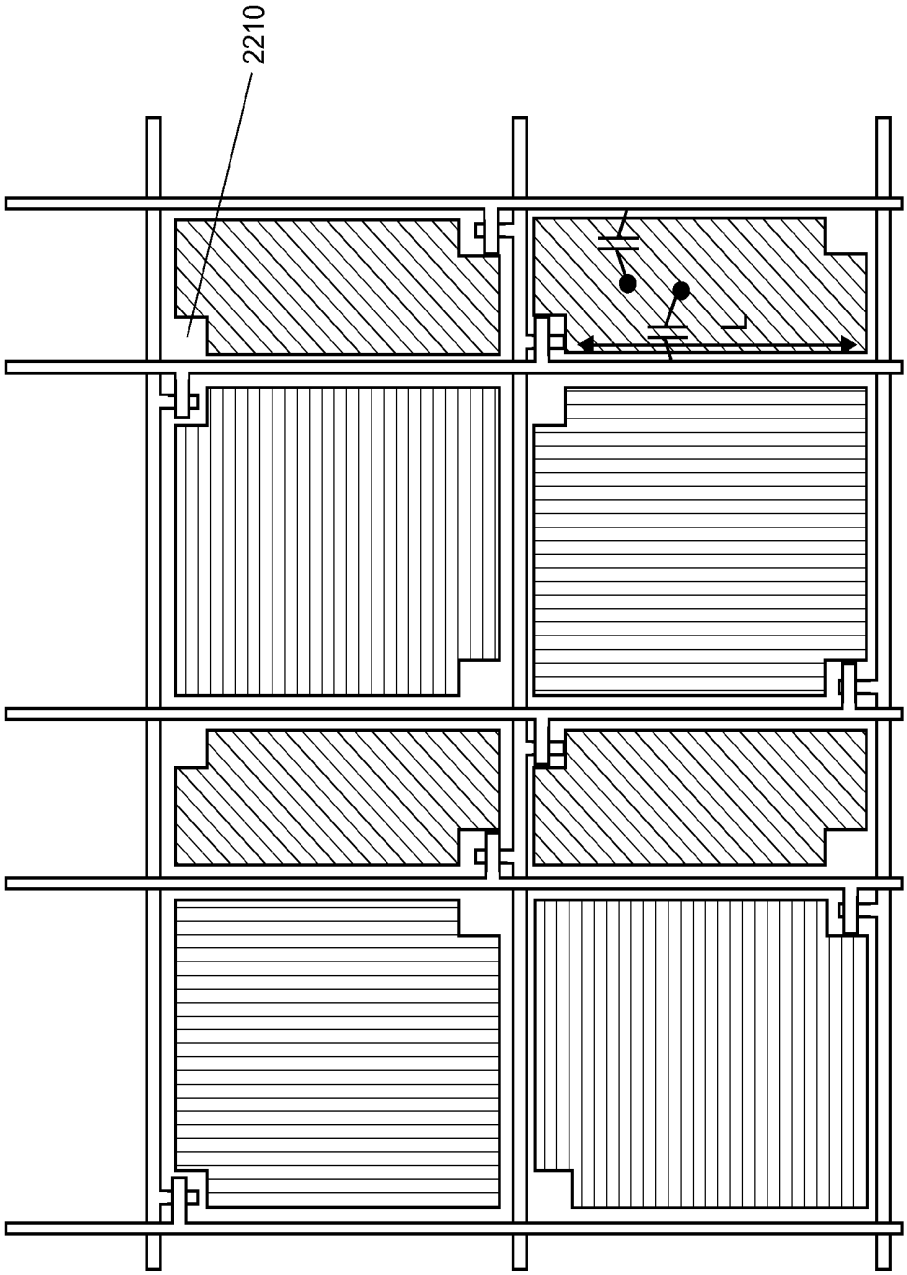



FIG. 22

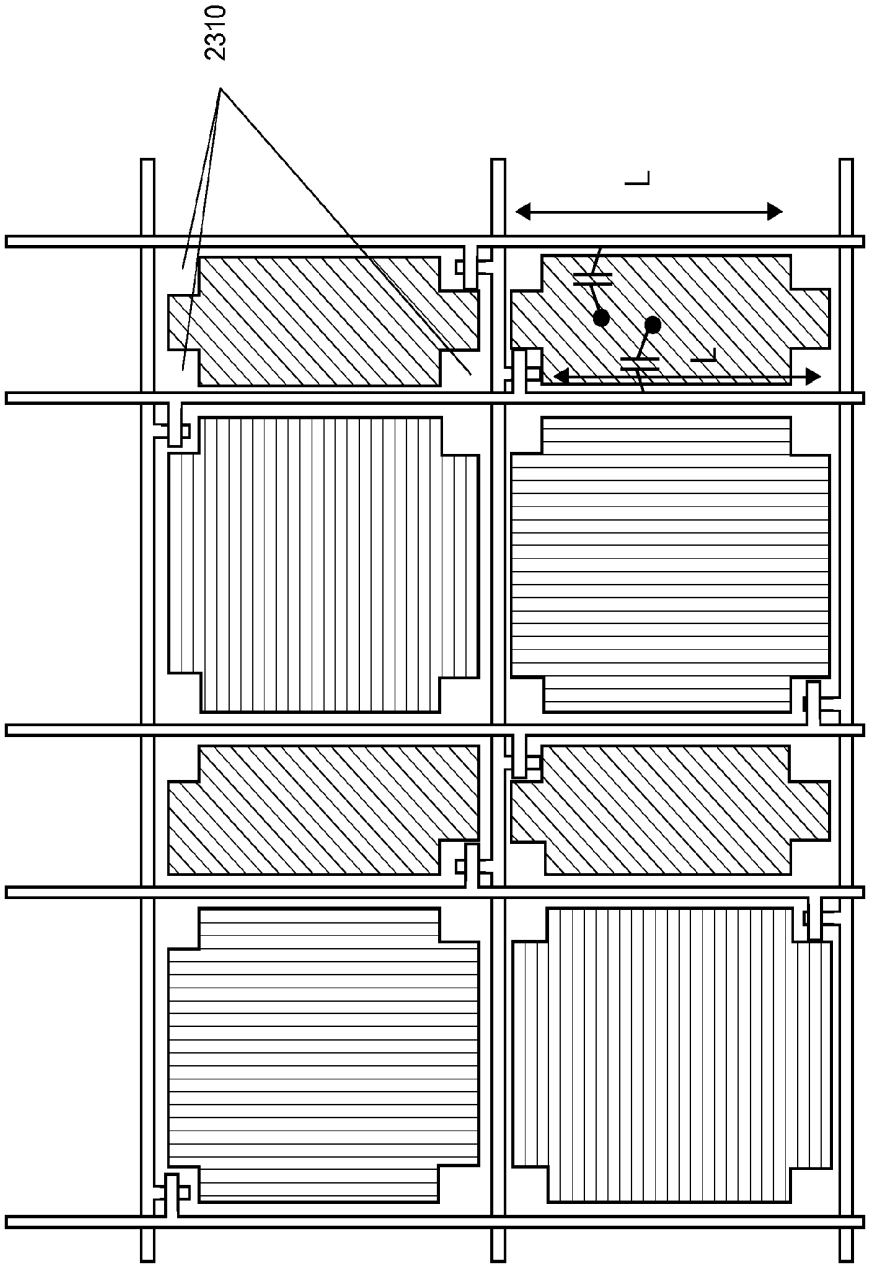



FIG. 23

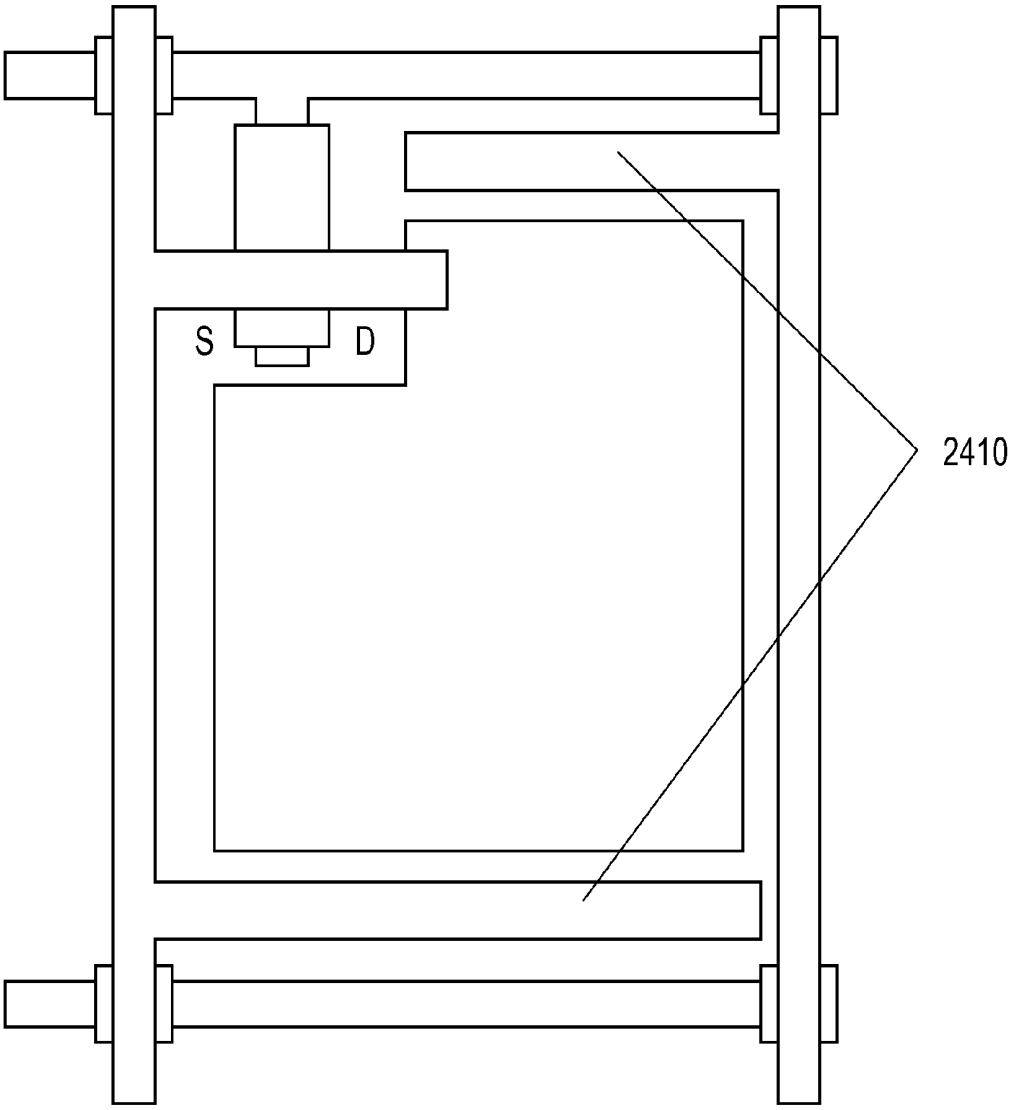



FIG. 24

# LIQUID CRYSTAL DISPLAY BACKPLANE LAYOUTS AND ADDRESSING FOR NON-STANDARD SUBPIXEL ARRANGEMENTS

**[0001]** This application is a continuation of U.S. patent application Ser. No. 10/456,838, filed on Jun. 6, 2003, and claims the benefit of priority thereof and is now issued as U.S. Pat. No. 7,397,455 which is hereby incorporated by reference.

## RELATED APPLICATIONS

**[0002]** The present application is related to commonly owned (and filed on even date) United States Patent Applications: (1) United States Patent Publication No. 2004/0246213 ("the '213 application") U.S. patent application Ser. No. 10/455,925 entitled "DISPLAY PANEL HAVING CROSS-OVER CONNECTIONS EFFECTING DOT INVERSION"; (2) U.S. Pat. No. 7,218,301 ("the '301 patent") U.S. patent application Ser. No. 10/455,931 entitled "SYSTEM AND METHOD OF PERFORMING DOT INVERSION WITH STANDARD DRIVERS AND BACKPLANE ON NOVEL DISPLAY PANEL LAYOUTS"; (3) U.S. Pat. No. 7,209,105 ("the '105 patent") U.S. patent application Ser. No. 10/455,927 entitled "SYSTEM AND METHOD FOR COMPENSATING FOR VISUAL EFFECTS UPON PANELS HAVING FIXED PATTERN NOISE WITH REDUCED QUANTIZATION ERROR"; (4) U.S. Pat. No. 7,187,353 ("the '353 patent") U.S. patent application Ser. No. 10/456,806 entitled "DOT INVERSION ON NOVEL DISPLAY PANEL LAYOUTS WITH EXTRA DRIVERS"; and (5) United States Patent Publication No. 2004/0246280 ("the '280 application") U.S. patent application Ser. No. 10/456,839 entitled "IMAGE DEGRADATION CORRECTION IN NOVEL LIQUID CRYSTAL DISPLAYS," which are hereby incorporated herein by reference.

## BACKGROUND

**[0003]** In commonly owned United States Patent Applications: (1) U.S. Pat. No. 6,903,754 ("the '754 patent") U.S. patent application Ser. No. 09/916,232 entitled "ARRANGEMENT OF COLOR PIXELS FOR FULL COLOR IMAGING DEVICES WITH SIMPLIFIED ADDRESSING," filed Jul. 25, 2001; (2) United States Patent Publication No. 2003/0128225 ("the '225 application") U.S. patent application Ser. No. 10/278,353 entitled "IMPROVEMENTS TO COLOR FLAT PANEL DISPLAY SUB-PIXEL ARRANGEMENTS AND LAYOUTS FOR SUB-PIXEL RENDERING WITH INCREASED MODULATION TRANSFER FUNCTION RESPONSE," filed Oct. 22, 2002; (3) United States Patent Publication No. 2003/0128179 ("the '179 application") U.S. patent application Ser. No. 10/278,352, entitled "IMPROVEMENTS TO COLOR FLAT PANEL DISPLAY SUB-PIXEL ARRANGEMENTS AND LAYOUTS FOR SUB-PIXEL RENDERING WITH SPLIT BLUE SUB-PIXELS," filed Oct. 22, 2002; (4) United States Patent Publication No. 2004/0051724 ("the '724 application") U.S. patent application Ser. No. 10/243,094, entitled "IMPROVED FOUR COLOR ARRANGEMENTS AND EMITTERS FOR SUB-PIXEL RENDERING," filed Sep. 13, 2002; (5) United States Patent Publication No. 2003/0117423 ("the '423 application") U.S. patent application Ser. No. 10/278,328, entitled "IMPROVEMENTS TO COLOR FLAT PANEL DISPLAY SUB-PIXEL ARRANGEMENTS AND LAYOUTS WITH REDUCED BLUE LUMINANCE WELL VISIBILITY," filed Oct. 22, 2002; (6) U.S. Pat. No. 7,283,142 ("the '142 patent") U.S. patent application Ser. No. 10/278,393, entitled "COLOR DISPLAY HAVING HORIZONTAL SUB-PIXEL ARRANGEMENTS AND LAYOUTS," filed Oct. 22, 2002; (7) United States Patent Publication No. 2004/0080479 ("the '479 application") U.S. patent application Ser. No. 10/347,001 entitled "IMPROVED SUB-PIXEL ARRANGEMENTS FOR STRIPED DISPLAYS AND METHODS AND SYSTEMS FOR SUB-PIXEL RENDERING SAME," filed Jan. 16, 2003, novel sub-pixel arrangements are therein disclosed for improving the cost/performance curves for image display devices and herein incorporated by reference.

**[0004]** These improvements are particularly pronounced when coupled with sub-pixel rendering (SPR) systems and methods further disclosed in those applications and in commonly owned United States Patent Applications: (1) U.S. Pat. No. 7,123,277 ("the '277 patent") U.S. patent application Ser. No. 10/051,612, entitled "CONVERSION OF A SUB-PIXEL FORMAT DATA TO ANOTHER SUB-PIXEL DATA FORMAT," filed Jan. 16, 2002; (2) U.S. Pat. No. 7,221,381 ("the '381 patent") U.S. patent application Ser. No. 10/150,355, entitled "METHODS AND SYSTEMS FOR SUB-PIXEL RENDERING WITH GAMMA ADJUSTMENT," filed May 17, 2002; (3) U.S. Pat. No. 7,184,066 ("the '066 patent") U.S. patent application Ser. No. 10/215,843, entitled "METHODS AND SYSTEMS FOR SUB-PIXEL RENDERING WITH ADAPTIVE FILTERING," filed Aug. 8, 2002; (4) United States Patent Publication No. 2004/0196302 ("the '302 application") U.S. patent application Ser. No. 10/379,767, entitled "SYSTEMS AND METHODS FOR TEMPORAL SUB-PIXEL RENDERING OF IMAGE DATA" filed Mar. 4, 2003; (5) U.S. Pat. No. 7,167,186 ("the '186 patent") U.S. patent application Ser. No. 10/379,765, entitled "SYSTEMS AND METHODS FOR MOTION ADAPTIVE FILTERING," filed Mar. 4, 2003; (6) U.S. Pat. No. 6,917,368 ("the '368 patent") U.S. patent application Ser. No. 10/379,766 entitled "SUB-PIXEL RENDERING SYSTEM AND METHOD FOR IMPROVED DISPLAY VIEWING ANGLES" filed Mar. 4, 2003; (7) U.S. Pat. No. 7,352,374 ("the '374 patent") U.S. patent application Ser. No. 10/409,413 entitled "IMAGE DATA SET WITH EMBEDDED PRE-SUBPIXEL RENDERED IMAGE" filed Apr. 7, 2003, which are hereby incorporated herein by reference.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0005]** The accompanying drawings, which are incorporated in, and constitute a part of this specification illustrate exemplary implementations and embodiments of the invention and, together with the description, serve to explain principles of the invention.

**[0006]** FIG. **1**A shows a conventional RGB stripe panel with 1×1 dot inversion.

**[0007]** FIG. **1**B shows a conventional RGB stripe panel with 1×2 dot inversion.

**[0008]** FIG. **2** shows a panel having a novel subpixel repeating group of even number of subpixels in a first (row) direction with a conventional 1×1 dot inversion scheme.

**[0009]** FIG. **3** shows the panel of FIG. **2** with a novel TFT backplane layout.

**[0010]** FIG. **4** depicts the operation of the panel of FIG. **3** during two row-writes.

**[0011]** FIG. **5** depicts another embodiment of a TFT backplane layout with a 1×1 dot inversion scheme.

**[0012]** FIG. **6** depicts the panel of FIG. **5** with a 1×2 dot inversion scheme.

**[0013]** FIG. **7** depicts a panel wherein at least two regions are defined with TFTs constructed in the a first region of a pixel and TFTs constructed in a second region of a pixel.

**[0014]** FIGS. **8** through **15** depict a general technique for remapping TFT to a backplane layout so as to effect a desired dot inversion scheme on a panel having a novel subpixel repeating group.

**[0015]** FIGS. **16**A and **16**B show a particular embodiment of a TFT backplane layout on a panel having a novel subpixel repeating group with a 1×2 dot inversion scheme.

**[0016]** FIG. **16**C shows yet another embodiment of a TFT backplane layout with a novel subpixel repeating group affecting a 1×2 dot inversion scheme.

**[0017]** FIGS. **17**A, **17**B, and **17**C show particular TFTs having a double source/drain structure.

**[0018]** FIG. **18** shows a TFT with a double gate structure.

**[0019]** FIGS. **19**A and **19**B show TFT structures in a normal orientation and a reverse orientation respectively.

**[0020]** FIGS. **20**A and **20**B show TFT structures in a normal orientation and a reverse orientation with an added gate crossover in the normal orientation to balance any parasitic capacitance found in the reverse orientation.

**[0021]** FIGS. **21**A and **21**B show TFT structures in a normal orientation and a reverse orientation with one fewer gate crossover in the reverse orientation to match any parasitic capacitance in the normal orientation.

**[0022]** FIG. **22** shows one novel pixel element design having a corner removed from the pixel to balance parasitic capacitances.

**[0023]** FIG. **23** shows yet another novel pixel element design having multiple corners removed to balance parasitic capacitances.

**[0024]** FIG. **24** shows yet another novel pixel structure in which at least one extra line is added to shield the pixel element from parasitic effects.

## DETAILED DESCRIPTION

**[0025]** Reference will now be made in detail to implementations and embodiments, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

**[0026]** FIG. **1**A shows a conventional RGB stripe structure on panel **100** for an Active Matrix Liquid Crystal Display (AMLCD) having thin film transistors (TFTs) **116** to activate individual colored subpixels—red **104**, green **106** and blue **108** subpixels respectively. As may be seen, a red, a green and a blue subpixel form a repeating group of subpixels **102** that comprise the panel.

**[0027]** As also shown, each subpixel is connected to a column line (each driven by a column driver **110**) and a row line (e.g. **112** and **114**). In the field of AMLCD panels, it is known to drive the panel with a dot inversion scheme to reduce crosstalk and flicker. FIG. **1**A depicts one particular dot inversion scheme—i.e. 1×1 dot inversion—that is indicated by a "+" and a "−" polarity given in the center of each subpixel. Each row line is typically connected to a gate (not shown in FIG. **1**A) of TFT **116**. Image data—delivered via the column lines—are typically connected to the source of each TFT. Image data is written to the panel a row at a time and is given a polarity bias scheme as indicated herein as either ODD ("O") or EVEN ("E") schemes. As shown, row **112** is being written with ODD polarity scheme at a given time while row **114** is being written with EVEN polarity scheme at a next time. The polarities alternate ODD and EVEN schemes a row at a time in this 1×1 dot inversion scheme.

**[0028]** FIG. **1**B depicts another conventional RGB stripe panel having another dot inversion scheme—i.e. 1×2 dot inversion. Here, the polarity scheme changes over the course of two rows—as opposed to every row, as in 1×1 dot inversion. In both dot inversion schemes, a few observations are noted: (1) in 1×1 dot inversion, every two physically adjacent subpixels (in both the horizontal and vertical direction) are of different polarity; (2) in 1×2 dot inversion, every two physically adjacent subpixels in the horizontal direction are of different polarity; (3) across any given row, each successive colored subpixel has an opposite polarity to its neighbor. Thus, for example, two successive red subpixels along a row will be either (+,−) or (−,+). Of course, in 1×1 dot inversion, two successive red subpixels along a column with have opposite polarity; whereas in 1×2 dot inversion, each group of two successive red subpixels will have opposite polarity. This changing of polarity decreases noticeable visual defects that occur with particular images rendered upon an AMLCD panel.

**[0029]** FIG. **2** shows a panel comprising a repeat subpixel grouping **202**, as further described in the '353 application. As may be seen, repeat subpixel grouping **202** is an eight subpixel repeat group, comprising a checkerboard of red and blue subpixels with two columns of reduced-area green subpixels in between. If the standard 1×1 dot inversion scheme is applied to a panel comprising such a repeat grouping (as shown in FIG. **2**), then it becomes apparent that the property described above for RGB striped panels (namely, that successive colored pixels in a row and/or column have different polarities) is now violated. This condition may cause a number of visual defects noticed on the panel—particularly when certain image patterns are displayed. This observation also occurs with other novel subpixel repeat grouping—for example, the subpixel repeat grouping in FIG. **1** of the '352 application—and other repeat groupings that are not an odd number of repeating subpixels across a row. Thus, as the traditional RGB striped panels have three such repeating subpixels in its repeat group (namely, R, G and B), these traditional panels do not necessarily violate the above noted conditions. However, the repeat grouping of FIG. **2** in the present application has four (i.e. an even number) of subpixels in its repeat group across a row (e.g. R, G, B, and G). It will be appreciated that the embodiments described herein are equally applicable to all such even modulus repeat groupings.

**[0030]** In order to affect improved performance, several embodiments are herein described. A first embodiment of an AMLCD panel **300** is shown in FIG. **3**. Box **302** encloses four TFTs **116** that drive their associated four colored subpixels. As may be seen, the gates of each TFT **116** are connected to a row line in such a manner as to have same colored subpixels—successively staggered—across each row affect opposite polarity. This effect is shown in FIG. **4**, for example, with red subpixels **408**, **410**, and **412**, etc. receiving (−, +, −, . . . ) polarities during a row write to line **404**. The same effect is shown for blue subpixels across line **404**. One possible benefit of this condition is that any parasitic capacitances (for example, as between the gate and the drain of the TFT, CGD, and as between the pixel and the gate line, CG-Pixel.) that

occur across a row/gate line with are minimized by having the same number of "+" and "−" polarities connected to the row/gate line.

**[0031]** It is further seen in FIG. **3** that the TFTs **116** in repeating group **302** are formed at the intersection of a pair of row and column lines at a given quadrant of the subpixel. For example, the upper red subpixel in group **302** has its TFT formed in the first quadrant; while the upper green subpixel has its TFT formed in the third quadrant. To affect a dot inversion scheme on a subpixel repeating group of an even number of subpixels in a row or column direction, one embodiment is to find a suitable remapping of the TFT backplane from their usual placement in one quadrant, so that the remapping may use any number of quadrants greater than one.

**[0032]** FIG. **4** depicts how panel **300** operates over the course of two successive row-writes. During the first row-write (panel **300** on the left hand side), row **402** sends an active gate signal down to the connected TFTs and their associated subpixels (shown in BOLD hatching) on an EVEN cycle. In this case, all of the green subpixels in two rows are activated. However, as may be seen, the TFTs have been advantageously replaced so that two bordering green subpixels in the vertical direction have opposite polarities. So, for example, green subpixel **406** has a "+" polarity; while green subpixel **408** has a "−" polarity. Additionally, as may be seen, the polarities of all of the green subpixels connected to row line **402** are balanced—i.e. the number of "+" polarity green subpixels equals the number of polarity green subpixels .

**[0033]** During the next row-write (as shown in panel **300** on the right hand side), row line **404** sends an active gate signal to its connected TFTs and their associated subpixels (also shown in BOLD hatching) on an ODD cycle. Again, given the replacement of the TFTs, each two adjacent subpixels in the vertical direction have opposite polarity. Additionally, as described above, same colored subpixels that are successively staggered along a row line are of opposite polarity.

**[0034]** Yet another embodiment comprising a TFT replacement (i.e. off from the traditional manner of consistently placing TFTs in a single position relative to the subpixels—such as the upper left hand corner) is shown in FIG. **5**. The repeat grouping of TFTs in this arrangement are shown as block **502**. With this arrangement, similar corrective polarity conditions as noted for FIGS. **3** and **4** are found with the TFT placement of FIG. **5**. For example, along row/gate line **504**, every two red subpixels alternate polarity—e.g. red subpixels **510** and **512** have "+" polarity; while red subpixels **514** and **516** have "−" polarity. As will be discussed in greater detail below, there are a number of different TFT placements that will achieve the same effects. Each such TFT placement (or TFT "remapping") is contemplated within the scope of the present invention and, as such, the present invention should not be limited to any particular TFT placement or remapping.

**[0035]** FIG. **6** is yet another embodiment of TFT remapping on panel **600** that may take into account additional parasitic capacitance effects between pixel and the CS electrode **602**. In this case, two successive row/gate lines are driven by a given polarity scheme (O or E). The polarity of each subpixel is shown in its center. It will be noted that along any given row (and hence along a given CS line), successive same colored subpixels alternate polarity.

**[0036]** Another TFT remapping that may produce similar beneficial effects is shown in FIG. **7**. In this case, the panel **700** is partitioned into sections (e.g. **702**, **704**) that place the TFTs of their associated subpixels in corners such that the polarity at the two columns at the partition line repeats. Thus, for example, column **710** and **712** have the same polarities of subpixels going down the respective columns. If the number of subpixels across a row defining a given partition is small enough, the accumulated parasitic capacitances in that partition may be sufficiently below a visually detectable (or at least manageable) level. This partitioning across a panel might occur a number of times in order to keep those parasitics at a low enough level. As an alternative embodiment, this panel could have a 1×2 dot inversion scheme - thereby effectively solving vertical crosstalk (i.e. whereby same colored subpixels have same polarity in a given column).

**[0037]** FIGS. **8** through **15** outline a general procedure for developing many different embodiments of TFT remappings that may effect reduced parasitic capacitance in an panel having even modulus for a subpixel repeating group. Starting with a basic grid **800** of FIG. **8**, a repeating subpixel grouping **902** is placed upon the grid in FIG. **9**. It will be appreciated that, as noted above, any repeating group would suffice here; but preferably one with an even number of subpixels across a row. A dot inversion scheme is selected in FIG. **10**—in this case, a 1×2 dot inversion scheme is selected with two polarity schemes or "phases" —O and E. Additionally, these two phases are repeated for every two row/gate lines—O, O, E, E, etc. If 1×1 dot inversion were desired, then the phases would alternate every row/gate line.

**[0038]** Any symmetries in the repeat grouping are now to be considered. For example, in FIG. **11**, it is noted that every other column is a line of blue subpixels. Thus, a possible symmetry to consider is in the other columns of alternating red and green subpixels. Now, consider all possible combinations of polarities for the first two subpixels in the columns of interest. In FIG. **11** for example, the first two red and green subpixels could assume a set of four possible polarity values. In general, if the first N subpixels in relevant rows or columns are considered, then 2N combinations of polarities may or should be considered.

**[0039]** Other symmetries may also be taken into consideration. In FIG. **12**, the polarities in one of the columns of same colored subpixels are considered. A listing of possible polarities are shown in list **1202** for the second column of blue subpixels—and the first four such blue subpixels in the column are considered. The list could be exhaustive of the possibilities of polarities and certainly another number other than four may be considered. As it may be advantageous to balance the polarities down a given column—all of those possibilities with a balanced number of polarities are noted as "OK". One OK combination **1204** is selected, solely for exemplary purposes, for grid **1206**.

**[0040]** FIG. **13** shows an initial selection of TFT placements on the grid. Initially, for optional visual aiding, the polarities accorded to each intersection of a row/gate line and a column/data line are placed on the grid—as either a "+" or a "−". It is noted that any TFT placed in any quadrant around an intersection point will effect the same polarity on its associated subpixel. As for the subpixels in FIG. **12** that have been assigned a polarity, there is a degree of freedom in selecting which intersection to place the TFT. For example, red subpixel **1302** has been assigned a "+" polarity and there are two possible intersections **1304** and **1306** at which to place its associated TFT. For exemplary purposes, the TFT is selected to be placed at intersection **1304**. Of course, the placement of TFTs could be affected by many possible factors—for

example, the desire to minimally impact design rules, to minimize ill effect (e.g. parasitic capacitances), etc. As may be seen, the other TFTs for the polarity-assigned subpixels in FIG. **13** have also been placed—as one possible embodiment and selection thereof. Of course, other embodiments/selections are also possible.

**[0041]** FIG. **14** extends this process of TFT placement to the remaining blue subpixels on the grid. Although there are other selections possible, this particular selection was made with the idea of balancing the polarities across any given row. As may be seen, the blue subpixels polarities balance out across any given row/gate line. FIG. **15** fills in the remaining red and green subpixel TFT placements. One possible goal is to assign the remaining TFTs in a grouping that may be repeated across the entire panel to form the backplane. One such repeat grouping is **1502** in FIG. **15**. Grouping **1502** is an 8×4 subpixel grouping that seeks to balance polarities across all subpixels in the row and column directions, as well as balancing polarities within each single color subpixel subgird in the row and column directions. It will be appreciated that by following the general procedure outlined above and exploiting the various degrees of freedom in design choice, many possible TFT placements or remappings are possible to develop a suitable TFT grid.

**[0042]** FIG. **16**A shows one possible TFT remapping grid effecting a 1×2 dot inversion scheme. FIG. **16**B shows how the remapping grid might be implemented on a panel with a little greater detail. TFT **1602** and **1604**—with TFT **1602** implemented at the bottom of a pixel area and TFT **1604** at the top of a pixel area—are possibly susceptible to some uneven effects that might be introduced during the manufacturing process. For example, if the gate metal or pixel electrode masks are translated upwards during manufacturing, then it may be possible for reduced parasitic capacitance for TFT **1602** and its associated pixel and for increased parasitic capacitance for TFT **1604** and its associated pixel. If the errors in parasitics are out of tolerance bounds, then the yield of manufacturing such panels with unconventional TFT remappings might decrease. Thus, it may desirable to redesign the TFT structure as described below in order to abate any uneven effects as noted above.

**[0043]** FIG. **16**C shows another embodiment of a panel having a novel subpixel repeating group **1650**. In this group, the pattern looks like:

**[0044]** R G B G

**[0045]** R G B G

**[0046]** B G R G

**[0047]** B G R G

**[0048]** When a 1×1 dot inversion scheme is applied to this repeat grouping, vertical crosstalk problems are solved. Additionally, all the TFTs may be place on the same side of the pixel structure—which may reduce some parasitic effects or imbalances.

**[0049]** One known attempt to correct for TFT misalignments and any associated increase in parasitic capacitance is found in U.S. Pat. No. 5,191,451 to Katayama et al. FIG. **17**A depicts the "double TFT" arrangement **1700** of the '451 patent. Source line **1704** connects to the TFT via source electrode **1706**. Two gate electrodes **1708** are connected to gate line **1702**. Two drain electrodes **1710** connect to the pixel and are formed such that the two gate electrodes **1708** affect conduction from the source electrode to the drain electrodes when activated. It is noted that there are two crossover regions **1712** that are connected to TFT may produce additional parasitic capacitance between the gate and the source. As discussed in the '451 patent, any vertical misalignment of the TFT placement is somewhat corrected by this double TFT arrangement as is discussed therein. FIGS. **17**B and **17**C provide different alternative embodiments for the double TFT structure to the one shown in FIG. **17**A. This structure will enable reduced source to gate capacitance, which can cause crosstalk in certain images. The gate to drain crossover will be less damaging to image quality. One advantage of the embodiment of FIG. **17**C is that there is only one crossover **1732** that may reduce parasitic capacitance.

**[0050]** Another manner of reducing the ill effects of TFT misalignment is shown in U.S. Pat. No. 5,097,297 to Nakazawa. FIG. **18** depicts a TFT **1800** made in the manner taught in the '297 patent. As may be seen in FIG. **18**, gate line **1802** delivers the gate signal to gate electrode **1808**. Source line **1804** sends image data to source electrodes **1806**. When the gate electrode is activated, the image data is transferred to the pixel via the drain electrode **1810**. It is noted that this TFT embodiment contains only one gate crossover **1812** which aids in reducing parasitic capacitance.

**[0051]** Another set of TFT redesigns are shown in FIGS. **19** through **21** to handle the unevenness of parasitic capacitance that might be introduced by the above described TFT remapping. As TFTs are remapped on the panel, it is possible for some TFTs on the panel to be implemented in different corners or quadrants of a pixel area. For example, some TFTs may be constructed in the upper left hand corner of the pixel area, some in the upper right hand corner of the pixel area and so on. If all such TFTs were constructed the same way, then it would be likely that the source-drain orientation would be reversed for left hand corner and right hand corner implementation. Such non-uniformity of construction might introduce uneven parasitic capacitance in the case of a given TFT misalignment.

**[0052]** FIG. **19** is one embodiment of a TFT built with a reverse orientation **1902** as compared with a TFT built with a typical orientation **1904**. For exemplary purposes, TFT **1904** is constructed within the upper left hand corner of its associated pixel in the usual manner—i.e. without any crossovers to avoid any introduced parasitic capacitance. It is noted that the source (S) and drain (D) electrodes are placed in a left-to-right fashion. TFT **1902** is shown constructed in the upper right hand corner of a pixel area in a reverse orientation—i.e. a crossover **1914** from source line **1906** is constructed so that the source electrode **1910** and drain electrode **1912** are also in left-to-right fashion. Thus, if there is a TFT misalignment in the horizontal direction, then TFTs **1902** and **1904** will receive the same amount of added parasitic capacitance—thus, keeping the panel's defects uniform. It will be appreciated that although TFT **1902** and TFT **1904** are depicted side-by-side and connected to the same column, this is primarily for explanatory purposes. It is unlikely that two adjoining subpixels would share the same column/data line—thus, TFT **1904** and its associated pixel is provided to show the distinction between a normal TFT orientation and TFT **1902** in a reverse orientation.

**[0053]** FIG. **20** shows another embodiment of TFTs **1902** and **1904**. As can be seen, a new crossover **2002** is added to TFT **1904** so as to balance the added parasitic capacitance via crossover **1914**. FIG. **21** is yet another embodiment of TFTs **1902** and **1904**. As may be seen here, the gate electrode

crossover **1914** has been removed in favor of a gate line crossover **2102** which may have a lesser impact on individual pixel elements.

**[0054]** FIGS. **22** and **23** are embodiments of pixel elements with corners **2210** and **2310** removed to match the one corner removed containing the TFT structure. These pixel elements as designed here may balance the parasitic capacitances more than a normal pixel structure.

**[0055]** FIG. **24** is another embodiment of a pixel structure that employs at least one extra metal line **2410** that may help to shield the pixel element from the parasitic capacitances between the gate lines and the pixel element. Additionally, if a dot inversion scheme is employed, then the opposing polarities on both lines **2410** will also help to balance any parasitic capacitance between the source lines and the pixel elements.

What is claimed is:

**1**. A liquid crystal display comprising:

a display panel substantially comprising a plurality of a subpixel repeating group tiled across said display panel in a regular pattern; the subpixel repeating group comprises at least two rows, each said row further comprising an even number of subpixels; wherein each row of subpixels comprises at least two same-colored subpixels;

each said subpixel having an associated thin film transistor (TFT) connecting to said subpixel at an intersection of a row line and a column line; said thin film transistor being formed in a corner of said subpixel in one of a group of quadrants with respect to said subpixel, the group comprising a first quadrant, a second quadrant, a third quadrant and a fourth quadrant;

driver circuitry configured to send image signals and polarity signals to said subpixels; and

further wherein said display panel is partitioned into a plurality of sections along a row direction wherein said subpixels in each at a first section have their associated TFTs in a first quadrant and said subpixels in a second section have their TFTs in a second quadrant such that the polarity signal sent to same colored subpixels in said first section are different from polarity signals sent to same colored subpixels in said second section.

**2**. The liquid crystal display of claim **1** wherein wherein said polarity signal comprises a 1×1 dot inversion polarity signal.

**3**. The liquid crystal display of claim **1** wherein wherein said polarity signal comprises a 1×2 dot inversion polarity signal.

**4**. The liquid crystal display of claim **1** wherein the partitioning of said display panel occurs with frequency across said row direction such that parasitic capacitance effects are substantially abated.

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| 专利名称(译) | 用于非标准子像素排列的液晶显示器背板布局和寻址 | | |
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| [标]申请(专利权)人(译) | 三星电子株式会社 | | |
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| 其他公开文献 | US8144094 | | |
| 外部链接 | Espacenet USPTO | | |


摘要(译)

公开了用于非标准子像素排列的液晶显示器底板布局和寻址。液晶显示器包括面板和多个晶体管。该面板基本上包括子像素重复组，该子像素重复组在第一方向上具有偶数个子像素。每个薄膜晶体管将一个子像素连接到一组象限中的一个象限中的交叉点处的行和列线。该组包括第一象限，第二象限，第三象限和第四象限，其中薄膜晶体管形成在与行和列线的交叉点相邻的背板结构中。薄膜晶体管也基本上形成在背板结构中的多于一个象限中。