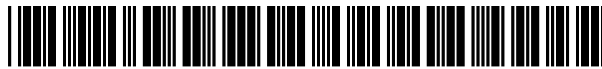


US007532263B2

(12) **United States Patent**
**Lee et al.**

(10) **Patent No.: US 7,532,263 B2**
(45) **Date of Patent: May 12, 2009**

(54) **ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY DEVICE WITH STORAGE ELECTRODES AND METHOD OF FABRICATING THE SAME**

(75) Inventors: **Seok-Woo Lee**, Gyeonggi-do (KR); **Yong-In Park**, Gyeonggi-do (KR)

(73) Assignee: **LG Display Co., Ltd.**, Seoul (KR)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 428 days.

(21) Appl. No.: **11/452,996**

(22) Filed: **Jun. 15, 2006**

(65) **Prior Publication Data**

US 2007/0103610 A1 May 10, 2007

(30) **Foreign Application Priority Data**

Nov. 9, 2005 (KR) ...................... 10-2005-0106840

(51) **Int. Cl.**

*G02F 1/1343* (2006.01)
*G02F 1/136* (2006.01)
*G02F 1/1335* (2006.01)
*H01L 31/036* (2006.01)
*H01L 29/15* (2006.01)
*G09G 3/36* (2006.01)

(52) **U.S. Cl.** ............................ **349/38**; 349/39; 349/43; 349/114; 257/59; 257/72; 345/92

(58) **Field of Classification Search** .................. 349/38, 349/39, 43, 114; 257/59, 72; 345/92
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,569,717 B1 * 5/2003 Murade ...................... 438/149
6,593,592 B1 * 7/2003 Yamazaki et al. ............ 257/71
6,657,688 B2 * 12/2003 Nagata et al. ............... 349/113

FOREIGN PATENT DOCUMENTS

CN 1680992 A 10/2005

* cited by examiner

*Primary Examiner*—David Nelms
*Assistant Examiner*—Hoan C Nguyen
(74) *Attorney, Agent, or Firm*—Morgan Lewis & Bockius LLP

(57) **ABSTRACT**

An array substrate for a liquid crystal display (LCD) device includes a substrate including a display region and a non-display region, a driving circuit in the non-display region, at least a first thin film transistor (TFT) in the display region, a storage capacitor in the display region including a first storage electrode, a second storage electrode, and a third storage electrode, wherein the first storage electrode includes a first semiconductor layer and a counter electrode, and the third storage electrode includes a first transparent electrode pattern and a first metal pattern, a gate line and a data line crossing each other to define a pixel region in the display region, and a pixel electrode connected to the first TFT in the pixel region.

**14 Claims, 55 Drawing Sheets**

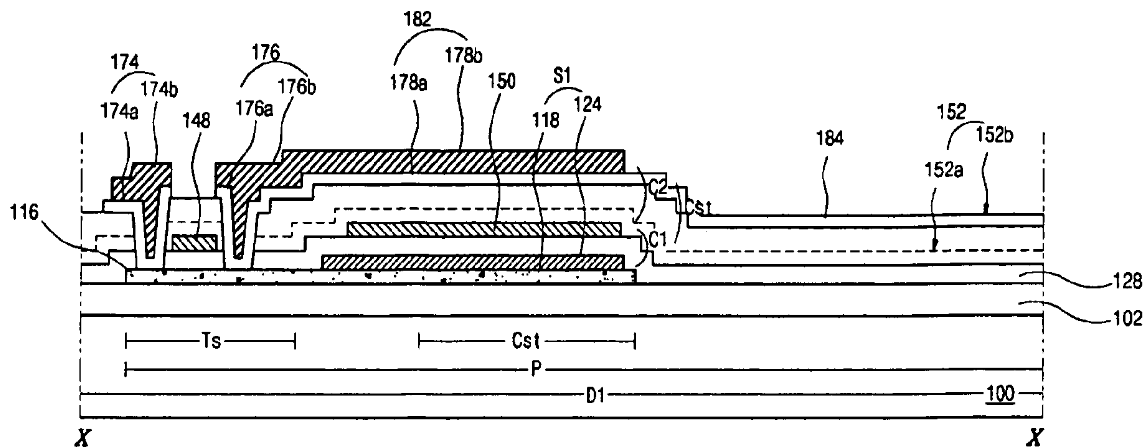


*FIG. 1*
*Related Art*

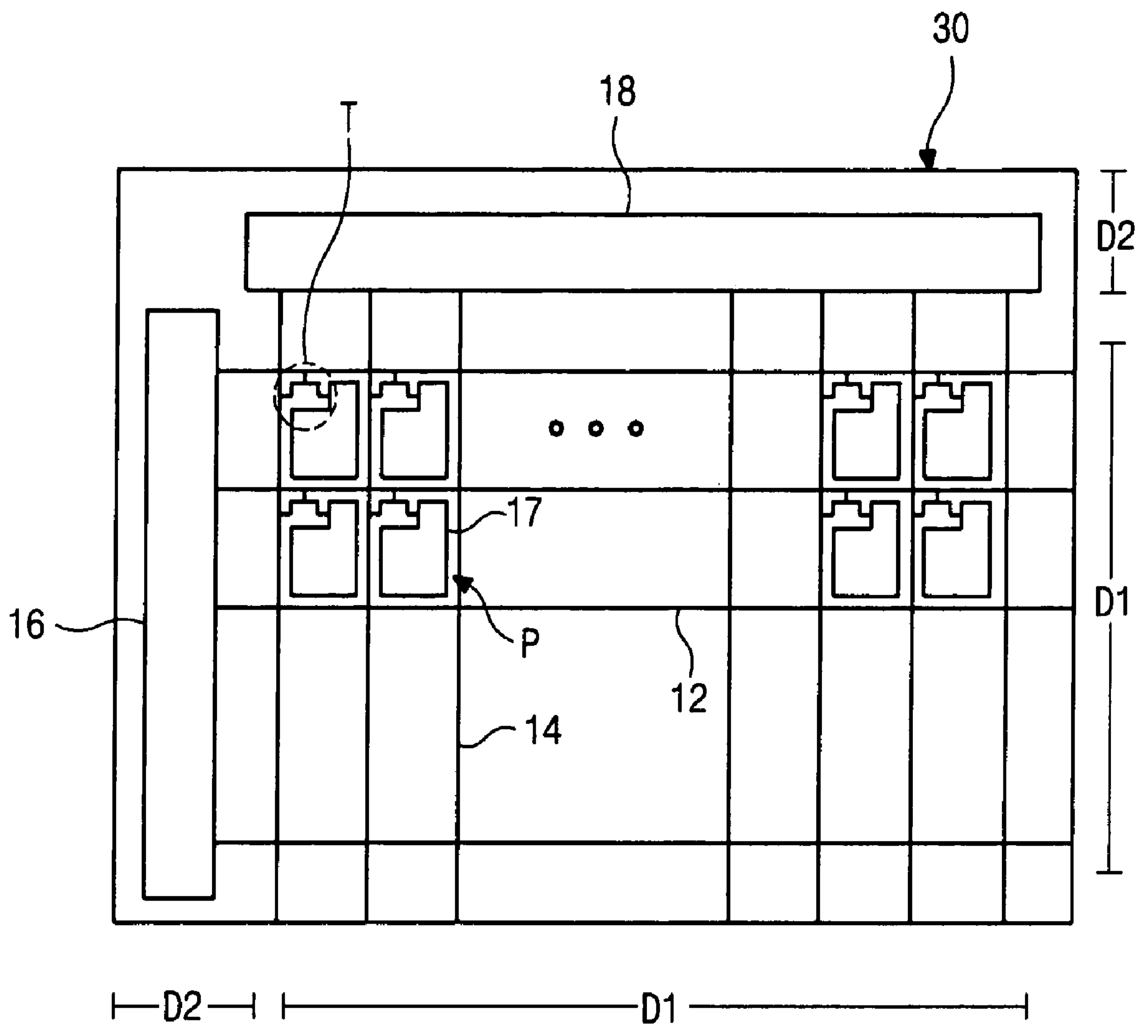


*FIG. 2*
*Related Art*

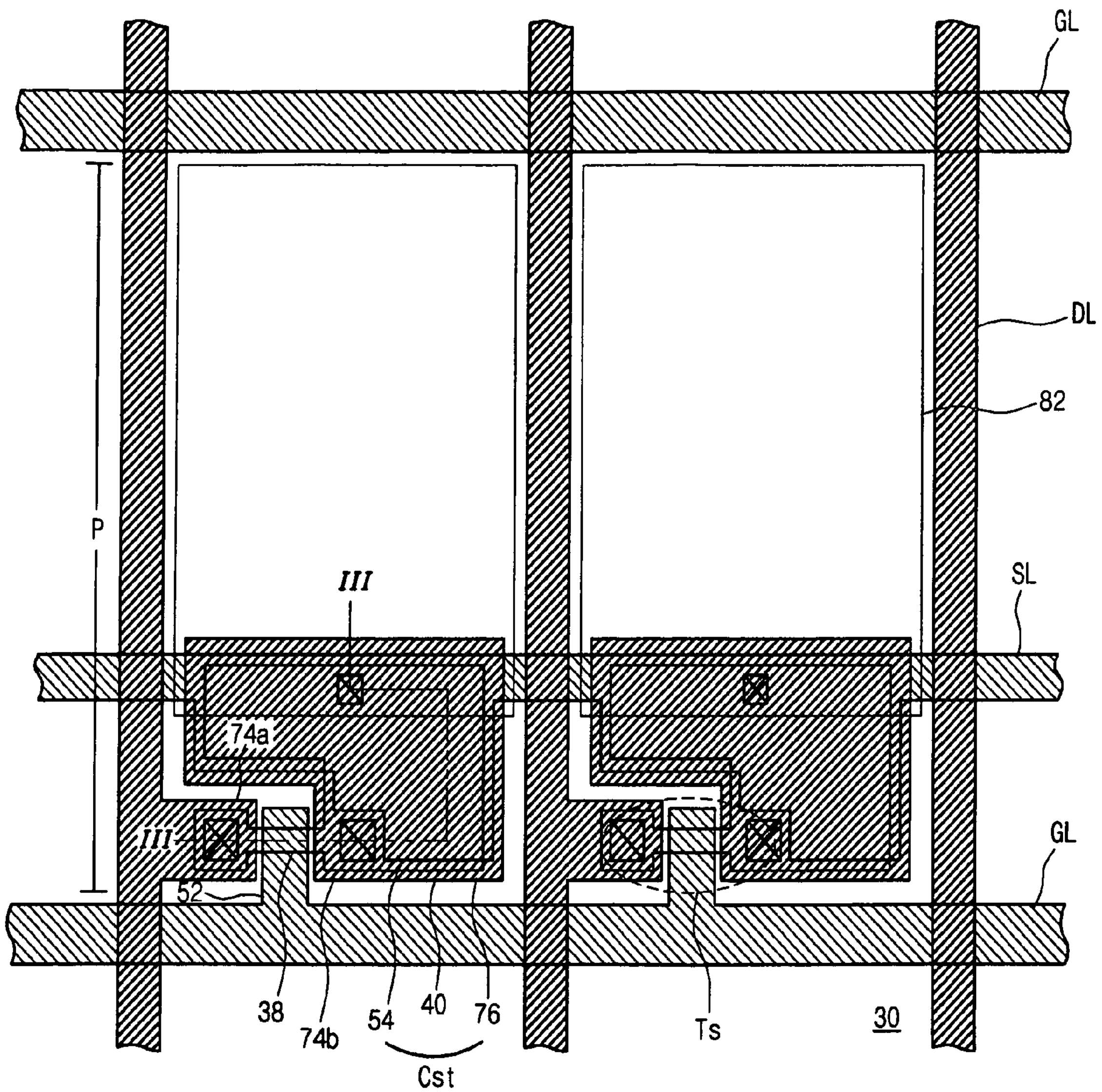


*FIG. 3*
*Related Art*

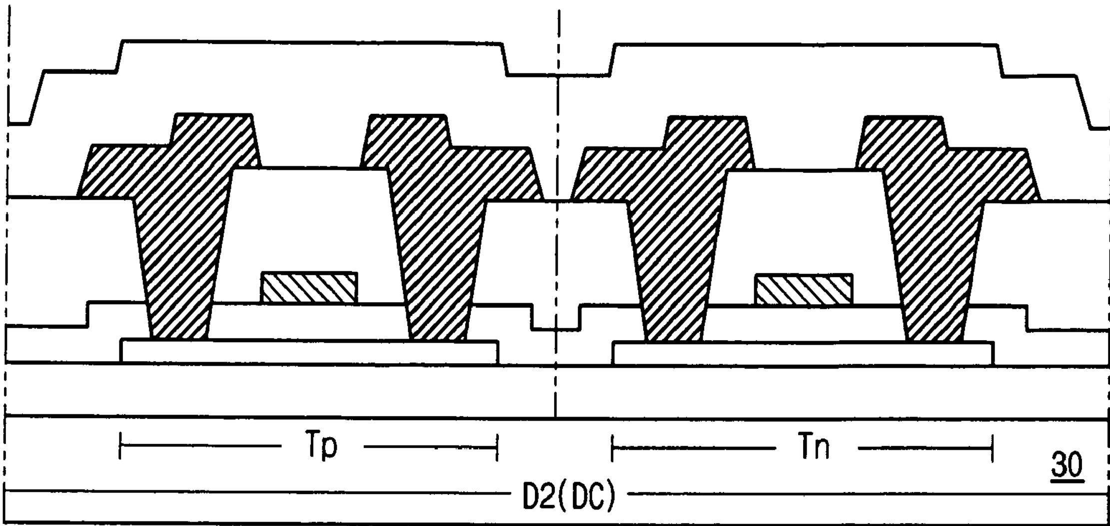


*FIG. 4*
*Related Art*

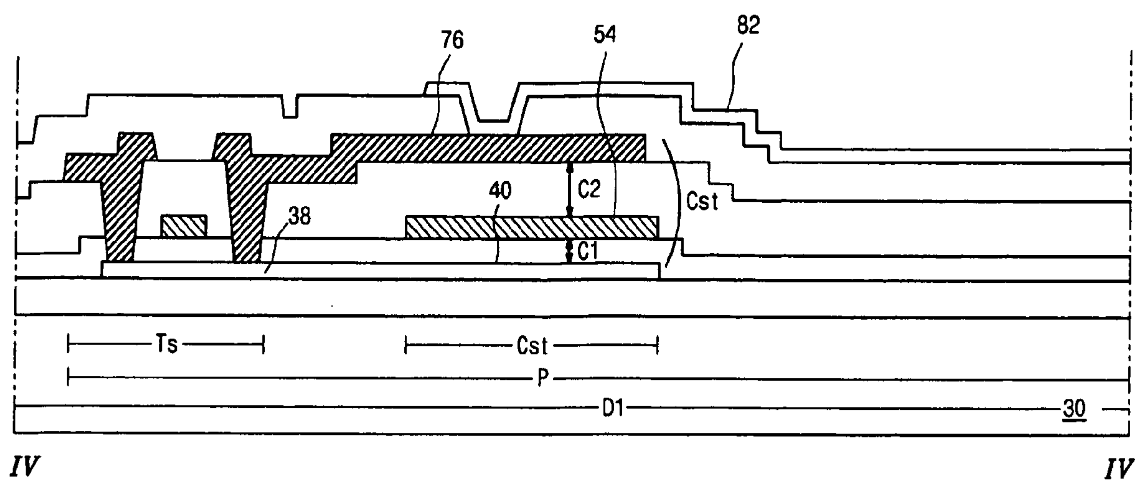


*FIG. 5A*
*Related Art*

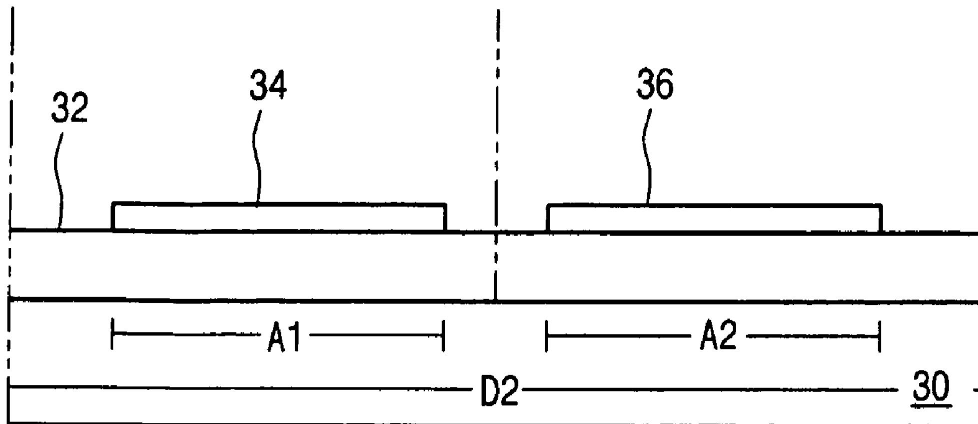



*FIG. 5B*
*Related Art*

doping with high concentration n-type impurities

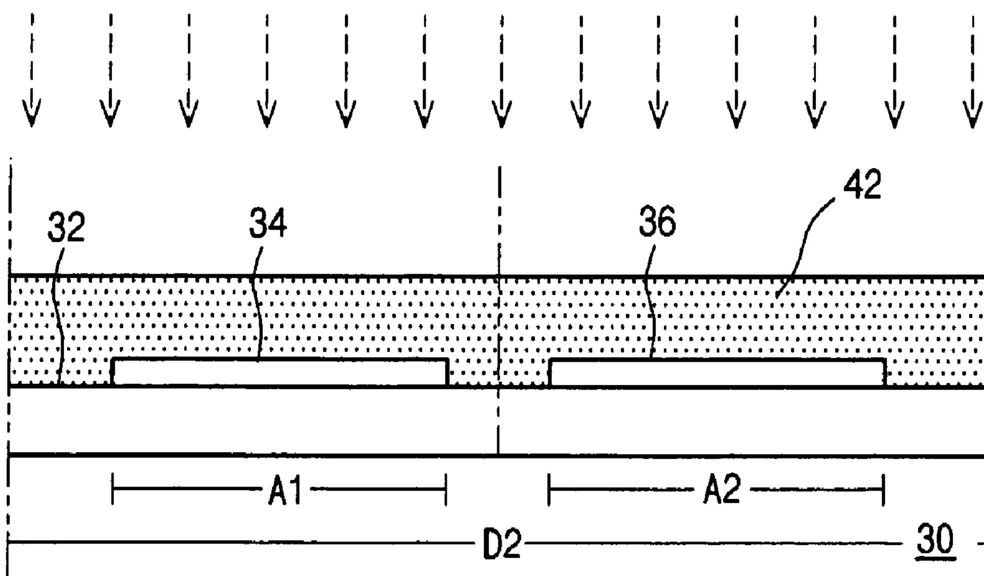


*FIG. 5C*
*Related Art*

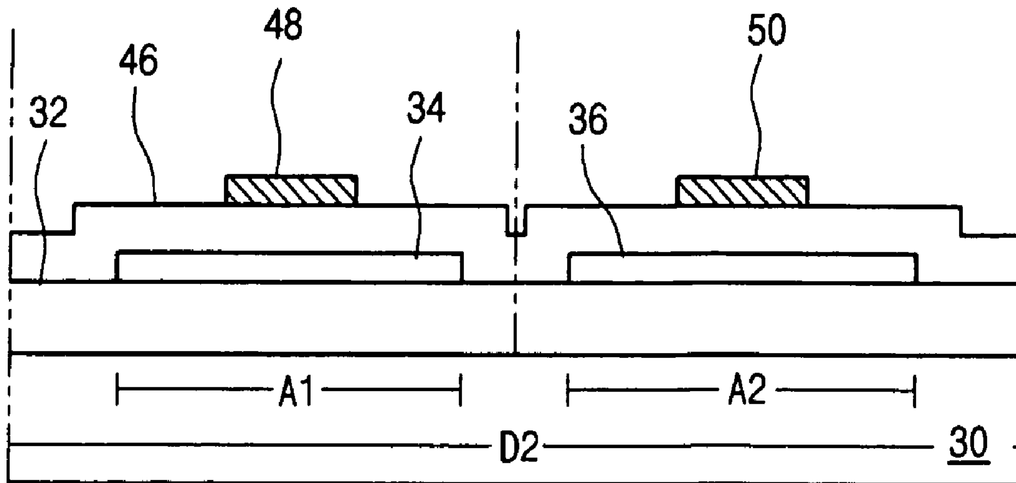
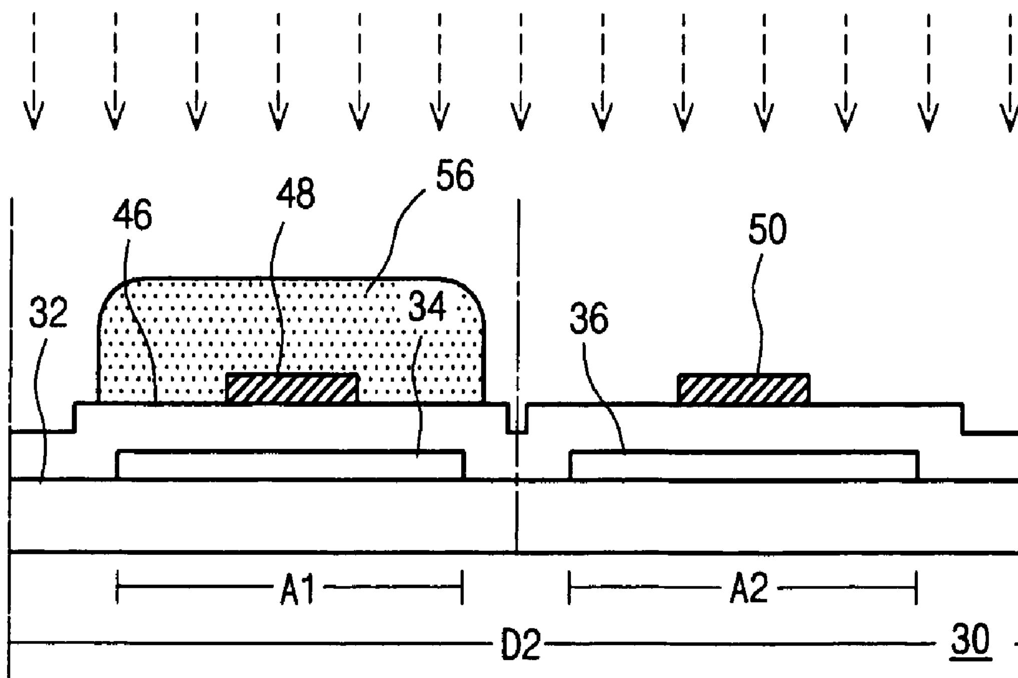


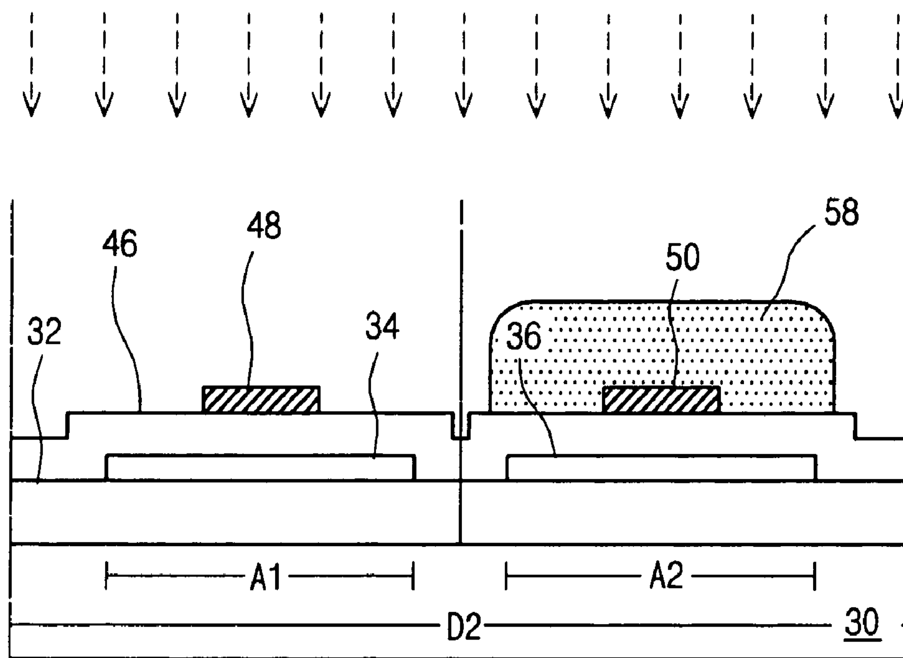

*FIG. 5D*
*Related Art*

doping with high concentration n-type impurities



# FIG. 5E
## Related Art

doping with high concentration p-type impurities




# FIG. 5F
## Related Art

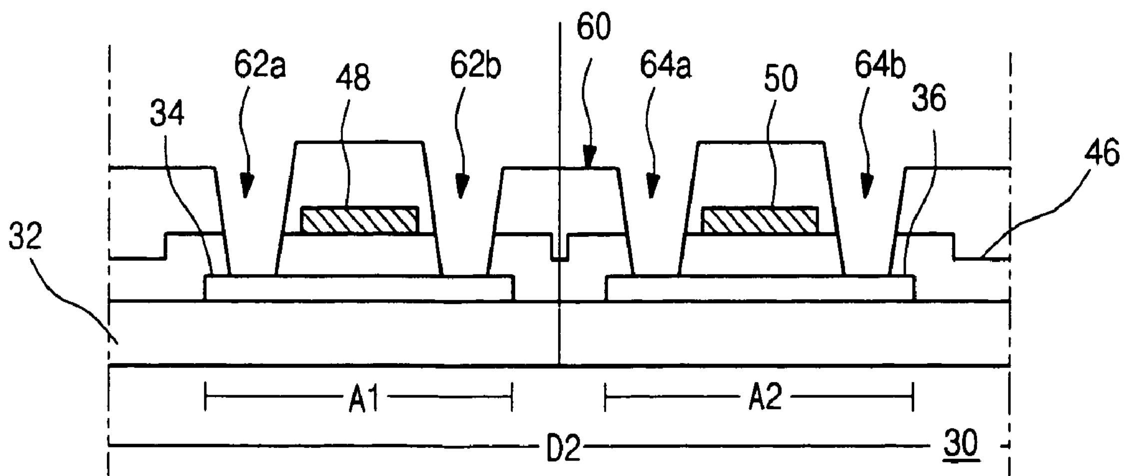


*FIG. 5G*
*Related Art*

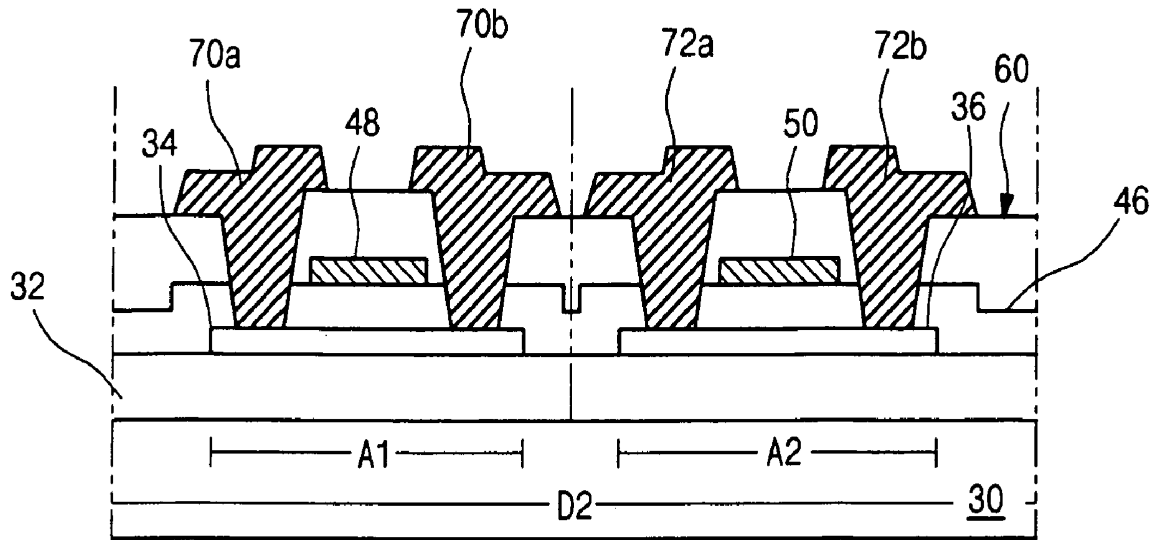



*FIG. 5H*
*Related Art*

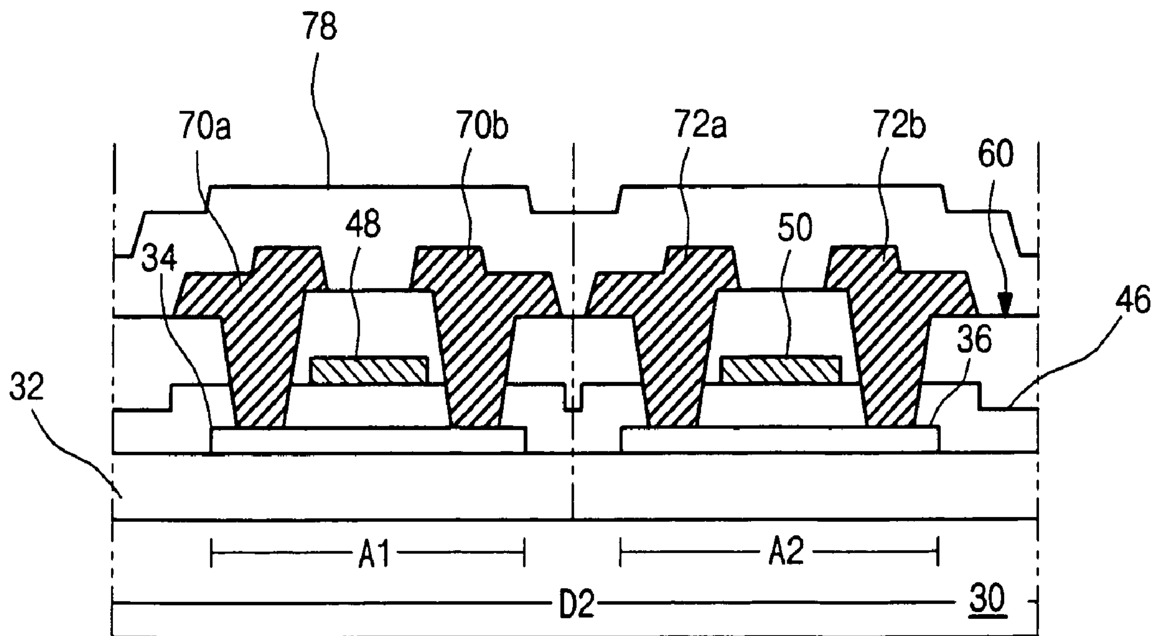


*FIG. 5I*
*Related Art*

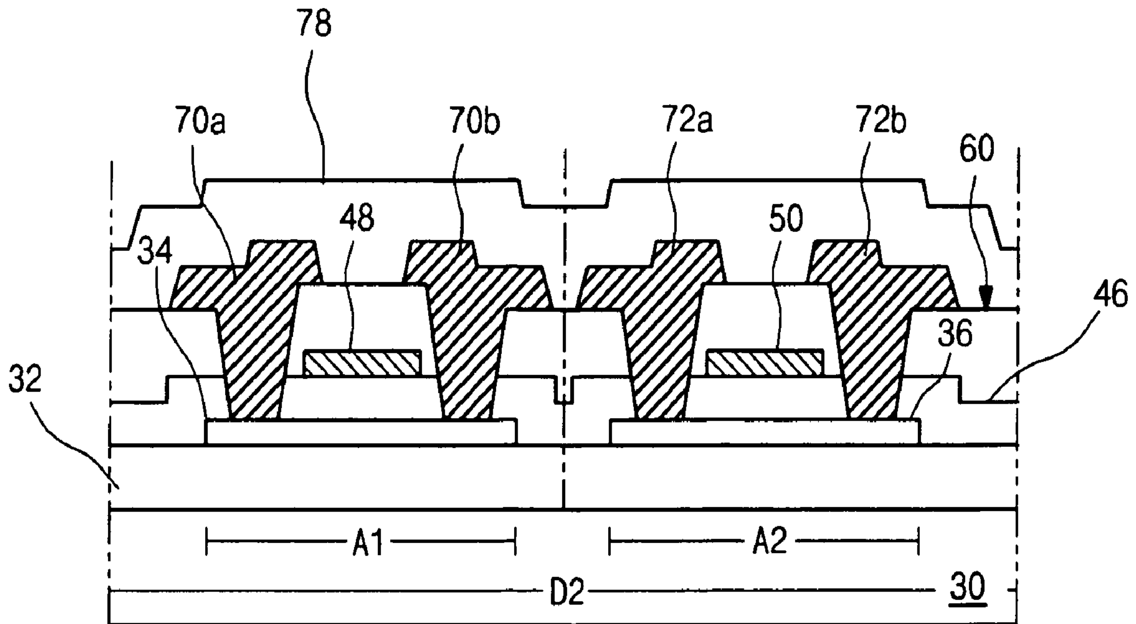



*FIG. 6A*
*Related Art*

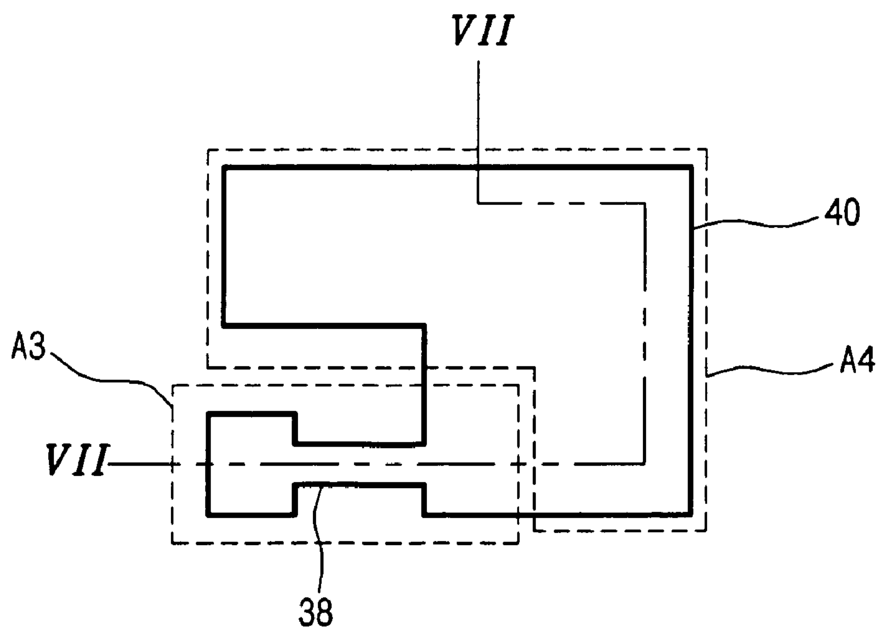


*FIG. 6B*
*Related Art*

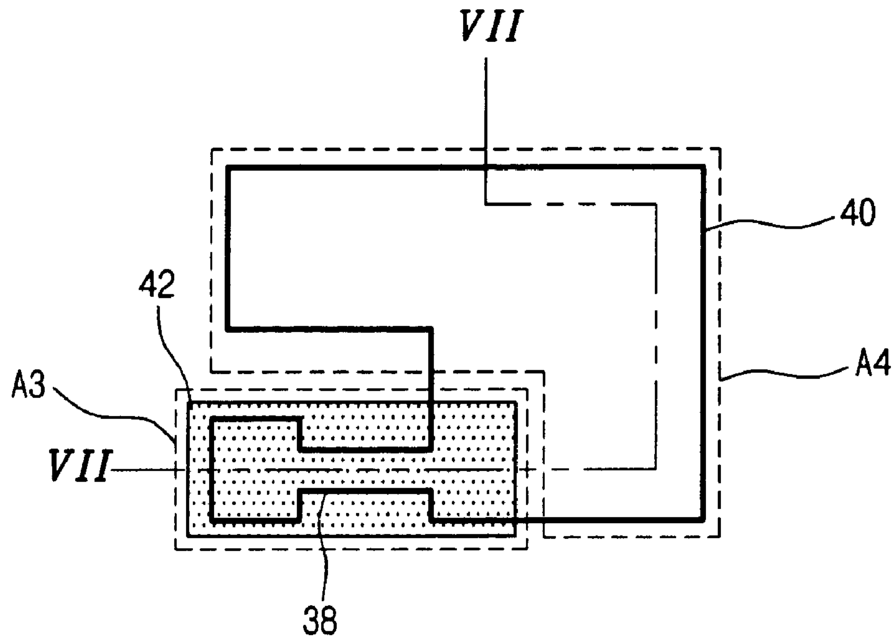



*FIG. 6C*
*Related Art*

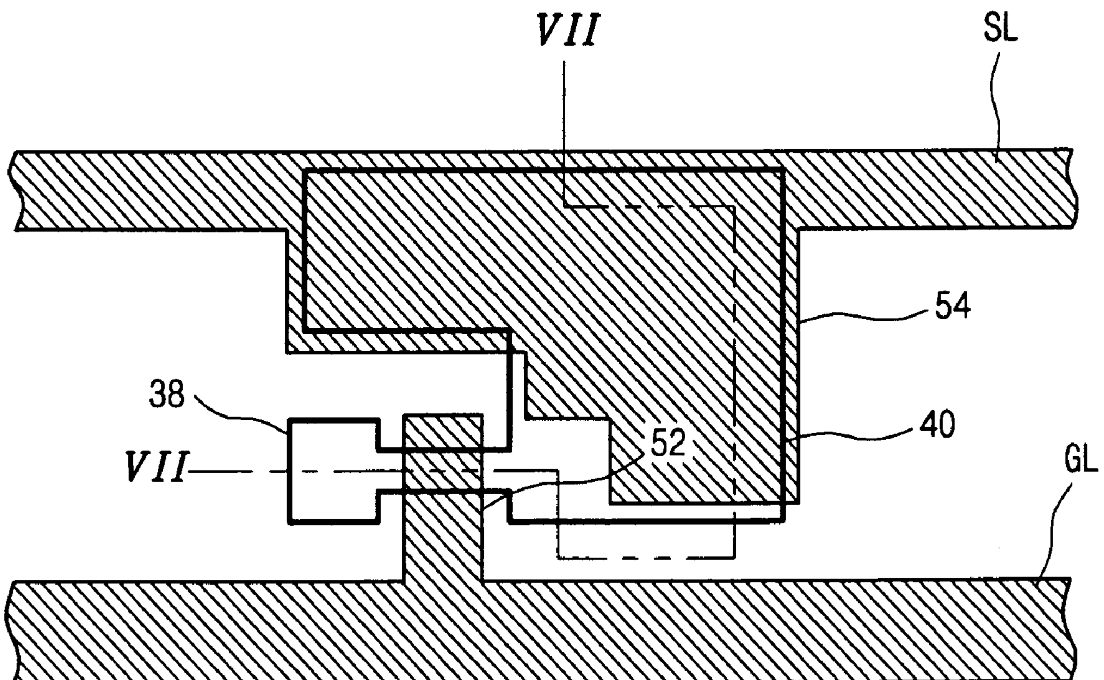


*FIG. 6D*
*Related Art*

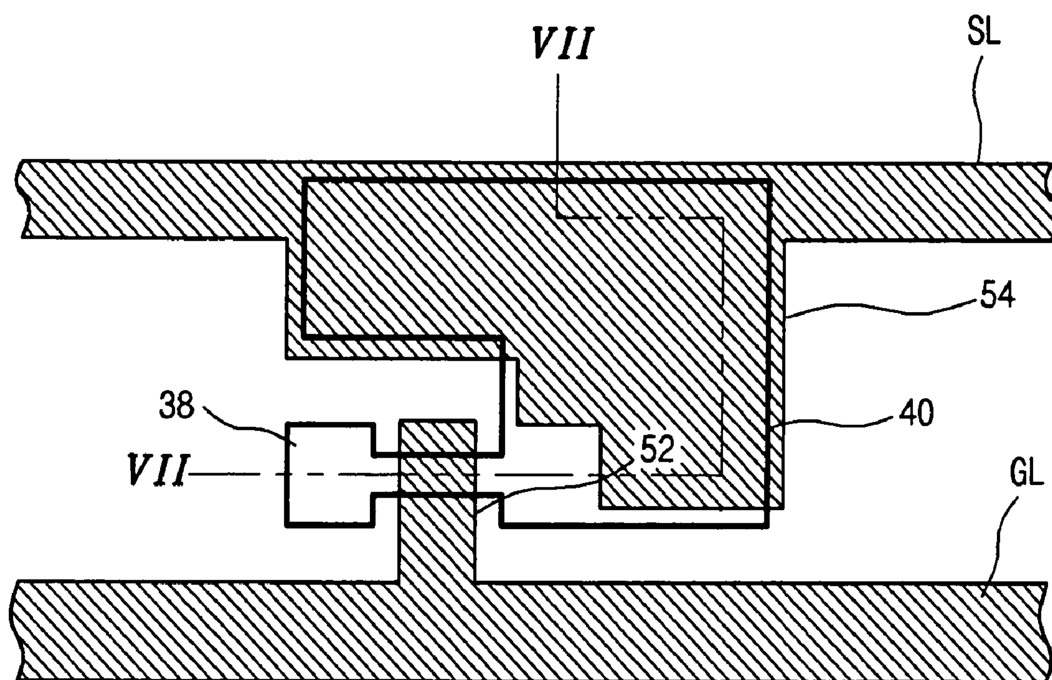


*FIG. 6E*
*Related Art*

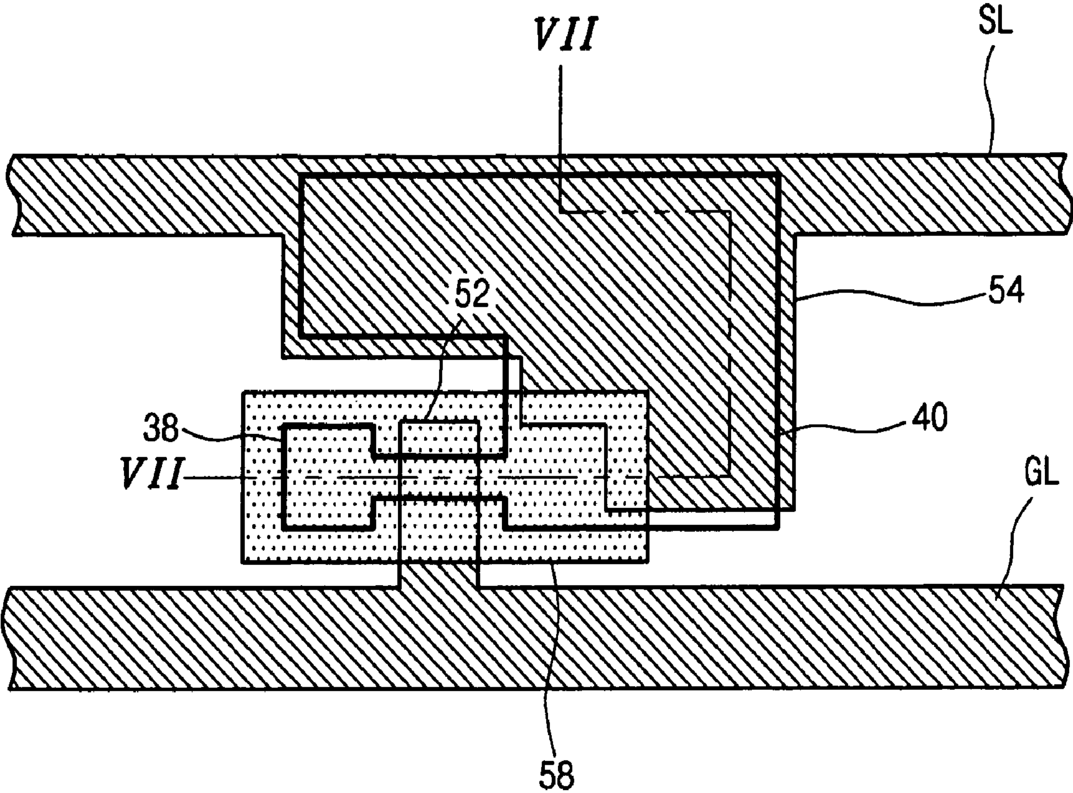


*FIG. 6F*
*Related Art*

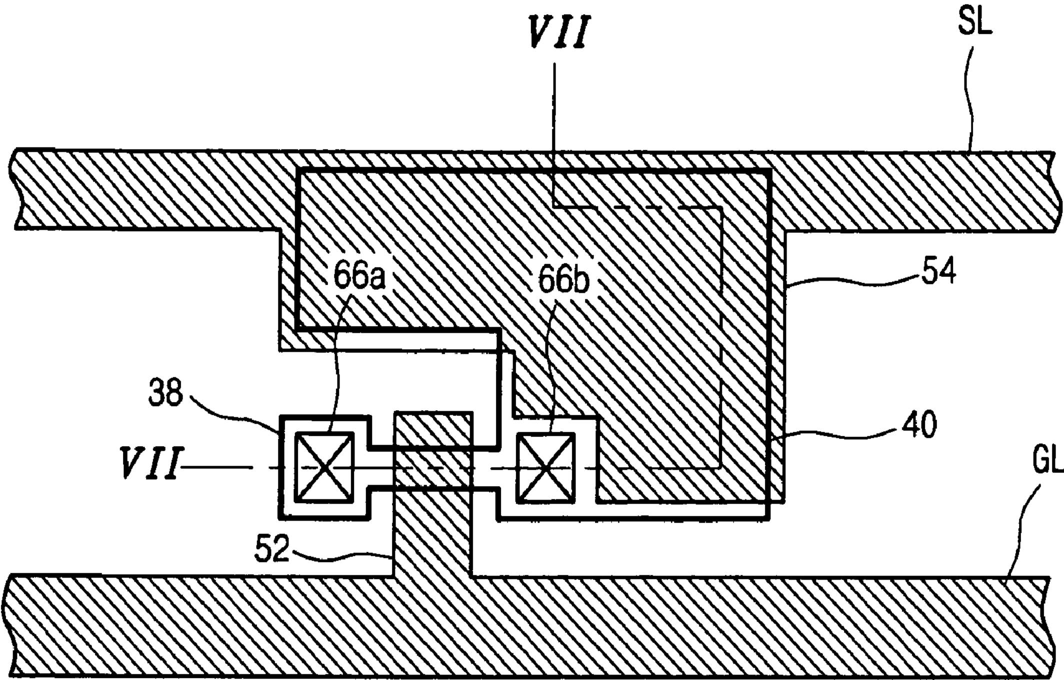


*FIG. 6G*
*Related Art*

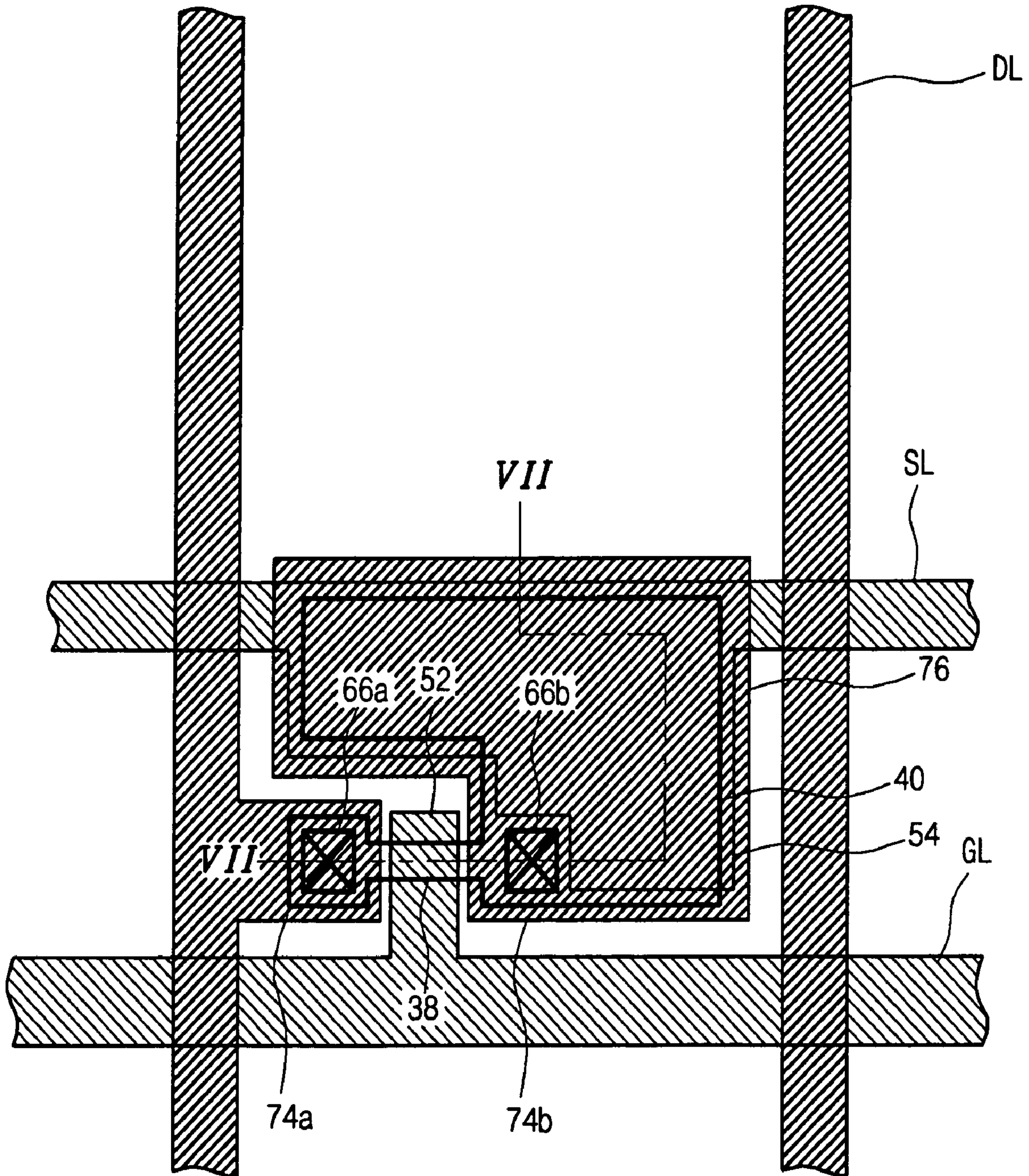


*FIG. 6H*
*Related Art*

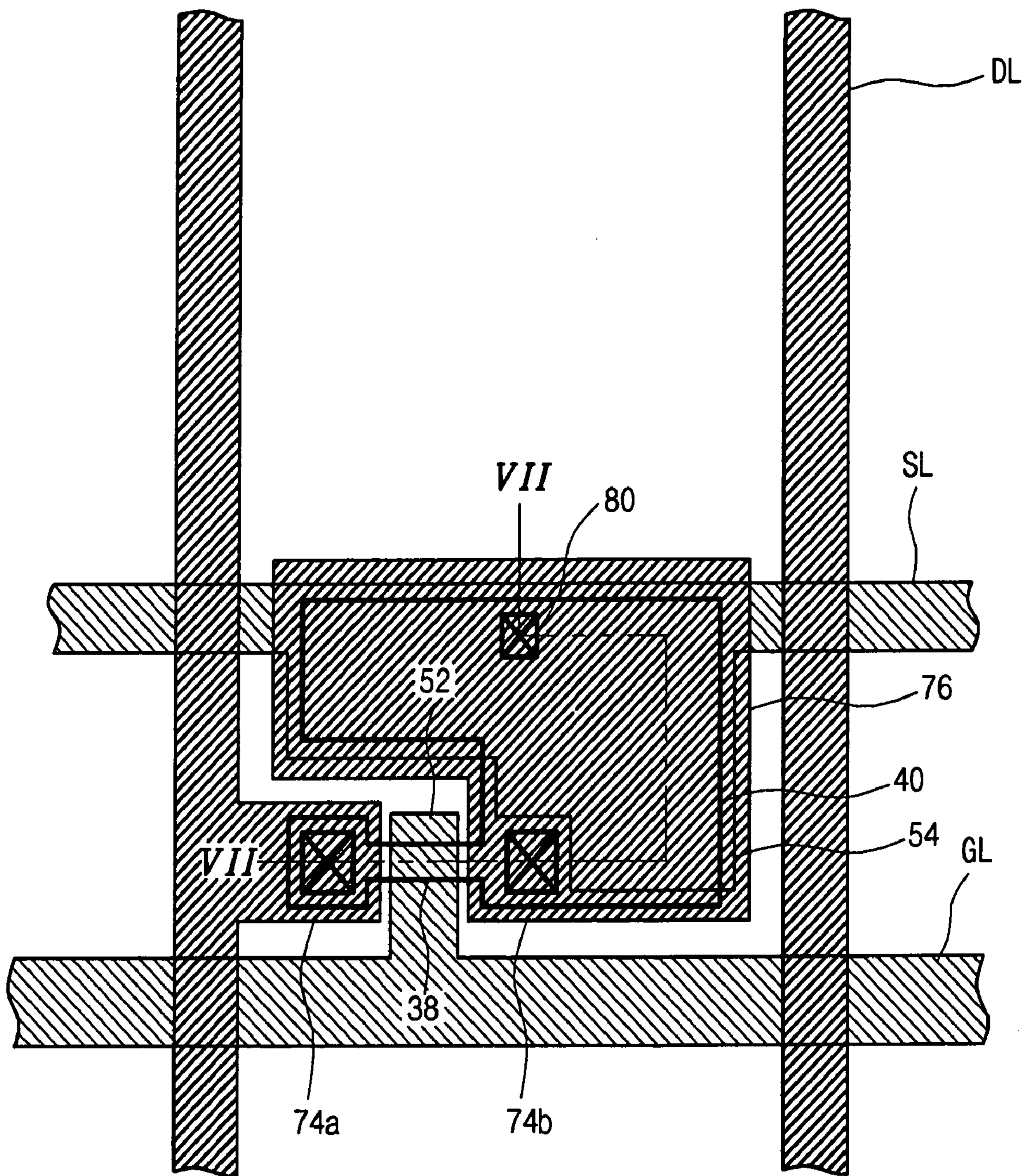


*FIG. 6I*
*Related Art*

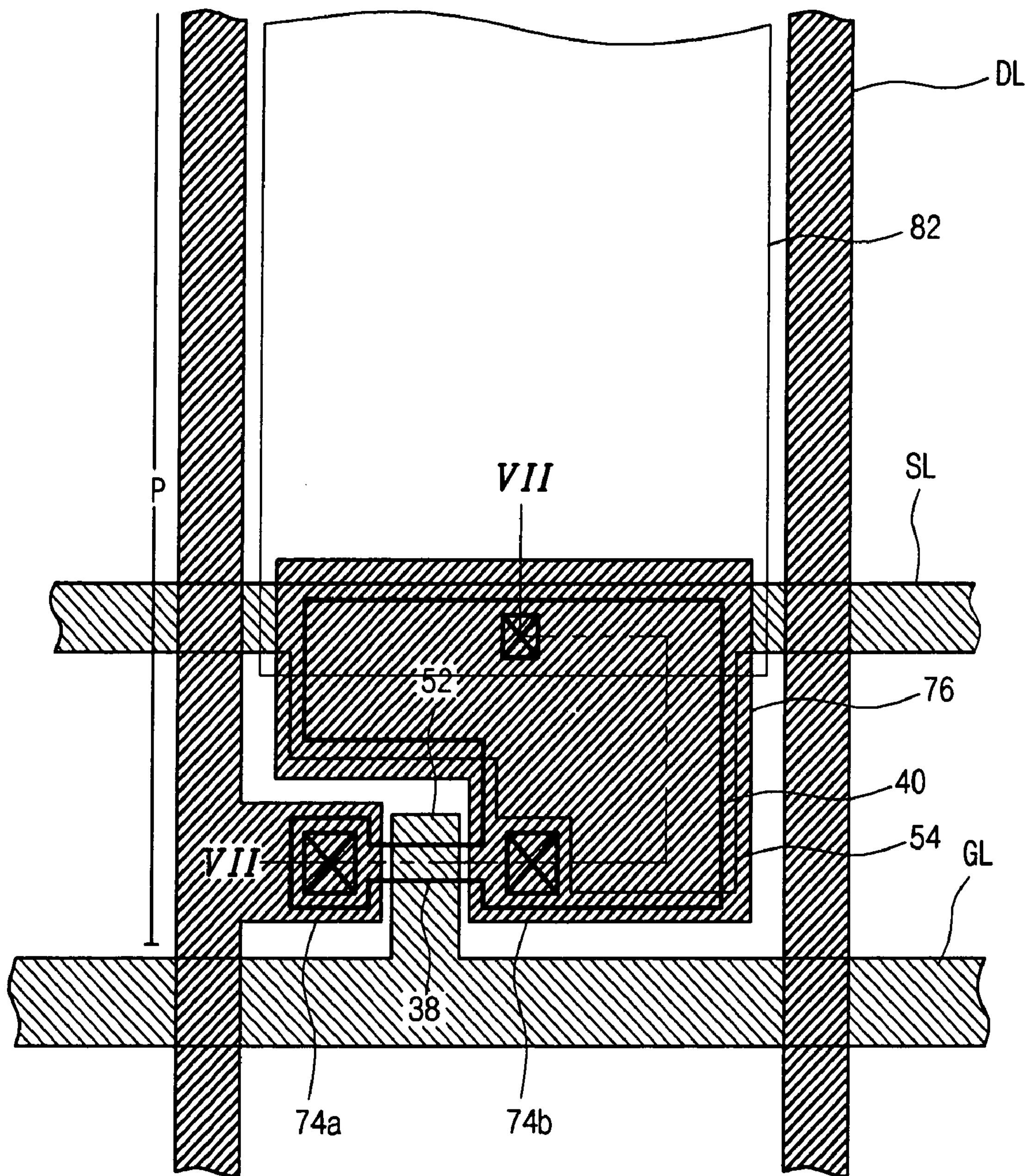


*FIG. 7A*
*Related Art*

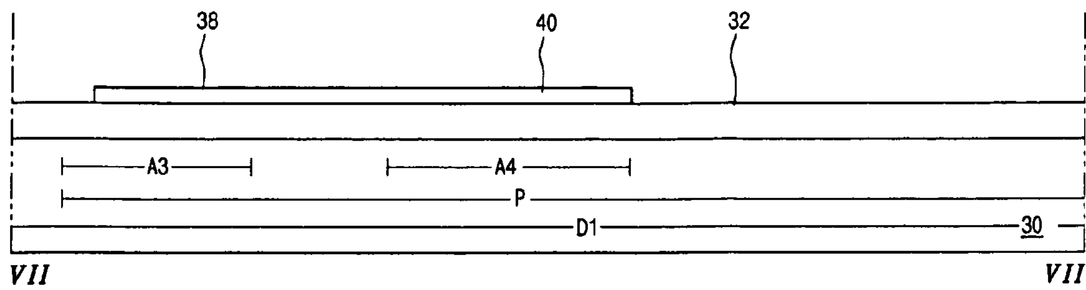



*FIG. 7B*
*Related Art*

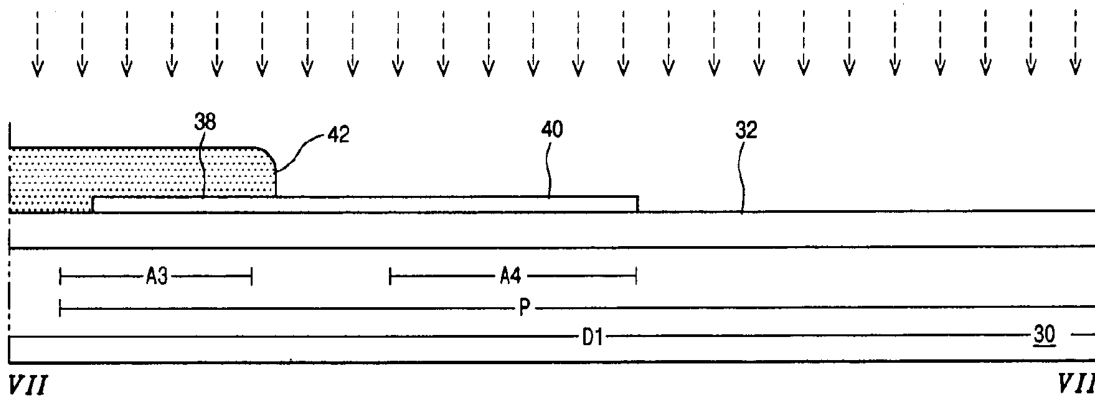


*FIG. 7C*
*Related Art*

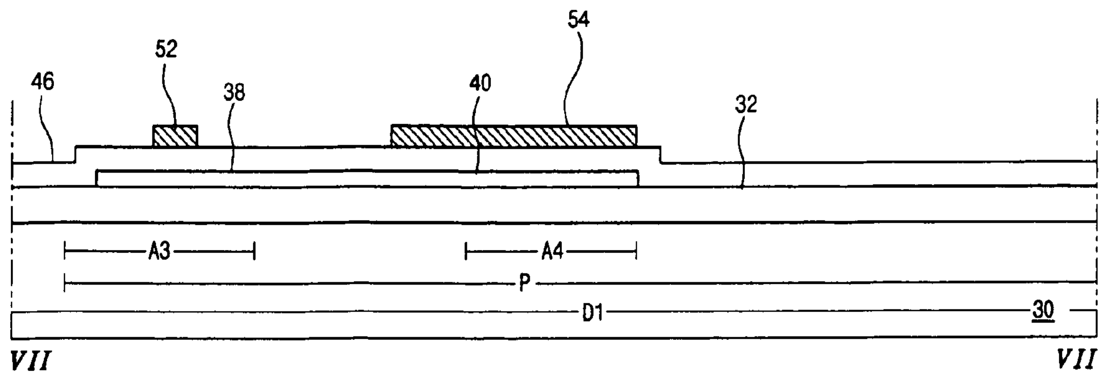
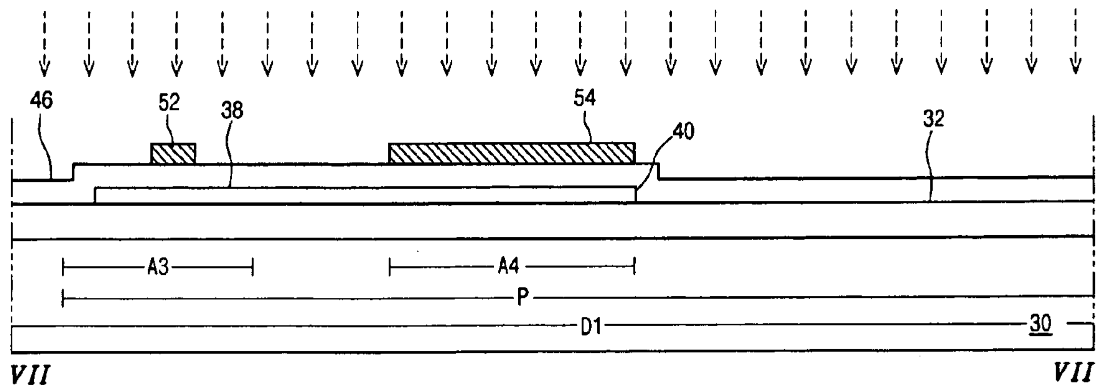
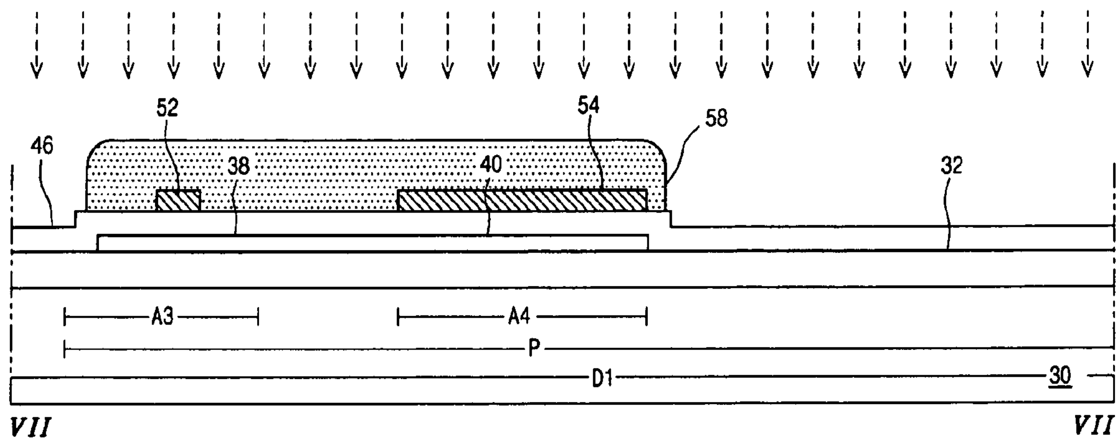



*FIG. 7D*
*Related Art*



## *FIG. 7E*
## *Related Art*




## *FIG. 7F*
## *Related Art*

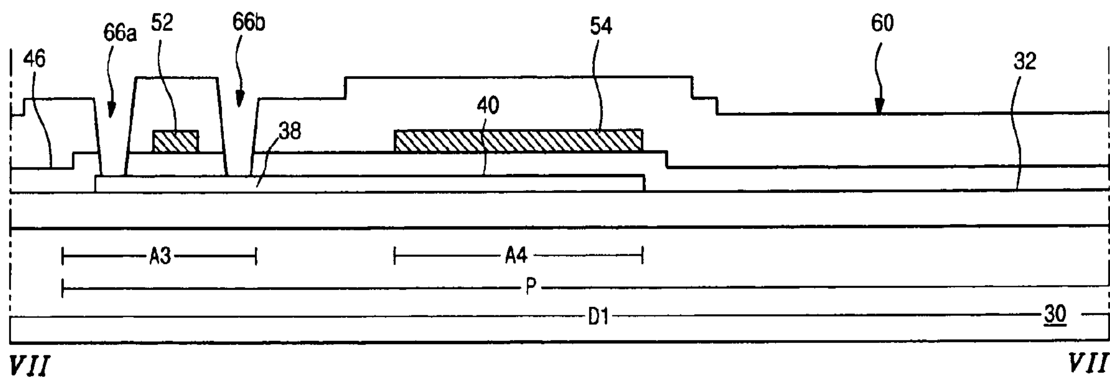


*FIG. 7G*
*Related Art*

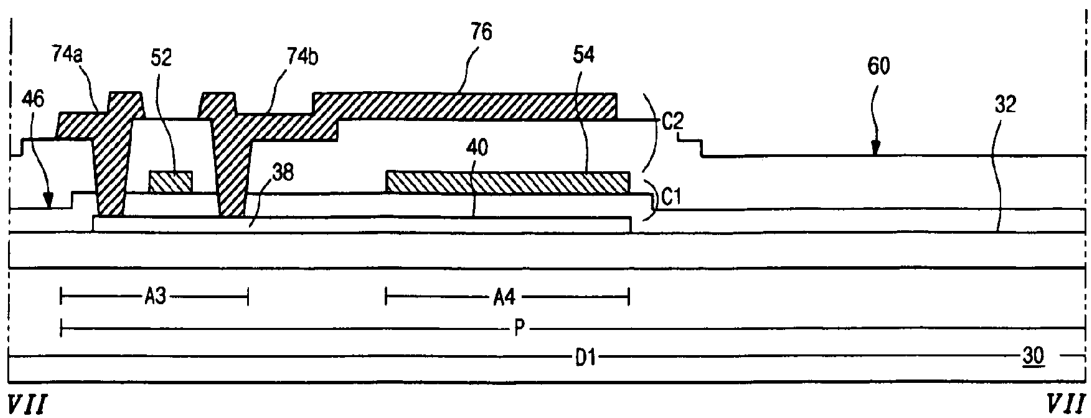



*FIG. 7H*
*Related Art*

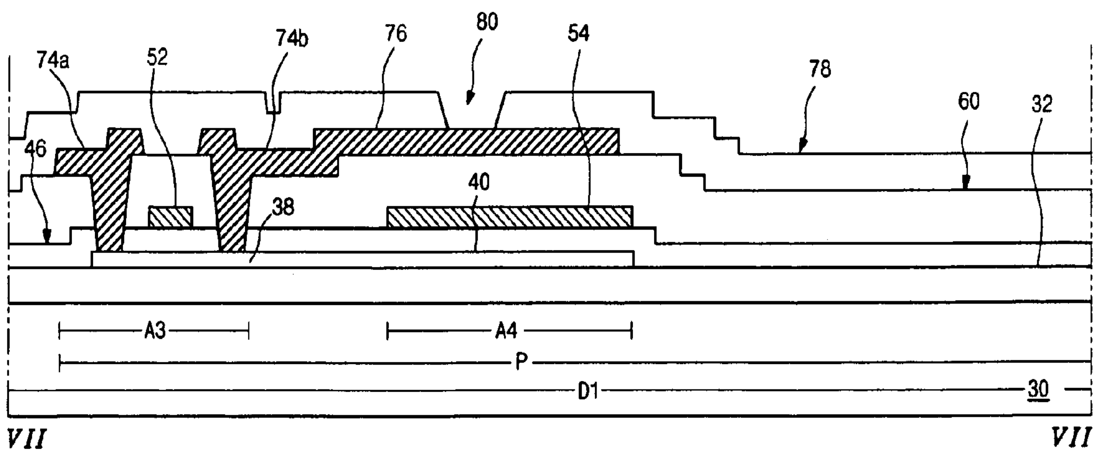


*FIG. 7I*
*Related Art*

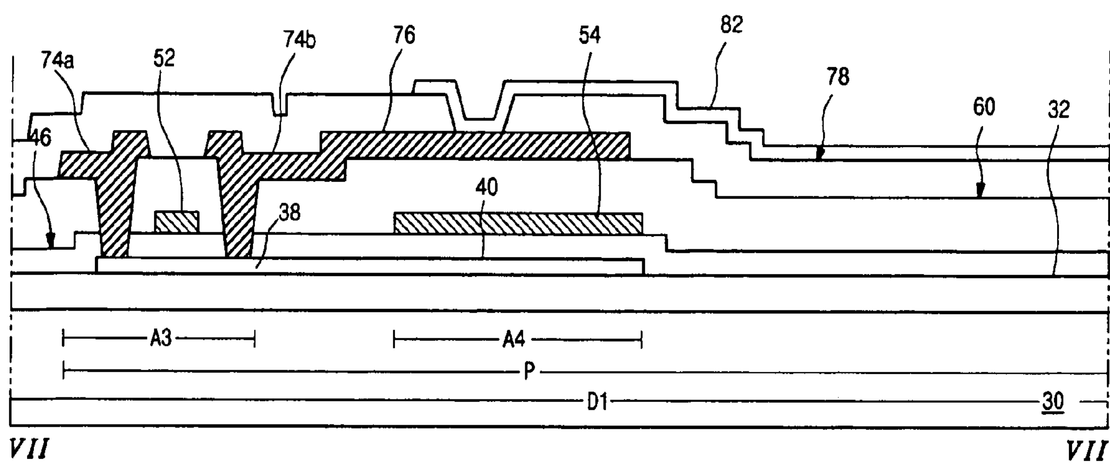


*FIG. 8*

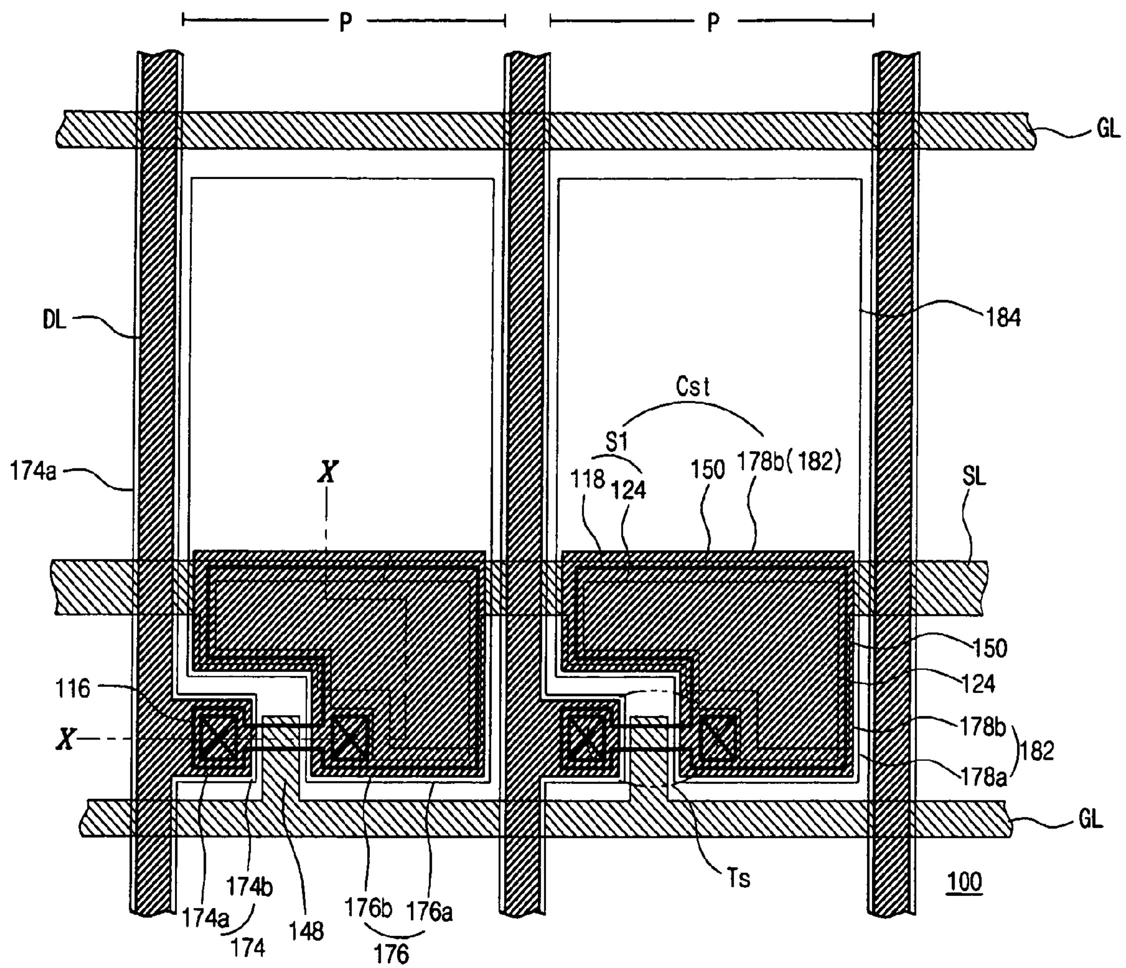


*FIG. 9*

166
166b
166a
168
168a 168b
136
170
170b
170a
172
172a 172b
146
114
112
152b
152
152a
128
102
T(p)
T(n)
D2(DC)
100

*FIG. 10*

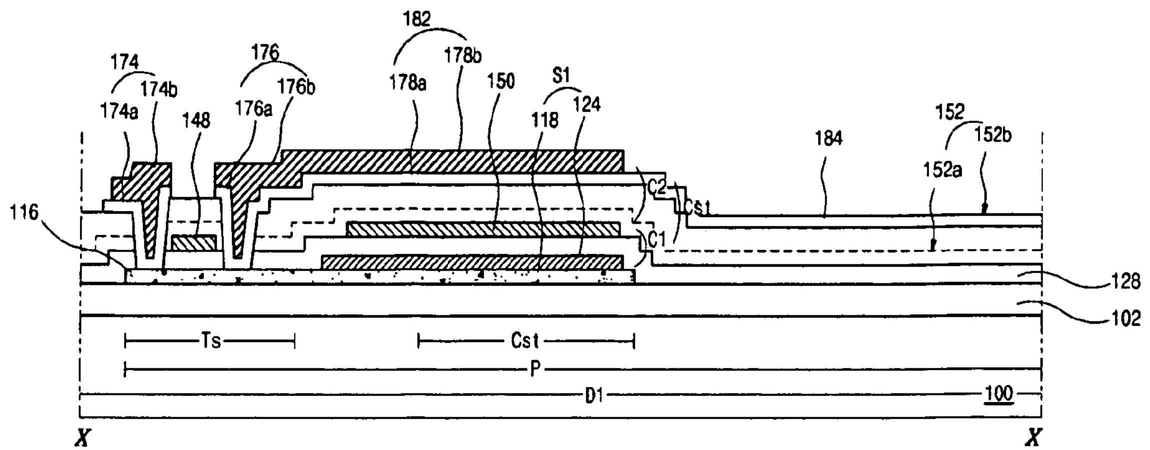



*FIG. 11A*

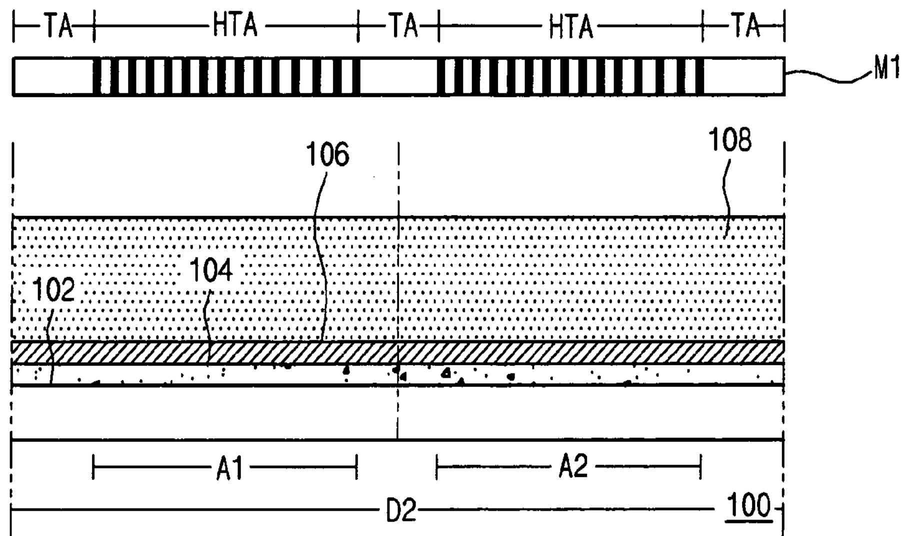


*FIG. 11B*

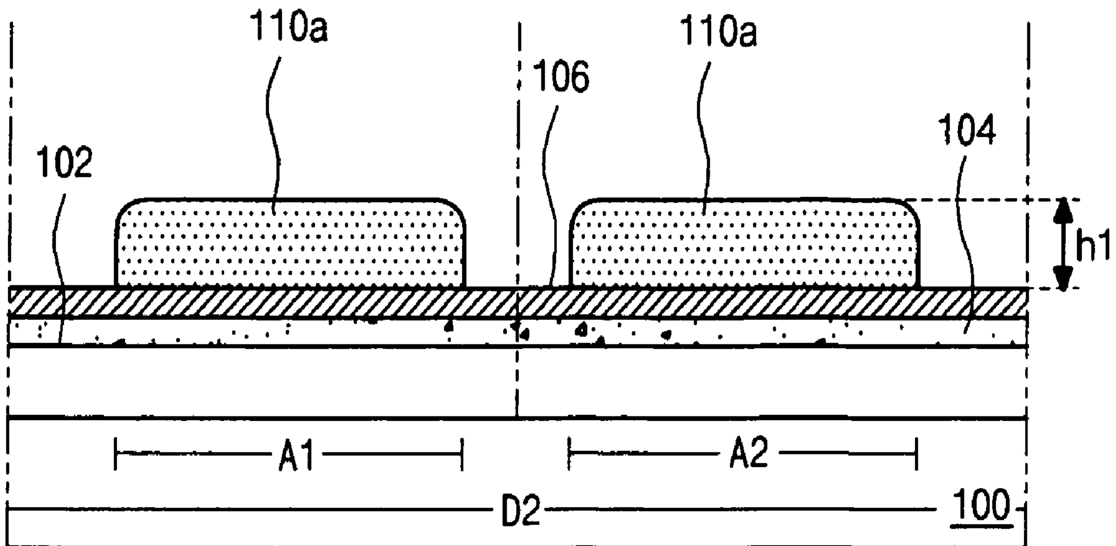
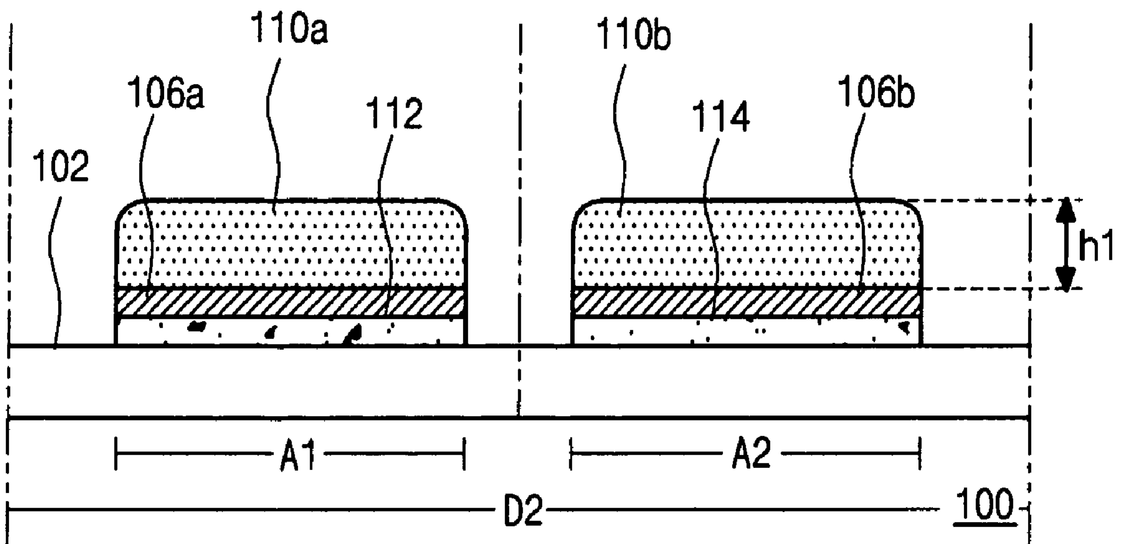
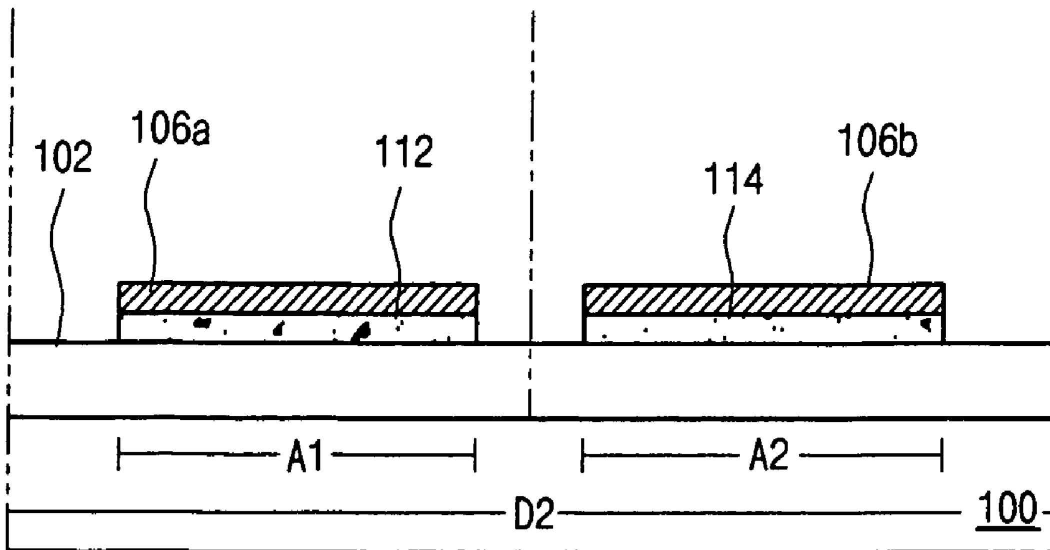


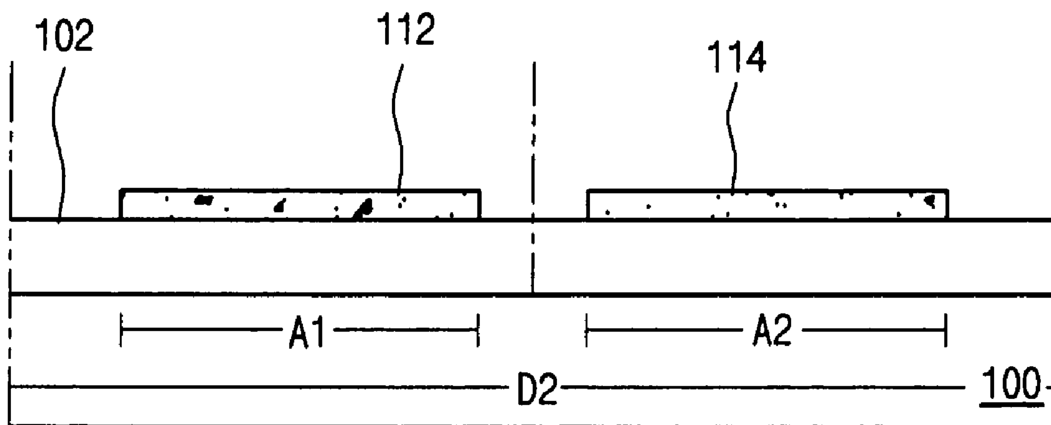

*FIG. 11C*



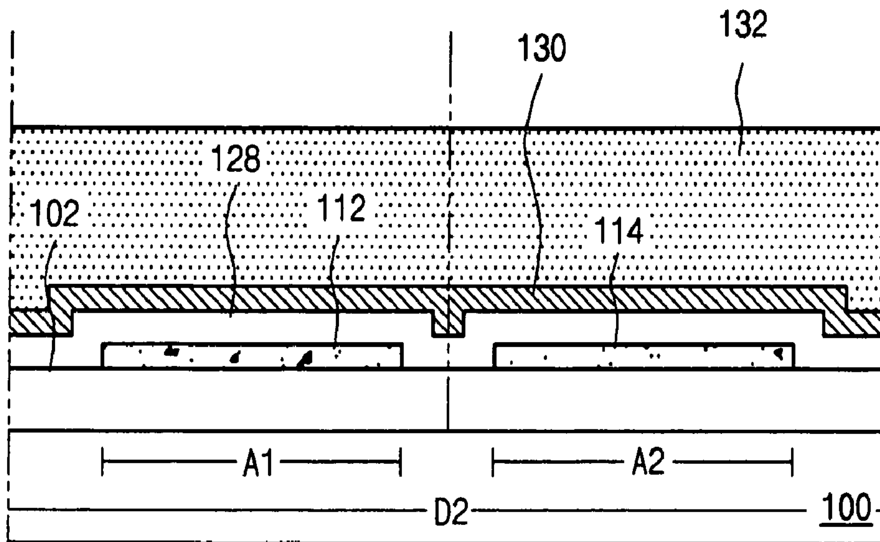
## FIG. 11D



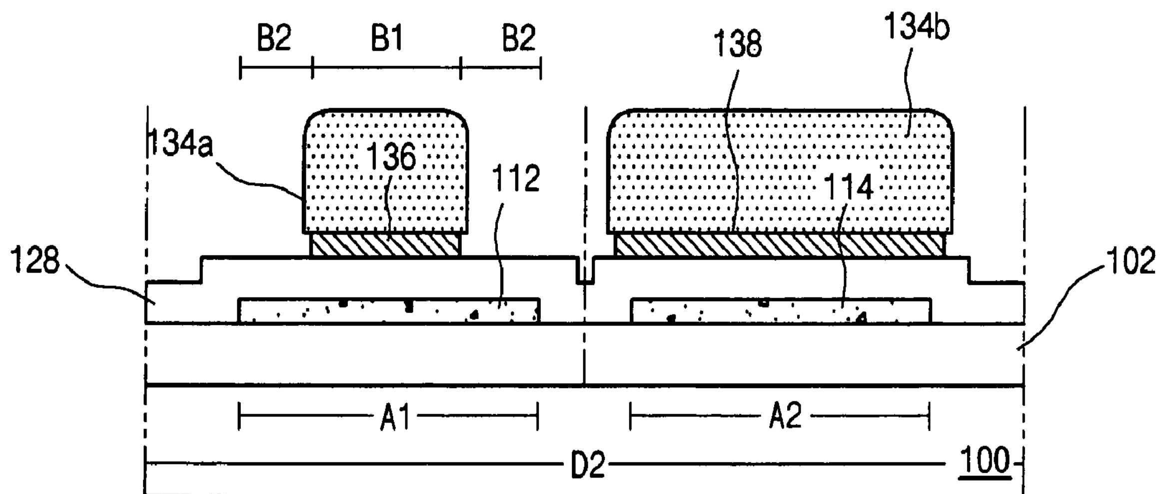

## FIG. 11E



## FIG. 11F

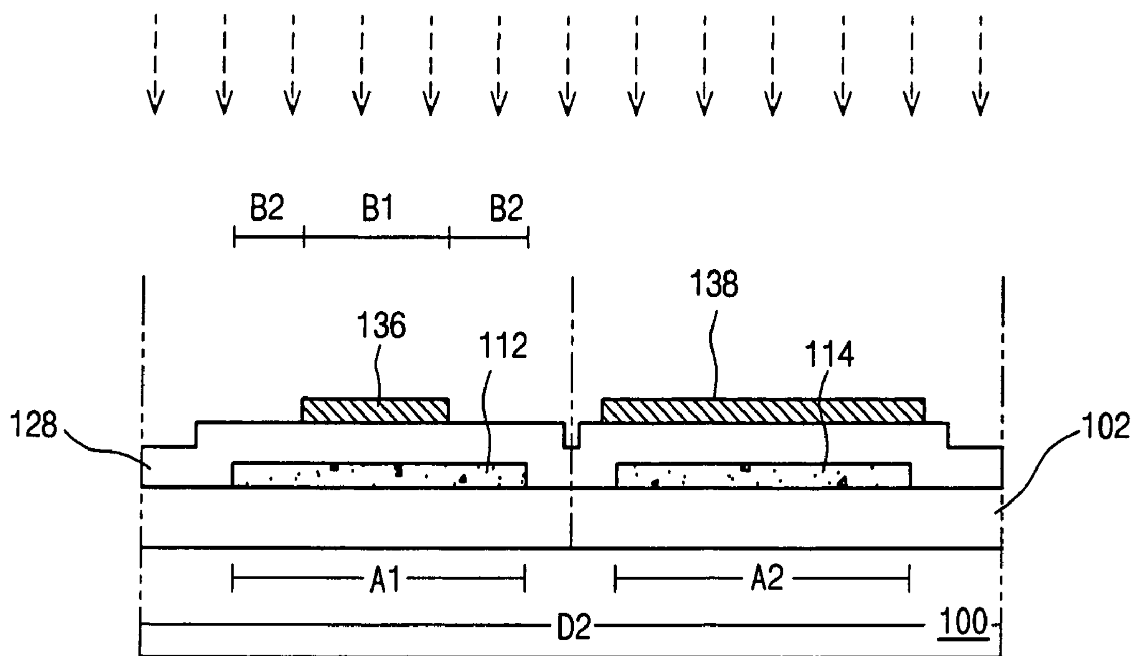



## FIG. 11G



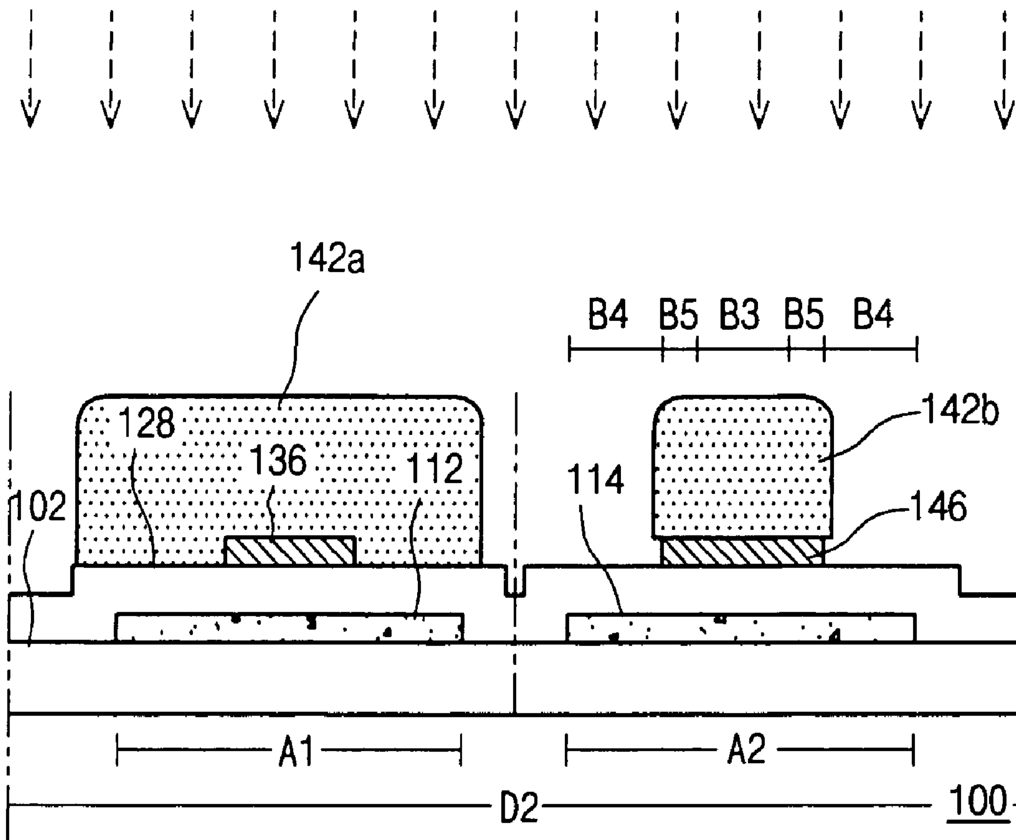
# FIG. 11H

doping with high concentration p-type impurities



# FIG. 11I

doping with high concentration n-type impurities




# FIG. 11J

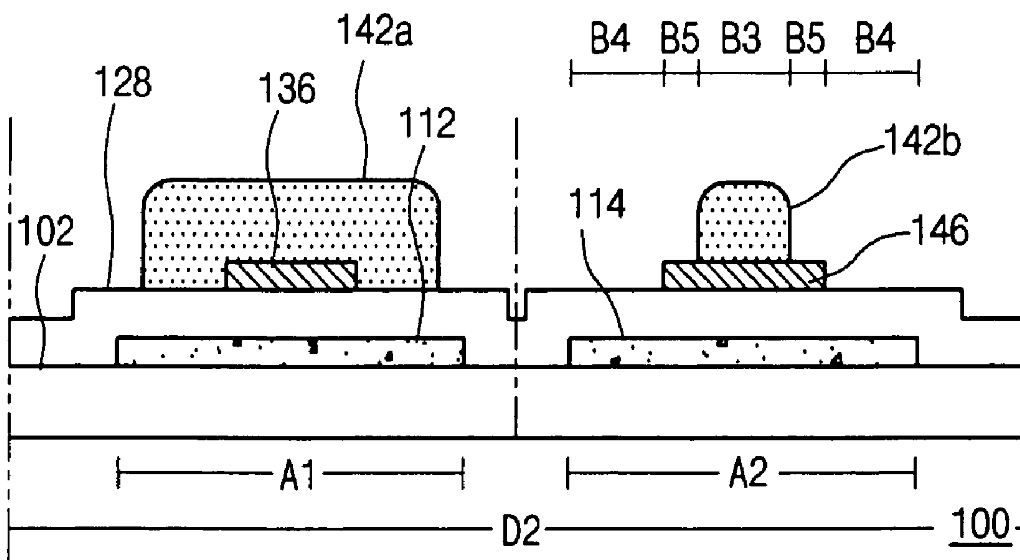


*FIG. 11K*

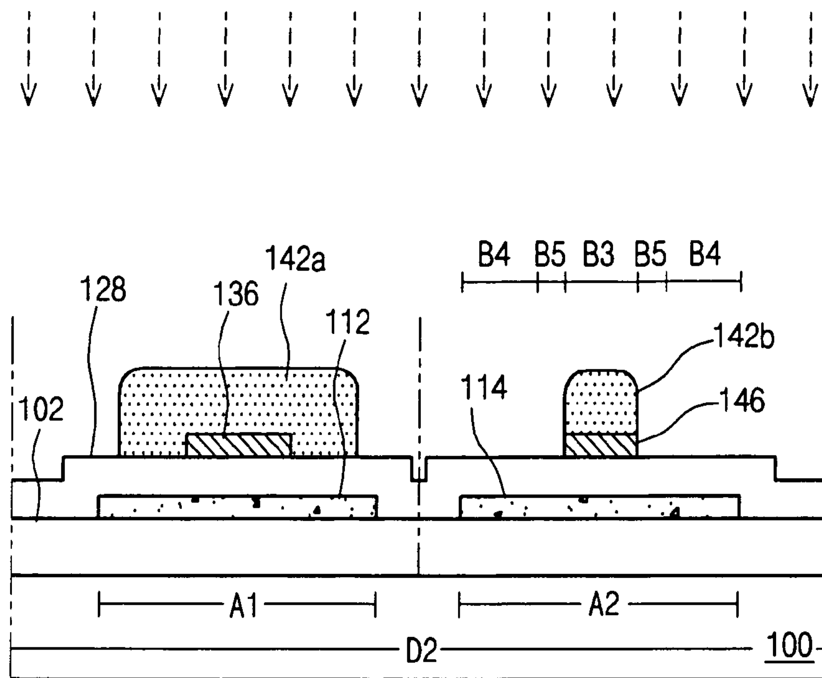



*FIG. 11L*

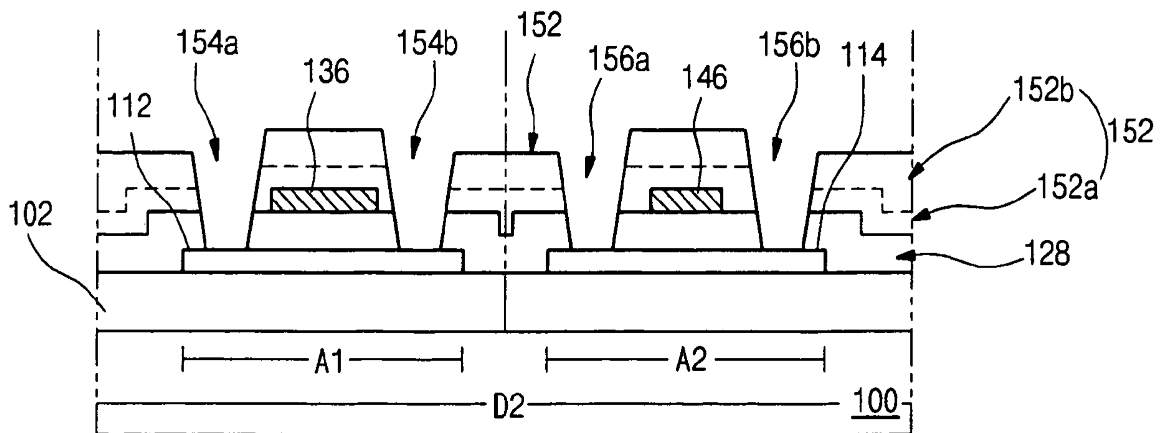


FIG. 11M



FIG. 11N

FIG. 11O

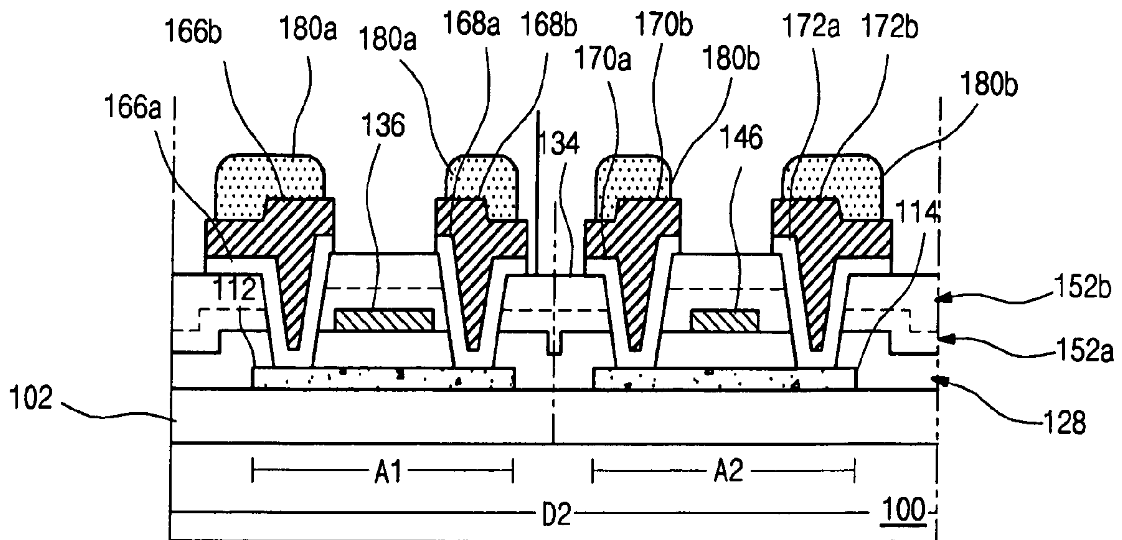



FIG. 11P

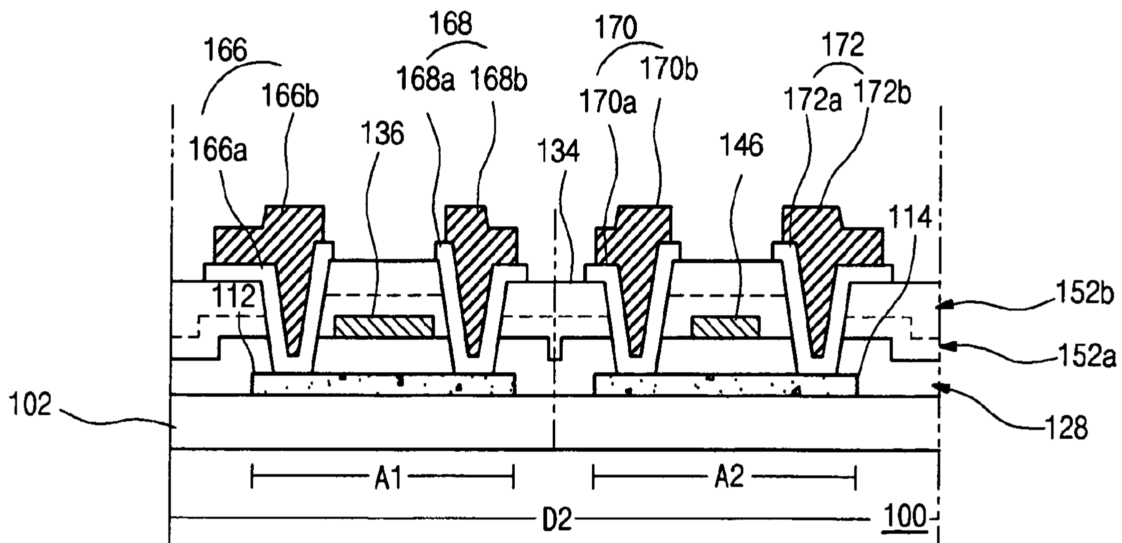


*FIG. 12A*

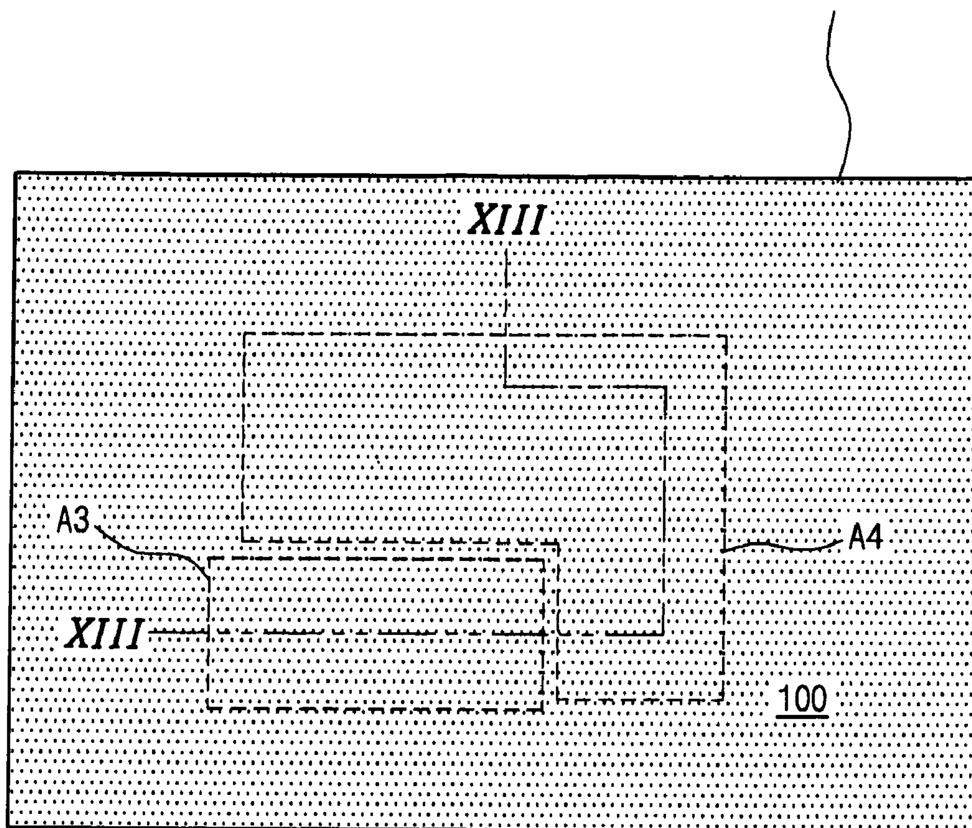


*FIG. 12B*

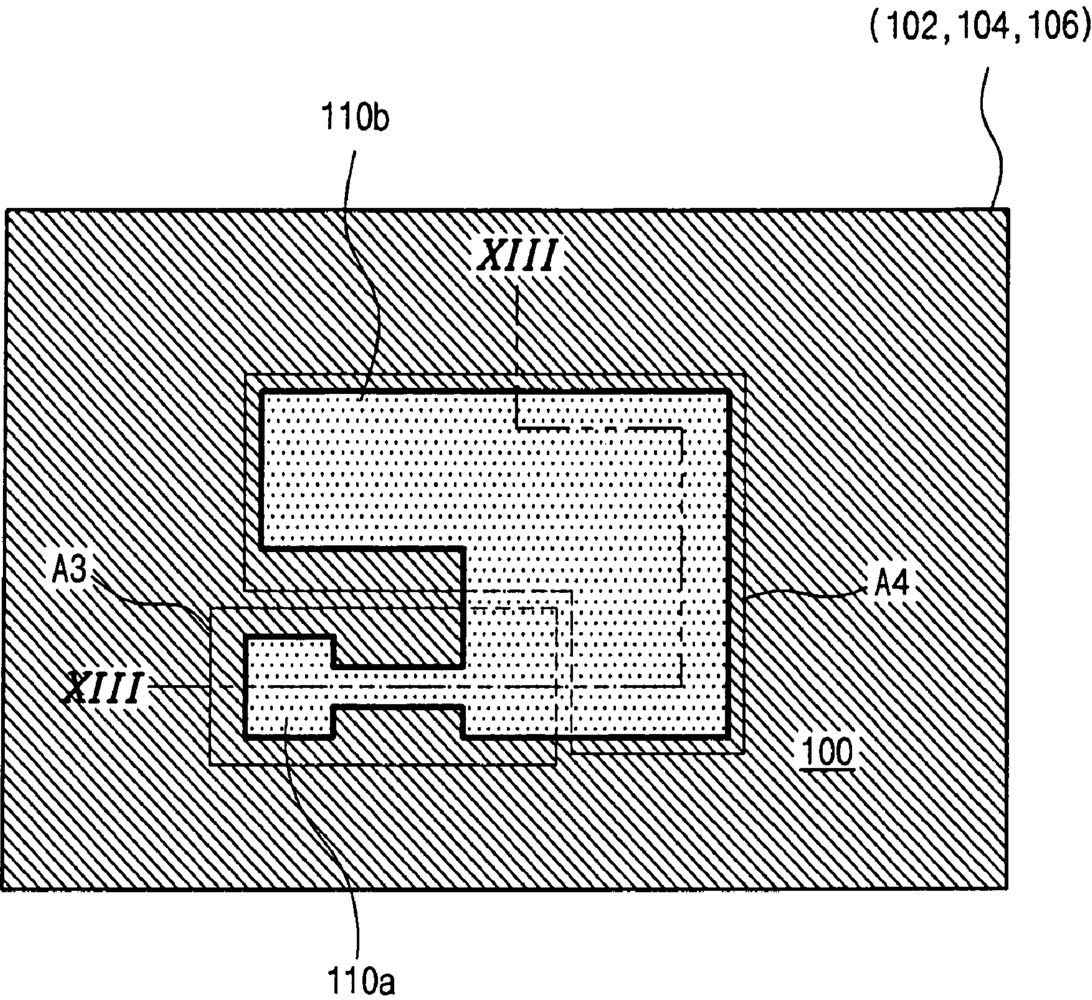


*FIG. 12C*

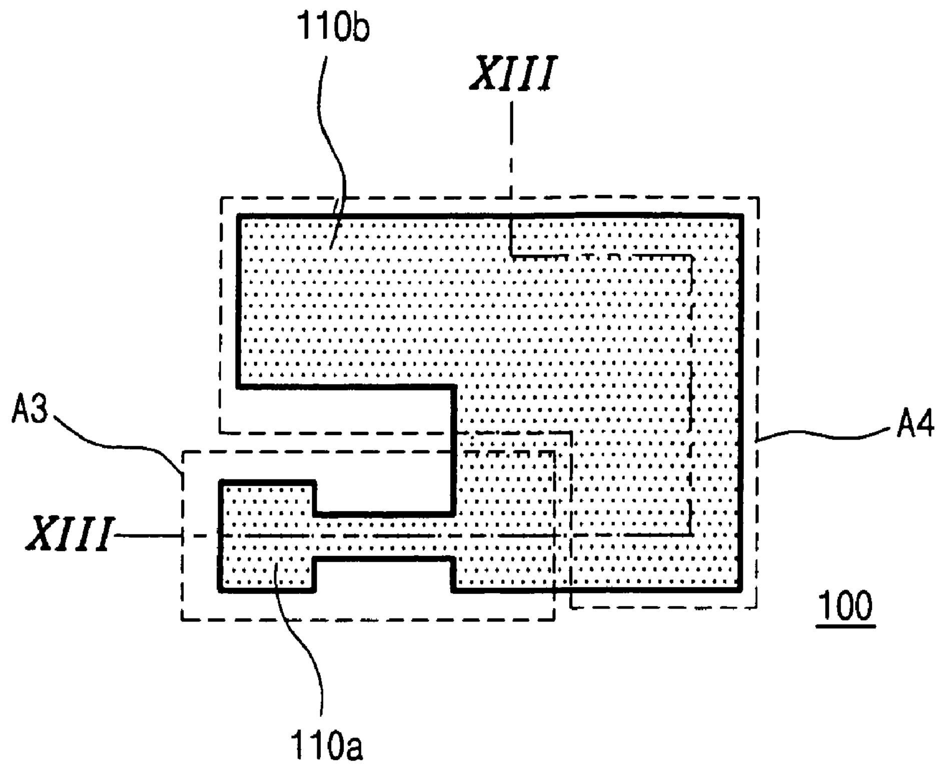



*FIG. 12D*

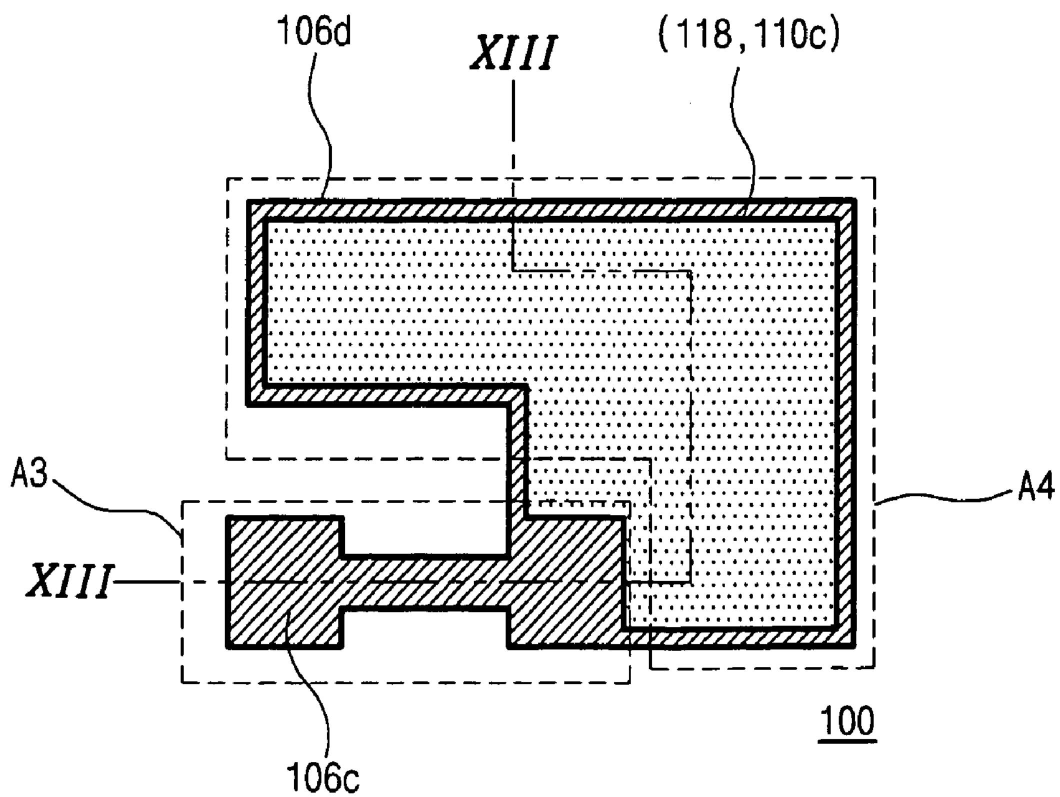


FIG. 12E

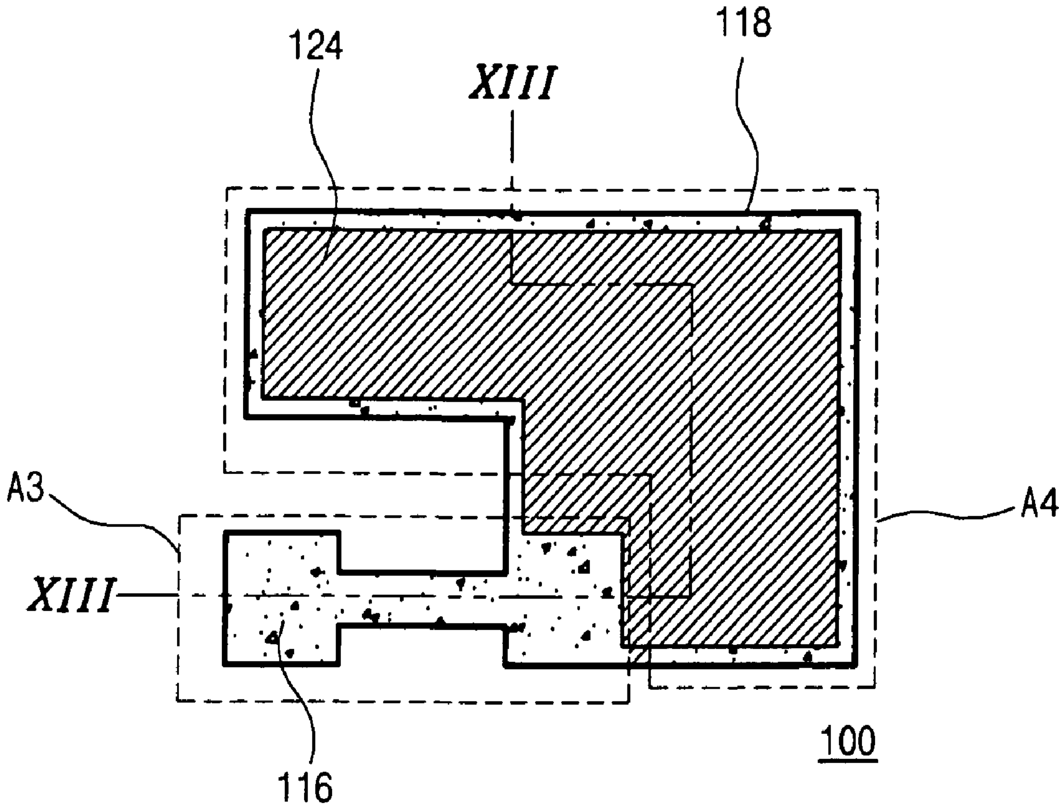


*FIG. 12F*

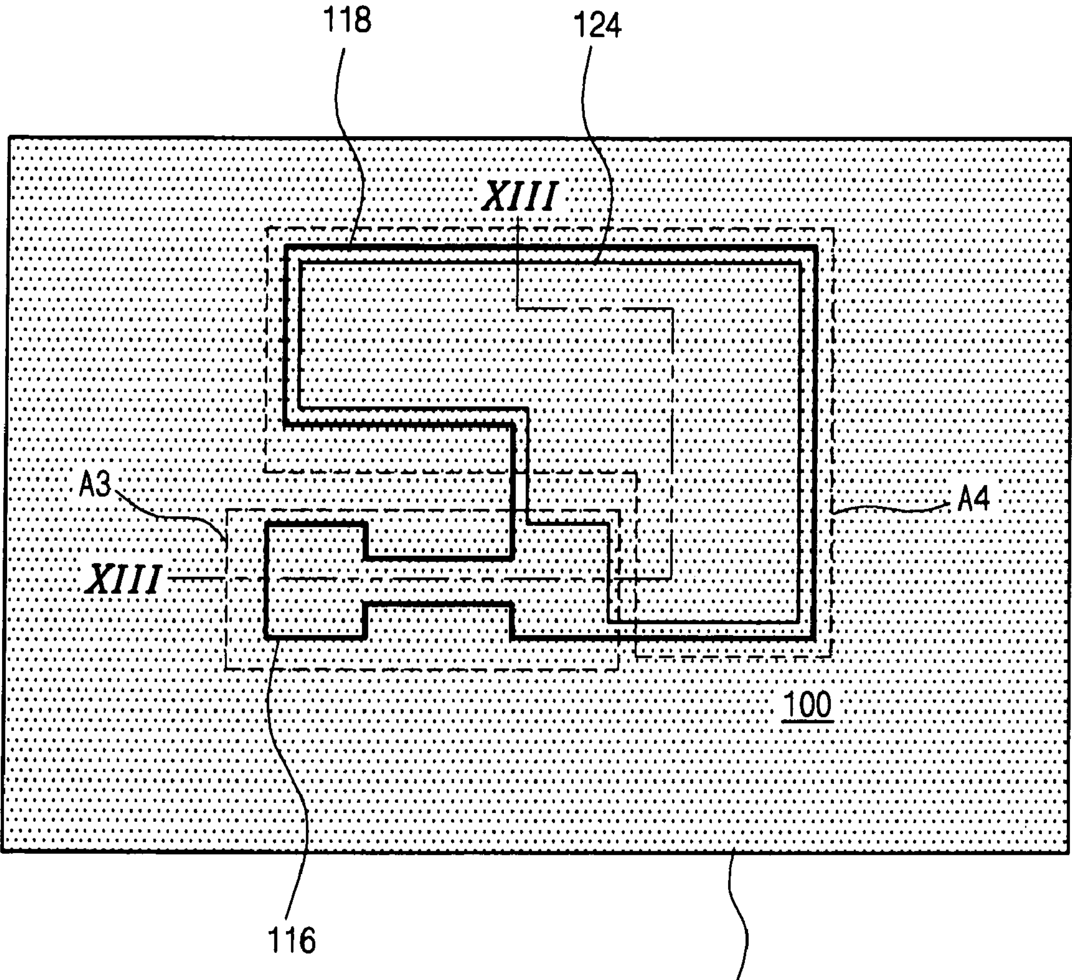


*FIG. 12G*

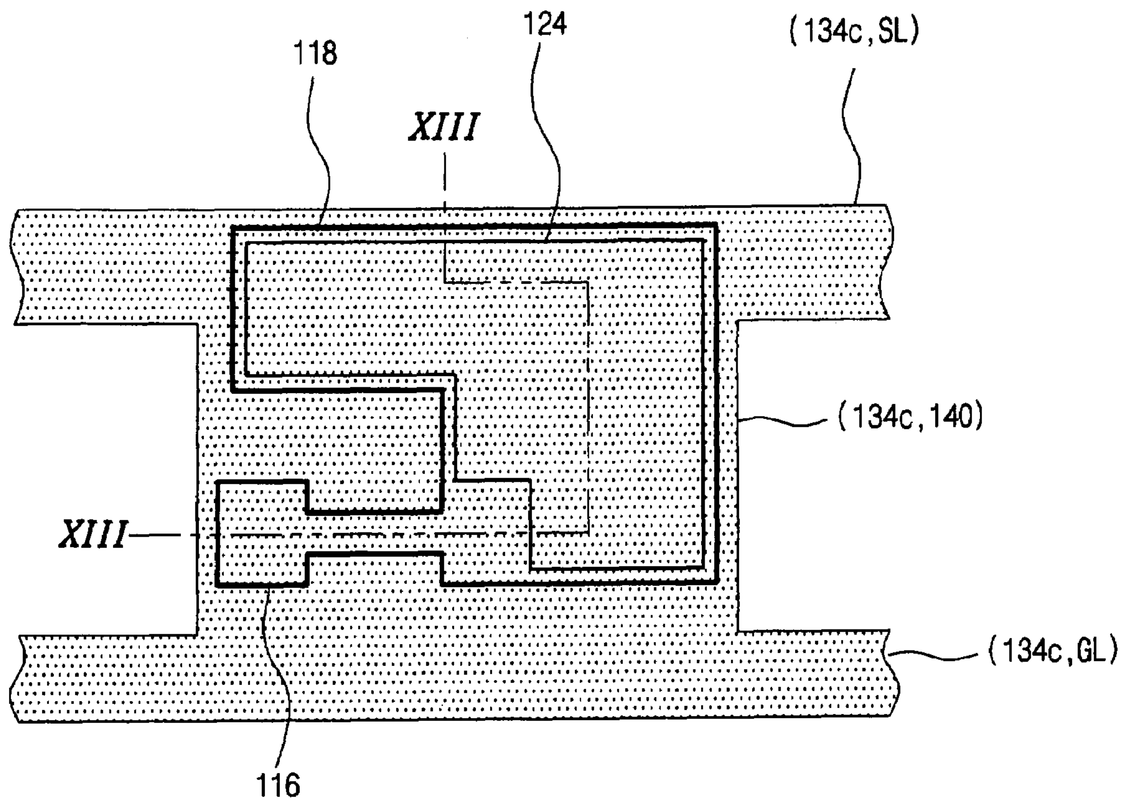


FIG. 12H

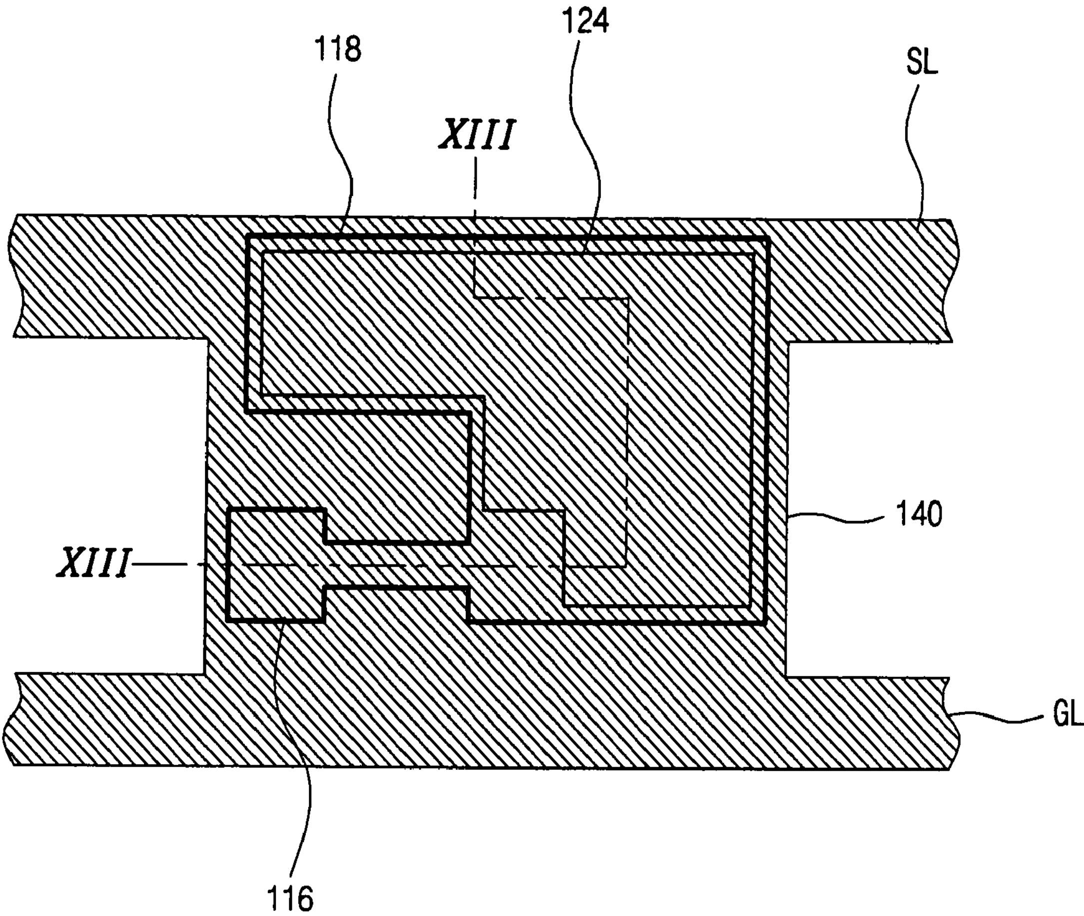


*FIG. 12I*

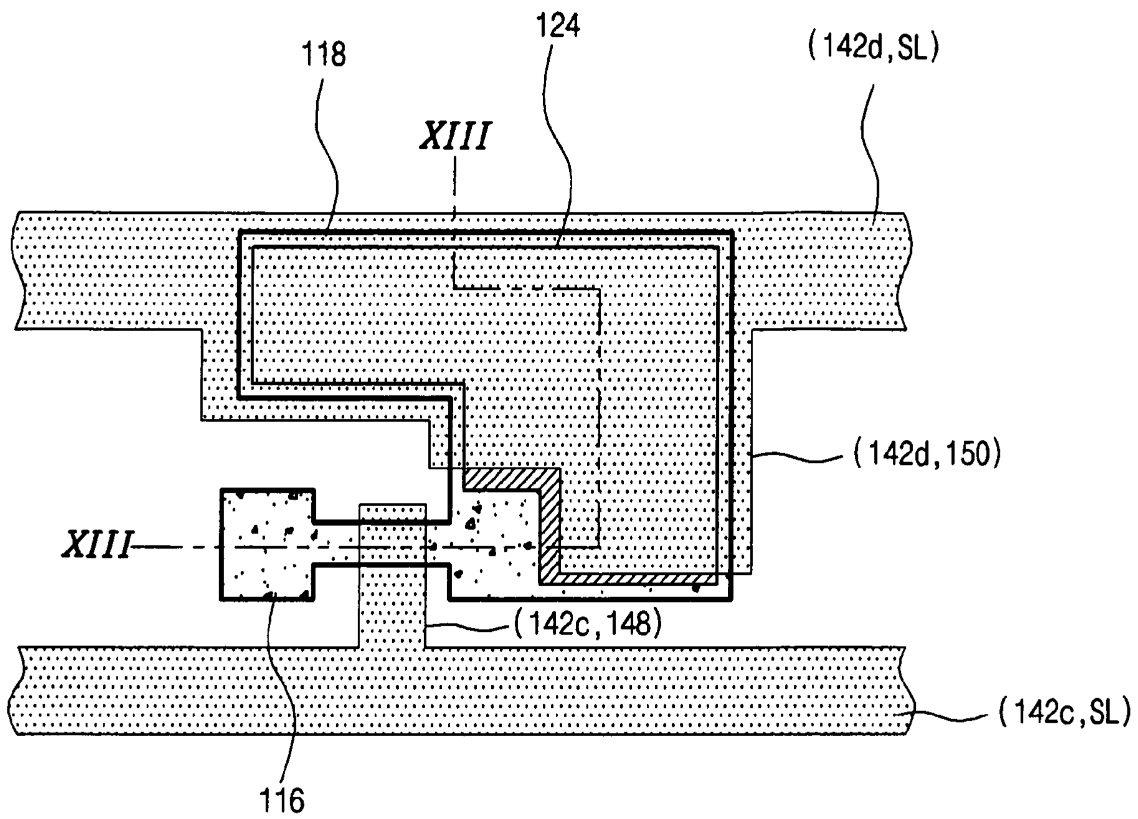


*FIG. 12J*

*FIG. 12K*

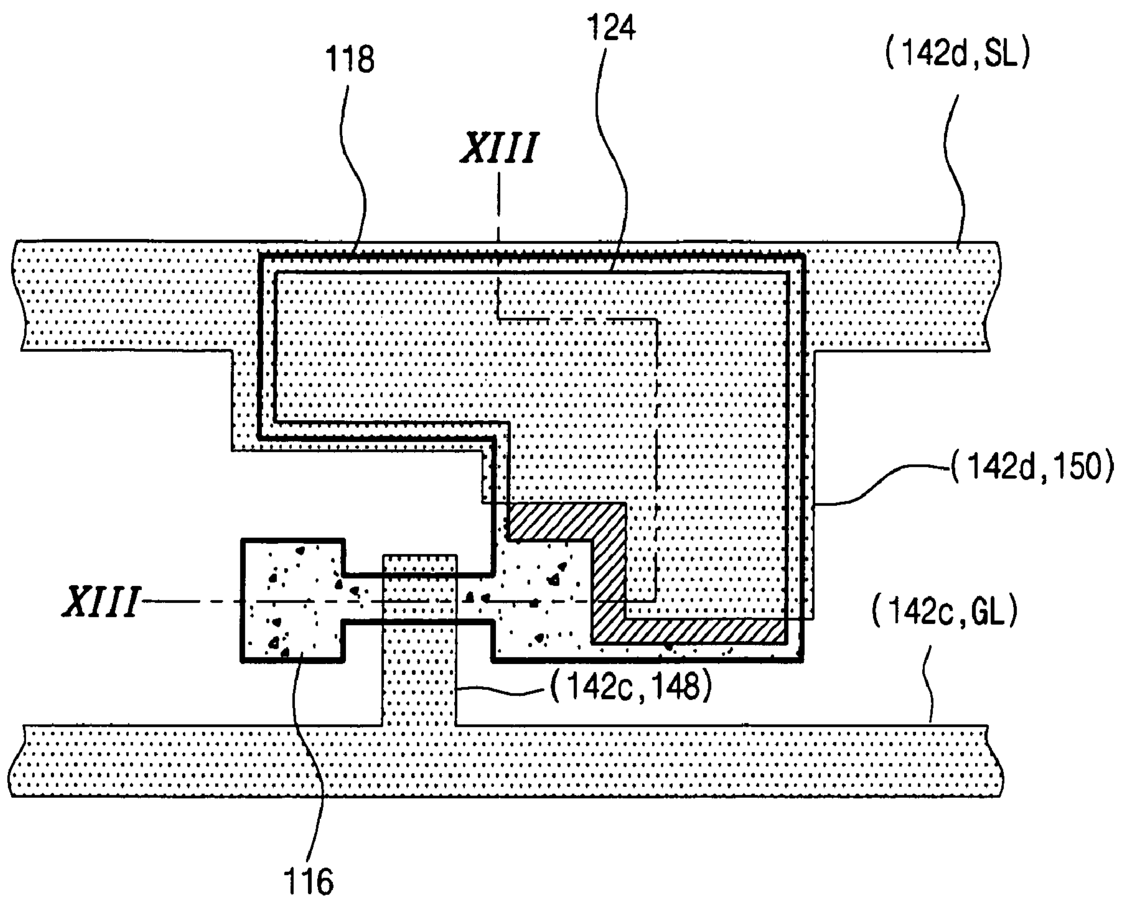


FIG. 12L

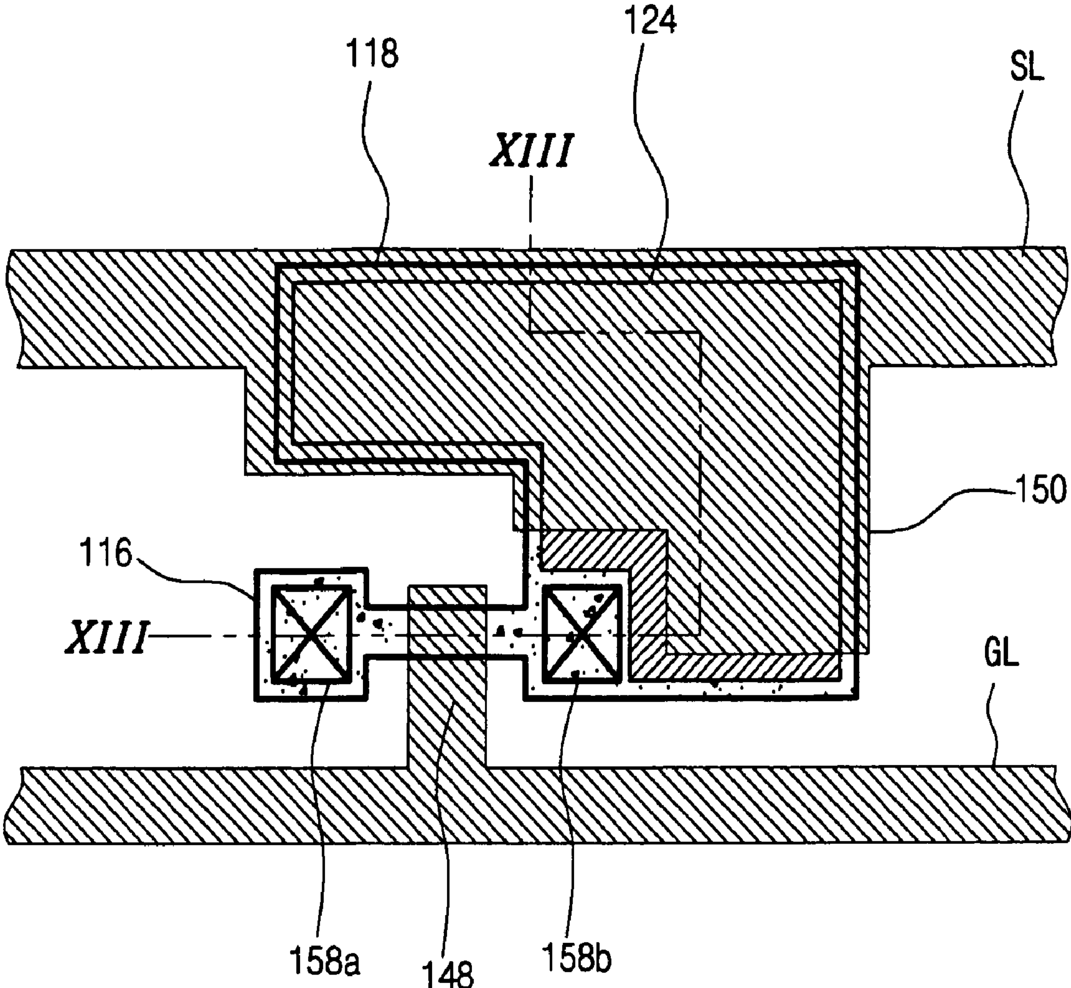


FIG. 12M

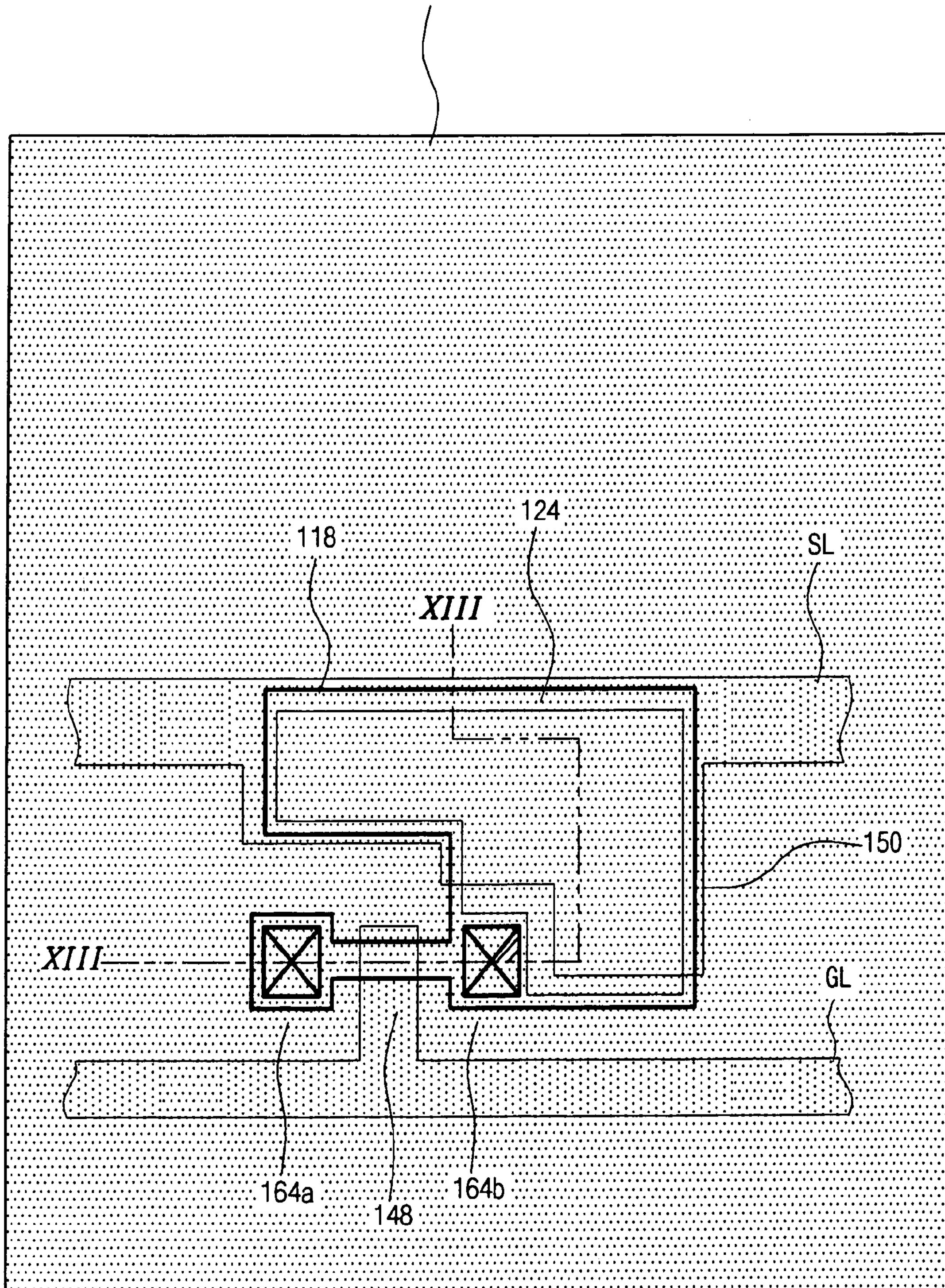


*FIG. 12N*

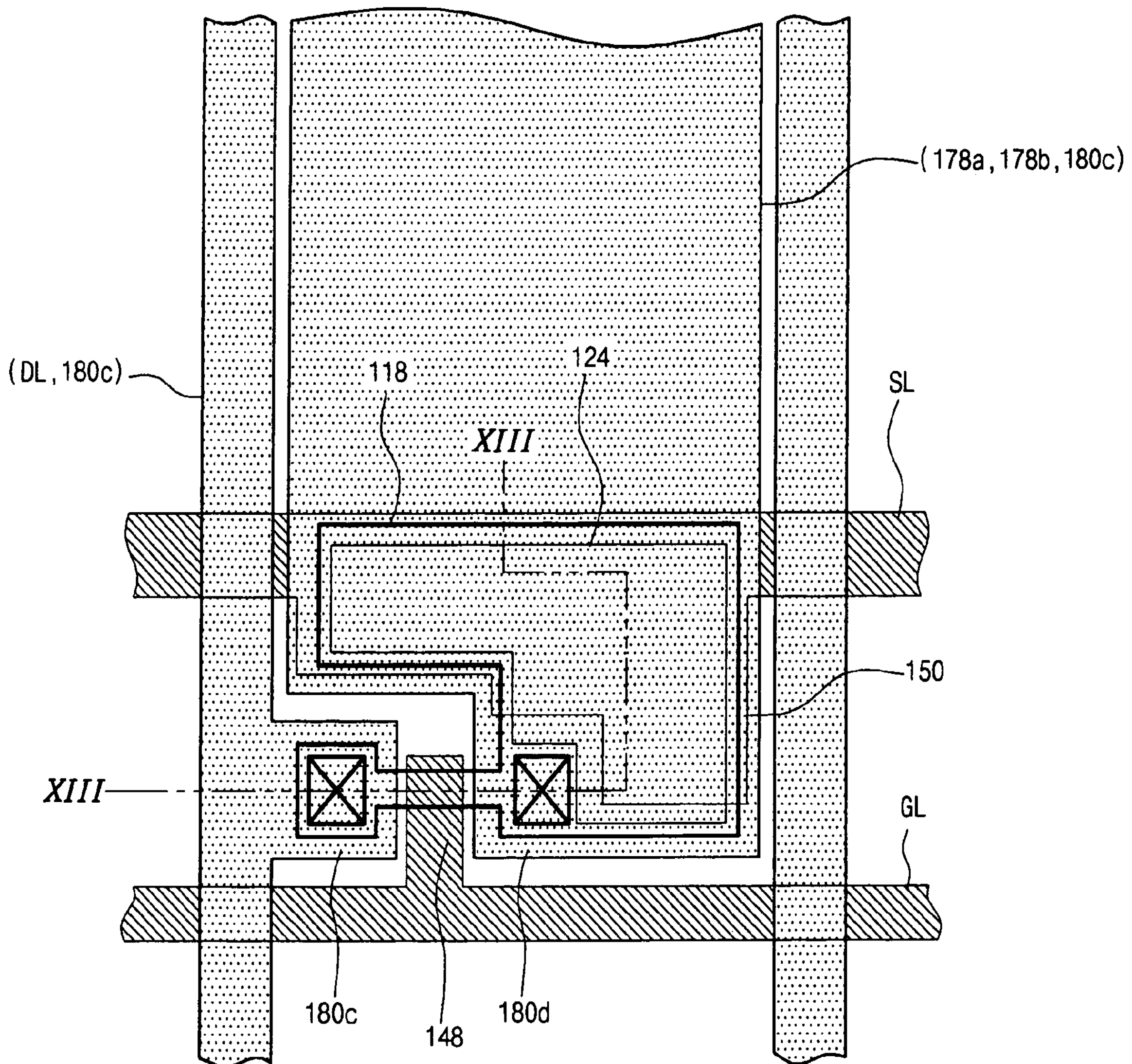


*FIG. 12O*

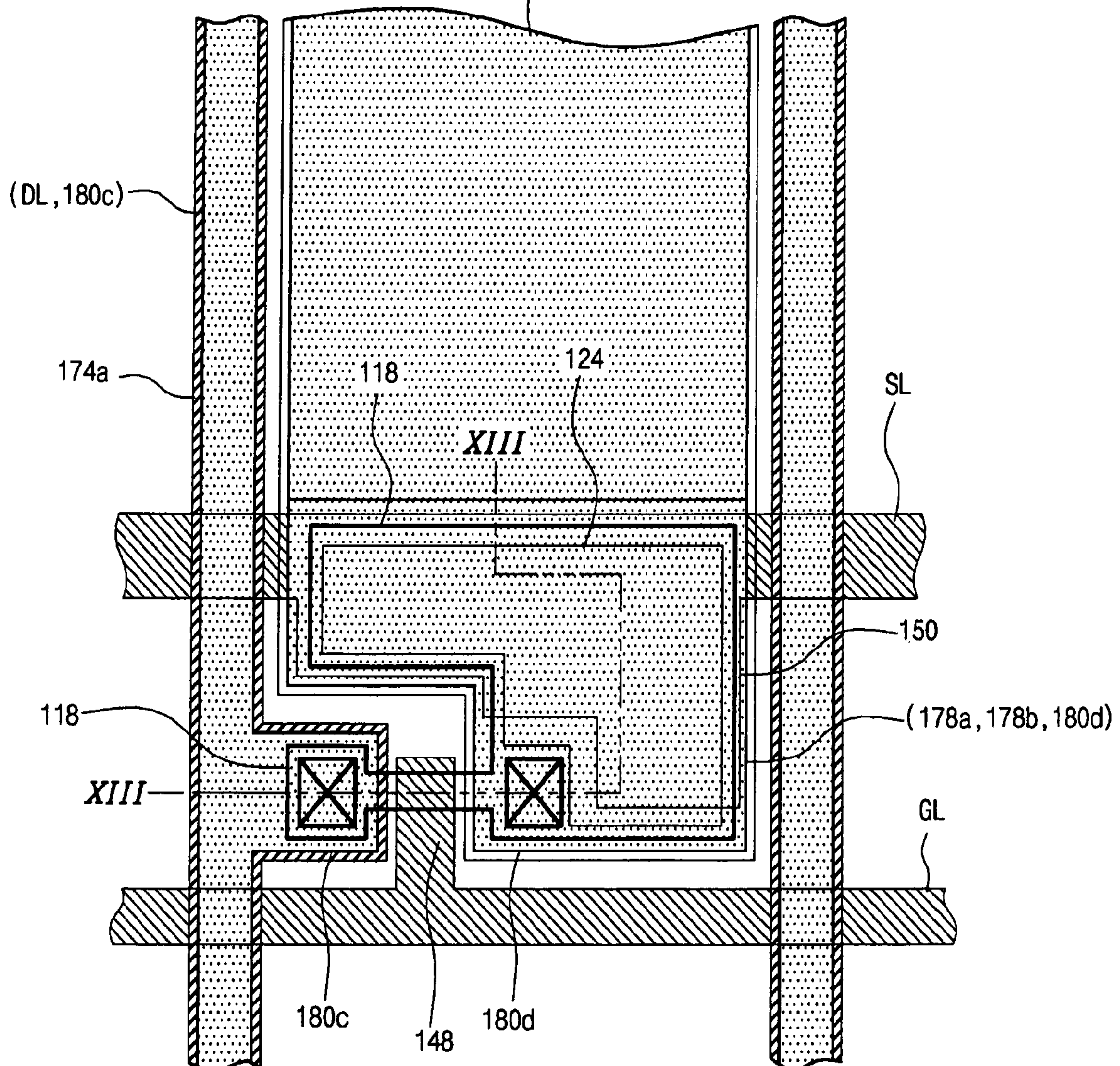
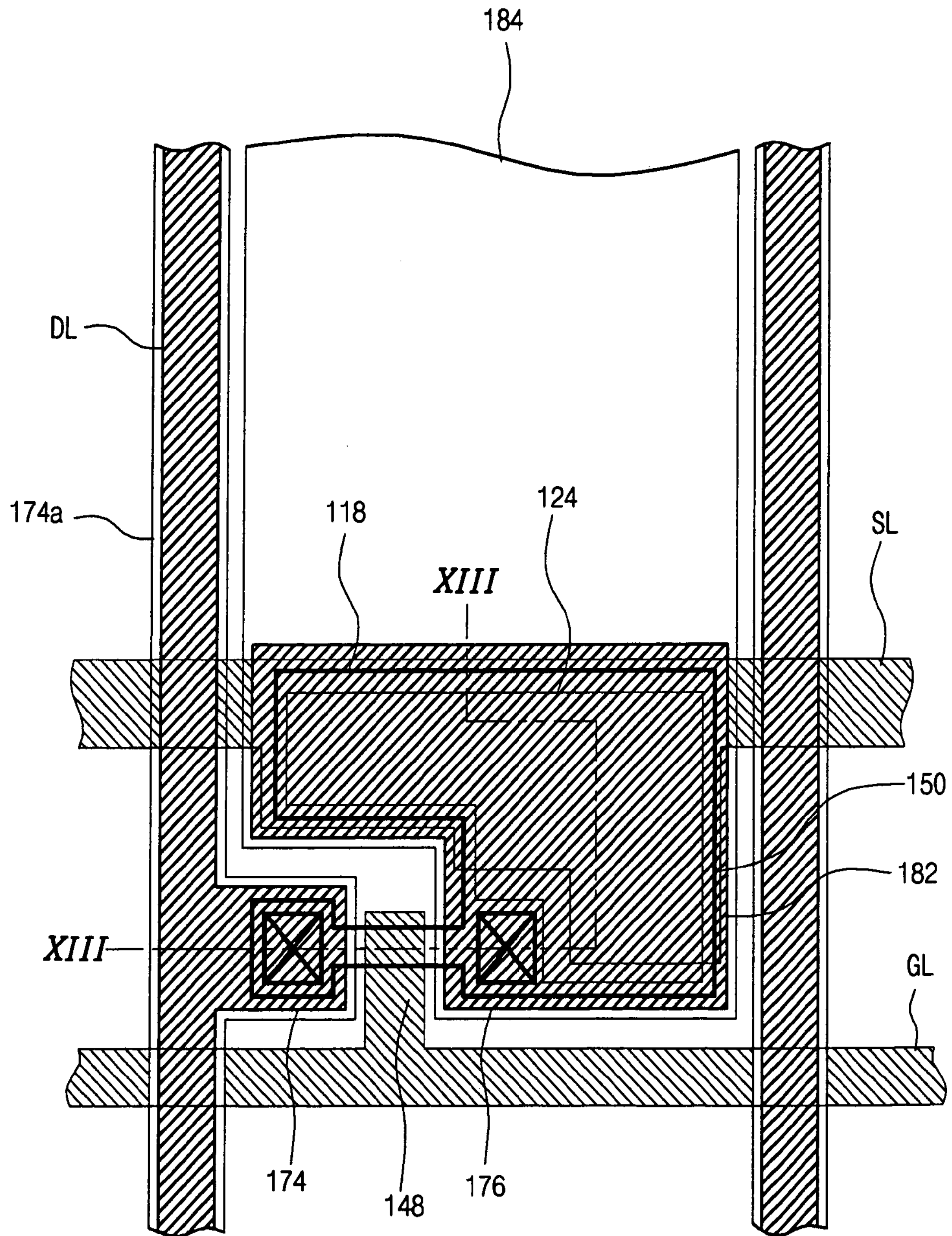
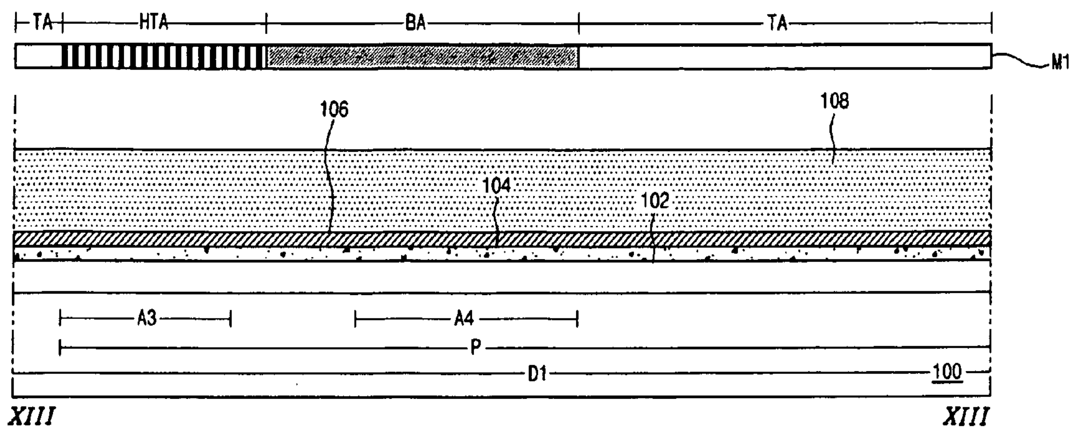


*FIG. 12P*



## FIG. 13A




## FIG. 13B

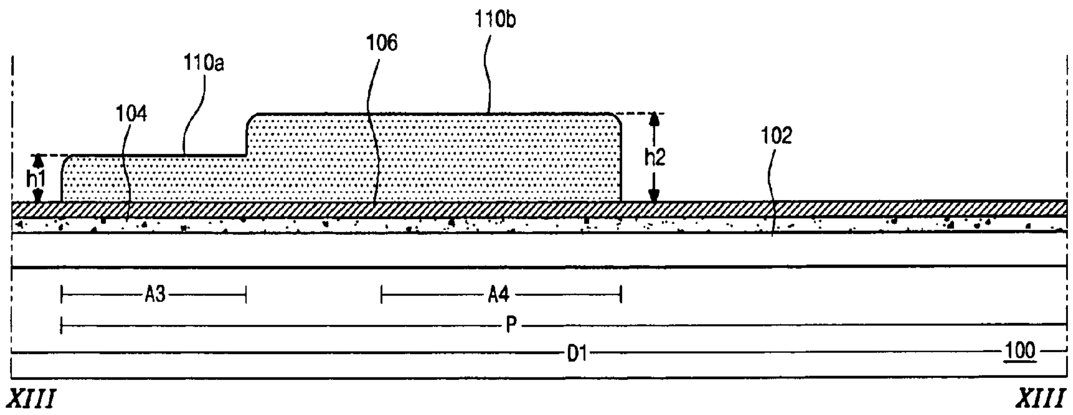


*FIG. 13C*

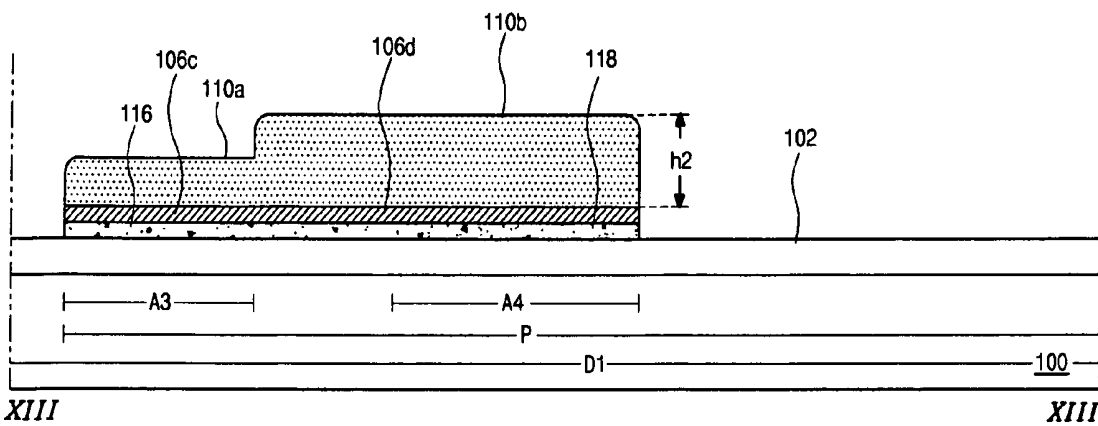



*FIG. 13D*

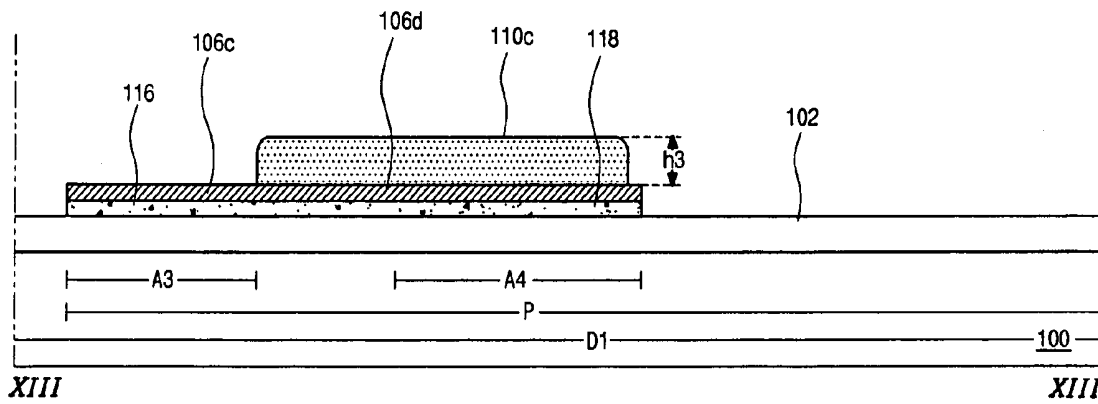


FIG. 13E

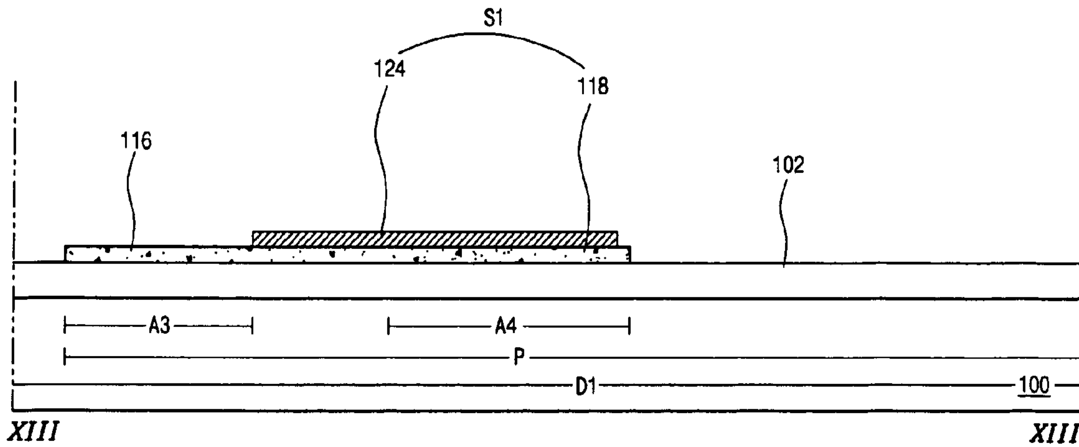
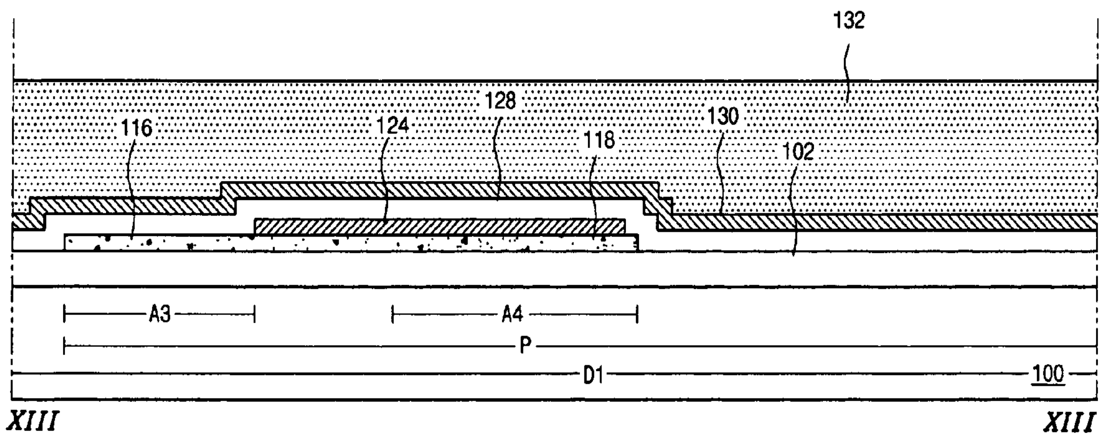
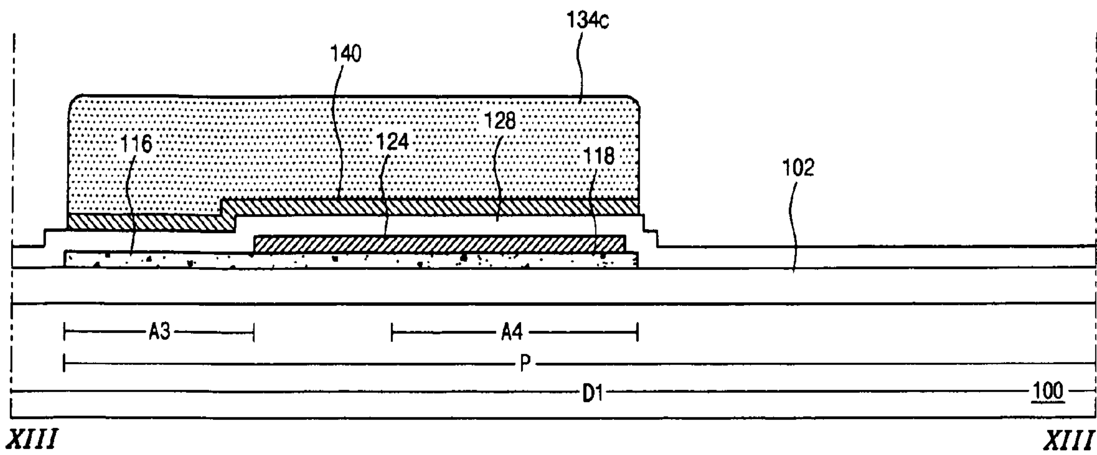



FIG. 13F

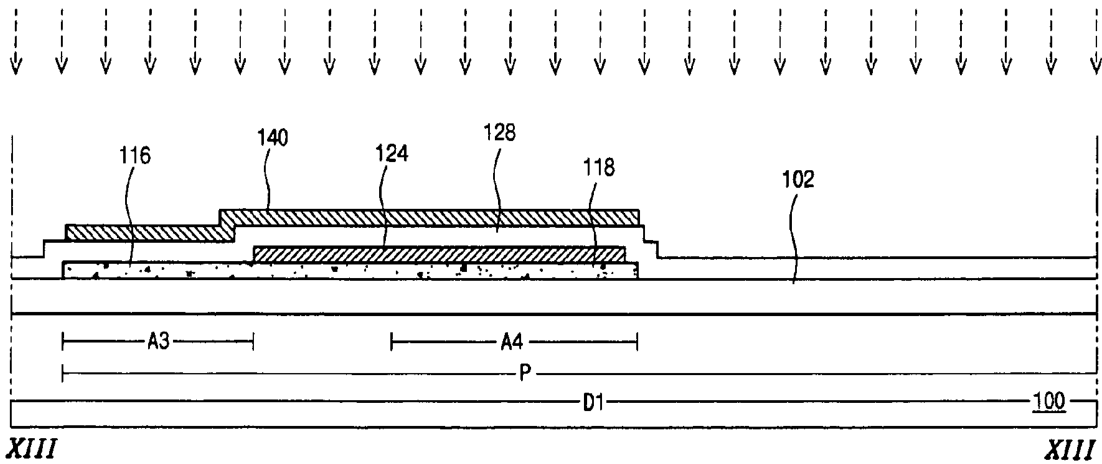


# FIG. 13G



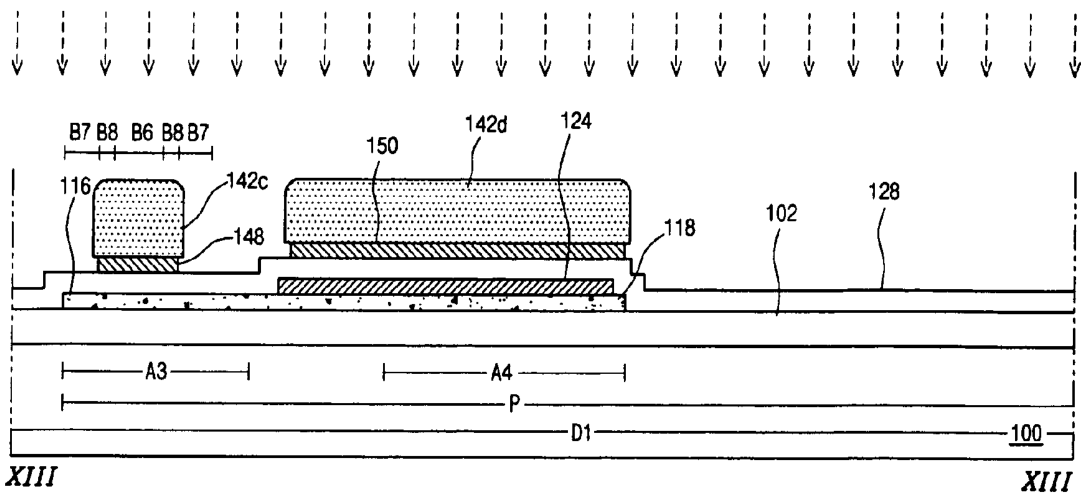

# FIG. 13H

doping with high concentration p-type impurities

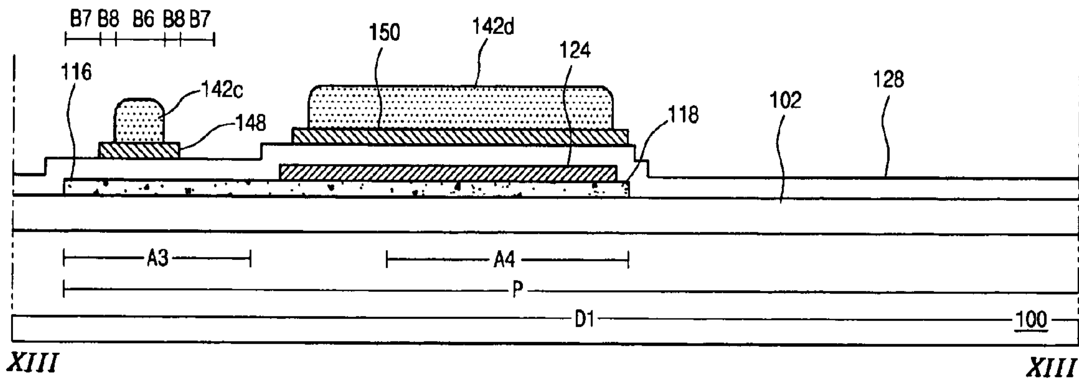


## FIG. 13I

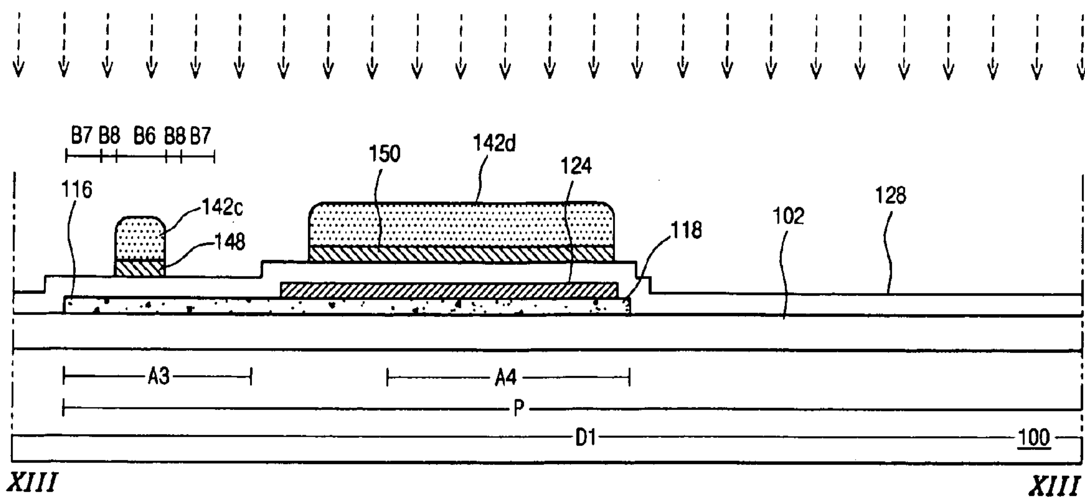
doping with high concentration n-type impurities




## FIG. 13J



## FIG. 13K




## FIG. 13L

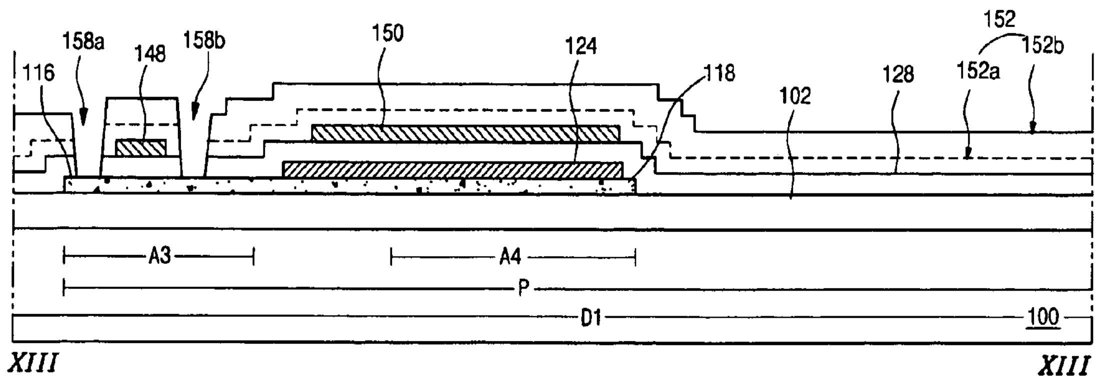


FIG. 13M

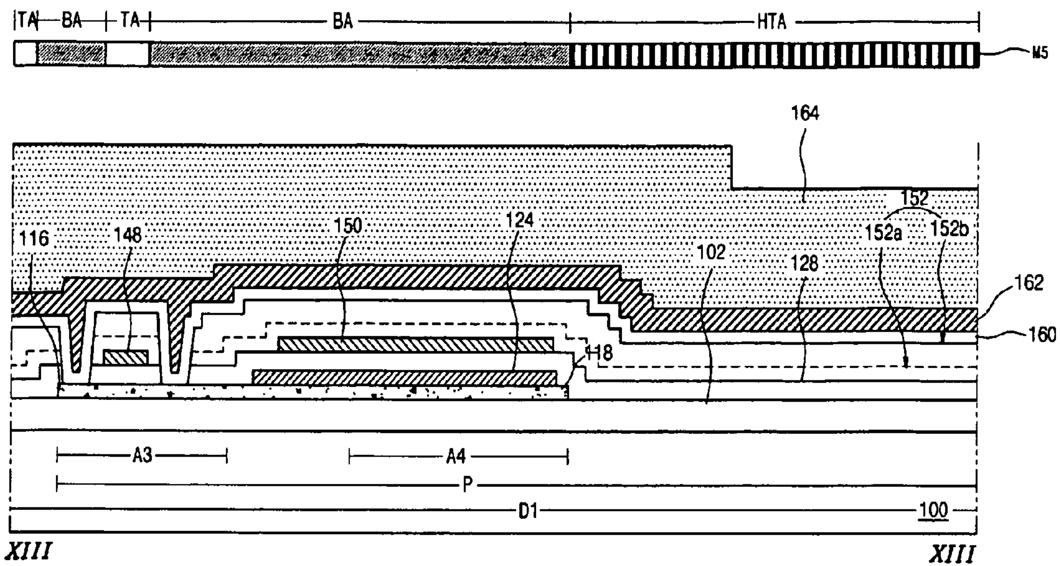
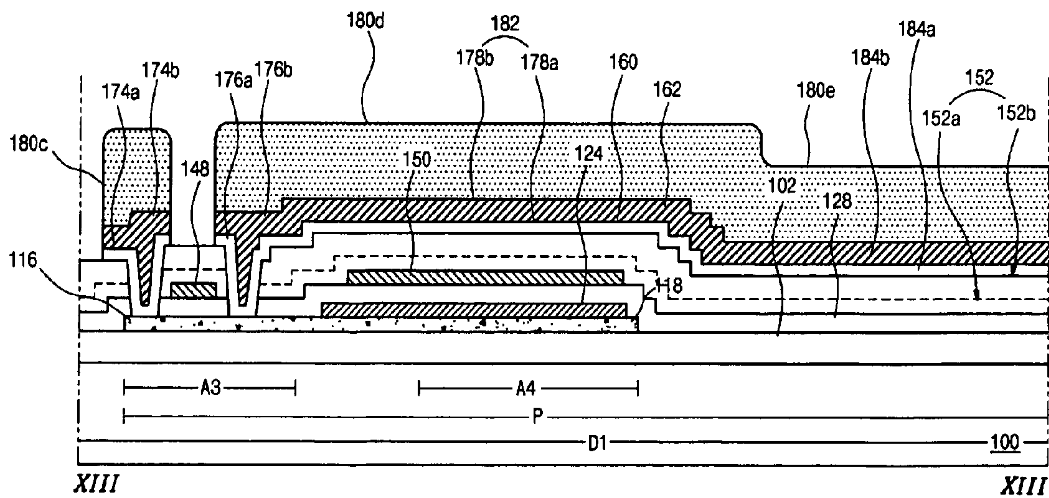
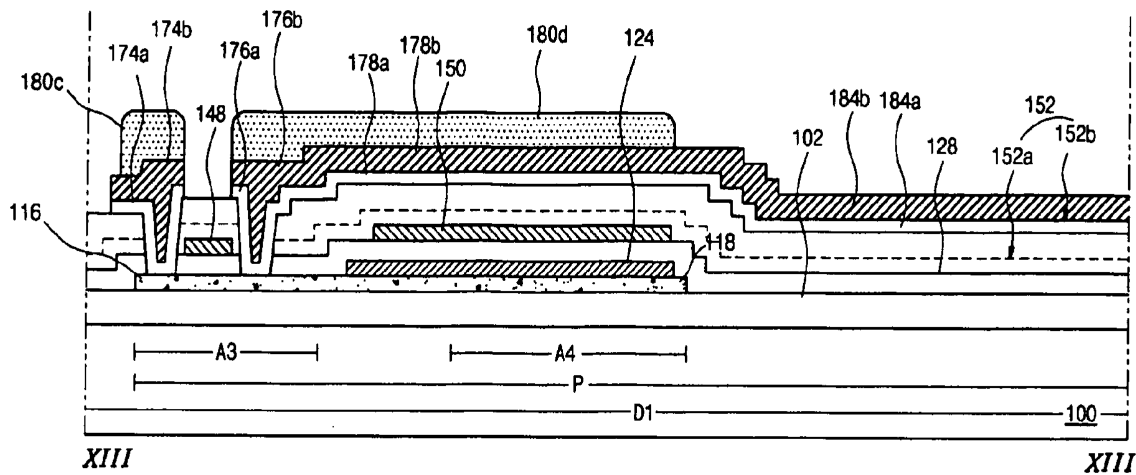


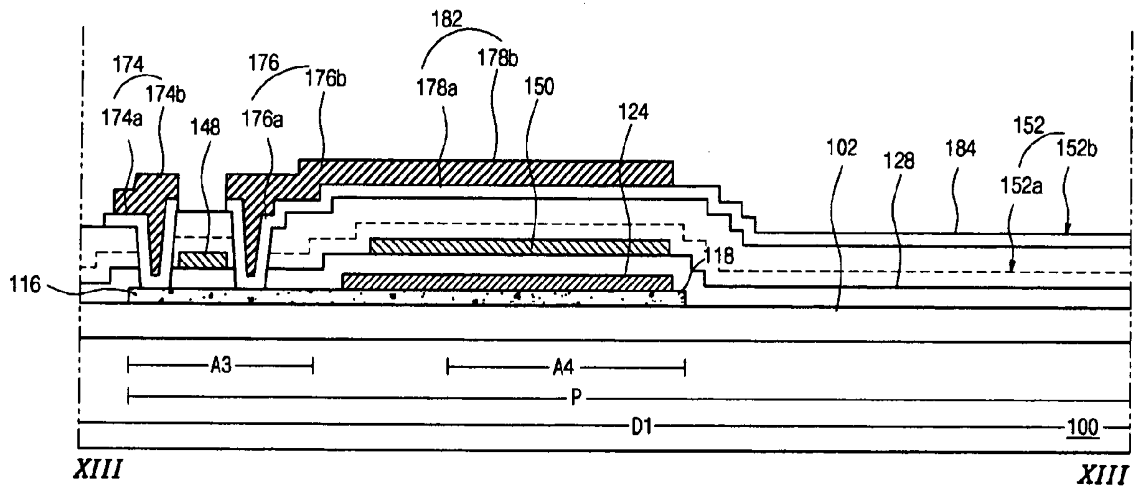

FIG. 13N



## FIG. 13O




## FIG. 13P



# ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY DEVICE WITH STORAGE ELECTRODES AND METHOD OF FABRICATING THE SAME

The present application claims the benefit of Korean Patent Application No. 2005-0106840 filed in Korea on Nov. 9, 2005, which is hereby incorporated by reference.

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an array substrate for a liquid crystal display device and a method of fabricating the same, and more particularly, to an array substrate having an integrated driving circuit.

2. Discussion of the Related Art

In general, a liquid crystal display (LCD) device uses optical anisotropy and polarization properties of liquid crystal molecules to display images. The LCD device includes first and second substrates facing each other and a liquid crystal layer interposed therebetween. The first substrate, typically referred to as an array substrate, includes thin film transistors (TFTs) as switching elements. The second substrate, typically referred to as a color filter substrate, includes a color filter. The TFT includes a semiconductor layer of amorphous silicon or polycrystalline silicon. Since a process using the amorphous silicon is performed in a relatively low temperature and requires a relatively inexpensive insulating substrate, the amorphous silicon has been widely used in fabricating the TFTs. However, since the amorphous silicon has randomly arranged silicon atoms, the amorphous silicon has weak bonding strengths between the silicon atoms, dangling bonds, and low field effect mobility. Accordingly, the TFTs made from amorphous silicon are not adequate for a driving circuit.

By contrast, the polycrystalline silicon has excellent field effect mobility. Hence, the polycrystalline silicon is typically used for fabricating the TFTs of the driving circuit. Further, by forming the driving circuit on the substrate using the polycrystalline silicon without using tape automated bonding (TAB), the LCD device becomes compact, and production cost of the LCD device decreases.

FIG. **1** is a schematic plane view showing an array substrate of an LCD device according to the related art. As shown in FIG. **1**, the first substrate **30** includes a display region D**1** and a non-display region D**2**. A switching TFT (Ts) and a pixel electrode **17** connected to the switching TFT (Ts) are formed in a pixel region P. A gate line **12** along a first direction and a data line **14** are formed to define the pixel region P. The pixel regions P are formed as a matrix in the display region D**1**.

A gate driving circuit **16** and a data driving circuit **18** are formed in the non-display region D2 of the first substrate **30**. The gate driving circuit **16** and the data driving circuit **18** supply control signals and data signals to the pixel regions P through the gate lines **12** and the data lines **14**, respectively. The gate driving circuit **16** and the data driving circuit **18** have TFTs having a complementary metal-oxide semiconductor (CMOS) structure to apply a suitable signal to the respective pixel region P. The TFTs having CMOS structure are typically used for rapidly treating signals in the driving circuit. The CMOS structure includes a combination of n-type (i.e., negative type) and p-type (i.e., positive type) TFTs.

FIG. **2** is a schematic plane view showing a display region of an LCD device having an integrated driving (IC) circuit on the first substrate according to the related art. As shown in FIG. **2**, the first substrate **30** includes the gate lines GL, the data lines DL, the switching TFTs Ts, the pixel electrodes **82**, and storage capacitors Cst. The gate lines GL and the data lines DL cross each other to define the pixel regions P, and the switching TFTs Ts including a gate electrode **52**, an active layer **38**, and source and drain electrodes **74***a* and **74***b* are formed at a crossing portion of the gate and data lines GL and DL. The pixel electrode **82** connected to the drain electrode **74***b* and the storage capacitor Cst including first, second, and third storage electrodes **40**, **54**, and **76** are formed in the pixel region P. The storage capacitors Cst are connected to a storage line SL.



The gate driving circuit **16** and a data driving circuit **18** is formed in a non-display region D2 at a periphery of the display region D**1**. The gate driving circuit **16** and the data driving circuit **18** supply signals to the gate and data lines GL and DL, respectively. Since the gate driving circuit **16** and the data driving circuit **18** have low leakage currents and easily control the signals supplied to the gate and data lines GL and DL, the gate driving circuit **16** and the data driving circuit **18** include TFTs of n-type or TFTs with the CMOS structure.

FIG. **3** is a cross-sectional view of a driving circuit, and FIG. **4** is a cross-sectional view taken along the line IV-IV of FIG. **2**. The driving circuit DC, which may be one of the gate driving circuit **16** and the data driving circuit **18**, is formed in the non-display region D2 and includes TFTs with CMOS structure, i.e., a combination of a first TFT Tp of p-type and second TFT Tn of n-type, as shown in FIG. **3**. As shown in FIG. **4**, a switching TFT Ts as a switching element, a pixel electrode **82**, and a storage capacitor Cst are formed in the display region D**1**. The TFT Ts is typically an n-type TFT. The storage capacitor Cst includes a first capacitor C**1** and a second capacitor C**2**, which are connected to each other in series. The first capacitor C**1** includes a first storage electrode **40** and a second storage electrode **54**. The second capacitor C**2** includes the second storage electrode **54** and a third storage electrode **76**. A process for fabricating the LCD device according to the related art is performed by a nine mask process including several doping process for forming the storage capacitor Cst, the first TFT Tp, and the second TFT Tn.

FIGS. **5**A to **5**I are cross-sectional views showing processes of fabricating a driving circuit according to the related art. FIGS. **6**A to **6**I are cross-sectional views showing processes of fabricating a display region of an array substrate according to the related art. FIGS. **7**A to **7**I are cross-sectional views showing processes of fabricating a portion taken along the lines VII-VII of FIGS. **6**A to **6**I.

A first mask process will now be described with reference to FIG. **5**A, FIG. **6**A and FIG. **7**A. As shown in FIG. **5**A, FIG. **6**A and FIG. **7**A, a buffer layer **32** is formed on the first substrate **30** by depositing a first insulating material. The non-display region D**2** having first and second areas A**1** and A**2** (FIG. **5**A) and the display region D**1** having third and fourth areas A**3** and A**4** in the pixel region P (FIG. **7**A) are defined on the first substrate **30**. Then, a first semiconductor layer **34** of polycrystalline silicon in the first area A**1**, a second semiconductor layer **36** of polycrystalline silicon in the second area A**2**, and a third semiconductor layer **38** of polycrystalline silicon in the third area A**3** and the first storage electrode **40** of polycrystalline silicon in the fourth area A**4** are formed on the buffer layer **32**. The layers of polycrystalline silicon are formed by depositing amorphous silicon, crystallizing the amorphous silicon using a laser, and patterning the crystallized amorphous silicon by a first mask process. The first, second, and third semiconductor layers **34**, **36**, and **38** function as an active layer, and the first storage electrode **40**

functions as an electrode of the first capacitor (C1 of FIG. 4). The third semiconductor layer 38 and the first storage electrode 40 may be integrated.

A second mask process for doping the first storage electrode 40 with impurities is described with reference to FIG. 5B, FIG. 6B, and FIG. 7B. As shown in FIG. 5B, FIG. 6B, and FIG. 7B, a first photoresist (PR) pattern 42 is formed on the first, second, and third semiconductor layers 34, 36, and 38 by coating and patterning a photoresist layer during a second mask process. The first PR pattern 42 covers the first, second, and third areas A1, A2, and A3 while exposing the first storage electrode 40 in the fourth area A4. Then, the first storage electrode 40 is doped with high concentration n-type impurities using the first PR pattern 42 as a doping mask. Since the first storage electrode 40 functions as the electrode of the first capacitor (C1 of FIG. 4), impurities are doped to decrease electrical resistance of the first storage electrode 40. Then, the first PR pattern 42 is removed.

A third mask process will now be described with reference to FIG. 5C, FIG. 6C, and FIG. 7C. As shown in FIG. 5C, FIG. 6C, and FIG. 7C, a gate insulating layer 46 is formed on the first, second, and third semiconductor layers 34, 36, and 38 and the first storage electrode 40 by depositing a first inorganic insulating material. The inorganic insulating material includes one of silicon nitride and silicon oxide. Then, a first gate electrode 48, a second gate electrode 50, a third gate electrode 52, and a second storage electrode 54 are formed on the gate insulating layer 46 by deposing and patterning a first conductive metal by the third mask process. The first gate electrode 48 corresponds to a center of the first semiconductor layer 34 and has a size smaller than the first semiconductor layer 34. The second gate electrode 50 corresponds to a center of the second semiconductor layer 36 and has a size smaller than the second semiconductor layer 36. The third gate electrode 52 corresponds to a center of the third semiconductor layer 38 and has a size smaller than the third semiconductor layer 38. The second storage electrode 54 corresponds to a center of the first storage electrode 40 and has substantially the same size as the first storage electrode 40. At the same time, the gate line GL extending from the third gate electrode 52 is formed along a side of the pixel region P (FIG. 6C). A storage line SL extending from the second storage electrode 54 is formed across the pixel region P (FIG. 6C).

A fourth mask process for doping the second and third semiconductor layers 36 and 38 with impurities is described with reference to FIG. 5D, FIG. 6D, and FIG. 7D. As shown in FIG. 5D, FIG. 6D, and FIG. 7D, a second PR pattern 56 is formed in the first area A1 by coating and patterning PR. The second PR pattern 56 covers the first semiconductor layer 34. Then, ends of the second semiconductor layer 36 and ends of the third semiconductor layer 38 are doped with high concentration n-type impurities using the second PR pattern, the second and third gate electrodes 50 and 52, and the second storage electrode 54 as a doping mask such that the ends of the second semiconductor layer 36 and ends of the third semiconductor layer 38 have an ohmic contact characteristic. Then, the second PR pattern 56 is removed.

A fifth mask process for doping the first semiconductor layer 34 with impurities will now be described with reference to FIG. 5E, FIG. 6E, and FIG. 7E. As shown in FIG. 5E, FIG. 6E, and FIG. 7E, a third PR pattern 58 is formed in the second, third, and fourth areas A2, A3, and A4 by coating and patterning a layer of photoresist. The third PR pattern 58 covers the second and third semiconductor layers 36 and 38 and the first storage electrode 40. Because the first storage electrode 40 is covered with the second storage electrode 54, the third PR pattern 58 in the fourth area A4 is not essential. Then, ends of the first semiconductor layer 34 are doped with high concentration p-type impurities using the third PR pattern 58 and the first gate electrode 48 as a doping mask such that the ends of the first semiconductor layer 34 has an ohmic contact characteristic. The third PR pattern 58 is then removed.

A sixth mask process will now be described with reference to FIG. 5F, FIG. 6F, and FIG. 7F. As shown in FIG. 5F, FIG. 6F, and FIG. 7F, an interlayer insulating layer 60 having first, second, third, fourth, fifth, and sixth contact holes 62*a*, 62*b*, 64*a*, 64*b*, 66*a*, and 66*b* is formed on the first, second, and third gate electrodes 48, 50, and 52, and the second storage electrode 54 by depositing and patterning a second inorganic insulating material. The inorganic insulating material includes one of silicon nitride and silicon oxide. The first and second contact holes 62*a*, 62*b* expose the ends of the first semiconductor layer 34, respectively. The third and fourth contact holes 64*a* and 64*b* expose the ends of the second semiconductor layer 36, respectively. The fifth and sixth contact holes 66*a* and 66*b* expose the ends of the third semiconductor layer 38, respectively.

A seventh mask process will now be described with reference to FIG. 5G, FIG. 6G, and FIG. 7G. First, second, and third source electrodes 70*a*, 72*a*, and 74*a* and first, second, and third drain electrodes 70*b*, 72*b* and 74*b* are formed on the interlayer insulating layer 60 by depositing and patterning a second conductive metal. The second conductive metal includes one of chrome, molybdenum, tungsten, copper, and aluminum alloy. The first source electrode 70*a* and the first drain electrode 70*b* contact the first semiconductor layer 34 through the first and second contact holes 62*a* and 62*b*, respectively. The second source electrode 72*a* and the second drain electrode 72*b* contact the second semiconductor layer 36 through the third and fourth contact holes 64*a* and 64*b*, respectively. The third source electrode 74*a* and the third drain electrode 74*b* contact the third semiconductor layer 38 through the fifth and sixth contact holes 64*a* and 64*b*, respectively. At the same time, a third storage electrode 76 extending from the third drain electrode 74*b* is formed in the fourth area A4. The second capacitor C2 includes of the second storage electrode 54 and the third storage electrode 76. The data line DL extending from the third source electrode 74*a* is formed along one side of the pixel region P and crosses the gate line GL to define the pixel region P.

Through the above-mentioned seven mask processes, the CMOS structure having a combination of the p-type TFT and the n-type TFT is formed in the non-display region D2, and the n-type switching TFT is formed in the third area A3 of the display region D1. Also, the first and second capacitors are formed in the fourth area A4 of the display region D1.

An eighth mask process is described with reference to FIG. 5H, FIG. 6H, and FIG. 7H. As shown in FIG. 5H, FIG. 6H, and FIG. 7H, a passivation layer 78 is formed on the source electrodes 70*a*, 72*a*, and 74*a* and drain electrodes 70*b*, 72*b*, and 74*b* by depositing and patterning a second insulating material. A drain contact hole 80 exposing one of the third drain electrode 74*b* and the third storage electrode 76 is formed in the passivation layer 78.

A ninth mask process will now be described with reference to FIG. 5I, FIG. 6I, and FIG. 7I. As shown in FIG. 5I, FIG. 6I, and FIG. 7I, a pixel electrode 82 is formed on the passivation layer 78 by depositing and patterning a transparent conductive metal. The transparent conductive metal includes one of indium-tin-oxide (ITO) and indium-zinc-oxide (IZO). The pixel electrode 82 contacts one of the third drain electrode 74*b* and the third storage electrode 76 through the drain contact hole 82.

Through the above-mentioned nine mask processes, the array substrate for the LCD device having the integrated driving circuit according to the related art is formed. However, due to the number of processes, processing time is delayed and production costs are increased. Also, since the array substrate is manufactured through so many processes, the defect rate increases.

## SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to array substrate for a liquid crystal display device and a method of fabricating the same that substantially obviate one or more of the problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide an array substrate having an integrated driving circuit that decreases the number of fabrication processes and decreases production cost.

Another object of the present invention is to provide a method of fabricating a liquid crystal display device having an integrated driving circuit that decreases the number of mask processes and decreases fabrication cost.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, the array substrate for a liquid crystal display (LCD) device includes a substrate including a display region and a non-display region, a driving circuit in the non-display region, at least a first thin film transistor (TFT) in the display region, a storage capacitor in the display region including a first storage electrode, a second storage electrode, and a third storage electrode, wherein the first storage electrode includes a first semiconductor layer and a counter electrode, and the third storage electrode includes a first transparent electrode pattern and a first metal pattern, a gate line and a data line crossing each other to define a pixel region in the display region, and a pixel electrode connected to the first TFT in the pixel region.

In another aspect, the method of fabricating an array substrate for a liquid crystal display (LCD) device includes preparing a substrate having a display region and a non-display region, forming a first semiconductor layer and a second semiconductor layer in the non-display region of the substrate, and a third semiconductor layer and a fourth semiconductor layer in the display region of the substrate, the first semiconductor layer including a first region and a second region, the second semiconductor layer including a third region, a fourth region, and a fifth region, and the third semiconductor layer including a sixth region, a seventh region, and an eighth region, forming a counter electrode on the fourth semiconductor layer to define a first storage electrode, forming a first gate electrode over the first region of the first semiconductor layer, a first metal pattern covering the second semiconductor layer, and a second metal pattern covering the third semiconductor layer and the counter electrode, doping the second region of the first semiconductor layer with high concentration p-type impurities, forming a second gate electrode over the third region of the second semiconductor layer, a third gate electrode over the sixth region of the third semiconductor layer, and a second storage electrode over the first storage electrode, wherein the second gate electrode formed from the first metal pattern, and the third gate electrode and the second storage electrode are formed from the second metal pattern, doping the fifth region of the second semiconductor layer and the eighth region of the third semiconductor layer with high concentration n-type impurities, and the fourth region of the second semiconductor layer and the seventh region of the third semiconductor layer with low concentration n-type impurities, forming an interlayer insulating layer to cover the first, second, and third gate electrodes and the second storage electrode, the interlayer insulating layer having first and second contact holes exposing the second region of the first semiconductor layer, third and fourth contact holes exposing the fifth region of the second semiconductor layer, and fifth and sixth contact holes exposing the eighth region of the third semiconductor layer, and forming first, second, and third source electrodes, first, second, and third drain electrodes, a third storage electrode, and a pixel electrode on the interlayer insulating layer, the first source electrode and the first drain electrode contacting the second region of the first semiconductor layer through the first and second contact holes, respectively, the second source electrode and the second drain electrode contacting the fifth region of the second semiconductor layer through the third and fourth contact holes, respectively, the third source electrode and the third drain electrode contacting the eighth region of the third semiconductor layer through the fifth and sixth contact holes.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

## BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. **1** is a schematic plane view showing an array substrate for an LCD device according to the related art.

FIG. **2** is a schematic plane view showing a display region of an LCD device having an integrated driving circuit on the first substrate according to the related art.

FIG. **3** is a cross-sectional view of a driving circuit according to the related art.

FIG. **4** is a cross-sectional view of a display region taken along the line IV-IV of FIG. **2**.

FIGS. **5**A to **5**I are cross-sectional views showing processes of fabricating a driving circuit according to the related art.

FIGS. **6**A to **6**I are cross-sectional views showing processes of fabricating a display region of an array substrate according to the related art.

FIGS. **7**A to **7**I are cross-sectional views showing processes of fabricating a portion taken along the lines VII-VII of FIGS. **5**A to **5**I.

FIG. **8** is a schematic plane view showing a display region of an LCD device having an integrated driving circuit on the first substrate according to an exemplary embodiment of the present invention.

FIG. **9** is a cross-sectional view of a driving circuit according to an exemplary embodiment of the present invention.

FIG. **10** is a cross-sectional view of display region taken along the line X-X of FIG. **8**.

FIGS. **11**A to **11**P are cross-sectional views showing fabricating processes of a driving circuit according to an exemplary embodiment of the present invention.

FIGS. **12**A to **12**P are cross-sectional views showing fabricating processes of a display region of an array substrate according to an exemplary embodiment of the present invention.

FIGS. **13**A to **13**P are cross-sectional views showing fabricating processes of a portion taken along the line XIII-XIII of FIGS. **12**A to **12**P.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

FIG. **8** is a schematic plane view showing a display region of an LCD device having an integrated driving circuit on the first substrate according to an exemplary embodiment of the present invention. As shown in FIG. **8**, gate lines GL and data lines DL are formed on a first substrate **100** and cross each other to define pixel regions P. A switching TFT Ts of polycrystalline silicon is formed at a crossing portion of the gate and data lines GL and DL and includes an active layer **116** of polycrystalline silicon, a gate electrode **148** and a source electrode **174** and a drain electrode **176**. A pixel electrode **184** is formed in the pixel region P and contacts the drain electrode **176** of the switching TFT Ts.

A storage capacitor Cst including a first storage electrode **S1**, a second storage electrode **150**, and a third storage electrode **182** is formed in the pixel region P. The first storage electrode **S1** includes a semiconductor layer **118** of polycrystalline silicon and a counter electrode **124** on the semiconductor layer **118**. The second storage electrode **150** extends from a storage line SL and is disposed over the first storage electrode **S1**. The third storage electrode **182** extends from the drain electrode **176** and is disposed over the second storage electrode **150**. It is characteristic that same signals are applied to the counter electrode **124** and the semiconductor layer **118**. The source electrode **174** includes a transparent electrode layer **174***a* and a conductive metal layer **174***b*. The drain electrode **176** includes a transparent electrode layer **176***a* and a conductive metal layer **176***b*. Also, the storage electrode **182** includes a transparent electrode layer **178***a* and a conductive metal layer **178***b*. It is characteristic that the transparent electrode layer **178***a* extends from the pixel electrode **184**.

FIG. **9** is a cross-sectional view of a driving circuit according to an exemplary embodiment of the present invention. FIG. **10** is a cross-sectional view of display region taken along line X-X of FIG. **8**. As shown in FIG. **9** and FIG. **10**, the first substrate **100** has two regions defined as a display region D**1** including the pixel region P (FIG. **10**) and a non-display region D**2** (FIG. **9**).

A driving circuit (DC) having a CMOS structure, for example, is formed in the non-display region D**2**. As shown in FIG. **9**, the CMOS structure includes a first TFT Tp of p-type and a second TFT Tn of n-type. The first TFT Tp includes a buffer layer **102**, a first semiconductor layer **112**, a gate insulating layer **128**, a first gate electrode **136**, an interlayer insulating layer **152** including a first interlayer insulating layer **152***a* and a second interlayer insulating layer **152***b*, a first source electrode **166** including a first transparent electrode pattern **166***a* and a first conductive metal pattern **166***b*, and a first drain electrode **168** including a second transparent electrode pattern **168***a* and a second conductive metal pattern **168***b*. The second TFT Tn includes the buffer layer **102**, a second semiconductor layer **114**, the gate insulating layer **128**, a second gate electrode **146**, the interlayer insulating layer **152** including the first interlayer insulating layer **152***a* and the second interlayer insulating layer **152***b*, a second source electrode **170** including a third transparent electrode pattern **170***a* and a third conductive metal pattern **170***b*, and a second drain electrode **172** including a fourth transparent electrode pattern **172***a* and a fourth conductive metal pattern **172***b*.

As shown in FIG. **10**, the switching TFT Ts, the storage capacitor Cst, and the pixel electrode **184** are formed in pixel region P. The switching TFT Ts includes the buffer layer **102**, a third semiconductor layer **116**, the gate insulating layer **128**, a third gate electrode **148**, the interlayer insulating layer **152** including the first interlayer insulating layer **152***a* and the second interlayer insulating layer **152***b*, a third source electrode **174** including a fifth transparent electrode pattern **174***a* and a fifth conductive metal pattern **174***b*, and a third drain electrode **176** including a sixth transparent electrode pattern **176***a* and a sixth conductive metal pattern **176***b*. The TFT Ts is an n-type TFT. However, other types of TFTs may be used without departing from the scope of the invention. The storage capacitor Cst includes a first capacitor C**1** and a second capacitor C**2** connected to each other in series. The first capacitor C**1** includes a first storage electrode **S1** and a second storage electrode **150**, and the second capacitor C**2** includes a second storage electrode **150** and a third storage electrode **182** including a seventh transparent electrode pattern **178***a* and a seventh conductive metal pattern **178***b*. The pixel electrode **184** contacts the switching TFT Ts.

FIGS. **11**A to **11**P are cross-sectional views showing processes of fabricating a driving circuit according to an exemplary embodiment of the present invention. FIGS. **12**A to **12**P are cross-sectional views showing processes of fabricating a display region of an array substrate according to an exemplary embodiment of the present invention. FIGS. **13**A to **13**P are cross-sectional views showing processes of fabricating a portion taken along the line XIII-XIII of FIGS. **12**A to **12**P.

A first mask process will now be described with reference to FIGS. **11**A to **11**E, FIGS. **12**A to **12**E, and FIGS. **13**A to **13**E. As shown in FIG. **11**A, FIG. **12**A, and FIG. **13**A, first and second areas **A1** and **A2** in the non-display region D**2** (FIG. **11**A) and third and fourth areas A**3** and A**4** in the display region D**1** (FIG. **13**A) are defined on the first substrate **100**. The buffer layer **102**, a polycrystalline silicon layer **104**, and a first metal layer **106** are formed on the first substrate **100**. The buffer layer **102** may be formed by depositing an inorganic insulating material, for example. The inorganic insulating material may be one of silicon nitride and silicon oxide. The polycrystalline silicon layer **104** may be formed by depositing an intrinsic amorphous silicon, for example, and crystallizing the intrinsic amorphous silicon into polycrystalline silicon. The first metal layer **106** may be formed by depositing a conductive metal, for example. The conductive metal may be one of tungsten, molybdenum, chrome, and moly-tungsten. Other materials for each of the layers may be used without departing from the scope of the invention.

Then, a first photoresist (PR) layer **108** is formed by coating a photoresist material on the first metal layer **106**. A first mask **M1** having a transparent area TA, a blocking area BA, and a half-transparent area HTA is disposed over an entire surface of the first PR layer **108**. The blocking area BA corresponds to the fourth area **A4** and the half-transparent area HTA corresponds to the first, second, and switching areas **A1**, **A2**, and **A3**. The half-transparent area HTA has a transmittance greater than the blocking area BA but less than the transparent area TA.

As shown in FIG. **11**B, FIG. **12**B, and FIG. **13**B, a first PR pattern **110***a* having a first height h**1** in the first, second, and third areas A**1**, A**2**, and A**3** and a second PR pattern **110***b* having a second height h**2** on the fourth area A**4** are formed by exposing and developing the first PR layer **108**. Since the first PR pattern **110***a* corresponds to the half-transparent area HTA, and the second PR pattern **110***b* corresponds to the blocking area BA, the second height h**2** is greater than the first height h**1**. The first PR pattern **110***a* in the third area A**3** and the second PR pattern **110***b* may be connected. The first metal layer **106** corresponding to the transparent area TA is exposed. Then, the exposed portions of the polycrystalline silicon layer **104** and the first metal layer **106** are removed such that first, second, third, and fourth metal patterns **106***a*, **106***b*, **106***c*, and **106***d* and the first, second, third, and fourth semiconductor layers **112**, **114**, **116**, and **118** are formed corresponding to the first and second PR patterns **110***a* and **110***b*, as shown in FIG. **11**C, FIG. **12**C, and FIG. **13**C.

As shown in FIG. **11**C, FIG. **12**C, and FIG. **13**C, the first metal pattern **106***a* and the first semiconductor layer **112** are disposed in the first area A**1**, and the second metal pattern **106***b* and the second semiconductor layer **114** are disposed in the second area A**2** (FIG. **11**C). The third metal pattern **106***c* and the third semiconductor layer **116** are disposed in the third area A**3**, and the fourth metal pattern **106***d* and the fourth semiconductor layer **118** are disposed in the fourth area A**4**. The third semiconductor layer **116** and the fourth semiconductor layer **118** as well as the third metal pattern **106***c* and the fourth metal pattern **106***d* may be connected, respectively.

As shown in FIG. **11**D, FIG. **12**D, and FIG. **13**D, a process for ashing the first and second PR patterns **110***a*, **110***b* is performed to expose the first, second, and third metal patterns **106***a*, **106***b*, and **106***c*. Because the height of the second PR pattern **110***b* (h**2**) is greater than the height of the first PR pattern **110***a* (h**1**), a portion of the second PR pattern **110***b* remains after the first PR pattern **110***a* is removed from the ashing process to form a third PR pattern **110***c*. The third PR pattern **110***c* has a smaller height (h**3**) than the second height h**2**.

As shown in FIG. **11**E, FIG. **12**E, and FIG. **13**E, the counter electrode **124** is formed on the fourth semiconductor layer **118** in the fourth area A**4** while the first, second, and third semiconductor layers **112**, **114**, and **116** are exposed by an etching process that removes the first, second, and third metal patterns **106***a*, **106***b* and **106***c* and the third PR pattern **110***c*. The first, second, third, and fourth semiconductor layers **112**, **114**, **116**, and **118** and the counter electrode **124** are formed by the above-mentioned first mask process. The fourth semiconductor layer **118** and the counter electrode **124** on the fourth semiconductor layer **118** function as the first storage electrode S**1**. Accordingly, a process of doping the fourth semiconductor layer **118** with impurities is omitted by forming the counter electrode **124** on the fourth semiconductor layer **118**.

A second mask process is described with reference to FIGS. **11**F and **11**G, FIGS. **12**F and **12**G, and FIGS. **13**F and **13**G. As shown in FIG. **11**F, FIG. **12**F, and FIG. **13**F, the gate insulating layer **128**, a second metal layer **130**, and a second PR layer **132** is sequentially formed on the first, second, third, semiconductor layers **112**, **114**, and **116** and the counter electrode **124**. Then, the second PR layer **132** is exposed and developed to form a fourth PR pattern **134***a* in the first area A**1**, a fifth PR pattern **134***b* in the second area A**2**, and a sixth PR pattern **134***c* in the third and fourth areas A**3** and A**4** using a second mask (not shown), as shown in FIG. **11**G, FIG. **12**G, and FIG. **13**G.

As shown in FIG. **11**G, FIG. **12**G, and FIG. **13**G, the fourth PR pattern **134***a* corresponds to a center of the first semiconductor layer **112** and has a smaller size than the first semiconductor layer **112**. The fifth PR pattern **134***b* corresponds to a center of the second semiconductor layer **114** and has substantially the same size as the second semiconductor layer **114**. The sixth PR pattern **134***c* corresponds to the third and fourth semiconductor layers **116** and **118** and has substantially the same size as an entire size of the third and fourth semiconductor layers **116** and **118**. Then, the first gate electrode **136** over the first semiconductor layer **112**, a fourth metal pattern **138** over the second semiconductor layer **114**, and a fifth metal pattern **140** are formed by removing the second metal layer **130** (FIG. **11**F, FIG. **12**F, and FIG. **13**F) exposed through portions between the fourth, fifth, and sixth PR patterns **134***a*, **134***b*, and **134***c*. At the same time, the gate line GL connected to one end of the fifth metal pattern **140** and the storage line SL connected to another end of the fifth metal pattern **140** are formed on the gate insulating layer **128** (FIG. **12**G). When the first semiconductor layer **112** includes a first active region B**1** and a second active region B**2** at ends of the first active region B**1**, the first gate electrode **136** corresponds to the first active region B**1**. Then, the fourth, fifth, and sixth PR patterns **134***a*, **134***b*, and **134***c* are removed.

A process of doping the first semiconductor layer with impurities will now be described with reference to FIG. **11**H, FIG. **12**H, and FIG. **13**H. As shown in FIG. **11**H, FIG. **12**H, and FIG. **13**H, the second active region B**2** of the first semiconductor layer **112** is doped with high concentration p-type impurities using the first gate electrode **136** and the fourth and fifth metal patterns **138** and **140** as a doping mask. The second active region B**2** serves as an ohmic contact.

A third mask process will now be described with reference to FIGS. **11**I to **11**K, FIGS. **12**I to **12**K, and FIGS. **13**I to **13**K. As shown in FIG. **11**I, FIG. **12**I and FIG. **13**I, a seventh PR pattern **142***a* on the first gate electrode **136**, an eighth PR pattern **142***b* on the fourth metal pattern **138**, a ninth PR pattern **142***c* and a tenth PR pattern **142***d* on the fifth metal pattern **140** are formed by coating and patterning a third PR layer (not shown) using a third mask (not shown). The seventh PR pattern **142***a* substantially covers the first gate electrode **136** and the first semiconductor layer **112**. The eighth PR pattern **142***b* corresponding to the fourth metal pattern **138** exposes ends of the fourth metal pattern **138**. The ninth PR pattern **142***c* corresponding to the third region A**3** exposes portions of the fifth metal pattern **140** in the third area A**3**. The tenth PR pattern **142***d* spaced apart from the ninth PR pattern **142***c* substantially covers the fifth metal pattern **140** in the fourth area A**4**. Then, the second gate electrode **146** is formed in the second area A**2** by etching the fourth metal pattern **138** using the eighth PR pattern **142***b* as a mask. The third gate electrode **148** is formed in the third area A**3** by etching the fifth metal pattern **140** in the third area A**3** using the ninth PR pattern **142***c* as a mask. In forming the third gate electrode **148**, the second storage electrode **150** is formed in the fourth area A**4** using the tenth PR pattern **142***d* as a mask. The third gate electrode **148** and the second storage electrode **150** protrude from the gate line GL and the storage line SL, respectively (FIG. **12**I).

When the second semiconductor layer **114** includes a third active region B**3**, a fourth active region B**4**, and a fifth active region B**5**, the second gate electrode **146** corresponds to the third and fifth active regions B**3** and B**5**. The fifth active region B**5** is disposed at the sides of the third active region B**3**, and the fourth active region B**4** is disposed at the outer sides of the fifth active region B**5**. Similarly, when the third semi-

conductor layer **116** includes a sixth active region B**6**, a seventh active region B**7**, and an eighth active region B**8**, the third gate electrode **148** corresponds to the sixth and eighth active regions B**6** and B**8**. The eighth active region B**8** is disposed at the sides of the sixth active region B**6**, and the seventh active region B**7** is disposed at the outer sides of eighth active region B**8**.

Next, the fourth active region B**4** of the second semiconductor layer **114** and the seventh active region B**7** are doped with high concentration n-type impurities using the seventh, eighth, ninth, and tenth PR patterns **142***a*, **142***b*, **142***c*, and **142***d* as a doping mask. The fourth active region B**4** and the seventh active region B**7** serves as an ohmic contact. At this time, since ends of the fourth semiconductor layer **118** is not covered with the counter electrode **124**, the ends of the fourth semiconductor layer **118** are doped with the high concentration n-type impurities.

A process for forming a lightly doped drain (LDD) region in the second and third semiconductor layer will now be described with reference to FIGS. **11**J and **11**K, FIGS. **12**J and **12**K and FIGS. **13**J and **13**K. As shown in FIG. **11**J, FIG. **12**J, and FIG. **13**J, a process of ashing the seventh, eighth, ninth, and tenth PR patterns **142***a*, **142***b*, **142***c*, and **142***d* is performed to expose ends of the second gate electrode **146** and ends of the third gate electrode **148**. The ends of the second gate electrode **146** correspond to the fifth active region B**5** of the second semiconductor layer **114**, and the ends of the third gate electrode **148** correspond to the eighth active region B**8**. At the same time, ends of the second storage electrode **150** are exposed. Also, the gate line and the storage line SL are partially exposed. Then, the ends of second gate electrode **146**, the ends of the third gate electrode **148**, and the ends of the second storage electrode **150** are removed, as shown in FIG. **11**K, FIG. **12**K, and FIG. **13**K.

As shown in FIG. **11**K, FIG. **12**K, and FIG. **13**K, the fifth active region B**5** and the eighth active region B**8** are doped with low concentration n-type impurities using the seventh, eighth, ninth, and tenth PR patterns **142***a*, **142***b*, **142***c*, and **142***d* and the counter electrode **124** as a doping mask such that the fifth active region B**5** and the eight active region B**8** are defined as the LDD region, respectively. The LDD region minimizes a leakage current from the semiconductor layers. Then, the seventh, eighth, ninth, and tenth PR patterns **142***a*, **142***b*, **142***c*, and **142***d* are removed. Ohmic contact regions, which are doped with high concentration n-type impurities in the first, second, and third semiconductor layers **112**, **114**, and **116**, the LDD regions, which are doped with low concentration n-type impurities in the second and third semiconductor layers **114** and **116**, the first gate electrode **118** over the first semiconductor layer **112**, the second gate electrode **146** over the second semiconductor layer **114**, the third gate electrode **148** over the third semiconductor layer **116**, and the second storage electrode over the counter electrode **124** are formed in the first substrate **100** by the above-mentioned second and third mask processes.

A fourth mask process will now be described with reference to FIG. **11**L, FIG. **12**L, and FIG. **13**L. As shown in FIG. **11**L, FIG. **12**L, and FIG. **13**L, the interlayer insulating layer **152** including the first and second interlayer insulating layers **152***a* and **152***b* is formed on the first, second, and third gate electrodes **136**, **146**, and **148** and the second storage electrode **150** by sequentially depositing and patterning silicon oxide and silicon nitride using a fourth mask (not shown). In other word, the first interlayer insulating layer **152***a* is made of silicon oxide, and the second interlayer insulating layer **152***b* is made of silicon nitride. The interlayer insulating layer **152** includes seventh, eighth, ninth, tenth, eleventh, and twelfth contact holes **154***a*, **154***b*, **156***a*, **156***b*, **158***a*, and **158***b*. The seventh and eighth contact holes **154***a* and **154***b* expose the second active region (B**2** of FIG. **11**G) of the first semiconductor layer **112**, the ninth and tenth contact holes **156***a* and **156***b* expose the fourth active regions (B**4** of FIG. **11**K) of second semiconductor layer **114**, and the eleventh and twelfth contact holes **158***a* and **158***b* expose the seventh active layer (B**7** of FIG. **113**K) of the third conductor layer **116**. A heating process of the first substrate **100** is performed after forming the first interlayer insulating layer **152***a*. The high concentration n-type impurities doped into the ends of the fourth semiconductor layer **118** are diffused into the counter electrode **124** by the above-mentioned heating process. Accordingly, the counter electrode **124** and the fourth semiconductor layer **118** have characteristic of ohmic contact such that same signals can be applied to the counter electrode **124** and the fourth semiconductor layer **118**. Also, a process of hydrogenation heating is performed on the first substrate **100** after forming the second interlayer insulating layer **152***b*. Since the fourth semiconductor layer **118** and the third semiconductor layer **116** may be connected, the interlayer insulating layer according to another exemplary embodiment of present invention may include a thirteenth contact hole (not shown) exposing an end of the fourth semiconductor layer **118** or the counter electrode **124** instead of the twelfth contact hole **158***b*.

A fifth mask process will now be described with reference to FIGS. **11**M to **11**P, FIGS. **12**M to **12**P, and FIGS. **13**M to **13**P. As shown in FIG. **11**M, FIG. **12**M, and FIG. **13**M, a transparent electrode layer **160**, a conductive metal layer **162**, and a fourth PR layer **164** are formed on the interlayer insulating layer **152**. The transparent electrode layer **160** is formed by depositing a transparent conductive material, such as ITO and IZO. The conductive metal layer **162** is formed by depositing a conductive material, such as chrome, molybdenum, tungsten, copper, and aluminum alloy. The conductive metal layer **162** may be opaque. The fourth PR layer **164** may be a positive type photoresist. A fifth mask M**5** having the transparent area TA, the half-transparent area HTA, and the blocking area BA is disposed over the fourth PR layer **164**. The blocking area BA corresponds to the seventh, eighth, ninth, tenth, eleventh, and twelfth contact holes **154***a*, **154***b*, **156***a*, **156***b*, **158***a*, and **158***b* and the fourth area A**4**. The blocking area BA has six-sub blocking areas of which five-sub blocking areas correspond to the seventh, eighth, ninth, and tenth contact holes (**154***a*, **154***b*, **156***a*, **156***b* of FIG. **11**L) and the eleventh contact hole (**158***a* of FIG. **13**L). The other sub-blocking area corresponds to the twelfth contact hole (**158***b* of FIG. **13**L) and the fourth area A**4**. The transparent areas TA are disposed between the six-sub blocking areas. The half-transmissive area HTA corresponds to the pixel electrode (**184** of FIG. **8**).

Then, eleventh, twelfth, thirteenth, fourteenth, and fifteenth PR patterns **180***a*, **180***b*, **180***c*, **180***d*, and **180***e* are formed on the conductive metal layer **162** by exposing and developing the fourth PR layer **164** using the fifth mask M**5**, as shown in FIG. **11**N, FIG. **12**N, and FIG. **13**N. The eleventh PR pattern **180***a* corresponds to the seventh and eighth contact holes (**154***a* and **154***b* of FIG. **11**L), and the twelfth PR pattern **180***b* corresponds to the ninth and tenth contact holes (**156***a* and **156***b* of FIG. **11**L). The thirteenth PR pattern **180***c* corresponds to the eleventh contact hole (**158***a* of FIG. **13**L), and the fourteenth PR pattern **180***d* corresponds to the twelfth contact hole (**158***b* of FIG. **13**L) and the fourth area A**4**. The fifteenth PR pattern **180***e* extends from the fourteenth PR pattern **180***d* and has a smaller height than the eleventh, twelfth, thirtieth, and fourteenth PR patterns **180***a*, **180***b*, **180***c*, and **180***d* due to the half-transparent area HTA. The

fifteenth PR pattern **180***e* corresponds to the pixel electrode (**184** of FIG. **8**). Next, the first, second, third, fourth, fifth, sixth, seventh, and eighth transparent electrode patterns **166***a*, **168***a*, **170***a*, **172***a*, **174***a*, **176***a*, **178***a*, and **184***a* and the first, second, third, fourth, fifth, sixth, seventh, and eighth conductive-metal patterns **166***b*, **168***b*, **170***b*, **172***b*, **174***b*, **176***b*, **178***b*, and **184***b* are formed on the interlayer insulating layer **152** by removing the conductive metal layer **162** exposed between the eleventh, twelfth, thirteenth, and fourteenth, PR patterns **180***a*, **180***b*, **180***c*, and **180***d* and the transparent electrode layer **160** between the eleventh, twelfth, thirteenth, and fourteenth PR patterns **180***a*, **180***b*, **180***c*, and **180***d*. At the same time, the data line DL extending from the third source electrode **174** is formed in the display region D**1**. The data line DL crosses the gate line GL to define the pixel region P. The data line DL includes a transparent electrode pattern (not shown) extending from the fifth transparent electrode pattern **174***a* and a conductive metal pattern (not shown) extending from the fifth conductive metal pattern **174***b*.

As shown in FIG. **11**O, FIG. **12**O, and FIG. **13**O, a process of ashing the eleventh PR pattern **180***a* to expose ends of the first conductive metal pattern **166***b* and ends of second conductive metal pattern **168***b*, the twelfth PR pattern **180***b* to expose ends of the third conductive metal pattern **170***b* and the fourth conductive metal pattern **172***b*, the thirteenth PR pattern **180***c* to expose ends of the fifth conductive metal pattern **174***b*, the fourteenth PR pattern **180***d* to expose an end of the sixth conductive metal pattern **176***b*, and the fifteenth PR pattern **180***e* to expose an end of the seventh conductive metal pattern **178***b* and the eighth conductive metal pattern **184***b*. Then, the first, second, and third source electrodes **166**, **170**, and **174**, the first, second, and third drain electrodes **168**, **172**, and **176**, the third storage electrode **182**, and the pixel electrode **184** are formed on the interlayer insulating layer **152** by removing the exposed ends of the first conductive metal pattern **166***b*, the second conductive metal pattern **168***b*, the third conductive metal pattern **170***b*, the fourth conductive metal pattern **172***b*, the fifth conductive metal pattern **174***b*, the sixth conductive metal pattern **176***b*, the seventh conductive metal pattern **178***b*, and the eighth conductive metal pattern **184***b*, as shown in FIG. **11**P, FIG. **12**P, and FIG. **13**P.

As shown in FIG. **11**P, FIG. **12**P, and FIG. **13**P, the first source electrode **166** in the first area A**1** includes the first transparent electrode pattern **166***a* and the first conductive metal pattern **166***b*, and the first drain electrode **168** in the first area A**1** includes the second transparent electrode pattern **168***a* and the second conductive metal pattern **168***b*. The second source electrode **170** in the second area A**2** includes the third transparent electrode pattern **170***a* and the third conductive metal pattern **170***b*, and the second drain electrode **172** in the first area A**2** includes the fourth transparent electrode pattern **172***a* and the fourth conductive metal pattern **172***b*. The third source electrode **174** in the third area A**3** includes the fifth transparent electrode pattern **174***a* and the fifth conductive metal pattern **174***b*, and the third drain electrode **176** in the third area A**3** includes the sixth transparent electrode pattern **176***a* and the sixth conductive metal pattern **176***b*. The third storage electrode **182** over the second storage electrode **150** in the fourth area A**4** includes the seventh transparent electrode pattern **178***a* and the seventh conductive metal pattern **178***b*. The pixel electrode **184** includes the eighth transparent electrode pattern **184***a*. The eleventh, twelfth, thirteenth, and fourteenth PR patterns **180***a*, **180***b*, **180***c*, and **180***d* are removed. As mentioned above, the first, second, and third source electrodes **166**, **170**, and **174**, the first, second, and third drain electrodes **168**, **172**, and **176**, the third storage electrode **182**, and the pixel electrode **184** are formed on the first substrate **100** only using the fifth mask (M**5** of FIG. **11**M).

Although not shown, the LCD device according to the exemplary embodiment of the present invention also includes a color filter substrate facing the array substrate. The color filter includes a second substrate, a black matrix, a color filter layer, and a common electrode. The black matrix on the second substrate may correspond to the non-display region of the first substrate, the gate and data lines, and the switching TFTs in the display region of the first substrate. The color filter layer on the black matrix includes three sub-color filters of red, green, and blue colors. The common electrode on the color filter layer corresponds to the pixel electrode such that an electric field between the common electrode and the pixel electrode is generated.

In the present invention, semiconductor layers of the driving circuit, the switching TFTs, the storage capacitors, and the counter electrodes of the storage capacitors are formed by a same mask process. In addition, the source and drain electrodes, the third storage electrodes and the pixel electrodes are formed by a same mask process. The array substrate according to the exemplary embodiment of the present invention is manufactured by a five mask process. The interlayer insulating layer includes a first layer of silicon oxide and a second layer of silicon nitride, for example. The second layer of silicon nitride and the pixel electrode have an improved interfacial characteristic. Since the array substrate according to the exemplary embodiment of the present invention is manufactured by the five mask process, the process of fabricating the array substrate for the LCD device is simplified.

It will be apparent to those skilled in the art that various modifications and variations can be made in the array substrate for a liquid crystal display device of the present invention and the method of fabricating the same without departing form the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

**1**. An array substrate for a liquid crystal display (LCD) device, comprising:

- a substrate including a display region and a non-display region;
- a driving circuit in the non-display region;
- at least a first thin film transistor (TFT) in the display region;
- a storage capacitor in the display region including a first storage electrode, a second storage electrode, and a third storage electrode, wherein the first storage electrode includes a first semiconductor layer and a counter electrode, and the third storage electrode includes a first transparent electrode pattern and a first metal pattern;
- a gate line and a data line crossing each other to define a pixel region in the display region; and
- a pixel electrode connected to the first TFT in the pixel region,
- wherein the second storage electrode is disposed between the first storage electrode and the third storage electrode, and the first storage electrode, the second storage electrode and the third storage electrode are insulated from each other.

**2**. The array substrate according to claim **1**, wherein the first TFT includes a second semiconductor layer having a first region, a second region at sides of the first region, and a third region at outer sides of the second region, a first gate electrode extending from the gate line, a first source electrode extend-

ing from the data line, and a first drain electrode, wherein the second region is doped with low concentration n-type impurities, the third region is doped with high concentration n-type impurities, and the first source electrode and the first drain electrode contact the third region, respectively.

**3**. The array substrate according to claim **2**, wherein each of the first source electrode and the first drain electrode includes a transparent electrode and an opaque electrode.

**4**. The array substrate according to claim **2**, wherein the first semiconductor layer and the second semiconductor layer are formed at a same layer level and are connected.

**5**. The array substrate according to claim **2**, wherein the first source electrode, the first drain electrode, and the third storage electrode are formed at a same layer level.

**6**. The array substrate according to claim **1**, wherein the driving circuit includes at least a second TFT of a p-type and a third TFT of an n-type.

**7**. The array substrate according to claim **6**, wherein the second TFT includes a third semiconductor layer having a fourth region and a fifth region at sides of the fourth region, a second gate electrode, a second source electrode, and a second drain electrode, wherein the fifth region is doped with high concentration p-type impurities, and the second source electrode and the second drain electrode contact the fifth region, respectively.

**8**. The array substrate according to claim **7**, wherein both of the second source electrode and the second drain electrode include a transparent electrode and an opaque electrode.

**9**. The array substrate according to claim **7**, wherein the first semiconductor layer and the third semiconductor layer are formed at a same layer level.

**10**. The array substrate according to claim **7**, wherein the third source electrode, the second drain electrode, and the third storage electrode are formed at a same layer level.

**11**. The array substrate according to claim **6**, wherein the third TFT includes a fourth semiconductor layer having a sixth region, a seventh region at sides of the sixth region, and a eighth region at outer sides of the seventh region, a third gate electrode, a third source electrode, and a third drain electrode, wherein the seventh region is doped with low concentration n-type impurities, the eighth region is doped with high concentration n-type impurities, and the third source electrode and the third drain electrode contact the eighth region, respectively.

**12**. The array substrate according to claim **11**, wherein both of the third source electrode and the third drain electrode include a transparent electrode and an opaque electrode.

**13**. The array substrate according to claim **11**, wherein the first semiconductor layer and the fourth semiconductor layer are formed at a same layer level.

**14**. The array substrate according to claim **11**, wherein the third source electrode, the third drain electrode, and the third storage electrode are formed at a same layer level.

* * * * *

patsnap

| 专利名称(译) | 用于具有存储电极的液晶显示装置的阵列基板及其制造方法 | | |
|---|---|---|---|
| 公开(公告)号 | US7532263 | 公开(公告)日 | 2009-05-12 |
| 申请号 | US11/452996 | 申请日 | 2006-06-15 |
| [标]申请(专利权)人(译) | 乐金显示有限公司 | | |
| 申请(专利权)人(译) | LG.PHILIPS LCD CO.，LTD. | | |
| 当前申请(专利权)人(译) | LG DISPLAY CO.，LTD. | | |
| [标]发明人 | LEE SEOK WOO<br>PARK YONG IN | | |
| 发明人 | LEE, SEOK-WOO<br>PARK, YONG-IN | | |
| IPC分类号 | G02F1/1343 G02F1/1335 G02F1/136 G09G3/36 H01L29/15 H01L31/036 | | |
| CPC分类号 | G02F1/136213 G02F1/13454 G02F2001/136231 | | |
| 代理机构(译) | 摩根路易斯律师事务所 | | |
| 审查员(译) | 内尔姆斯，DAVID | | |
| 优先权 | 1020050106840 2005-11-09 KR | | |
| 其他公开文献 | US20070103610A1 | | |
| 外部链接 | Espacenet USPTO | | |


摘要(译)

一种用于液晶显示（LCD）装置的阵列基板，包括：显示区域和非显示区域的基板;非显示区域中的驱动电路;显示区域中的至少第一薄膜晶体管（TFT）显示区域中的存储电容器，包括第一存储电极，第二存储电极和第三存储电极，其中第一存储电极包括第一半导体层和对电极，第三存储电极包括第一透明电极图案和第一金属图案，栅极线和数据线彼此交叉以限定显示区域中的像素区域，以及像素电极连接到像素区域中的第一TFT。