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(54) **Method of addressing a cholesteric liquid crystal display**

(57) Method of addressing a cholesteric liquid crystal display having a plurality of pixels arranged in rows and columns, wherein: addressing a specific one of said plurality of pixels comprises a plurality of addressing phases; during each of said plurality of addressing phases, a sequence RS, RNS of row voltage pulses and a sequence CON, COFF, CGRAY of column voltage pulses is applied; said sequence RS, RNS of row voltage pulses and sequence CON, COFF, CGRAY of column voltage pulses comprise three voltage levels of 0 volt, UL volt and UH volt; during a preparation phase as a first addressing phase of said plurality of addressing phases, a first sequence RS, RNS of row voltage pulses and a first sequence CON, COFF, CGRAY of column voltage pulses are applied; and UH is only comprised in said sequence RS, RNS of row voltage pulses and said sequence CON, COFF, CGRAY of column voltage pulses during said preparation phase, with 0 < UL = UH.

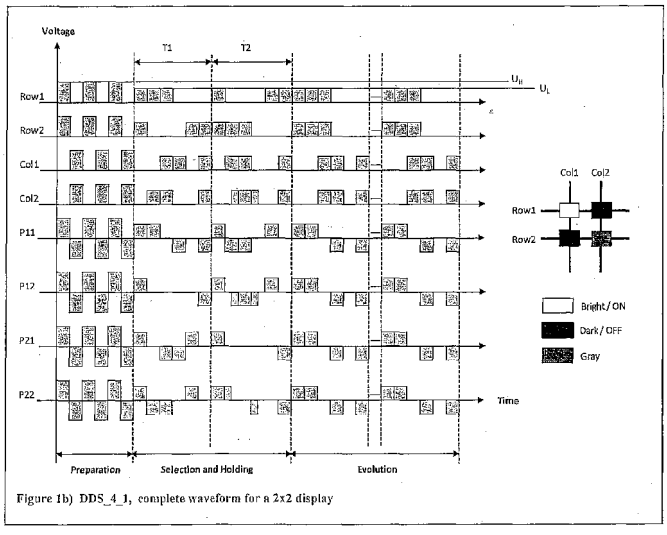

Figure 1b) DDS_4_1, complete waveform for a 2x2 display

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Description

[0001] The present invention refers to a method of addressing a cholesteric liquid crystal display. Specifically, the present invention refers to a method of addressing a cholesteric liquid crystal display capable of grayscale operation.

[0002] Liquid crystal displays (LCDs) are flat displays that employ the light modulating properties of liquid crystals, a state of matter having properties between those of a conventional liquid and a solid crystal. LCDs may be mainly distinguished in terms of the order or phase of the liquid crystal molecules they contain, which may be either "nematic" (with various modifications such as "twisted nematic", "super twisted nematic" and "double super twisted nematic") or "smectic". In the nematic phase, the molecules do not have any positional order but tend to point in the same direction, i. e. their longitudinal axes are parallel on the average (the term is derived from the Greek prefix *nemato*, meaning "threadlike"). In the smectic phase, the molecules in addition exhibit a positional order at least along one dimension, i. e. in a smectic order, the molecules form a layered structure with the molecules oriented parallel or tilted relative to the layer normal (the term is derived from the Greek word for soap, because slippery substance often found at the bottom of a soap dish is actually a type of smectic liquid crystal). There can be associated different geometrical properties or concepts with each of the nematic phase and the smectic phase; they are not to be confused with the respective phase itself). For example, the nematic phase may feature the property of chirality or handedness. A chiral object has a shape that can not be superimposed on its mirror image. Chirality is not a state of matter, and there can thus be no phase transition between chiral and antichiral; an object can be either chiral or antichiral, never both. The nematic phase of a chiral substance is called the cholesteric phase, originating from cholesteryl benzoate, a chiral substance where liquid crystal phases were firstly discovered. In the cholesteric phase, the molecules are helically arranged, with the helical axis extending normal to the average of the longitudinal axes of the molecules. This leads to the formation of a three-dimensional structure which can be visualized as a stack of very thin two-dimensional nematic-like layers with the director (longitudinal axes) in each layer twisted with respect to those adjacent to it. ChLCDs exhibit the above cited twisted nematic structure, where the director rotates about an axis as one moves through the material.

[0003] Cholesteric LCDs (ChLCDs) have some excelling properties, the most important one of which is the bistability of their phases, i. e. the property to be able to maintain either one of two distinct phases without application of any electric or magnetic field. This allows for information display without any power consumption. The two states are named the "planar state" and the "focal conic state" (also found in a certain type of smectic materials called smectic A). Further advantageous properties are a wide viewing angle, because no polarizer is needed, and high contrast.

[0004] When a ChLCD is in its planar state, it reflects light of a certain wavelength region, and appears, therefore, in the corresponding color. In contrast, when a ChLCD is in its focal conic state, incident light is only weakly scattered, making the pixels assume the color of the substrate behind them, usually black. That is, when there is a black absorber attached to the display backside, a front observer sees either the color of the reflected light (planar state) or the color of the absorber material (focal conic state). In both states the liquid crystal molecules are arranged in a helical structure. It should be noted that the liquid crystalline structure inside the display is divided into many tiny subdomains, enabling the coexistance of the planar state and the focal conic state inside an individual pixel of the ChLCD, making the ChLCD capable of gray scale operation.

[0005] Formerly, the individual pixels of ChLCDs were addressed in a so called static driving scheme such as a conventional passive matrix driving scheme resulting in a slow refresh rate as the number of times per second that a ChLCD draws data (which is not to be confused with the frame rate which is usually lower than the refresh rate). In order to overcome this drawback, a so called "dynamic drive scheme" (DDS) has been proposed which enables refresh times of approximately 1ms per display row (cf. e. g. "Dynamic Drive of Cholesteric Liquid Crystal Displays"; X. Y. Huang, J. W. Doane, D. K. Yang; J. SID 5/3, 129 (1997)).

[0006] However, the DDS of Huang et al. has the disadvantage that the display driving circuitry has to be very complicated, as many different voltage levels are necessary to drive the display.

[0007] This disadvantage has been overcome with the invention of the "two-level DDS" (cf. "Bistable Cholesteric Reflective Displays: Two-Level Dynamic Drive Schemes"; A. Rybalochka, V. Sorokin, S. Valyukh; J. SID 12/2, 165 (2004)). Here, each row and column of the display is addressed either with a voltage U or zero. This makes the driving circuitry simple, because only a single voltage has to be generated. In addition to that, it is possible to use off-the-shelf display drivers that are commercially available.

[0008] However, the type two-level-DDS developed by Rybalochka et al. has the disadvantage that the proposed schemes (called therein $U/\sqrt{2}$-, $U/\sqrt{3}$-, and $U/\sqrt{3/2}$- schemes) do not provide the desired possibility of gray-level-imaging.

[0009] It is an object of the present invention to provide a method of addressing a cholesteric liquid crystal display that overcomes the above discussed disadvantages, especially is capable of grayscale operation.

[0010] This object is solved by the features of claims 1. Further advantageous are defined in the dependent

claims.

[0011] The present invention (claim 1) defines a method of addressing a cholesteric liquid crystal display having a plurality of pixels arranged in rows and columns, wherein addressing a specific one of the plurality of pixels comprises a plurality of addressing phases; during each of the plurality of addressing phases, a sequence R_S, R_{NS} of row voltage pulses and a sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses is applied; the sequence R_S, R_{NS} of row voltage pulses and sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses comprise three voltage levels of 0 volt, U_L volt and U_H volt; during a preparation phase as a first addressing phase of the plurality of addressing phases, a first sequence R_S, R_{NS} of row voltage pulses and a first sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses are applied; and U_H is only comprised in the sequence R_S, R_{NS} of row voltage pulses and the sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses during the preparation phase, with $0 < U_L \leq U_H$. Preferably, the plurality of pixels are arranged as a (n x m)-matrix of a plurality of n rows and m columns, each of the plurality of pixels having a unique address given by two values (a, b), with $1 < a < n$, and $1 < b < m$. Alternatively, one of n and m may be "one", that is the cholesteric liquid crystal display may include only a single row or a single column. According to the present invention, there is always a preparation phase as a first addressing phase, followed by at least one further phase. Advantageously, the plurality of addressing phases are arranged successively on a time axis, starting with the preparation phase and continued with a second phase, a third phase etc. During the preparation phase, the liquid crystal is re-set, so to speak, i. e. it is completely driven to an unstable, "neutral" state called the homeotrophic state. The homeotrophic state only exists in the presence of an electric field, that is large enough to unwind the helical structure of the liquid crystal molecules, and develops into one of the above cited planar state and focal-conic state or gray state. Preferably, the voltage pulses of both the sequence of row voltage pulses and the sequence of column voltage pulses have the same polarity. It should be noted that there is a maximum or highest voltage level applied to the rows and columns, where either both of U_L and U_H are at that level ($0 < U_L = U_H$) or $U_L < U_H$ ($0 < U_L < U_H$). To put it differently, U_H defines the highest level, and U_L with $U_L > 0$ is either of the same level or below it. It should be noted that the term "only" in the last feature of claim 1 refers to the phase, i. e. the preparation phase, and that in that phase U_H may be comprised in the sequences of row voltage pulses or in the sequences of column voltage pulses or in both of them.

[0012] According to a preferred aspect of the present invention (claim 2), (i) in case of $U_H > U_L$, U_L is only comprised in said sequence R_S, R_{NS} of row voltage pulses and said sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses during addressing phases other than said preparation phase, and all pulse widths of said sequences R_S, R_{NS}, C_{ON}, C_{OFF}, C_{GRAY} of row and column voltage pulses are each equal in all addressing phases; and (ii) in case of $U_H = U_L$, the pulse widths of said sequences R_S, R_{NS}, C_{ON}, C_{OFF}, C_{GRAY} of row and column voltage pulses in said addressing phase are different from said pulse widths of said sequences R_S, R_{NS}, C_{ON}, C_{OFF}, C_{GRAY} of row voltage pulses and column voltage pulses during addressing phases other than said preparation phase. That is, whereas according to claim 1, U_H is 'restricted' to the preparation phase (nothing is said about U_L), according to feature (i), U_L is 'excluded' from the preparation phase. This results in a situation where in each of the addressing phases, either U_H or U_L occurs, not both of them. In contrast, the distinction that can be made via the pulse height is compensated in feature (ii) by the variation of the pulse width.

[0013] According to a further preferred aspect of the present invention (claim 3), said plurality of addressing phases for said specific pixel comprise a 'selection and holding phase' as a second addressing phase during which a second sequence R_S, R_{NS} of row voltage pulses and a second sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses are applied; and an 'evolution phase' as a third addressing phase during which a third sequence R_S, R_{NS} of row voltage pulses and a third sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses are applied. Therefore, claim 3 defines two further addressing phases of the plurality of addressing phases as a "selection and holding phase", and an "evolution phase", respectively. During the selection and holding phase, the pixels are individually selected and set by applying appropriate row and column voltage pulses (shortly "row signals" and "column signals", respectively). This is done by first selecting a specific row and then a specific column by providing the corresponding signals. Having selected a row, the column signal determines whether the pixel is finally transferred to the planar state (ON-state) or to the focal-conic state (OFF-state) or the gray state. During the evolution phase (3rd phase), as during the preparation phase (1st phase), all rows and columns are addressed simultaneously with voltages U_H and 0V in the case of $U_H > U_L$. Preferably, the selection and holding phase may be time divided into a plurality of successive selection phases and holding phases. Most preferably, the selection and holding phase may be time divided into a selection phase sandwiched between two holding phases.

[0014] According to a further preferred aspect of the present invention (claim 4), during said selection and holding phase, (i) at any time, any one of said sequences of row voltage pulses is such that the corresponding one of said rows is either a selected row (in case of R_S) or a non-selected row (in case of R_{NS}); (ii) at any time, there is only a single selected row, wherein said specific pixel is defined by said single selected row and one of said columns; and (iii) any one of said sequences C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses is such that the corresponding column is either a planar-state setting column by applying the sequence C_{ON} of column voltage pulses, resulting in a planar state of said specific pixel at the end

of said evolution phase, a focal-conic-state-setting column, by applying the sequence C_{OFF} of column voltage pulses resulting in focal-conic state of said specific pixel at the end of said evolution phase, or a gray-state setting column by applying the sequence C_{GRAY} of column voltage pulses, resulting in a gray-state of the specific pixel at the end of the evolution phase. As for feature (i), depending on the voltage scheme (or rather the strength of the present electric fields) applied (to the individual columns) subsequent to the preparation phase (during the selection and holding phase, to be precise), the corresponding pixel inside the selected row is transferred to either the planar state or the focal-conic state or the gray state. According to feature (ii), no more than one row can be selected to be the selected row. Otherwise, it would not be possible to address a single pixel by an n-tuple (a, b). According to feature (iii), the type of column, being either a planar-state setting column or a focal-conic-state setting column or a gray-state setting column, determines the type of pixel, i. e. its perceived brightness.

[0015] According to a further preferred aspect of the present invention (claim 5), the sequence R_S of voltage pulses applied to the single selected row is different from the sequences R_{NS} of voltage pulses applied to each of said non-selected rows.

[0016] According to a another preferred aspect of the present invention (claim 6), there are defined: across-pixel voltages P_{ON} which each are a difference $P_{ON} = R_S - C_{ON}$ between a sequence R_S of row voltage pulses of the single selected row and a sequence C_{ON} of column voltage pulses of one of the planar-state setting columns; across-pixel voltages P_{OFF} which each are a difference $P_{OFF} = R_S - C_{OFF}$ between a sequence R_S of row voltage pulses of the single selected row and a sequence C_{OFF} of column voltage pulses of one of the focal-state-setting columns; across-pixel voltages P_{GRAY} which each are a difference $P_{GRAY} = R_S - C_{CRAY}$ between said sequence R_S of row voltage pulses of said single selected row and a sequence C_{GRAY} of column voltage pulses of one of said gray-state setting columns; across-pixel voltages P_{Hd1} which each are a difference $P_{Hd1} = R_{NS} - C_{ON}$ between a sequence R_{NS} of row voltage pulses of one of the non-selected rows and a sequence C_{ON} of column voltage pulses of one of the planar-state setting columns; and across-pixel voltages P_{Hd2} which each are a difference $P_{Hd2} = R_{NS} - C_{OFF}$ between a sequence R_{NS} of row voltage pulses of one of the non-selected rows and a sequence C_{OFF} of column voltage pulses of one of the focal-state-setting columns; and across-pixel voltages P_{HD} which each are a difference $P_{HD} = R_{NS} - C_{CRAY}$ between said sequence R_{NS} of row voltage pulses of said non-selected rows and said sequence C_{GRAY} of column voltage pulses of one of said gray-state setting columns. Furthermore, each of the across-pixel voltages P_{ON}, P_{OFF}, P_{GRAY}, P_{Hd1}, P_{Hd2}, and P_{HD} is a DC-free voltage that contains at least one continuous waiting time with zero voltage, and a ratio between a waiting time of the across-pixel voltage P_{OFF} to a waiting time of either the across-pixel voltage P_{Hd1} or the across-pixel voltage P_{Hd2} is either 4:1, 4:2 or 3:2. That is, an "across-pixel voltage" is a potential difference between a potential applied to a column and a potential applied to a row (either a selected or a non-selected row), the rows and columns thus can uniquely define or address (and thereby control) the specific pixel. Therefore, the totality of pixels form a two-dimensional matrix and are addressable by two values, a row number and a column number (the above n-tuple (a, b)).

[0017] According to a another preferred aspect of the present invention (claim 7), in a method according to the preferred aspect defined in claim 6, (i) each of said sequences C_{ON} and C_{OFF} of column voltage pulses comprises a first subsequence of a single non-zero voltage pulse, and a second subsequence of two consecutive non-zero voltage pulses (ii) in one of said sequences C_{ON} and C_{OFF} of column voltage pulses, there is a separation of a single zero voltage pulse between said first subsequence and said second subsequence, whereas in the other one of said sequences C_{ON} and C_{OFF} of column voltage pulses, said separation is two zero voltage pulses, (iii) said sequence C_{GRAY} of column voltage pulses is generated by shifting, in said one of said sequences C_{ON} and C_{OFF} of column voltage pulses in which said second separation is two consecutive zero voltage pulses, said second sequence towards said first subsequence about a distance smaller than said separation; and (iv) an intensity of a said gray-state is determined by an amount of said distance. To put it more simply, gray-levels can easily be achieved by shifting the position of the broader non-zero voltage pulse in the column voltage signal to a position between its respective position in the sequences C_{ON} and C_{OFF} of column voltage pulses. The resulting across-pixel voltage drives the corresponding pixel inside the selected row into a gray-state.

[0018] According to a another preferred aspect of the present invention (claim 8), each of said sequences R_S, R_{NS} of row voltage pulses and sequences C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses comprise six voltage pulses.

[0019] Further advantages and features of the present invention will become apparent from the following detailed description of preferred embodiments in combination with the attached drawings. In the drawings, there are:

Fig. 1a first sequences of voltage pulses applied to rows and columns during the holding and selection phase, and Fig. 1b a complete set of first sequences of voltage pulses (for the preparation, selection and holding, and evolution phase), according to a first embodiment of the present invention;

Fig. 2a first sequences of voltage pulses applied to rows and columns during the holding and selection phase, and Fig. 2b a complete set of first sequences of voltage pulses (for the preparation, selection and

holding, and evolution phase), according to a second embodiment of the present invention; and

Fig. 3a first sequences of voltage pulses applied to rows and columns during the holding and selection phase, and Fig. 3b a complete set of first sequences of voltage pulses (for the preparation, selection and holding, and evolution phase), according to a third embodiment of the present invention.

Figs. 1a and 1b explain first sequences of voltage pulses (DDS_4_1), Figs. 2a and 2b explain second sequences of voltage pulses (DDS_4_2) and Figs. 3a and 3b explain third sequences of voltage pulses (DDS_3_2) according to the present invention. In addition, while Figs. 1a, 2a, and 3a show sequences of voltage pulses applied during the "holding and selection" phase, Figs. 1b, 2b, and 3b show the sequences of voltage pulses applied during all addressing phases for the exemplary case of a (2x2)-display. In the following "sequences of voltage pulses" is abbreviated to "voltage signal"

[0020] Each of Figs. 1a, 2a, and 3a is a matrix or table of voltage signals showing in the first row 'column voltage signals' C_{ON}, C_{OFF}, and C_{GRAY}, in the first column 'row voltage signals' R_S, and R_{NS}, and in the other table elements differences between one of the column voltage signals and one of the row voltage signals, wherein:

- R_S is the voltage signal applied to a selected row (there is only a single selected row at a time);
- R_{NS} is the voltage signal applied to non-selected rows, which are all rows other than the selected row;
- C_{ON} is the voltage signal applied to a column (planar-state setting column) in order to transfer the corresponding pixel inside the selected row to the planar state (ON state);
- C_{OFF} is the voltage signal applied to a column (focal-conic state setting column) in order to transfer the corresponding pixel inside the selected row to the focal-conic state (OFF state);
- C_{GRAY} is the voltage signal applied to a column in order to achieve gray levels;
- P_{ON} = R_S-C_{ON};
- P_{OFF} = R_S-C_{OFF};
- P_{Gray} = R_S-C_{Gray};
- P_{Hd1} = R_{NS}-C_{ON};
- P_{Hd2} = R_{NS}-C_{OFF}; and
- P_{Hd} = R_{NS}-C_{Gray}

[0021] The across-pixel voltage signal P_{ON} = R_S-C_{ON} transfers the corresponding pixel in the selected row to the planar state (ON state). The across-pixel voltage signal P_{OFF} = R_S-C_{OFF} transfers the corresponding pixel in the selected row to the focal conic state (OFF state). The across-pixel voltage signals P_{Hd1} = R_{NS}-C_{ON} and P_{Hd2} = R_{NS}-C_{OFF} are applied to all pixels in not-selected rows. Furthermore, gray-levels can easily be achieved by shifting the position of the broader pulse in the column-signal between its position in C_{ON} and C_{OFF} (see the column signal C_{Gray}). The resulting across-pixel voltage P_{Gray} = R_S-C_{Gray} transfers the corresponding pixel in the selected row to a gray state.

[0022] As can be seen in all figures, each voltage signal (also called 'addressing frame') is divided into six subparts, where a voltage of U_H is applied to subparts depicted as gray rectangles, a voltage of U_L is applied to subparts depicted as gray squares, and 0 volt is applied to subparts depicted as white boxes. Furthermore, the pulses forming the voltage signals R_S, R_{NS}, C_{ON}, C_{OFF}, and C_{Gray} have the same polarity, whereas the pulses forming the across-pixel voltage signals, being each a difference, have different polarity. Specifically, all across-pixel voltages are free of DC-voltage (as many positive pulses as negative pulses per frame), otherwise the liquid crystal could be damaged.

[0023] A characteristic feature of the voltages signals P_{OFF}, P_{Hd1}, and P_{Hd2} in each of the cases DDS_4_1 (Fig. 1 a), DDS_4_2 (Fig. 2a) and DDS_3_2 (Fig. 3a) are the waiting times, i. e. subparts with neither a positive nor a negative voltage applied. For instance, in DDS_4_1, there is a waiting time of four subparts in P_{OFF} and a waiting time of one subpart in P_{Hd1} and P_{Hd2}, in DDS_4_2, there is a waiting time of four subparts in P_{OFF} and a waiting time of two subparts in P_{Hd1} and P_{Hd2}, and in DDS_3_2, there is a waiting time of three subparts in P_{OFF} and a waiting time of two subparts in P_{Hd1} and P_{Hd2}. Therefore, in the notation DDS_x_y, x and y refer to the number of subparts forming the waiting times in P_{OFF} and P_{Hd1}/ P_{Hd2}, respectively. The ratio x/y of these waiting times (for example 4:1 in DDS_4_1) has to be chosen according to the electro-optical characteristics of the ChLCD. The electro-optical characteristic curve of a ChLCD determines which of our three novel waveforms is best suited to achieve good contrast.

[0024] Figs. 1b, 2b and 3b show the complete voltage signals for a 2x2-display. The row voltage signals are denoted by Row1 and Row2. The column voltage signals are denoted by Col1 and Col2. The resulting across-pixel voltage signals are denoted by P11, P12, P21 and P22.

[0025] The pixel P11 (first row, first column) is driven to the planar state (ON-state). The pixels P12 and P21 are driven to the focal conic state (OFF-state). Pixel P22 is driven to a gray state. The highest voltage U_H is only used during the preparation phase. During the preparation phase all pixels are simultaneously addressed with an identical waveform.

[0026] The selection and holding phase is divided into two parts T1 and T2 (because there are two rows). During the interval T1, the first row is selected. During T2 the second row is selected. In the evolution phase all pixels are again addressed simultaneously with an identical waveform.

Claims

1. Method of addressing a cholesteric liquid crystal display having a plurality of pixels arranged in rows and columns, wherein:

   - addressing a specific one of said plurality of pixels comprises a plurality of addressing phases;
   - during each of said plurality of addressing phases, a sequence R_S, R_{NS} of row voltage pulses and a sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses is applied;
   - said sequence R_S, R_{NS} of row voltage pulses and sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses comprise three voltage levels of 0 volt, U_L volt and U_H volt;
   - during a preparation phase as a first addressing phase of said plurality of addressing phases, a first sequence R_S, R_{NS} of row voltage pulses and a first sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses are applied; and
   - U_H is only comprised in said sequence R_S, R_{NS} of row voltage pulses and said sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses during said preparation phase, with $0 < U_L \leq U_H$.

2. Method according to claim 1, wherein:

   - in case of $U_H > U_L$,
   - U_L is only comprised in said sequence R_S, R_{NS} of row voltage pulses and said sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses during addressing phases other than said preparation phase; and
   - all pulse widths of said sequences R_S, R_{NS}, C_{ON}, C_{OFF}, C_{GRAY} of row and column voltage pulses are each equal in all addressing phases; and
   - in case of $U_H = U_L$,
   - said pulse widths of said sequences R_S, R_{NS}, C_{ON}, C_{OFF}, C_{GRAY} of row voltage pulses and column voltage pulses in said addressing phase are different from said pulse widths of said sequences R_S, R_{NS}, C_{ON}, C_{OFF}, C_{GRAY} of row voltage pulses and column voltage pulses during addressing phases other than said preparation phase.

3. Method of claim 1 or 2, wherein said plurality of addressing phases for said specific pixel comprise:

   - a selection and holding phase as a second addressing phase during which a second sequence R_S, R_{NS} of row voltage pulses and a second sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses are applied; and
   - an evolution phase as a third addressing phase during which a third sequence R_S, R_{NS} of row voltage pulses and a third sequence C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses are applied.

4. Method of claim 3, wherein during said selection and holding phase:

   - at any time, any one of said sequences of row voltage pulses is such that the corresponding one of said rows is either a selected row or a non-selected row;
   - at any time, there is only a single selected row, wherein said specific pixel is defined by said single selected row and one of said columns; and
   - any one of said sequences C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses is such that the corresponding column is either a planar-state setting column by applying said sequence C_{ON} of column voltage pulses, resulting in a planar state of said specific pixel at the end of said evolution phase, a focal-conic-state setting column by applying said sequence C_{OFF} of column voltage pulses, resulting in focal-conic-state of said specific pixel at the end of said evolution phases.; or a gray-state setting column by applying said sequence C_{GRAY} of column voltage pulses, resulting in a gray-state of said specific pixel at the end of said evolution phase.

5. Method of claim 4, wherein said sequence R_S of voltage pulses applied to said single selected row is different from the sequences R_{NS} of voltage pulses applied to each of said non-selected rows.

6. Method of claim 4 or claim 5, wherein:

   - there are defined:
   - across-pixel voltages P_{ON} which each are a difference $P_{ON} = R_S - C_{ON}$ between a sequence R_S of row voltage pulses of said single selected row and a sequence C_{ON} of column voltage pulses of one of said planar-state setting columns;
   - across-pixel voltages P_{OFF} which each are a difference $P_{OFF} = R_S - C_{OFF}$ between said sequence R_S of row voltage pulses of said single selected row and a sequence C_{OFF} of column voltage pulses of one of said focal-conic-state setting columns;
   - across-pixel voltages P_{GRAY} which each are a difference $P_{GRAY} = R_S - C_{CRAY}$ between said sequence R_S of row voltage pulses of said single selected row and a sequence C_{GRAY} of column voltage pulses of one of said gray-state setting columns;
   - across-pixel voltages P_{Hd1} which each are a difference $P_{Hd1} = R_{NS} - C_{ON}$ between a sequence R_{NS} of row voltage pulses of one of said non-selected rows and said sequence C_{ON} of

column voltage pulses of one of said planar-state setting columns; and

- across-pixel voltages P_{Hd2} which each are a difference $P_{Hd2} = R_{NS} - C_{OFF}$ between said sequence R_{NS} of row voltage pulses of one of said non-selected rows and said sequence C_{OFF} of column voltage pulses of one of said focal-state setting columns;
- across-pixel voltages P_{HD} which each are a difference $P_{HD} = R_{NS} - C_{CRAY}$ between said sequence R_{NS} of row voltage pulses of one of said non-selected rows and said sequence C_{GRAY} of column voltage pulses of one of said gray-state setting columns;
- each of said across-pixel voltages P_{ON}, P_{OFF}, P_{GRAY}, P_{Hd1}, P_{Hd2}, and P_{HD} is a DC-free voltage that contains at least one continuous waiting time with zero voltage; and
- a ratio between a waiting time of said across-pixel voltage P_{OFF} to a waiting time of either said across-pixel voltage P_{Hd1} or said across-pixel voltage P_{Hd2} is either 4:1, 4:2 or 3:2.

7. Method of one of claims1 to 6, wherein:

- each of said sequences C_{ON} and C_{OFF} of column voltage pulses comprises a first subsequence of a single non-zero voltage pulse, and a second subsequence of two consecutive non-zero voltage pulses;
- in one of said sequences C_{ON} and C_{OFF} of column voltage pulses, there is a separation of a single zero voltage pulse between said first subsequence and said second subsequence, whereas in the other one of said sequences C_{ON} and C_{OFF} of column voltage pulses, said separation is two zero voltage pulses;
- said sequence C_{GRAY} of column voltage pulses is generated by shifting, in said one of said sequences C_{ON} and C_{OFF} of column voltage pulses in which said second separation is two consecutive zero voltage pulses, said second sequence towards said first subsequence about a distance smaller than said separation; and
- an intensity of a said gray-state is determined by an amount of said distance.

8. Method of one of claims 1 to 7, wherein each of said sequences R_S, R_{NS} of row voltage pulses and sequences C_{ON}, C_{OFF}, C_{GRAY} of column voltage pulses comprise six voltage pulses.

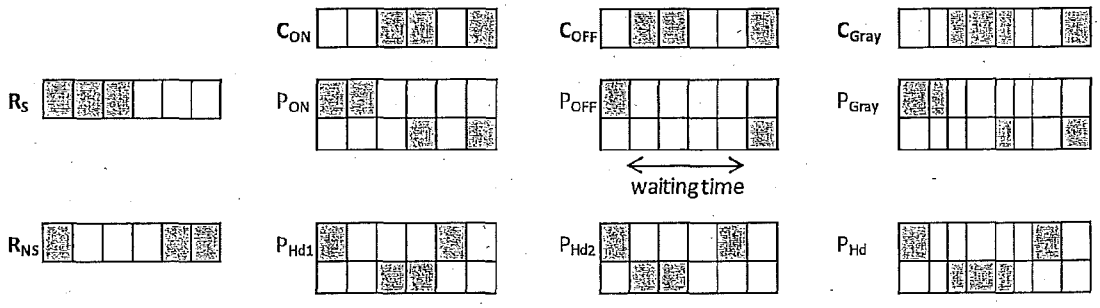

Figure 1a) Waveform DDS_4_1, signals applied to rows and columns during "holding & selection" phase.

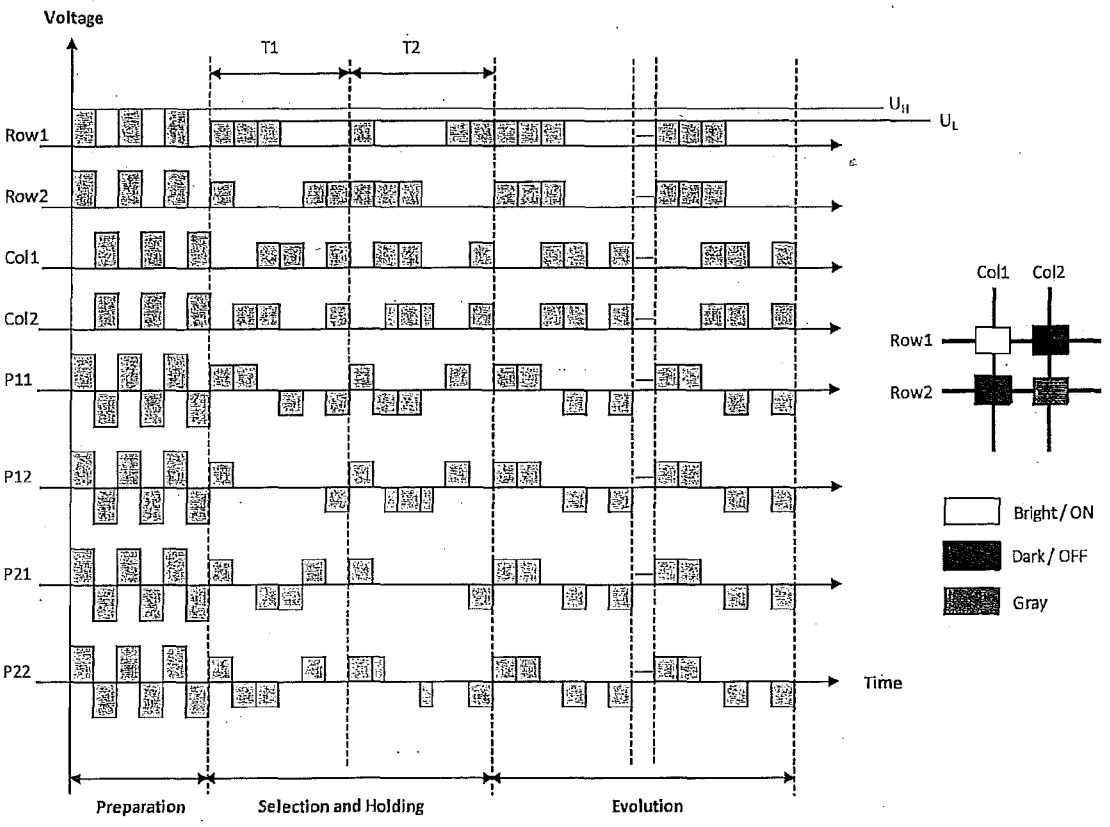

Figure 1b) DDS_4_1, complete waveform for a 2x2 display

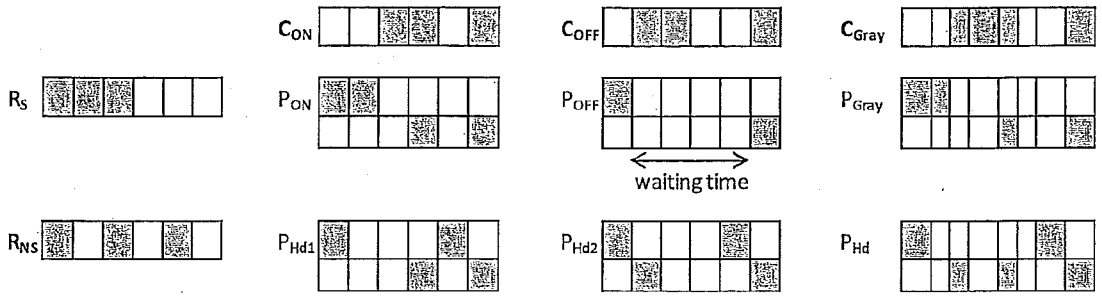

Figure 2a) Waveform DDS_4_2, signals applied to rows and columns during "holding & selection" phase.

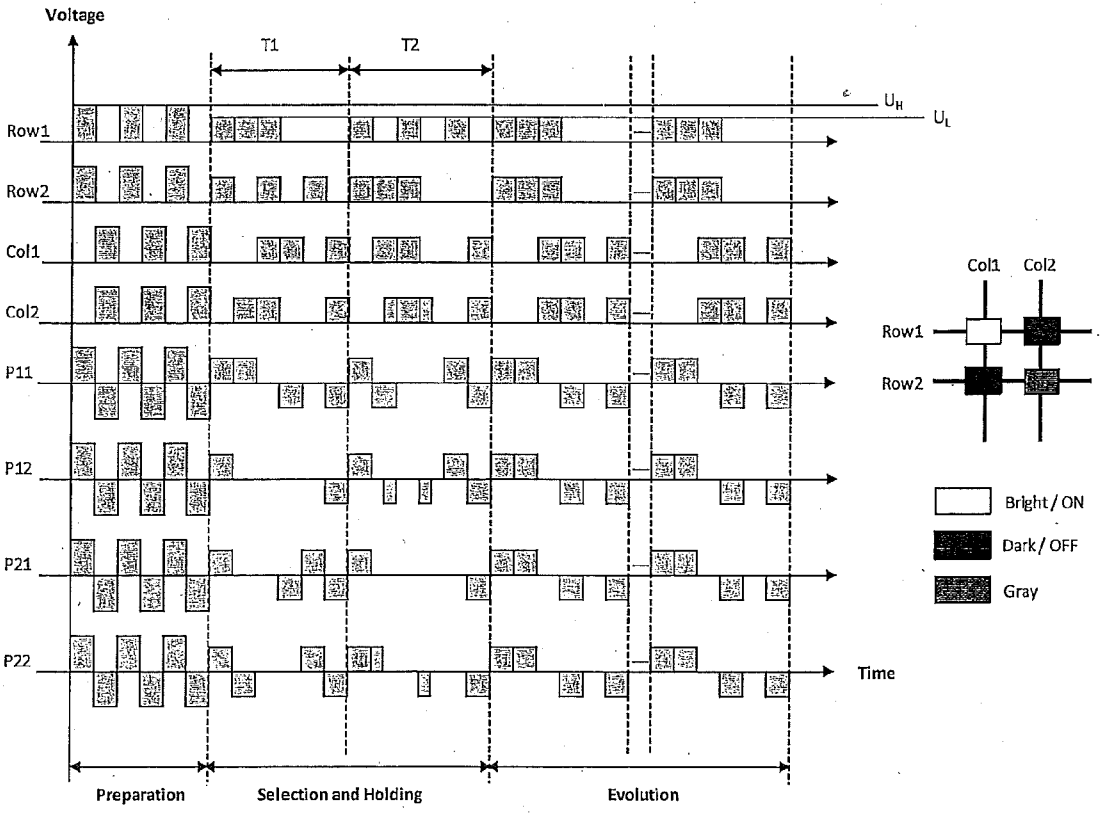

Figure 2b) DDS_4_2, complete waveform for a 2x2 display

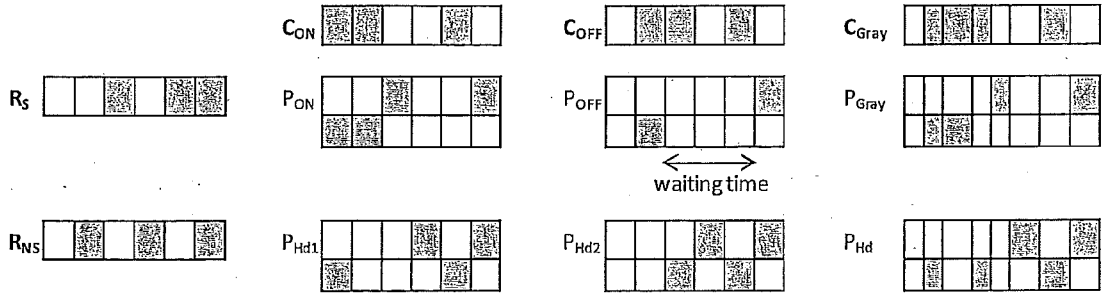

Figure 3a) Waveform DDS_3_2, signals applied to rows and columns during "holding & selection" phase.

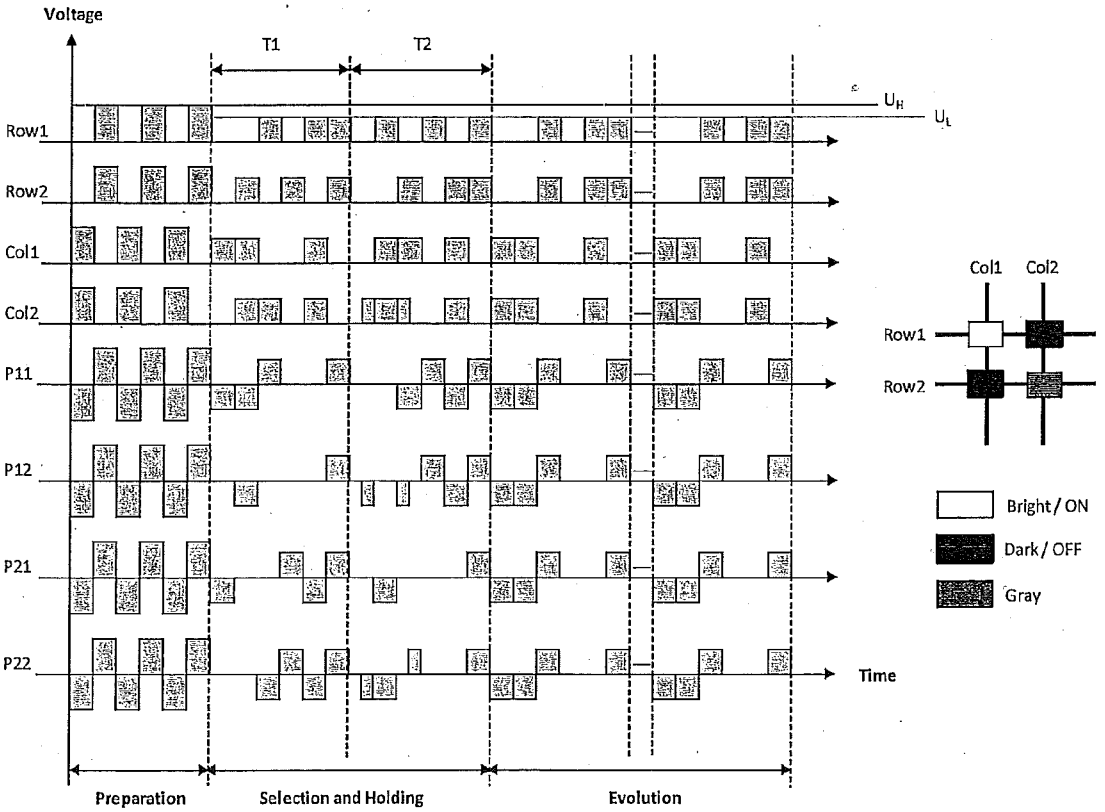

Figure 3b) DDS_3_2, complete waveform for a 2x2 display

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EUROPEAN SEARCH REPORT

Application Number
EP 12 16 1891

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2010/156967 A1 (WATANUKI TSUNEO [JP] ET AL) 24 June 2010 (2010-06-24) * paragraphs [0101] - [0114], [0003], [0058] - [0060], [0085] - [0087]; figures 4,7-10 * -----	1-5	INV. G09G3/36
A	US 2003/206147 A1 (MI XIANG-DONG [US] ET AL) 6 November 2003 (2003-11-06) * paragraphs [0002], [0048] - [0057]; figures 4A-8D * -----	1	
A	RYBALOCHKA A ET AL: "P-85: Simple Drive Scheme for Bistable Cholesteric LCDs", 2001 SID INTERNATIONAL SYMPOSIUM - JUNE 3-8, 2001, SAN JOSE CONVENTION CENTER, CALIFORNIA, vol. XXXII, 3 June 2001 (2001-06-03), page 882, XP007007885, * the whole document * -----	1	
A	ANDRIY RYBALOCHKA AND VIKTOR SOROKIN ET AL: "P-176: New High-Performance Algorithm for 2+2 Dynamic Drive Scheme for Cholesteric LCDs", SID 2008, 2008 SID INTERNATIONAL SYMPOSIUM, SOCIETY FOR INFORMATION DISPLAY, LOS ANGELES, USA, vol. XXXIX, 18 May 2008 (2008-05-18), pages 1869-1872, XP007016822, ISSN: 0008-966X * the whole document * -----	1	TECHNICAL FIELDS SEARCHED (IPC) G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	29 June 2012	Demin, Stefan

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
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E : earlier patent document, but published on, or after the filing date
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29-06-2012

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010156967 A1	24-06-2010	US 2010156967 A1	24-06-2010
		WO 2009037768 A1	26-03-2009
US 2003206147 A1	06-11-2003	EP 1359565 A2	05-11-2003
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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	寻址胆甾型液晶显示器的方法		
公开(公告)号	EP2571015A1	公开(公告)日	2013-03-20
申请号	EP2012161891	申请日	2012-03-28
[标]申请(专利权)人(译)	在现代informationssyst AEG		
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[标]发明人	BAYRLE REINER BADER OTTO BITTER THOMAS SUPRITZ CHRISTOPH WIEDEMANN MICHAEL		
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CPC分类号	G09G3/3629 G09G3/2025 G09G3/3622 G09G2300/0486 G09G2310/0245 G09G2320/0204		
优先权	2011181297 2011-09-14 EP		
外部链接	Espacenet		

摘要(译)

寻找具有以行和列排列的多个像素的胆甾型液晶显示器的方法，其中：寻址所述多个像素中的特定一个包括多个寻址相位;在所述多个寻址阶段中的每一个期间，施加行电压脉冲的序列RS，RNS和列电压脉冲的序列CON，COFF，CGRAY;所述序列RS，行电压脉冲的RNS和列电压脉冲的序列CON，COFF，CGRAY包括0伏，UL伏和UH伏的三个电压电平;在准备阶段期间，作为所述多个寻址阶段的第一寻址阶段，施加第一序列RS，行电压脉冲的RNS和列电压脉冲的第一序列CON，COFF，CGRAY;在所述准备阶段期间，UH仅包括在行电压脉冲的所述序列RS，RNS和列电压脉冲的所述序列CON，COFF，CGRAY中，其中0 <UL = UH。

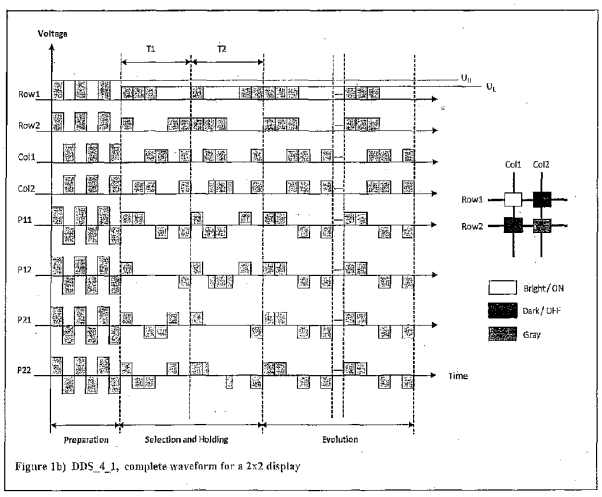

Figure 1b) DDS_4_1, complete waveform for a 2x2 display