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(54) Apparatus and method for automatic brightness control of a backlight of a liquid crystal display device

Vorrichtung und Verfahren zur automatischen Helligkeitssteuerung einer Rückbeleuchtung einer Flüssigkristallanzeigevorrichtung

Appareil et procédé de contrôle automatique de la luminosité d' un rétroéclairage d' un dispositif d'affichage à cristaux liquides

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Description

Field of the Invention

[0001] The present invention relates to a liquid crystal display (LCD) device, and more particularly to an apparatus and method for automatic brightness control for use in the LCD device.

Background of the Invention

[0002] An LCD or thin film transistor liquid crystal display (TFT-LCD) module is generally used as a display device in a system such as a portable computer, a television set, and a monitor. FIG. 1 shows a structure of a general LCD module 100. Referring now to FIG. 1, the LCD module 100 comprises an LCD panel 10 for displaying all sorts of information having a liquid crystal material between two glass substrates, a driving unit having driving circuits 20, 30 for driving the LCD panel 10 and a timing controller 40 for generating control signals to control the driving circuits 20, 30, a backlight 60 for guiding light to the LCD panel 10, and a chassis (not shown) for holding and protecting the LCD panel 10 and components of the backlight 60.

[0003] The backlight 60 includes an inverter 62, a fluorescent lamp 64 such as a cold cathode fluorescent tube (CCFT) or a hot cathode fluorescent tube (HCFT), and a plurality of sheets including a reflecting sheet 66 for guiding light to the front. The backlight 60 functions to guide light from the fluorescent lamp 64 to the LCD panel 10. The LCD panel 10 displays color images by shielding or passing light from the backlight 60 through each pixel therein in response to a signal voltage of respective corresponding pixel inputted from the driving circuits 20, 30.

[0004] FIG. 2 is a block diagram showing a conventional backlight brightness control scheme of the LCD module 100 when it is used as a display device in a portable computer or a desktop computer. The portable computer or desktop computer is generally driven by the direct current, whereas the backlight 60 is lit up on by the alternating current. Thus, it is essential for the LCD module 100 to have the inverter 62 for transforming the direct current into the alternating current as shown in the drawing. The inverter 62 includes a dimming circuit (not shown) to control the brightness of the fluorescent lamp 64 as well as to transform the direct current into the alternating current, as well known in the art.

[0005] Referring to FIG. 2, in the operation, as a brightness control command is inputted by the computer operation of user, a central processing unit (CPU) or main body 200 of the computer generates a brightness control voltage CTL_V for controlling brightness, to the inverter 62. In response to the brightness control voltage CTL_V from the main body 200, the dimming circuit of the inverter 62 controls an amount of current of the fluorescent lamp 64 to adjust the brightness of the backlight 60. For example, If the computer is a portable computer, the brightness control voltage CTL_V is within the range of 0 through 3.3 V. That is, when the brightness control voltage CTL_V is 0 V, a most dark brightness, i.e., black appears, and when the brightness control voltage CTL_V is 3.3 V, a most light brightness, i.e., white appears.

[0006] However, the conventional brightness control scheme of the LCD module is characterized that once the brightness is controlled, a value or level of the controlled brightness is unchanged even though the properties of data for each picture or frame to be displayed through the LCD module 100 vary. That is, the conventional brightness control scheme may raise a problem that increases the power consumption since the brightness is uniformly maintained regardless of a change in light and darkness between frames or a quick change of pictures or frames such as in motion images. Also, a picture of red (R) or blue (B) color of low transmissivity is not greatly brightened, no matter how much the brightness of the backlight may be increased. Therefore, in this case, the effect obtained through increasing the brightness is small compared to the power consumption increase.

Summary of the Invention

[0007] The present invention is implemented in the context of an improved apparatus and method for automatic brightness control for use in an LCD device, which can automatically control a brightness for each picture by controlling a duty rate for each picture automatically.

[0008] The improved apparatus and the method for automatic brightness control in the LCD device can properly accommodate a brightness control by a user request and an automatic brightness control for each picture without conflicts therebetween.

[0009] The improved apparatus and method for automatic brightness control for use in the LCD device can improve a contrast for each picture displayed through an LCD module.

[0010] The improved apparatus and method for automatic brightness control for use in the LCD device can reduce the power consumption of an LCD module, by controlling a brightness according to data characteristic for each picture.

[0011] It is an object of the present invention to provide an improved apparatus and a method for automatic brightness control for use in an LCD device, which can control a brightness of backlight corresponding to a state of red (R), green (G) and blue (B) colors of a picture to be displayed in the LCD device, and thereby reduce the power consumption of the LCD module.

[0012] This and other objects are provided, according to one aspect of the present invention, by an apparatus for automatic brightness control of a backlight of an LCD device according to the appended claim 1.

[0013] According to other aspect of the present invention, there is provided a method for automatic brightness control of a backlight of an LCD according to the appended claim 5.

[0014] Other preferred embodiments of the present invention are defined by the appended dependent claims.

Brief Description of the Drawings

[0015] The foregoing and other objects, features and advantages of the invention will become more apparent from the following detailed description of preferred embodiments thereof made with reference to the attached drawings.

FIG. 1 is a schematic perspective view showing a structure of a general LCD module.

FIG. 2 is a block diagram showing a conventional backlight brightness control scheme of an LCD module.

FIG. 3 is a block diagram showing a backlight brightness control scheme of an LCD module to which a preferred first embodiment of the present invention is applied.

FIG. 4 is a diagram showing waveforms of a variable brightness control voltage outputted from a duty controller and an R-C circuit when the backlight brightness control scheme of FIG. 3 is applied to the present invention.

FIG. 5 is a diagram showing waveforms of a variable brightness control voltage outputted from a duty controller and an R-C circuit when the backlight brightness control scheme of FIG. 3 is applied to the present invention.

FIG. 6 is a diagram showing a relation between the current and the brightness of a lamp linearly determined according to the variable brightness control voltage outputted from the duty controller and the R-C circuit when the backlight brightness control scheme of FIG. 3 is applied to the present invention.

FIG. 7 is a diagram showing a brightness for each color in a general 64 gray level TFT LCD.

FIG. 8 is a block diagram showing a duty controller in the backlight brightness control scheme of the LCD module which is in accordance with the first embodiment of the present invention shown in FIG. 3.

FIG. 9 is a flowchart showing an automatic brightness control program of the duty controller in the backlight brightness control scheme of the LCD module which can be used in the first embodiment of the present invention.

FIG. 10 a diagram showing the power consumption of the LCD module in the present invention monitored in real time.

FIG. 11 is a block diagram showing a backlight brightness control scheme of an LCD module in a second explanatory example.

FIG. 12 is a diagram showing the results of the backlight brightness control carried out by the backlight brightness control scheme of the LCD module shown in FIG. 11 and the results of the contrast display according thereto.

FIG. 13 is a diagram showing the power consumption when the backlight brightness is controlled by the backlight brightness control scheme of the LCD module shown in FIG. 11.

FIG. 14 is a block diagram showing a backlight brightness control scheme of an LCD module in a third explanatory example.

FIG. 15 is a block diagram showing a backlight brightness control scheme of an LCD module in a fourth explanatory example.

FIG. 16 is a diagram showing output waveforms at each of function blocks shown in FIG. 15.

FIG. 17 is a flowchart showing an automatic brightness control method which can be used in an LCD module in accordance with the present invention.

Detailed Description of Preferred Embodiments

[0016] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which explanatory examples and preferred embodiments of the invention are shown. Like numbers refer to like elements throughout.

[0017] In a first explanatory example, an LCD device automatically controls a brightness of backlight according to a duty rate signal generated in proportion to an average gray level of pixels to be displayed in the LCD device.

[0018] FIG. 3 is a block diagram showing a backlight brightness control scheme of an LCD module in accordance with this first explanatory example, which is applied to a portable computer or desktop computer. Referring to FIG. 3, the LCD module includes a timing controller 400 having a duty controller 420 for calculating an average of gray levels in terms of one horizontal line period, i.e., 1H, to one picture or frame to be displayed on the LCD module and generating a duty rate signal DUTY corresponding to the calculated average value of the gray levels, and an R-C circuit 500 for summating the duty rate signals DUTY generated in terms of 1H from the timing controller 400 during one frame and generating a variable brightness control voltage Vduty that changes the electric potential in proportion to the gray levels of the picture to be displayed. An inverter 62 connected to the R-C circuit 500 controls an amount of current of a fluorescent lamp 64 through a dimming circuit (not shown) to adjust brightness of the backlight in response to the variable brightness control voltage Vduty.

[0019] The operation of this LCD module will now be described in detail with reference with the drawings.

[0020] First, the timing controller 400 outputs pulse waves in terms of 1H. Each pulse wave has a duty rate corresponding to an average value of gray levels of pixel data for 1H. For example, in an LCD module with a VGA resolution having 640 pixels for 1H, if an average value of gray levels of all pixels for 1H is 'black', a duty rate signal DUTY of 0 % which outputs a logic high value as much as 0 pixel clock is generated. If an average value of gray levels of all pixels for 1H is 'white', a duty rate signal DUTY of 100 % which outputs logic high values as much as 640 pixel clocks is generated. Also, if an average value of gray levels of all pixels for 1H is 'middle' grade, a duty rate signal DUTY of 50 % is generated.

[0021] Tables 1 and 2 illustrated below show duty rates as percentages in an LCD module having a VGA resolution where the number of horizontal pixels is 640 and the number of an average gray level in 1 horizontal line is 16. In particular, Table 1 shows duty rates when a gamma constant is 1, whereas Table 2 shows duty rates when a gamma constant is 2.2.

[Table 1]

GRAY LEVEL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DUTY [%]	0	6.7	13.3	20	26.7	33.3	40.0	46.7	53.3	60.0	66.7	73.3	80.0	86.7	93.3	100
PIXEL CLOCK [Number]	0	43	85	128	171	213	256	299	341	384	427	469	512	555	597	640

[Table 2]

GRAY LEVEL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DUTY [%]	0	0.3	1.2	2.9	5.5	8.9	13.3	18.7	25.1	32.5	41.0	50.5	61.2	73.0	85.9	100
PIXEL CLOCK [Number]	0	2	8	19	35	57	85	120	161	208	262	32.3	392	467	550	640

[0022] In Tables 1 and 2, each duty rate indicates the number of pixels having logic high values for 1H as a percentage. Accordingly, the duty rate signals DUTY generated from the timing controller 400 output pulse waves, each of which has logic high values as much as the number of pixel clocks as illustrated in Tables 1 and 2 according to the average value of the gray levels of the pixel data for 1H.

[0023] In order to generate the duty rate signals DUTY, the duty controller 420 of the timing controller 400 includes a memory buffer register (MBR) or a storage register to calculate the average value of gray levels of pixel data for 1H. For example, supposing that in case a 4 bit pixel data able to indicate 16 gray levels is inputted, an average value of gray levels to 1H among data of 1 frame is calculated, first the duty controller 420 deletes data stored in the register every 1H. Then, the duty controller 420 receives a 4 bit pixel data, summates it to a value accumulated in the register and stores the summated result in the register. And then, until a 4 bit pixel data corresponding to the end of the 1 horizontal line is inputted, i.e., all 4 bit pixel data of the 1 horizontal line are inputted, the duty controller 420 repeats the summation operation as described above. Thereafter, when all 4 bit pixel data of the 1 horizontal line are inputted, the duty controller 420 selects 4 bit data of the highest rank among a data stored in the resistor and generates a duty rate signal DUTY for 1H outputting high values as much as the number of pixel clocks shown in Tables 1 and 2. Thus, the duty rate signal DUTY for the 4 bit data expressing the 16 gray levels is generated. In case of 6 or 8 bit pixel data, the duty control principle of the duty controller 420 can be applied as the 4 bit pixel data explained above.

[0024] When the duty controller 420 generates the duty rate signal DUTY corresponding to the average gray level in terms of 1H, the R-C circuit 500 accumulates the duty rate signals DUTY generated from the timing controller 400 over 1 frame and output a variable brightness control voltage Vduty according thereto.

[0025] The operation of the R-C circuit 500 will now be described in detail.

[0026] First, supposing that an initial charged voltage of a capacitor is Vo and a signal of 1H having an amplitude Vc and a high duration time T1, i.e., a high duty rate signal (D=T1/1H*100%) is outputted from the timing controller 400, a variable brightness control voltage Vduty outputted from the R-C circuit 500 every 1 H is defined as the following mathematical formula.

[Mathematical formula 1]

$$Vduty=\{Vo+(Vc-Vo)\times[1-EXP[-T1/(R\times C)]]\}\times EXP[(T1-1H)/(R\times C)]$$

[0027] As apparent from the formula, the variable brightness control voltage Vduty for controlling the brightness of the backlight has a voltage level in proportion to the high duration time T1 of the duty rate signal DUTY generated from the timing controller 400, and the response time of the variable brightness control voltage Vduty is determined by means of an RC time constant of the R-C circuit 500.

[0028] FIG. 4 is a diagram showing waveforms of the variable brightness control voltage Vduty outputted from the duty controller 420 and the R-C circuit 500 shown in FIG. 3. Referring to FIG. 4, graphs 1 and 2 show waveforms of the variable brightness control voltages Vduty of 0-15 gray levels (duty rate of 100%) and a middle gray level (duty rate of 50%), respectively, when the RC time constant is ten times as much as 1H. In this case, the variable brightness control voltage Vduty comes to a saturation state at 50H. This means that the duty rate of 50H is determined by means of the RC time constant of the R-C circuit 500.

[0029] FIG. 6 is a diagram showing a relation between the current and the brightness of the lamp 64 linearly determined according to the variable brightness control voltage Vduty outputted from the duty controller 420 and the R-C circuit 500 shown in FIG. 3. Referring to FIG. 6, when the variable brightness control voltage Vduty outputted from the R-C circuit 500 is used as an input voltage of the inverter 62 of the backlight, the inverter 62 generates a current CTL_I corresponding to the inputted variable brightness control voltage Vduty. The brightness of the backlight is determined in proportion to an amount of the current.

[0030] As apparent from the relation between the current and the brightness, the above described LCD module generates the variable brightness control voltage Vduty by automatically controlling duty rates for one picture to be displayed thereon, and adjusts the brightness of the backlight automatically by controlling the amount of current of the lamp 64 generated through the inverter 62 according to the variable brightness control voltage Vduty.

Embodiment 1

[0031] According to an aspect of the present invention, an LCD module can automatically control a brightness of backlight by generating a variable brightness control voltage having a duty rate corresponding to a color state of pixel data from a duty controller and controlling an amount of current of the backlight, i.e., a fluorescent lamp in response to the variable brightness control voltage. Alternatively, the LCD module can be set to generate the variable brightness control voltage having the duty rate corresponding to the average gray level of the pixel data from the duty controller, as described with reference to the first explanatory example, as well as to the color state of the pixel data.

[0032] Referring to FIG. 7, a brightness magnitude of white is obtained by summating brightness magnitudes of green (G), red (R) and blue (B). For example, if the brightness magnitudes of the three colors are 73.62, 29.45 and 21.24 respectively, the brightness magnitude of white comes to 124.3. This means that in a color filter of the TFT LCD, the transmissivity of R, G and B is determined in order of G > R > B. Accordingly, in an embodiment of the present invention, when R, G and B are displayed at a same gray level, the brightness magnitude is controlled to be lowered in order of G, R and B. That is, the brightness of the backlight is maximized at G, thereby to feel the picture or image more brightly. Also, the brightness of the backlight is set to be lowered at R and B to reduce the power consumption of the LCD module. The reason is that a picture of G which shows a high transmissivity is more brightly seen even though the brightness of the backlight is slightly increased, whereas pictures of R and B which show a low transmissivity are not bright enough compared with increase of the power consumption, however much the brightness may be increased.

[0033] FIG. 3 is a block diagram showing an LCD module to which a backlight brightness control scheme in accordance with the first embodiment of the present invention is applied. The composition and operation in the LCD module of the first embodiment is the same as the first explanatory example, except generating a variable brightness control voltage having a duty rate corresponding to a color state of pixel data from a duty controller and controlling an amount of current of the backlight according to the variable brightness control voltage. In a preferred embodiment, the transmissivity is set at a rate of G : R : B=1 : 0.66 : 0.49, so that pictures of G, R and B generate a maximum brightness, a half of the maximum brightness, and a quarter of the maximum brightness, respectively.

[0034] Referring to FIG. 3, the LCD module comprises a timing controller 400, an R-C circuit 500, an inverter 62, and a lamp 64.

[0035] The timing controller 400 includes a duty controller 420 and components of an integrated circuit of a general timing controller such as an input processor, a signal processor, a clock processor, and a data processor that are not shown in the drawing. The duty controller 420 generates a duty rate signal DUTY for controlling the brightness of the backlight automatically in response to a color state of a pixel data inputted from a host (not shown), for example,

[0036] As shown in FIG. 8, the duty controller 420 includes a pixel data acquisition and conversion unit 421, an adder 422, a summer 423, a divider 424, a duty register/down-counter 426, a pulse generator 427 and a control unit 428.

[0037] The pixel data acquisition and conversion unit 421, which has a plurality of memory registers, for example R, G, and B registers and accumulation registers, receives a pixel data R[5:0], G[5:0], B[5:0] from the host outputting a video information and generates a pixel data R'[5:0], G'[5:0], B'[5:0] converted according to a color state R, G, B through given processes S40 through S54 of FIG. 9. The adder 422 adds the converted pixel data R'[5:0], G'[5:0], B'[5:0] generated from the pixel data acquisition and conversion unit 421 and stores it. When the added pixel data SUM[7:0] is data for one horizontal line period 1 H, the summer 423 summates the accumulated data in the adder 422 and stores the summated result. The divider 424 divides the sum total TSUM[17:0] of the pixel data for 1H outputted from the summer 423 by a divisor, for example 3. The duty register/down-counter 426 loads 6 bit data MSB[15:10] of the highest rank among data outputted from the divider 424 and down-counts them. This can set, levels for controlling the brightness according to the color state, since the 6 bit data MSB[15:10] of the highest rank correspond to 64 gray levels of white through black. The pulse generator 427 outputs a duty rate signal DUTY corresponding to an output signal of the duty register/down-counter 426 to the R-C circuit 500.

[0038] The control unit 428 receives a pixel clock signal CLK and a video signal DE having an information of 1H from the host to clear the registers (not shown) of the pixel data acquisition and conversion unit 421 periodically, and generates load signals DATA_LOAD1, DATA_LOAD2, a clock signal DOWN_COUNT, control signals PIXEL_ADD, LINE_ADD, DIV for controlling the calculation operation such as addition, summation, and division, so as to control the operation of each component of the duty controller 420 properly.

[0039] The operation of the LCD module in accordance with the first embodiment will now be described.

[0040] First, an R, G, B data of 6 bits, for example a pixel data in which G[5:0] is 111111 and R[5:0] and B[5:0] are 000000 is inputted into the pixel data acquisition and conversion unit 421 from the host. The pixel data acquisition and conversion unit 421 then converts it into a pixel data in which G'[5:0], R'[5:0] and B'[5:0] are 111111 respectively, under the control of the control unit 428. And then, the adder 422 adds the converted pixel data, i.e., G'[5:0] + R'[5:0] + B'[5:0]. As a result, the added pixel data SUM[7:0] comes to 10111101. The summer 423 receives the added pixel data SUM[7:0] and accumulates them for 1H. For example, in case of a LCD module of an XGA having 1024 pixels for one horizontal line a data SUM[17:0] accumulated for 1H becomes to 101111010000000000, if a pixel data for 1H having G[5:0] of 111111 and R[5:0] and B[5:0] of 000000 is inputted.. Thereafter, the divider 424 divides the accumulated data TSUM[17:0] by 3. The result of dividing the accumulated data TSUM[17:0] by 3 is 1111110000000000. The duty register/down-counter 426 loads 6 bit data MSB[15:10] of the highest rank among data outputted from the divider 424, into a duty register therein, and down-counts them in response to a down-count clock signal DOWN_COUNT outputted from the control unit 428. At this time, the down-count clock signal DOWN_COUNT is a clock signal having a period divided a time of 1H by the number 2^6 (64) which can be presented by 6 bits. Accordingly, the pulse generator 427 outputs a duty rate signal DUTY corresponding to an output signal of the duty register/down-counter 426 while values of the duty register are down-counted. That is, the pulse generator 427 maintains an output signal in a high level state until the down-counted value of the duty register comes to 000000. For this, the pulse generator 427 can be formed of an 1 bit input OR gate in which each bit of the duty resistor is an input. Thus, when the pixel data in which G[5:0] is 111111 and R[5:0] and B[5:0] are 000000 is inputted, a duty rate signal of 100% which is in a high level state for 1H is outputted. Of course, when pixel data in which R[5:0] is 111111 and G[5:0] and B[5:0] are 000000, and B[5:0] is 111111 and G[5:0] and R[5:0] are 000000 are inputted, duty rate signals of 66% and 49% of a maximum brightness are respectively outputted for 1H.

[0041] Referring now to FIG. 3, the R-C circuit 500 generates a variable brightness control voltage Vduty in response to the duty rate signal DUTY from the duty controller 420. The duty rate signal DUTY has a duty rate determined according to the color state of the pixel data. For example, as described above, when the color state of the pixel data is green, red and blue, the duty rate signal DUTY has a duty rate of 100%, 66%, and 49% of the maximum brightness, respectively.

[0042] The inverter 62 receives the variable bright control voltage Vduty from the R-C circuit 500 and outputs a current CTL_I for controlling the brightness of the backlight 60, i.e., the fluorescent lamp 64. Accordingly, the brightness of the backlight 60 is automatically controlled in proportion to the current CTL_I.

[0043] Thus, in the LCD module of the invention, the duty controller 420 of the timing controller 400 outputs the duty rate signal Duty having the duty rate corresponding to the color state of the picture to be displayed, and the R-C circuit 500 generates the variable brightness control voltage Vduty according to the duty rate signal DUTY. The inverter 62 controls the amount of the current CTL_I of the fluorescent lamp 64 in response to the variable brightness control voltage Vduty to adjust the brightness of backlight 60 automatically.

[0044] FIGs. 5 and 6 are diagrams showing waveforms of the variable brightness control voltage Vduty and the output current CTL_I of the inverter 62.

[0045] Referring to FIGs. 5 and 6, the R-C circuit 500 outputs the variable brightness control voltage Vduty that is linearly determined in proportion to the duty rate signal DUTY. Accordingly, the inverter 62 generates the current CTL_I for controlling the brightness of the backlight determined linearly according to the variable brightness control voltage Vduty, and thereby the LCD module carries out an automatic brightness control function corresponding to the duty rate signal DUTY outputted according to the color state of R, G and B.

[0046] FIG. 9 is a flowchart showing an automatic brightness control program of the duty controller 420 of the LCD module which can be used the first embodiment of the present invention. The program which are carried out by the duty controller 420 are stored in an inner memory (not shown) of the control unit 428.

[0047] Referring to FIG. 9, first the control unit 428 clears R, G, B registers of the pixel data acquisition and conversion unit 421 (S40). The R, G, B registers then latches a pixel data R[5:0], G[5:0], B[5:0] outputted from the host (S42). And then, the control unit 428 determines whether a value of the G register is not 0 and values of the R, B registers are 0, respectively (S44). When the result of the step S44 is YES, the value of the G register is loaded into the R, G registers (S46) and otherwise, the control unit 428 determines whether a value of the R register is not 0 and values of the G, B registers are 0, respectively (S48). Continually, when the result of the step S48 is YES, a half of the value of the R register is loaded into the G, B registers (S50) and otherwise, the control unit 428 determines whether a value of the B register is not 0 and values of the R, G registers are 0, respectively (S52). When the result of the step S52 is YES, a quarter of the value of the B register is loaded into the R, G registers (S54). These steps show that the pixel data R[5:0], G[5:0], B[5:0] is transformed into a data R'[5:0], G'[5:0], B'[5:0] according to the color state thereof.

[0048] Continually, when the result of the step S52 is NO, the control unit 428 controls the adder 422 to add the values of the R, G, B registers (S56). Then, the control unit 428 determines whether the present pixel data is a last data of 1H (S58). When the determined result of the step S58 is No, the operation step is returned to the second step S42 to repeat the operations of S42 through S56 as described above.

[0049] And then, when the result of the step S58 is YES, the divider 424 divides an accumulated data TSUM[17:0] of the R, G, B registers by 3 and the duty register/down-counter 426 stores 6 bit data MSB[15:10] of the highest rank among data outputted from the divider 424, in the duty register (S60). Continually, the duty register/down-counter 426 down-counts the values MSB[15:10] of the duty register (S62).

[0050] The pulse generator 427 determines whether the down-counted value of the duty register is 0 (S64). In result, when it is NO, the pulse generator 427 outputs a duty rate signal DUTY corresponding to the down-counted value of the duty register and otherwise, the program is ended.

[0051] The operation of the control unit 428 will now be described in detail by using an example which the pixel data of R, G, B explained with reference to FIG. 8 are 6 bit data, respectively.

[0052] First, the control unit 428 clears the R, G, B registers of the pixel data acquisition and conversion unit 421. The R, G, B registers then latches a pixel data R[5:0], G[5:0], B[5:0] outputted from the host.

[0053] At this time, when a value of the G register is not 0 and values of the R, B registers are 0 respectively, the value of the G register is loaded in the R, G registers. When a value of the R register is not 0 and values of the G, B registers are 0 respectively, a half of the value of the R register is loaded in the G, B registers. Also, when a value of the B register is not 0 and values of the R, G registers are 0 respectively, a quarter of the value of the B register is loaded in the R, G registers. For example, in case of 6 bit pixel data, when a value G[5:0] of the G register is 101010 and values R[5:0], B[5:0] of the R, B registers are 000000 respectively, each of the R, G, B registers loads 101010 which is the value G[5:0] of the G register. When a value R[5:0] of the R register is 101010 and values G[5:0], B[5:0] of the G, the B register are 000000 respectively, the R register loads 101010 and the G, B registers load 010101 that is a half of the value R[5:0] of the R register. In other words, the value R[5:0] of the R register is shifted one bit to the right. Also, when a value B[5:0] of the B register is 101010 and values R[5:0], G[5:0] of the R, G registers are 000000 respectively, the B register loads 101010 and the R, G registers load 001010 which is a quarter of the value B[5:0] of the B register. In other words, the value B[5:0] of the B register is shifted two bits to the right. In cases other than the three cases explained above, the operations are skipped.

[0054] Continually, the control unit 428 controls the adder 422 to add the values of R, G, B registers. The added value SUM[7:0] is then accumulated in the R, G, B registers. And then, the divider 424 divides the accumulated data TSUM[17:0] of the R, G, B registers by 3 and the duty register/down-counter 426 stores 6 bit data MSB[15:10] of the highest rank among data outputted from the divider 424, in the duty register. In succession, the duty register/down-counter 426 down-counts the values [15:10] of the duty register and at the same time, the pulse generator 427 outputs a duty rate signal DUTY having a duty rate corresponding to the value of the duty register that outputs signal of logic 1, until the down-counted value of the duty register comes to 000000. At this time, the duty rate signal DUTY has a period of 1H. Also, the down-count clock signal DOWN_COUNT is a clock signal having a period divided a time of 1H by the number 2^6 (64) which can be presented by 6 bits.

[0055] Supposing that in case of a pixel data of white in which R[5:0], G[5:0], B[5:0] are 111111 respectively, the result of converted pixel data, i.e., R'[5:0]+G'[5:0]+B'[5:0] is 189 and a duty rate is 100%, when a pixel data G[5:0] is 111111 and pixel data R[5:0], B[5:0] are 000000 respectively, a converted pixel data R'[5:0], G'[5:0], B'[5:0] of the R, G, B registers come to 111111 respectively and R'[5:0]+G'[5:0]+B'[5:0] comes to 189, to generate a duty rate signal DUTY of 100%. Also, when a pixel data R[5:0] is 111111 and pixel data G[5:0], B[5:0] are 000000 respectively, a converted pixel data R'[5:0] of the R register comes to 111111 and converted data G'[5:0], B'[5:0] of the G, B registers come to 011111 respectively and R'[5:0]+G'[5:0]+B'[5:0] comes to 125 and generate a duty rate signal DUTY of 66%. Also, when a pixel data B[5:0] is 111111 and pixel data R[5:0], G[5:0] are 000000 respectively, a converted pixel data B'[5:0] of the B register becomes 111111 and converted data R'[5:0], G'[5:0] of the R, G registers become 001111 respectively, rendering R'[5:0]+G'[5:0]+B'[5:0] as 93 and generate a duty rate signal DUTY of 49%. That is, when a brightness of one of R, G and B is white, the duty rate signals having the duty rates of 66%, 100%, and 49% respectively are generated. Thus, according to the color state of R, G and B, a different brightness is outputted. Particularly, a brightness magnitude is reduced in the order of G, R and B, so that a contrast for each picture displayed on the LCD module can be improved and the power consumption can be reduced.

[0056] FIG. 10 shows the results of monitoring the power consumption in real time when motion images, for example, a file of DVD format are played. As shown in FIG. 10, the power consumption of the LCD module in accordance with the present invention was about 4.1 W, whereas the power consumption of the conventional brightness control method was 5.4W. Accordingly, the present invention can reduce an average power consumption of about 1.3W, compared to the conventional brightness control method. Also, as shown in the below Table 3, a driving time of battery in the present invention is extended about 2.23 hours compared with the conventional brightness control method when the same batteries having a power capacity of 38Wh were used.

[Table 3]

	The average power consumption	The driving time of battery
The conventional method	5.4W	7.04h
The invention	4.1W	9.27h
Improvements	1.3W reduced	2.23h lengthened

[0057] In a second explanatory example, an LCD module as in the present invention can perform a brightness control requested by a user as well as an automatic brightness control for each picture. For this, the LCD module includes a merging circuit that accommodates two control functions without conflicts. The composition of the LCD module having the merging circuit will now be explained.

[0058] FIG. 11 is a block diagram showing a backlight brightness control scheme of an LCD module as in this second explanatory example when it is used as a display device in a portable computer or a desk top computer. Referring to the drawing, the composition of the LCD module shown in FIG. 11 is the same as that of the LCD module shown in FIG.

3 except for a merging circuit 600 that generates a variable brightness control voltage Vduty to the R-C circuit 500 in response to the brightness control voltage CTL_V generated from a CPU or main body 200 of the computer and the duty rate signal DUTY generated from the duty controller 420 disposed in the timing controller 400. Accordingly, for facilitating the explanation, like numbers refer to like blocks having same function throughout. The explanation for the like blocks will not be repeated.

[0059] The merging circuit 600 includes a first transistor T1 having a base for receiving a duty rate signal DUTY in the terms of 1H connected to the timing controller 400 through the resistor R3, an emitter connected to an input end of the R-C circuit 500, and a collector for receiving the brightness control voltage from the main body 200 of the computer. The emitter of the first transistor T1 is connected to a ground through a resistor R2. The first transistor T1 is composed of an NPN transistor. Here should be noted that the first transistor T1 forming the merging circuit is explained as an example, and other circuit elements such as NMOS transistors and operational amplifiers can be used to form it depending on the circuit design.

[0060] The first transistor T1 of the merging circuit 600 functions as a gating circuit for receiving the brightness control voltage CTL_V generated from the main body 200 of the computer and the duty rate signal DUTY generated from the duty controller 420, and outputting the brightness control voltage CTL_V selectively to the R-C circuit 500 when the duty rate signal DUTY is a high level. The R-C circuit 500 receives the brightness control voltage CTL_V selectively outputted from the merging circuit 600 to charge the capacitor C1, and generates a variable brightness control voltage Vduty by means of voltage charged to the capacitor C1. Here, it should be noted that the brightness control voltage CTL_V generated from the main body 200 of the computer can be freely set within the range of a given value by user and an electric potential of the variable brightness control voltage Vduty outputted through the R-C circuit 500 in the merging circuit 600 varies according to a gray level or/and a color state of a picture to be displayed.

[0061] For example, when a brightness control voltage CTL_V of 2V generated from the main body 200 of the computer is outputted to a terminal of the collector of the first transistor T1, the merging circuit 600 outputs a brightness control voltage CTL_V in response to a duty rate signal DUTY inputted to the base of the first transistor T1. The R-C circuit 500 charges the capacitor C1 by means of the brightness control voltage CTL_V selectively outputted according to the duty rate signal DUTY and outputs a voltage of 0-2V charged to the capacitor C1 as a variable brightness control voltage Vduty. Also, when a brightness control voltage CTL_V of 1V generated from the main body 200 of the computer is outputted to the terminal of the collector of the first transistor T1, the merging circuit 600 outputs a variable brightness control voltage Vduty of 0-1V through the R-C circuit 500 in response to a duty rate signal DUTY inputted to the base of the first transistor T1.

[0062] The duty rate signal DUTY inputted to the base of the first transistor T1 cannot only generate at the timing controller 400, but also at the LCD panel or a graphic controller (not shown) in the main body 200 of the computer. Accordingly, the merging circuit 600 can be disposed in the LCD panel or the main body 200 of the computer as well as a circuit substrate for the inverter 62 in the LCD module.

[0063] FIG. 12 is a diagram showing the results of the backlight brightness control performed by the LCD module shown in FIG. 11 and the results of the contrast display FIG. 13 is a diagram showing the power consumption according to the backlight brightness control performed by the LCD module shown in FIG. 11.

[0064] Referring to FIG. 12, it can be appreciated from the results of the backlight brightness control carried out by the LCD module of the present invention that in a dark picture such as 'black', the brightness of the invention was lower than that of the conventional technique, in a light picture such as 'white', the brightness of the invention was the same as that of the conventional technique, and 'contrast' showing the contrast of 'black' and 'white' in the invention was evidently higher than that of the conventional technique. Consequently, in the LCD module of the present invention, the contrast of 'black' and 'white' is more distinct, so that pictures to be displayed through the LCD module can be more lively felt.

[0065] Referring to FIG. 13, when the dark picture such as 'black' was displayed, the power consumption of the LCD module of the invention decreases by 2.2W than the conventional technique. When a picture such as 'mosaic pattern' representing the display of a general picture was displayed, the power consumption of the invention decreases by 0.9W than the conventional technique. Thus, since the LCD module of the present invention includes the merging circuit 600, the brightness for each picture can be actively controlled within the range of the brightness control voltage determined from the main body 200 of the computer.

[0066] In a third explanatory example, a PNP transistor can replace the NPN transistor T1 of the merging circuit 600. The composition of the merging circuit including the PNP transistor is shown in FIG. 14.

[0067] FIG. 14 is a block diagram showing a backlight brightness control scheme of an LCD module as in this third explanatory example when it is used as a display device in a portable computer or a desk top computer. Referring to FIG. 14, the composition of the LCD module is the same as that of the LCD module shown in FIG. 11 except for a merging circuit 600' having the PNP transistor T2 instead of the merging circuit 600 having the NPN transistor T1, and an R-C circuit 500' having a resistor R6 connected to an output end thereof. Accordingly, for facilitating the explanation, like numbers refer to like blocks having same function throughout. The explanation for the like blocks will not be repeated.

[0068] The merging circuit 600' includes a second transistor T2 having an emitter for receiving a brightness control voltage CTL_V from the main body 200 of the computer through a resistor R4, a base for receiving a duty rate signal DUTY in the terms of 1H connected to a timing controller 400 through a resistor R7, and a collector connected to a ground. The emitter of the second transistor T2 is connected to an input end of the R-C circuit 500'.

[0069] The second transistor T2 of the merging circuit 600' functions as a gating circuit for receiving the brightness control voltage CTL_V generated from the main body 200 of the computer and the duty rate signal DUTY generated from the duty controller 420, and outputting the brightness control voltage CTL_V selectively to the R-C circuit 500' when the duty rate signal DUTY is a high level. The R-C circuit 500' receives the brightness control voltage CTL_V selectively outputted from the merging circuit 600' to charge the capacitor C2, and generates a variable brightness control voltage Vduty by means of voltage charged to the capacitor C2. It should be noted that the brightness control voltage CTL_V generated from the main body 200 of the computer can be freely set within the range of a given value by user and an electric potential of the variable brightness control voltage Vduty outputted through the R-C circuit 500' changes according to a gray level or/and a color state of a picture to be displayed. The resistor R6 connected to an output end of the R-C circuit 500' distributes the variable brightness control voltage Vduty outputted through the R-C circuit 500' at a given rate.

[0070] Here, it should be noted that in the drawing, the second transistor T2 is illustrated as a PNP transistor, but it is explained as an example and other circuit elements such as NMOS transistors and operational amplifiers can be used to form it according to the circuit design method.

[0071] In the LCD module described above, when a brightness control voltage CTL_V of 0V generated from the main body 200 of the computer is outputted, a variable brightness control voltage Vduty of 0V cannot be outputted to the R-C circuit 500' due to a base-emitter voltage Vbe of the second transistor T2 in the merging circuit 600'. Accordingly, to remove the influence of the base-emitter voltage Vbe, a level shifter is added in the LCD module, as shown in FIG. 15.

[0072] FIG. 15 is a block diagram showing a backlight brightness control scheme of an LCD module as in a fourth explanatory example when it is used as a display device in a portable computer or a desk top computer. Referring to FIG. 15, the composition of the LCD module is similar to the LCD module shown in FIG. 14 except for a level shifter 700 interposed between the timing controller 400 and the merging circuit 600'. Accordingly, for facilitating the explanation, like numbers refer to like blocks having same function throughout. The explanation for the like blocks will not be repeated.

[0073] The level shifter 700 includes an NPN type third transistor T3 having an emitter connected to an input end of the merging circuit 600', a base connected to the timing controller 400 through a resistor R8, and a collector connected to a power source voltage V_{DD}, a resistor R9 having one end connected to the emitter, a diode D1 connected between the other end of the resistor R9 and a ground or earth, and a resistor R10 connected between the other end of the resistor R9 and a turn-off voltage Voff end of transistor.

[0074] The level shifter 700 generates a drop in voltage as much as a base-emitter voltage Vbe of the third transistor T3 on a current path comprising the ground, the diode D1, the resistors R9, R10, and the turn-off voltage Voff, for example, a voltage of below -5V, of the transistor and provides its drop value to a terminal of the emitter of the third transistor T3 and the resistor R9. Consequently, the transistor T2 of the merging circuit 600' is fully swung, so that even though a brightness control voltage CTL_V of 0V is outputted, a variable brightness control voltage Vduty of 0V can be outputted to the R-C circuit 500'.

[0075] The operation of the LCD module having the level shifter 700 will he explained with reference to FIG. 16 showing output wave forms at each node.

[0076] First, a duty rate signal DUTY of 0 to 3V generated from the timing controller 400 is inputted to the level shifter 700. When the duty rate signal DUTY is 0V, the level shifter 700 outputs a level shift voltage Vshift of -0.6V, i.e., -Vbe, whereas when the duty rate signal DUTY is 3V, i.e., the power source voltage V_{DD} level, the level shifter 700 outputs a level shift voltage Vshift of 3V-Vbe, i.e., 2.4V. That is, the level shifter 700 generates the level shift voltage Vshift of -0.6 to 2.4V in response to the duty rate signal DUTY of 0 to 3V.

[0077] Next, when the level shift voltage Vshift generated from the level shifter 700 is inputted to the merging circuit 600' having the PNP transistor T2, the R-C circuit 500' outputs a variable brightness control voltage Vduty. For example, when the level shift voltage Vshift of -0.6V, i.e., -Vbe is inputted, an electrical potential of the emitter of the PNP transistor T2 becomes -0.6V(-Vbe)+Vbe to output a brightness control voltage CTL_V' of 0V. When the level shift voltage Vshift of 2.4V is inputted, the PNP transistor T2 outputs a brightness control voltage CTL_V' of 3V to the R-C circuit 500'. The emitter voltage CTL_V' of the PNP transistor T2, i.e., the brightness control voltage generated from the main body 200 of the computer is charged through the R-C circuit 500' and then outputted as a variable brightness control voltage Vduty. The variable brightness control voltage Vduty is outputted to the inverter 62 to control the brightness of the backlight. At the emitter voltage CTL_V' of FIG. 16, dotted lines show ranges of the brightness control voltage that can be controlled by user. Accordingly, the brightness of the backlight is automatically controlled within the ranges.

[0078] FIG. 17 is a flowchart showing an automatic brightness control method of the LCD module which can be used in the present invention. Referring to FIG. 17, the duty controller 420 of the timing controller 400 calculates an average value of gray levels in terms of 1H, to pixel data to be displayed in one picture (S10). In the present invention, at the step S10, the duty controller 420 can additionally carry out an operation for determining a color state of the pixel data for 1H. Then, the duty controller 420 generates a duty rate signal DUTY corresponding to the calculated average value of the gray levels or/and the determined color state to the merging circuit 600, 600' (S12). And then, the merging circuit 600, 600' generates a variable brightness control voltage Vduty in response to the duty rate signal DUTY and a brightness control voltage generated from the main body 200 of the computer, and the inverter 62 receives the variable brightness control voltage Vduty to control the brightness of the backlight automatically (S14).

[0079] Thus, an LCD module as used in the present invention may merge the duty rate signals DUTY generated from the duty controller 420 of the timing controller 400 and the brightness control voltage CTL_V generated from the main body 200 of the computer by user setting, to control the brightness of the backlight automatically. As a result, as shown in FIGs. 12 and 13, the contrast for each picture displayed on the LCD module can be improved and thereby the power consumption can be reduced.

[0080] As apparent from the foregoing description, such an LCD module can automatically control the brightness for each picture by controlling the duty rate for each picture automatically.

[0081] Also, such an LCD module can properly combine the brightness control by a user request and the automatic brightness control function for each picture without conflicts.

[0082] Further, the contrast for each picture displayed in the LCD module can be improved, and thereby the power consumption of the LCD module can be reduced. The present invention can control the brightness of the backlight automatically by generating the variable brightness control voltage having the duty rate corresponding to the color state of pixel data from the duty controller, and thereby reduce the power consumption of the LCD module to extend battery usage in the system such as the portable computer.

[0083] Also, such an LCD module can control to feel pictures or images more brightly and thereby to experience a cubic effect when the pictures are changed from a dark color to a bright color since a brightness change of white and black for R, G and B colors is greatly enhanced by controlling the brightness according to the color state of R, G, and B of the pixel data.

[0084] In the drawings and specification, there have been disclosed explanatory examples and typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purpose of limitation, the scope of the invention being set forth in the appended claims.

Claims

1. An apparatus for automatic brightness control of a backlight (64) of an LCD device displaying video data, comprising:

    control signal generating means configured to receive video data comprising a plurality of frames of pixel data; wherein the control signal generating means comprises:

        a timing controller (400) including a duty controller (420) configured to determine color states of said pixel data, and calculate an average of color states for each horizontal line and generate a duty rate signal corresponding to the calculated average of the color states; and
        an R-C circuit (500) configured to sum the duty rate signals over one frame and generate a brightness control signal for controlling a brightness of the backlight to correspond to the determined color state of the frame;

    and an inverter (62) configured to control the brightness of the backlight automatically in response to said brightness control signal from said control signal generating means.

2. The apparatus for automatic brightness control according to claim 1, wherein the duty rate signal has a duty rate reduced in order of green, red, and blue when the determined color state is green, red, and blue.

3. The apparatus for automatic brightness control according to claim 2, wherein the duty rate of the duty rate signal is set to have a rate of green : red : blue = 1 : 0.66 : 0.49 when the determined color state is green, red, and blue.

4. The apparatus for automatic brightness control according to any one of the preceding claims, wherein said duty controller (420) includes:

    a control unit (428) configured to control various operations of said duty controller to determine the color state of the pixel data and to generate the duty rate signal;
    a pixel data acquisition and conversion unit (421) configured to receive the pixel data and convert the pixel data according to the determined color state, under the control of said control unit (428);

a computing unit (425) configured to receive the converted pixel data and calculate an average of color states for each horizontal line, under the control of said control unit, the computing unit consisting of a summer (423), configured to summate the converted pixel data and store the summated result, and of a divider (424), configured to generate the output of the computing unit by dividing that summated result by a divisor;
a duty register (426) configured to store 6 bit data of the highest rank among data output from the computing unit (425) and count down the values of the duty register under the control of said control unit; and
a pulse generator (427) configured to generate the duty rate signal corresponding to an output signal of said duty register until the value of the duty register is zero.

5. A method for automatic brightness control of a backlight (64) of an LCD device displaying video data, comprising the steps of:

receiving video data comprising a plurality of frames of pixel data;
determining color states of the pixel data;
converting the pixel data according to the determined color state;
determining whether the pixel data is a last data of one horizontal line period;
outputting a duty rate signal corresponding to a calculated average of color states of the pixel data in the horizontal line period; and
summing the duty rate signals over one frame in an R-C circuit to generate a brightness control signal; and
controlling a brightness of the backlight in response to the brightness control signal.

6. The method for automatic brightness control according to claim 5, wherein said converting step further comprises converting said pixel data into data corresponding to a brightness reduced in order of green, red, and blue when the determined color state is green, red, and blue.

7. The method for automatic brightness control according to claim 6, wherein the pixel data are converted into data corresponding to 100%, 66% and 49% of the maximum brightness when the determined color state is green, red, and blue, respectively.

Patentansprüche

1. Vorrichtung zur automatischen Helligkeitsregelung einer Hintergrundbeleuchtung (64) einer LCD-Einrichtung, die Videodaten anzeigt, Folgendes umfassend:

ein Steuersignal-Erzeugungsmittel, konfiguriert zum Empfangen von Videodaten, die eine Vielzahl von Teilbildern von Pixeldaten umfassen;
worin das Steuersignal-Erzeugungsmittel Folgendes umfasst:

eine Zeitsteuereinrichtung (400), die einen Tastverhältniscontroller (420) einschließt, konfiguriert zum Bestimmen von Farbzuständen der Pixeldaten und Berechnen eines Mittelwerts von Farbzuständen für jede Horizontalzeile und Erzeugen eines Tastverhältnissignals, das dem berechneten Mittelwert der Farbzustände entspricht; und
eine RC-Schaltung (500), konfiguriert zum Summieren der Tastverhältnissignale über ein Teilbild und Erzeugen eines Helligkeitssteuersignals zum Steuern einer Helligkeit der Hintergrundbeleuchtung, damit sie dem bestimmten Farbzustand des Teilbilds entspricht;
und einen Inverter (62), konfiguriert zum automatischen Steuern der Helligkeit der Hintergrundbeleuchtung als Antwort auf das Helligkeitssteuersignal vom Steuersignal-Erzeugungsmittel.

2. Vorrichtung zur automatischen Helligkeitsregelung nach Anspruch 1, worin das Tastverhältnissignal ein Tastverhältnis hat, das in der Reihenfolge Grün, Rot und Blau reduziert wird, wenn der bestimmte Farbzustand Grün, Rot und Blau ist.

3. Vorrichtung zur automatischen Helligkeitsregelung nach Anspruch 2, worin das Tastverhältnis des Tastverhältnissignals so eingestellt wird, dass es ein Grün-Rot-Blau-Verhältnis = 1 : 0,66 : 0,49 hat, wenn der bestimmte Farbzustand Grün, Rot und Blau ist.

4. Vorrichtung zur automatischen Helligkeitsregelung nach einem der vorhergehenden Ansprüche, worin der Tastverhältniscontroller (420) Folgendes einschließt:

eine Steuereinheit (428), konfiguriert zum Steuern von verschiedenen Operationen des Tastverhältniscontrollers zum Bestimmen des Farbzustands der Pixeldaten und Erzeugen des Tastverhältnissignals;
eine Pixeldatenerfassungs- und Konvertierungseinheit (421), konfiguriert zum Empfangen der Pixeldaten und Konvertieren der Pixeldaten gemäß dem bestimmten Farbzustand unter der Steuerung der Steuereinheit (428);
eine Recheneinheit (425), konfiguriert zum Empfangen der konvertierten Pixeldaten und Berechnen eines Mittelwerts von Farbzuständen für jede Horizontalzeile unter der Steuerung der Steuereinheit, wobei die Recheneinheit aus einem Summierer (423) besteht, konfiguriert zum Summieren der konvertierten Pixeldaten und Speichern des summierten Ergebnisses, und einem Dividierer (424), konfiguriert zum Erzeugen der Ausgabe der Recheneinheit durch Dividieren dieses summierten Ergebnisses durch einen Divisor;
ein Tastverhältnisregister (426), konfiguriert zum Speichern von 6 Bitdaten des höchsten Ranges aus Datenausgabe von der Recheneinheit (425) und Rückwärtszählen der Werte des Tastverhältnisregisters unter der Steuerung der Steuereinheit; und
einen Impulsgenerator (427), konfiguriert zum Erzeugen des Tastverhältnissignals, das einem Ausgangssignal des Tastverhältnisregisters entspricht, bis der Wert des Tastverhältnisregisters null ist.

5. Verfahren zur automatischen Helligkeitsregelung einer Hintergrundbeleuchtung (64) einer LCD-Einrichtung, die Videodaten anzeigt, die folgenden Schritte umfassend:

Empfangen von Videodaten, die eine Vielzahl von Teilbildern von Pixeldaten umfassen;
Bestimmen von Farbzuständen der Pixeldaten;
Konvertieren der Pixeldaten gemäß dem bestimmten Farbzustand;
Bestimmen, ob die Pixeldaten letzte Daten einer Horizontalzeilenperiode sind;
Ausgeben eines Tastverhältnissignals, das einem berechneten Mittelwert von Farbzuständen der Pixeldaten in der Horizontalzeilenperiode entspricht; und
Summieren der Tastverhältnissignale über ein Teilbild in einer RC-Schaltung zum Erzeugen eines Helligkeitssteuersignals; und
Steuern einer Helligkeit der Hintergrundbeleuchtung als Antwort auf das Helligkeitssteuersignal.

6. Verfahren zur automatischen Helligkeitsregelung nach Anspruch 5, worin der Konvertierungsschritt außerdem das Konvertieren der Pixeldaten in Daten umfasst, die einer Helligkeit entsprechen, die in der Reihenfolge Grün, Rot und Blau reduziert wird, wenn der bestimmte Farbzustand Grün, Rot und Blau ist.

7. Verfahren zur automatischen Helligkeitsregelung nach Anspruch 6, worin die Pixeldaten in Daten konvertiert werden, die 100%, 66% und 49% der maximalen Helligkeit entsprechen, wenn der bestimmte Farbzustand Grün, Rot bzw. Blau ist.

Revendications

1. Appareil permettant une commande automatique de luminosité d'un éclairage arrière (64) d'un dispositif LCD affichant des données vidéo, comprenant :

un moyen de génération de signal de commande configuré pour recevoir des données vidéo comprenant une pluralité de trames de données de pixel ;
dans lequel le moyen de génération de signal de commande comprend :

un contrôleur de temporisation (400) comprenant un contrôleur de service (420) configuré pour déterminer des états de couleur desdites données de pixel, et calculer une moyenne des états de couleur pour chaque ligne horizontale et générer un signal de vitesse de service correspondant à la moyenne calculée des états de couleur ; et
un circuit R-C (500) configuré pour additionner les signaux de vitesse de service pour une trame et générer un signal de commande de luminosité permettant de commander une luminosité de l'éclairage arrière de manière à ce qu'elle corresponde à l'état de couleur déterminé de ladite trame ;
et un convertisseur (62) configuré pour commander la luminosité de l'éclairage arrière de manière automatique en réaction audit signal de commande de luminosité provenant dudit moyen de génération de signal de commande.

2. Appareil permettant une commande automatique de luminosité selon la revendication 1, dans lequel le signal de vitesse de service présente une vitesse de service réduite dans un ordre vert, rouge, et bleu lorsque l'état de couleur déterminé est vert, rouge, et bleu.

3. Appareil permettant une commande automatique de luminosité selon la revendication 2, dans lequel la vitesse de service du signal de vitesse de service est ajustée afin de présenter un taux de vert : rouge : bleu = 1 : 0,66 : 0,49 lorsque l'état de couleur déterminé est vert, rouge, et bleu.

4. Appareil permettant une commande automatique de luminosité selon l'une quelconque des revendications précédentes, dans lequel ledit contrôleur de service (420) comprend :

une unité de commande (428) configurée pour commander diverses actions dudit contrôleur de service afin de déterminer l'état de couleur des données de pixel et générer le signal de vitesse de service ;
une unité d'acquisition et de conversion de données de pixel (421) configurée pour recevoir les données de pixel et convertir les données de pixel en fonction de l'état de couleur déterminé, sous le contrôle de ladite unité de commande (428) ;
une unité de calcul (425) configurée pour recevoir les données de pixel converties et calculer une moyenne des états de couleur pour chaque ligne horizontale, sous le contrôle de ladite unité de commande, l'unité de calcul étant constituée d'un additionneur (423), configuré pour additionner les données de pixel converties et stocker le résultat additionné, et d'un diviseur (424), configuré pour générer la sortie de l'unité de calcul grâce à une division dudit résultat additionné par un diviseur ;
un registre de service (426) configuré pour stocker des données 6 bits du rang le plus élevé parmi la sortie de données en provenance de l'unité de calcul (425) et décompter les valeurs du registre de service sous le contrôle de ladite l'unité de commande ; et
un générateur d'impulsions (427) configuré pour générer le signal de vitesse de service correspondant à un signal de sortie dudit registre de service jusqu'à ce que la valeur du registre de service soit égale à zéro.

5. Procédé permettant une commande automatique de luminosité d'un éclairage arrière (64) d'un dispositif LCD affichant des données vidéo, comprenant les étapes consistant à :

recevoir des données vidéo comprenant une pluralité de trames de données de pixel ;
déterminer des états de couleur des données de pixel ;
convertir les données de pixel en fonction de l'état de couleur déterminé ;
déterminer si les données de pixel sont au moins des données d'une période de ligne horizontale ;
produire un signal de vitesse de service correspondant à une moyenne calculée d'états de couleur de données de pixel dans la période de ligne horizontale ; et
additionner les signaux de vitesse de service pour une trame dans un circuit R-C afin de générer un signal de commande de luminosité ; et
commander une luminosité de l'éclairage arrière en réaction au signal de commande de luminosité.

6. Procédé permettant une commande automatique de luminosité selon la revendication 5, dans lequel ladite étape de conversion comprend en outre une étape consistant à convertir lesdites données de pixel en données qui correspondent à une luminosité réduite dans un ordre vert, rouge, et bleu lorsque l'état de couleur déterminé est vert, rouge, et bleu.

7. Procédé permettant une commande automatique de luminosité selon la revendication 6, dans lequel les données de pixel sont converties en données qui correspondent à 100 %, 66 % et 49 % de la luminosité maximale lorsque l'état de couleur déterminé est vert, rouge, et bleu, respectivement.

Fig. 1

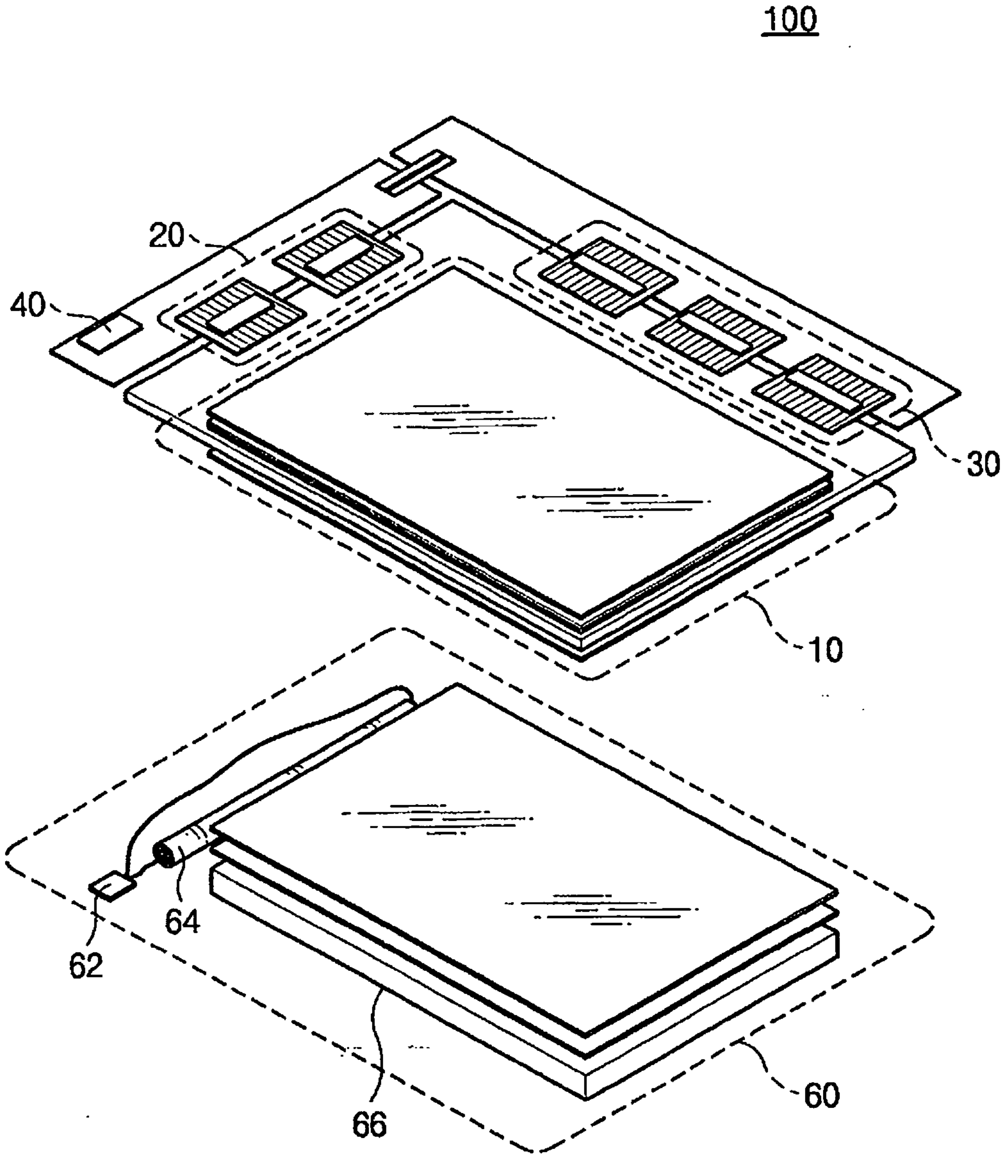


Fig. 2

(Prior Art)

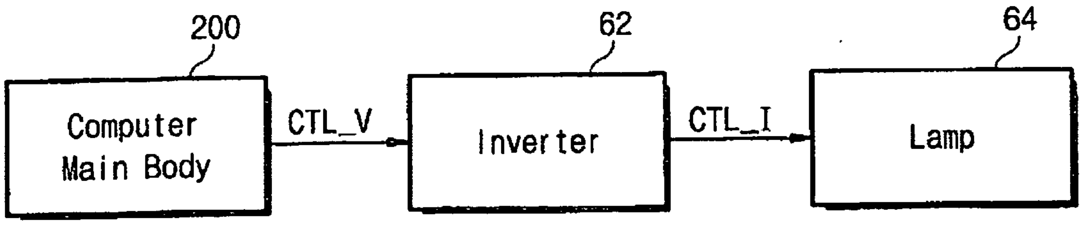


Fig. 3

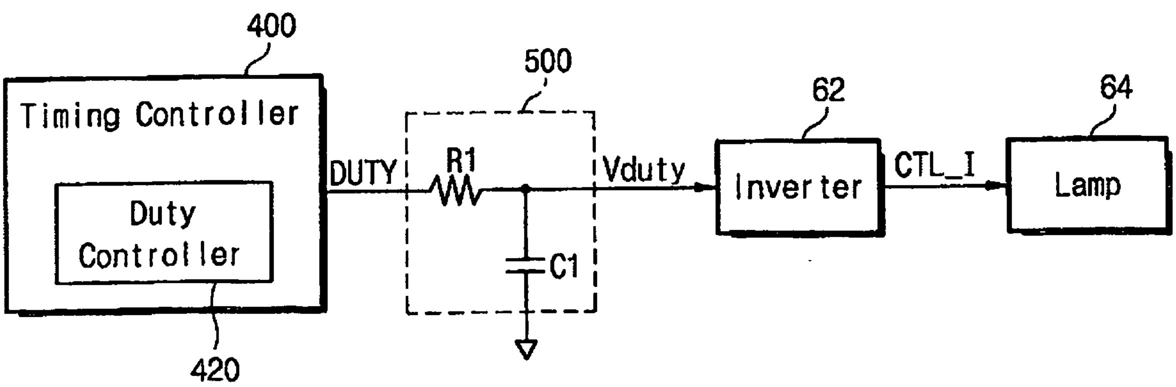


Fig. 4

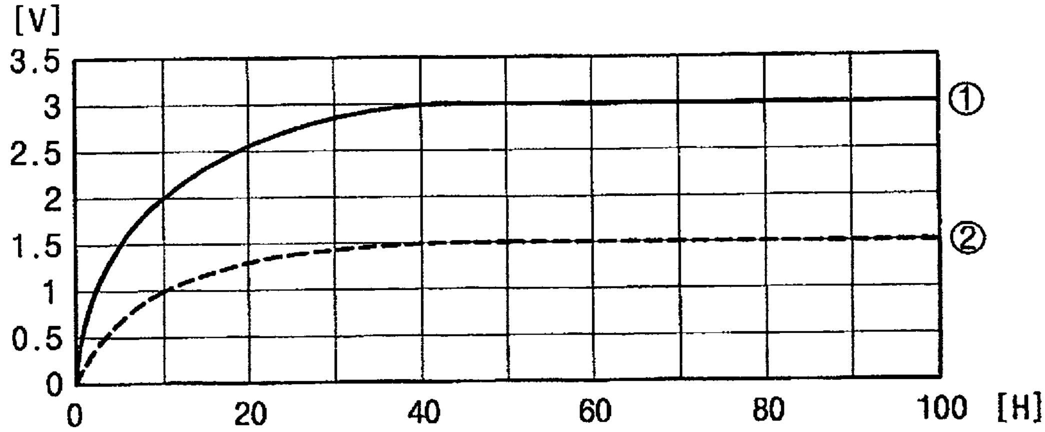


Fig. 5

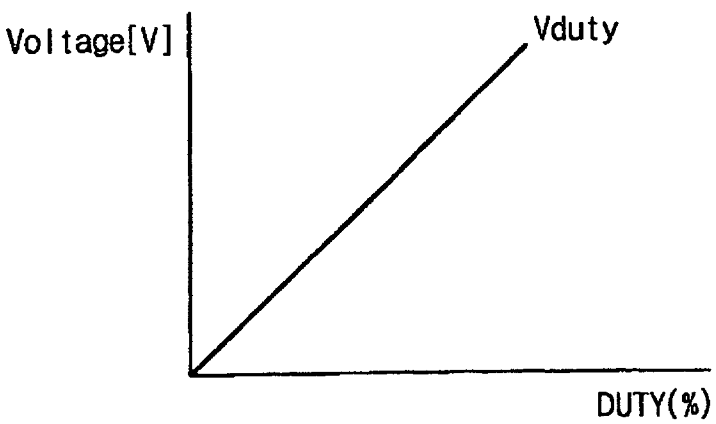


Fig. 6

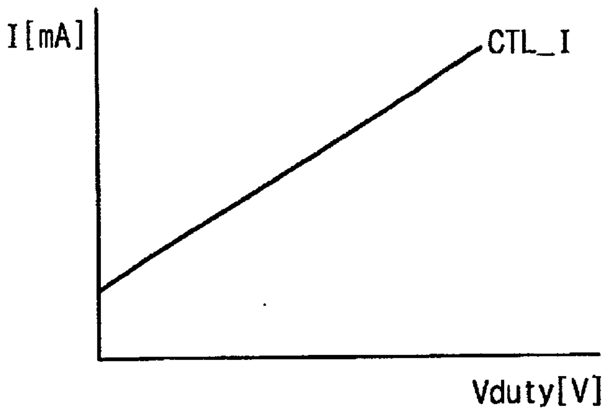

I[mA]
CTL_I
Vduty[V]

Fig. 7

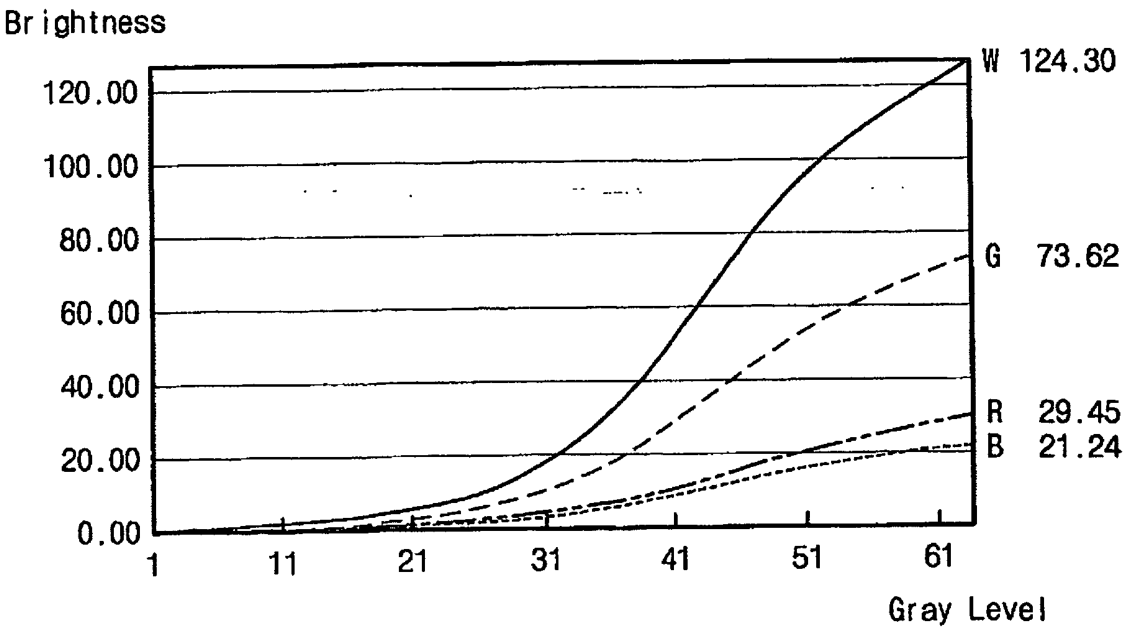

Brightness
120.00
100.00
80.00
60.00
40.00
20.00
0.00
1
11
21
31
41
51
61
Gray Level
W 124.30
G 73.62
R 29.45
B 21.24

Fig. 8

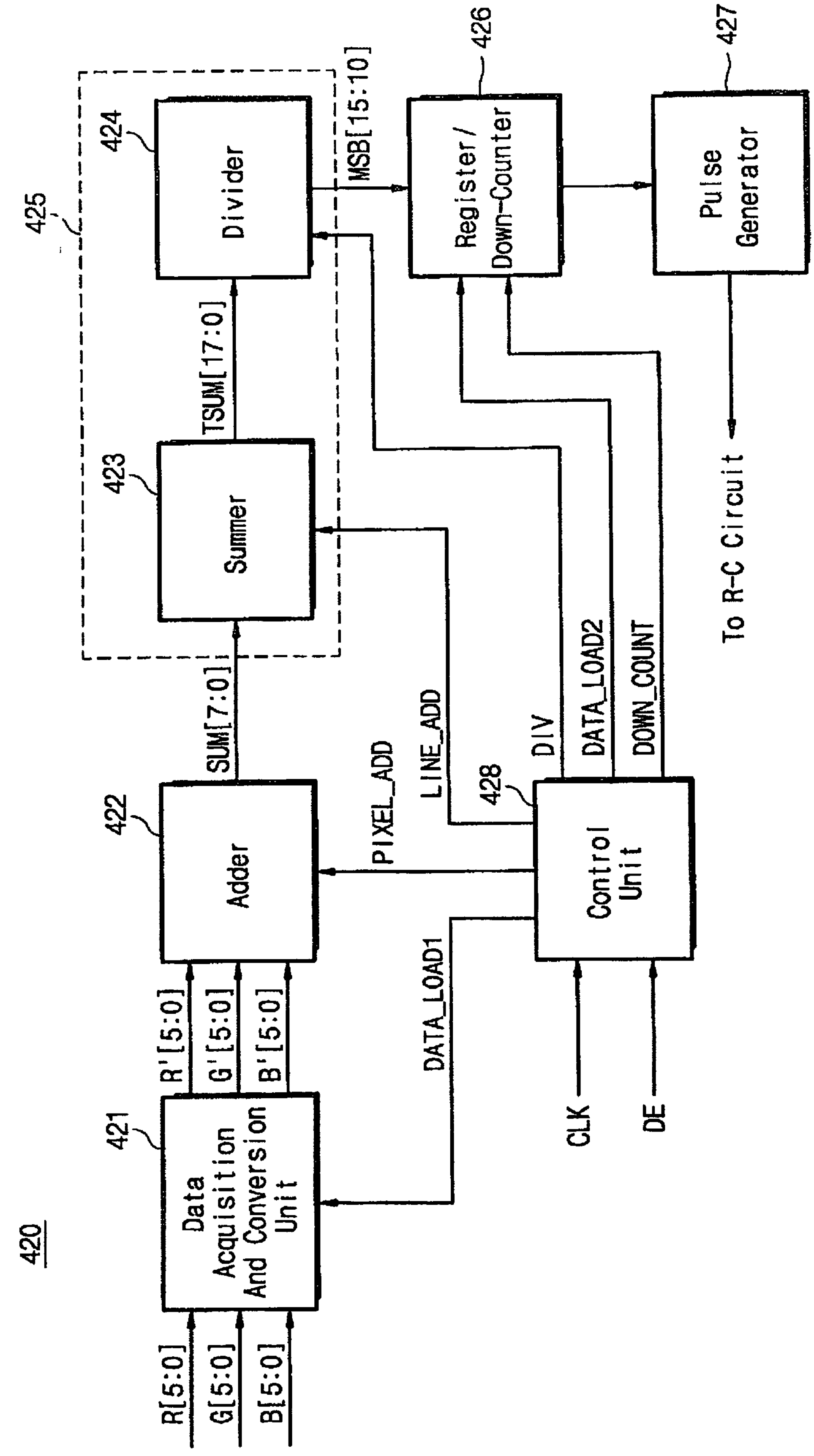

420
425
R[5:0]
G[5:0]
B[5:0]
421
Data Acquisition And Conversion Unit
R'[5:0]
G'[5:0]
B'[5:0]
422
Adder
SUM[7:0]
423
Summer
TSUM[17:0]
424
Divider
MSB[15:10]
426
Register/ Down-Counter
427
Pulse Generator
To R-C Circuit
428
Control Unit
PIXEL_ADD
LINE_ADD
DIV
DATA_LOAD1
DATA_LOAD2
DOWN_COUNT
CLK
DE

Fig. 9

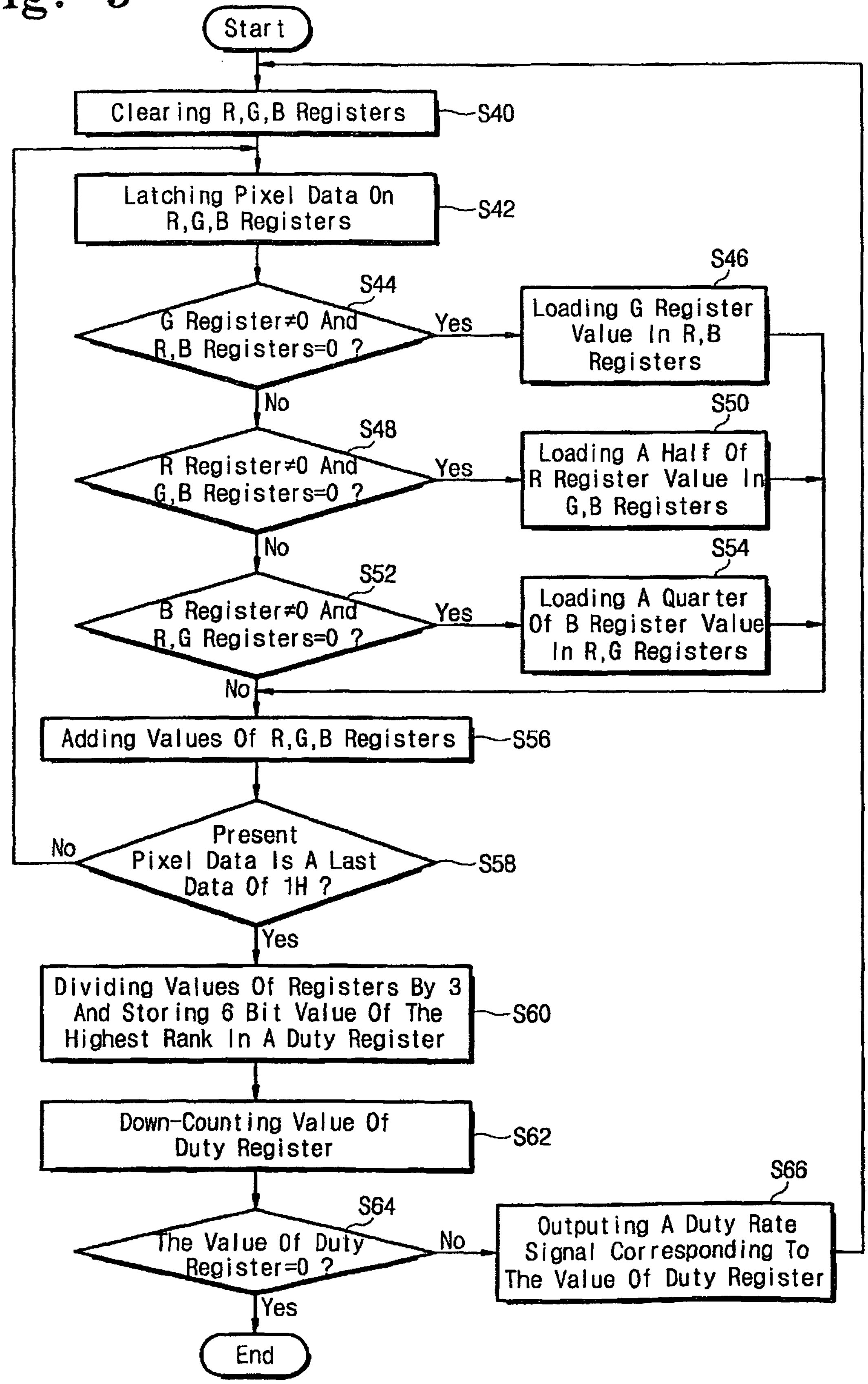

Start
Clearing R,G,B Registers
S40
Latching Pixel Data On R,G,B Registers
S42
S44
G Register≠0 And R,B Registers=0 ?
Yes
S46
Loading G Register Value In R,B Registers
No
S48
R Register≠0 And G,B Registers=0 ?
Yes
S50
Loading A Half Of R Register Value In G,B Registers
No
S52
B Register≠0 And R,G Registers=0 ?
Yes
S54
Loading A Quarter Of B Register Value In R,G Registers
No
Adding Values Of R,G,B Registers
S56
Present Pixel Data Is A Last Data Of 1H ?
No
S58
Yes
Dividing Values Of Registers By 3 And Storing 6 Bit Value Of The Highest Rank In A Duty Register
S60
Down-Counting Value Of Duty Register
S62
S64
The Value Of Duty Register=0 ?
No
S66
Outputting A Duty Rate Signal Corresponding To The Value Of Duty Register
Yes
End

Fig. 10

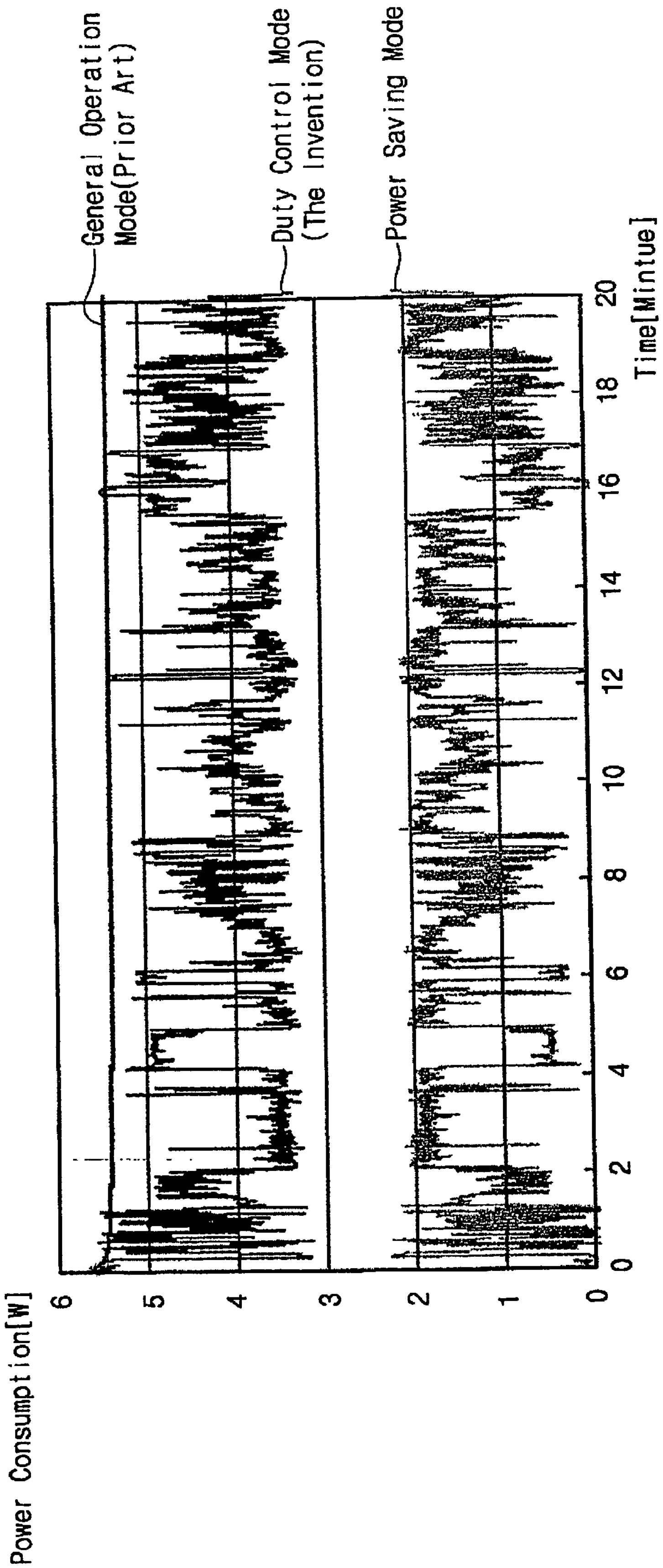

General Operation Mode(Prior Art)
Duty Control Mode (The Invention)
Power Saving Mode
Power Consumption[W]
6
5
4
3
2
1
0
0
2
4
6
8
10
12
14
16
18
20
Time[Mintue]

Fig. 11

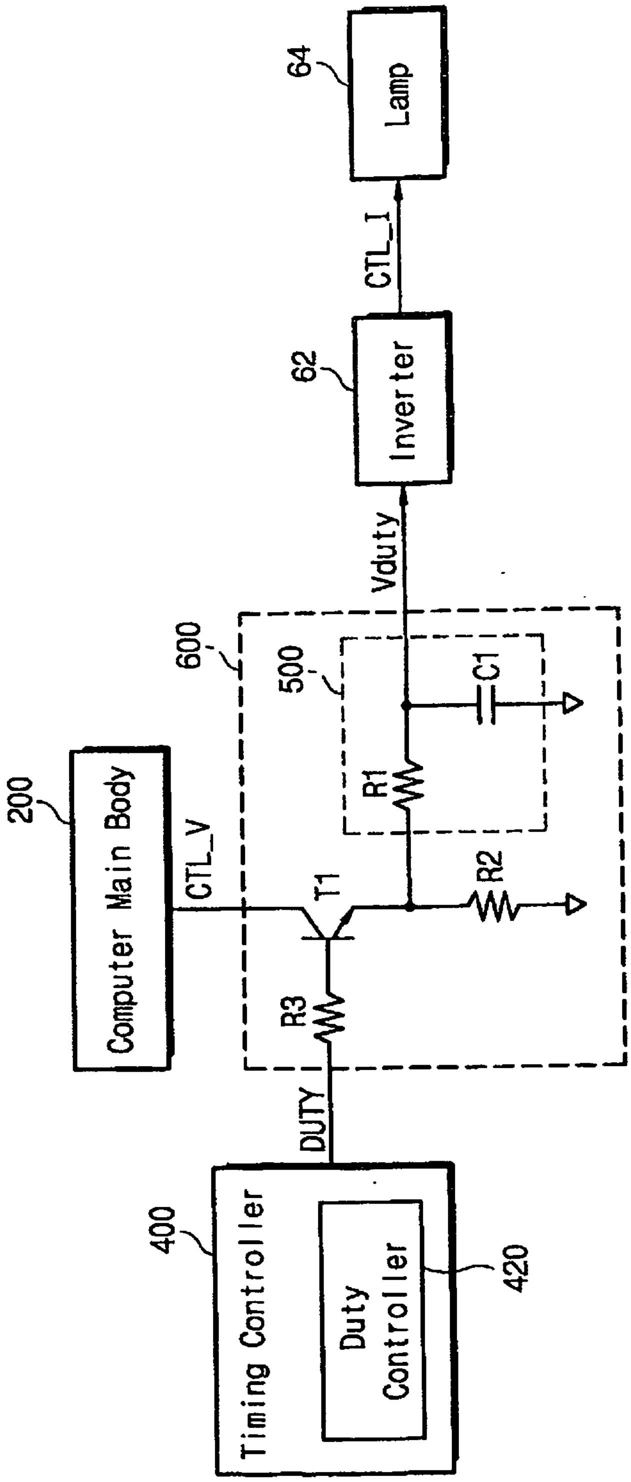

64
Lamp
CTL_I
62
Inverter
Vduty
600
500
C1
R1
200
Computer Main Body
CTL_V
T1
R2
R3
DUTY
400
Timing Controller
Duty Controller
420

Fig. 12

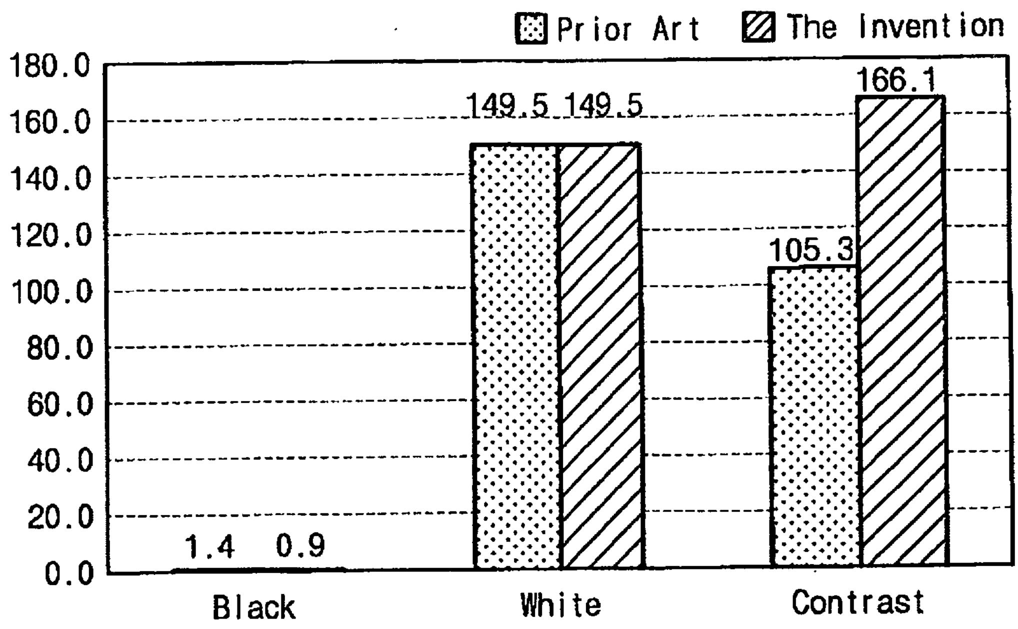

Prior Art
The Invention
180.0
160.0
140.0
120.0
100.0
80.0
60.0
40.0
20.0
0.0
1.4
0.9
149.5
149.5
105.3
166.1
Black
White
Contrast

Fig. 13

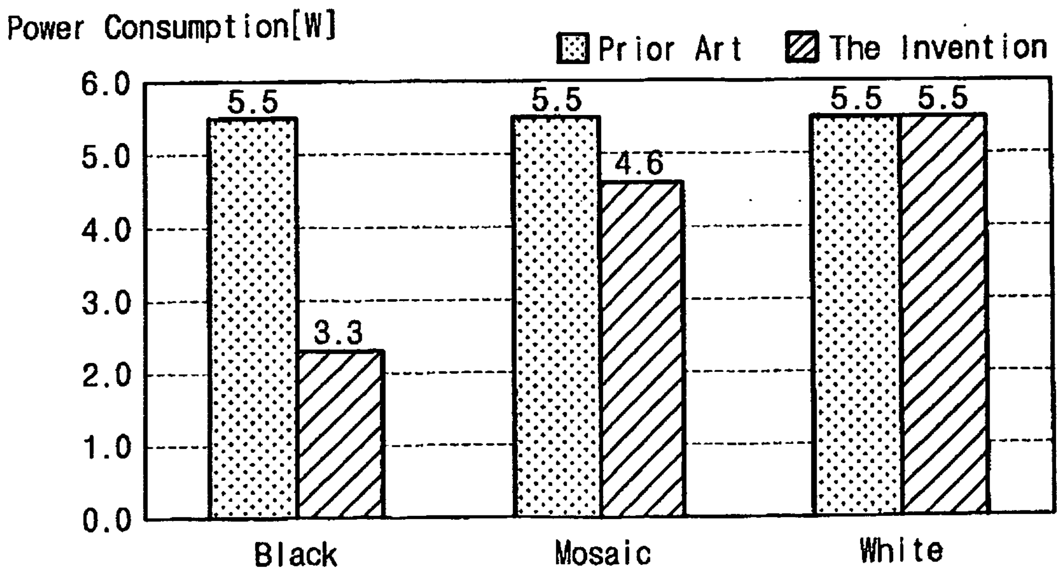

Power Consumption[W]
Prior Art
The Invention
6.0
5.0
4.0
3.0
2.0
1.0
0.0
5.5
3.3
5.5
4.6
5.5
5.5
Black
Mosaic
White

Fig. 14

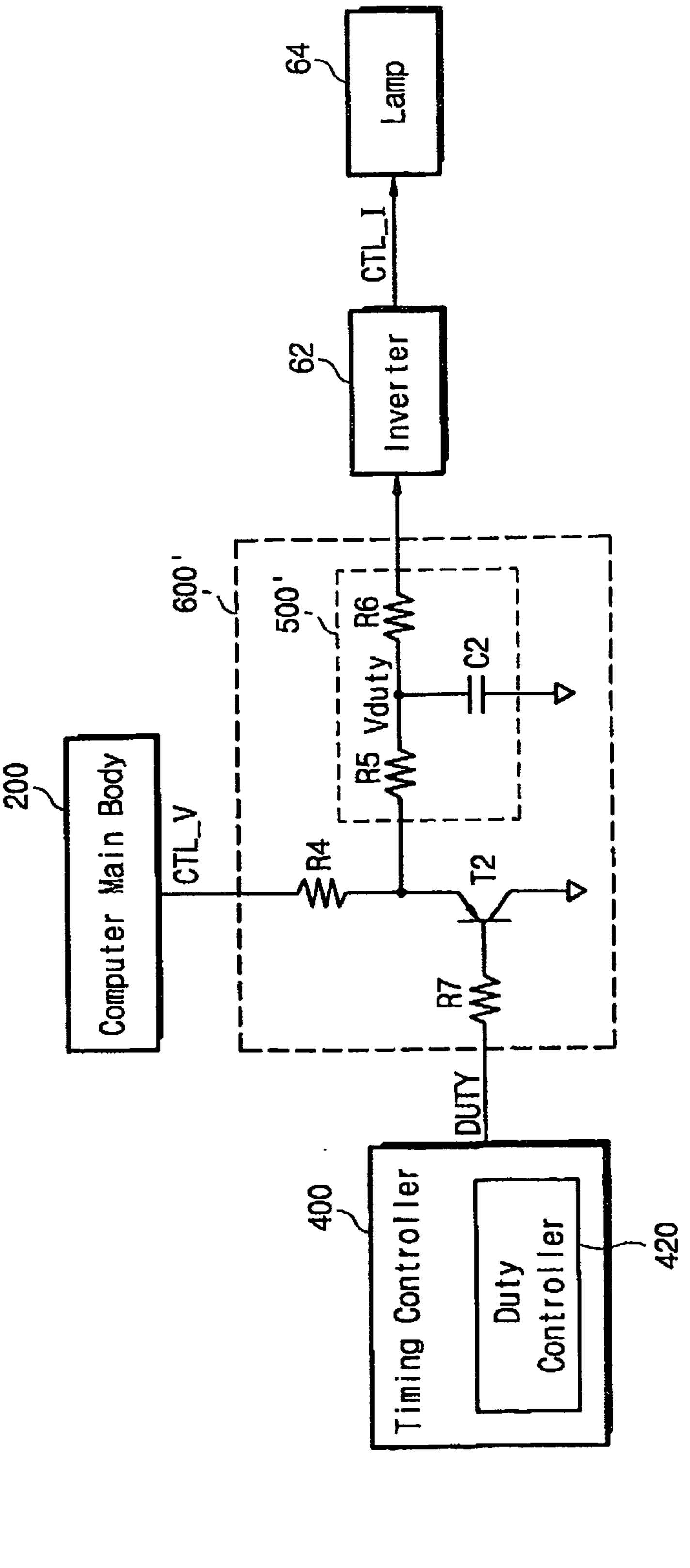

64
Lamp
CTL_I
62
Inverter
600'
500'
R6
C2
Vduty
R5
200
Computer Main Body
CTL_V
R4
T2
R7
DUTY
400
Timing Controller
Duty Controller
420

Fig. 15

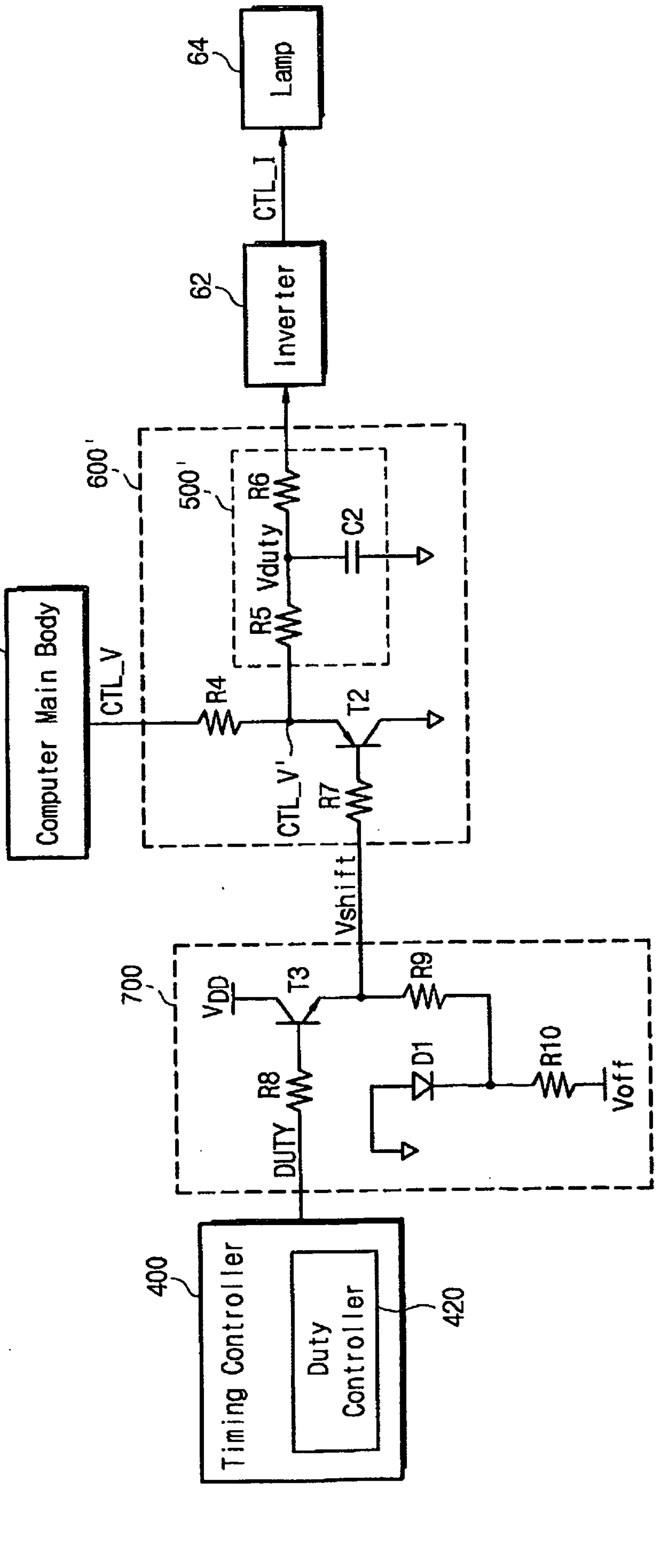

64
Lamp
CTL_I
62
Inverter
600'
500'
R6
C2
Vduty
R5
200
Computer Main Body
CTL_V
R4
T2
CTL_V'
R7
Vshift
700
VDD
T3
R9
R8
D1
R10
DUTY
Voff
400
Timing Controller
Duty Controller
420

Fig. 16

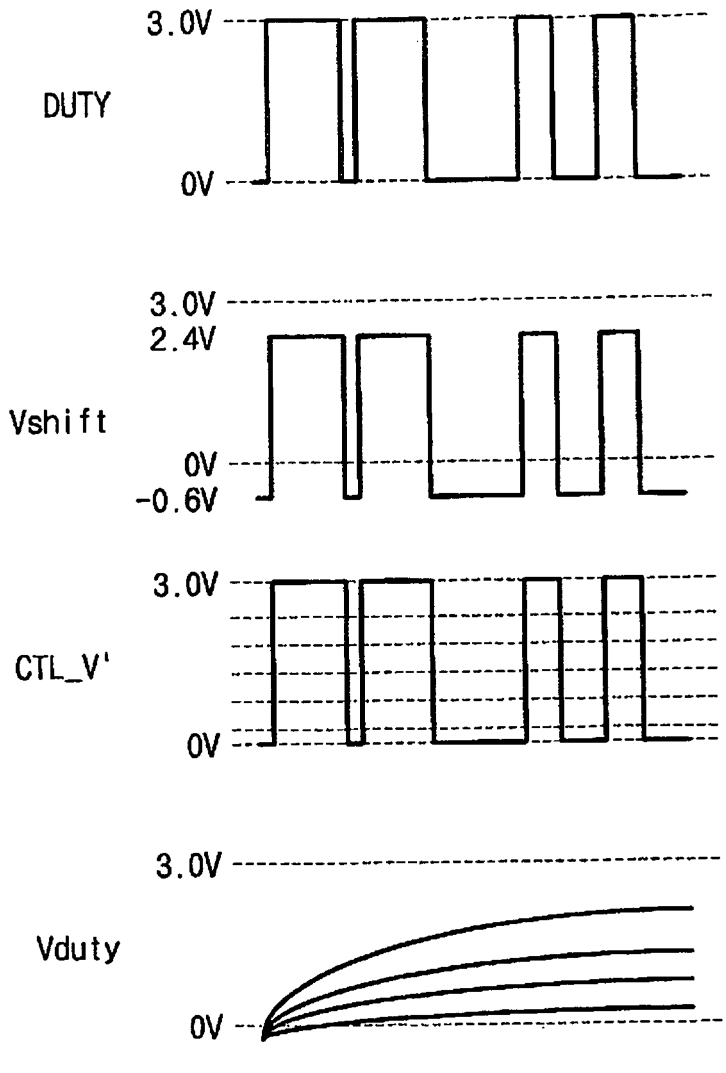
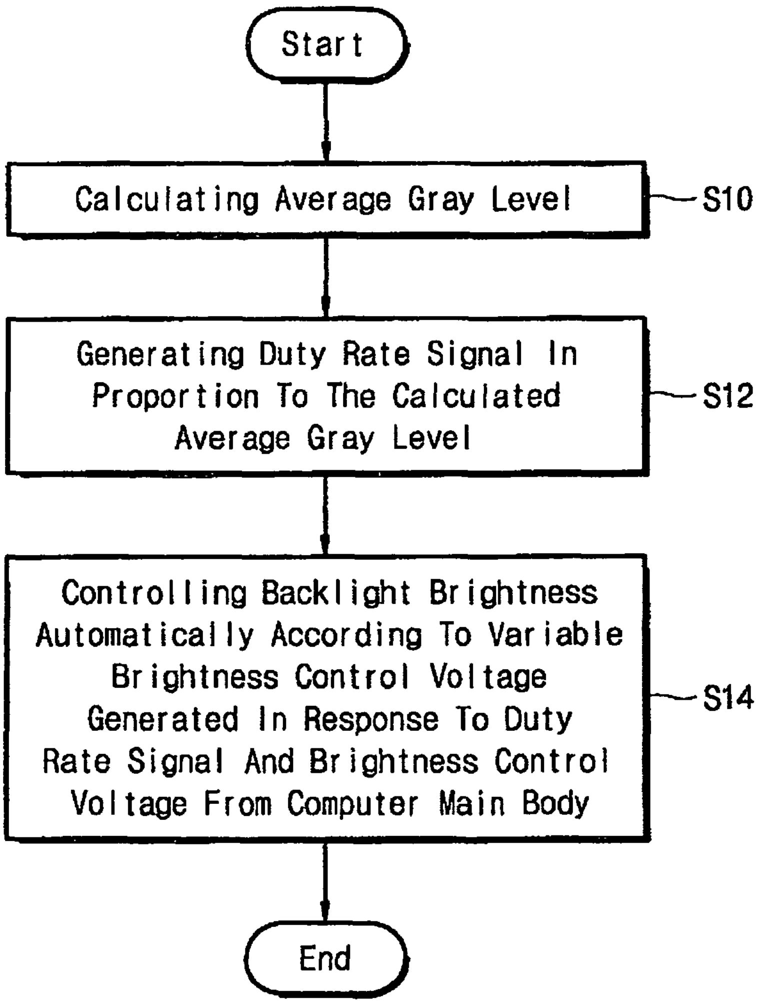


Fig. 17


Start
Calculating Average Gray Level
S10
Generating Duty Rate Signal In Proportion To The Calculated Average Gray Level
S12
Controlling Backlight Brightness Automatically According To Variable Brightness Control Voltage Generated In Response To Duty Rate Signal And Brightness Control Voltage From Computer Main Body
S14
End

专利名称(译)	用于液晶显示装置的背光的自动亮度控制的装置和方法		
公开(公告)号	EP2463850B1	公开(公告)日	2016-07-27
申请号	EP2012157986	申请日	2001-11-07
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	MOON SEUNG HWAN KIM SANG SOO PARK DONG WON CHOI HYEONG BAE		
发明人	MOON, SEUNG-HWAN KIM, SANG-SOO PARK, DONG-WON CHOI, HYEONG-BAE		
IPC分类号	G09G3/34 G02F1/133 G09G3/20 G09G3/36 H04N5/66 H05B41/40 H05B41/42		
CPC分类号	G09G3/3406 G09G3/2011 G09G3/3413 G09G2320/0238 G09G2320/0276 G09G2320/0606 G09G2320/0613 G09G2320/064 G09G2320/0653 G09G2330/021 G09G2360/16		
优先权	1020000085540 2000-12-29 KR 1020010026136 2001-05-14 KR		
其他公开文献	EP2463850A1		
外部链接	Espacenet		

摘要(译)

具有背光的LCD装置响应于与要在LCD装置上显示的图像数据的平均灰度级和/或颜色状态相对应的占空比信号以及从主装置产生的亮度控制电压而产生背光亮度控制信号。用户的身体，根据背光亮度控制信号自动控制背光的亮度。

[Mathematical formula 1]

Vduty={Vo+(Vc-Vo)x[1-EXP[-T1/(Rx C)]]}x EXP[(T1-1H)/(R x C)]