



(51) International Patent Classification:

H01L 27/15 (2006.01) H01L 33/00 (2010.01)

(21) International Application Number:

PCT/CN2018/117703

(22) International Filing Date:

27 November 2018 (27.11.2018)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicants: **BOE TECHNOLOGY GROUP CO., LTD.**

[CN/CN]; No.10 Jiuxianqiao Rd., Chaoyang District, Beijing 100015 (CN). **HEFEI XINSHENG OPTO-ELECTRONICS TECHNOLOGY CO., LTD.** [CN/CN]; Xinzhan Industrial Park, Hefei, Anhui 230012 (CN).

(72) Inventors: **CHEN, Peng**; No.9 Dize Rd., BDA, Beijing

100176 (CN). **ZHANG, Xinxia**; No.9 Dize Rd., BDA, Beijing 100176 (CN). **LI, Hengbin**; No.9 Dize Rd., BDA, Beijing 100176 (CN). **WANG, Guolei**; No.9 Dize Rd., BDA, Beijing 100176 (CN).

(74) Agent: **TEE&HOWE INTELLECTUAL PROPERTY ATTORNEYS**;

Yuan CHEN, 10th Floor, Tower D, Minsheng Financial Center, 28 Jianguomenmei Avenue, Dongcheng District, Beijing 100005 (CN).

(81) Designated States (unless otherwise indicated, for every

kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,

OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every

kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: METHOD OF FABRICATING MICRO LIGHT EMITTING DIODE ARRAY SUBSTRATE, MICRO LIGHT EMITTING DIODE ARRAY SUBSTRATE, MICRO LIGHT EMITTING DIODE DISPLAY APPARATUS

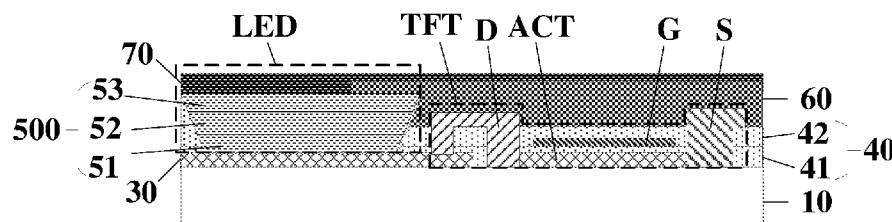


FIG. 5

(57) Abstract: A method of fabricating a micro light emitting diode (micro LED) array substrate having a plurality of micro LEDs is provided. The method includes forming a plurality of signal lines on a base substrate (10); depositing a semiconductor material on the base substrate (10) to form a semiconductor material layer; and patterning the semiconductor material layer to form a semiconductor layer (500) of the plurality of micro LEDs. A surface of the plurality of signal lines away from the base substrate (10) is uncovered during depositing the semiconductor material. The plurality of signal lines form a grid for facilitating epitaxial growth of the semiconductor material.



**METHOD OF FABRICATING MICRO LIGHT EMITTING DIODE  
ARRAY SUBSTRATE, MICRO LIGHT EMITTING DIODE ARRAY  
SUBSTRATE, MICRO LIGHT EMITTING DIODE DISPLAY  
APPARATUS**

**TECHNICAL FIELD**

**[0001]** The present invention relates to display technology, more particularly, to a method of fabricating a micro light emitting diode array substrate, a micro light emitting diode array substrate, and a micro light emitting diode display apparatus.

**BACKGROUND**

**[0002]** In recent years, miniaturized electro-optics devices are proposed and developed, including micro light emitting diode (micro LED). The micro LED-based display panels have the advantages of high brightness, high contrast ratio, fast response, and low power consumption. The micro LED-based display technology has found a wide range of applications in the display field, including smartphones and smart watches.

**SUMMARY**

**[0003]** In one aspect, the present invention provides a method of fabricating a micro light emitting diode (micro LED) array substrate having a plurality of micro LEDs, comprising forming a plurality of signal lines on a base substrate; depositing a semiconductor material on the base substrate to form a semiconductor material layer; and patterning the semiconductor material layer to form a semiconductor layer of the plurality of micro LEDs; wherein a surface of the plurality of signal lines away from the base substrate is uncovered during depositing the semiconductor material, the plurality of signal lines forming a grid for facilitating epitaxial growth of the semiconductor material.

**[0004]** Optionally, prior to forming the plurality of signal lines, the method further comprises forming a growth layer on the base substrate, the epitaxial growth of the semiconductor material being formed on the growth layer.

**[0005]** Optionally, the method further comprises forming a plurality of thin film transistors on the base substrate for respectively driving light emission of the plurality of micro LEDs; wherein each of the plurality of thin film transistors is formed to comprise an active layer;

and the growth layer and the active layer are formed in a same layer using a same material, and in a single patterning process using a single mask plate.

**[0006]** Optionally, each of the plurality of thin film transistors is formed to comprises a source electrode and a drain electrode; and the source electrode, the drain electrode, and the plurality of signal lines are formed in a same layer using a same material, and in a single patterning process using a single mask plate.

**[0007]** Optionally, subsequent to forming the active layer and the growth layer and prior to forming the plurality of signal lines, the source electrode, and the drain electrode, the method further comprises forming an insulating layer on a side of the active layer and the growth layer away from the base substrate; and forming a first via, a second via, and a third via respectively extending through the insulating layer; wherein the source electrode is formed to be connected to the active layer through the first via; and the drain electrode is formed to be connected to the active layer through the second via and connected to the growth layer through the third via.

**[0008]** Optionally, the growth layer and the active layer are formed using a material comprising silicon.

**[0009]** Optionally, subsequent to patterning the semiconductor material layer to form the semiconductor layer of the plurality of micro LEDs, the method further comprises forming a pixel definition layer defining a plurality of subpixel apertures; and forming a contact pad layer on a side of the semiconductor layer away from the base substrate.

**[0010]** Optionally, the plurality of signal lines are a plurality of data lines of the micro LED array substrate.

**[0011]** Optionally, the semiconductor layer of the plurality of micro LEDs is selected from a group consisting of an n-layer, a p-layer, and a multiple quantum well layer of the plurality of micro LEDs.

**[0012]** In another aspect, the present invention provides a micro light emitting diode (micro LED) array substrate having a plurality of micro LEDs, comprising a base substrate; a growth layer on the base substrate; a plurality of semiconductor layers of the plurality of micro LEDs on a side of the growth layer away from the base substrate; and a plurality of thin film transistors on the base substrate; wherein each of the plurality of thin film transistors

comprises an active layer; and the growth layer and the active layer are in a same layer and comprise a same semiconductor material.

**[0013]** Optionally, the micro LED array substrate further comprises an insulating layer on a side of the growth layer and the active layer away from the base substrate; and a plurality of signal lines on a side of the insulating layer away from the base substrate.

**[0014]** Optionally, each of the plurality of thin film transistors comprises a source electrode and a drain electrode; and the source electrode, the drain electrode, and the plurality of signal lines are in a same layer and comprise a same material.

**[0015]** Optionally, the micro LED array substrate further comprises a first via, a second via, and a third via respectively extending through the insulating layer; wherein the source electrode is connected to the active layer through the first via; and the drain electrode is connected to the active layer through the second via and connected to the growth layer through the third via.

**[0016]** Optionally, the micro LED array substrate further comprises a pixel definition layer defining a plurality of subpixel apertures on a side of the plurality of signal lines away from the base substrate, the plurality of semiconductor layers being in the plurality of subpixel apertures; wherein the pixel definition layer is in direct contact with at least one of the plurality of semiconductor layers of the plurality of micro LEDs; and the pixel definition layer is in direct contact with the plurality of signal lines.

**[0017]** Optionally, an upper surface of the plurality of signal lines away from the base substrate are in direct contact with the pixel definition layer; and an upper most surface of the plurality of semiconductor layers of the plurality of micro LEDs is in direct contact with the pixel definition layer.

**[0018]** Optionally, the plurality of semiconductor layers in each of the plurality of subpixel apertures has a cross-section along a plane perpendicular to a main surface of the base substrate; the cross-section has a first side away from the base substrate and a second side opposite to the first side and facing the base substrate; and the first side is wider than the second side in each of the plurality of subpixel apertures.

**[0019]** Optionally, the micro LED array substrate further comprises a contact pad layer on a side of the plurality of semiconductor layers away from the base substrate.

[0020] Optionally, the growth layer and the active layer comprise a material comprising silicon.

[0021] Optionally, the plurality of signal lines are a plurality of data lines of the micro LED array substrate.

[0022] In another aspect, the present invention provides a micro light emitting diode (micro LED) display apparatus, comprising the micro LED array substrate described herein or fabricated by a method described herein, and one or more integrated circuits connected to the micro LED array substrate.

#### BRIEF DESCRIPTION OF THE FIGURES

[0023] The following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present invention.

[0024] FIG. 1A is a plan view diagram illustrating an intermediate step of fabricating a micro LED array substrate in some embodiments according to the present disclosure.

[0025] FIG. 1B is a cross-sectional view along an A-A' line in FIG. 1A.

[0026] FIG. 1C is a cross-sectional view along a B-B' line in FIG. 1A.

[0027] FIG. 2A is a plan view diagram illustrating an intermediate step of fabricating a micro LED array substrate in some embodiments according to the present disclosure.

[0028] FIG. 2B is a cross-sectional view along a C-C' line in FIG. 2A.

[0029] FIG. 2C is a cross-sectional view along a D-D' line in FIG. 2A.

[0030] FIG. 3A is a plan view diagram illustrating an intermediate step of fabricating a micro LED array substrate in some embodiments according to the present disclosure.

[0031] FIG. 3B is a cross-sectional view along an E-E' line in FIG. 2A.

[0032] FIG. 3C is a cross-sectional view along an F-F' line in FIG. 2A.

[0033] FIG. 4 is a cross-sectional view diagram illustrating a step of fabricating a micro LED array substrate in some embodiments according to the present disclosure.

[0034] FIG. 5 is a schematic diagram illustrating the structure of a micro LED array substrate in some embodiments according to the present disclosure.

[0035] FIG. 6 is a cross-sectional view of a micro LED array substrate in some embodiments according to the present disclosure.

[0036] FIG. 7 is a schematic diagram illustrating the structure of a micro LED display panel in some embodiments according to the present disclosure.

#### DETAILED DESCRIPTION

[0037] The disclosure will now be described more specifically with reference to the following embodiments. It is to be noted that the following descriptions of some embodiments are presented herein for purpose of illustration and description only. It is not intended to be exhaustive or to be limited to the precise form disclosed.

[0038] In fabricating a micro light emitting diode (micro LED) display panel, each of the micro LED has to be transferred from a growth substrate to an array substrate. Considering the display panel includes thousands to millions of micro LEDs, a pick-and-place transfer process is extremely time-consuming, and thus not suitable for large-scale fabrication of micro LED display panels. An improvement to the pick-and-place transfer is to use a printing head for transferring a plurality of micro LEDs at one time. Still, a process of transferring a large number of micro LEDs using a printing head is too complicated and time-consuming. Moreover, misalignment between the micro LEDs and the bonding contacts in the target substrate occurs frequently in the pick-and-place transfer or the transfer process using a printing head, resulting in defects in the display panel.

[0039] Accordingly, the present disclosure provides, *inter alia*, a method of fabricating a micro light emitting diode (micro LED) array substrate having a plurality of micro LEDs, a micro light emitting diode array substrate having a plurality of micro LEDs, and a micro light emitting diode display apparatus that substantially obviate one or more of the problems due to limitations and disadvantages of the related art. In one aspect, the present disclosure provides a method of fabricating a micro light emitting diode array substrate having a plurality of micro LEDs. In some embodiments, the method includes forming a plurality of signal lines on a base substrate; depositing a semiconductor material on the base substrate to form a semiconductor material layer; and patterning the semiconductor material layer to form a semiconductor layer of the plurality of micro LEDs. A surface of the plurality of signal lines away from the base substrate is uncovered during depositing the semiconductor material, the plurality of signal lines form a grid for facilitating epitaxial growth of the semiconductor

material. In the present disclosure, the plurality of micro LEDs are directly fabricated in an array substrate, obviating the complicated and error-prone transfer process.

**[0040]** FIG. 1A is a plan view diagram illustrating an intermediate step of fabricating a micro LED array substrate in some embodiments according to the present disclosure. FIG. 1B is a cross-sectional view along an A-A' line in FIG. 1A. FIG. 1C is a cross-sectional view along a B-B' line in FIG. 1A. Referring to FIGs. 1A to 1C, the method of fabricating a micro light emitting diode array substrate having a plurality of micro LEDs includes first forming a plurality of signal lines 20 on a base substrate 10.

**[0041]** In conventional fabrication methods of display panels, it is to be avoided to have exposed metallic signal lines when depositing semiconductor materials, to avoid contact between the signal lines and the semiconductor material. Typically, before depositing the semiconductor material, an insulating layer is first formed on the substrate to cover up the signal lines so that they are not exposed during the deposition of the semiconductor material. It is discovered in the present disclosure, when depositing a semiconductor material for forming a semiconductor layer of the plurality of micro LEDs, the plurality of signal lines 20 form a grid that can facilitate epitaxial growth of the semiconductor material. Specifically, the epitaxial growth of the semiconductor material is promoted by the grid of the plurality of signal lines 20 to have a certain lattice orientation. Moreover, the epitaxial growth of the semiconductor material in the grid of the plurality of signal lines 20 results in an inverted trapezoidal growth profile of the semiconductor material layer. The lattice orientation, in combination with the unique growth profile, leads to a significantly enhanced emission efficiency of the plurality of micro LEDs fabricated by the present method.

**[0042]** Various appropriate signal lines of the array substrate may be used as the grid for promoting epitaxial growth of the semiconductor material. Examples of appropriate signal lines include gate lines, data lines, common electrode signal lines (for providing a common voltage to common electrodes), touch signal lines, or any combination thereof. FIGs. 1A to 1C illustrate an example in which a plurality of data lines are used as the grid for promoting epitaxial growth of the semiconductor material.

**[0043]** FIG. 2A is a plan view diagram illustrating an intermediate step of fabricating a micro LED array substrate in some embodiments according to the present disclosure. FIG. 2B is a cross-sectional view along a C-C' line in FIG. 2A. FIG. 2C is a cross-sectional view along a D-D' line in FIG. 2A. Referring to FIGs. 2A to 2C, a semiconductor material is

deposited on the base substrate 10 to form a semiconductor material layer 50'. As shown in FIG. 2C, a cross-section of the semiconductor material layer 50' along a plane perpendicular to a main surface MS of the base substrate 10 has an inverted trapezoidal shape. The cross-section has a first side S1 away from the base substrate 10 and a second side S2 opposite to the first side S1 and facing the base substrate 10. The first side S1 is wider than the second side S2 in each of a plurality of subpixel apertures SA. Each of the plurality of subpixel apertures SA corresponds to one of a plurality of subpixels in a display panel having the micro LED array substrate. For example, each of the plurality of subpixels in the display panel having the micro LED array substrate includes one of the plurality of micro LEDs, and each of the plurality of subpixel apertures SA is an aperture formed for depositing the semiconductor material of a respective one of the plurality of micro LEDs.

**[0044]** Referring to FIG. 2B and FIG. 2C, a surface of the plurality of signal lines 20 away from the base substrate 10 is uncovered during depositing the semiconductor material. The plurality of signal lines 20 form a grid for facilitating epitaxial growth of the semiconductor material.

**[0045]** In some embodiments, prior to depositing the semiconductor material, a growth layer is first formed on the base substrate 10 for epitaxial growth of the semiconductor material. Referring to FIGs. 1A to 1C, prior to forming the plurality of signal lines 20, a growth layer 30 is first formed on the base substrate 10. The epitaxial growth of the semiconductor material is formed on the growth layer 30. Various appropriate materials may be used for making the growth layer 30. Examples of appropriate growth layer materials include silicon, sapphire, quartz, GaN, SiC, and alumina. In one example, the growth layer 30 is made of a semiconductor material such as silicon.

**[0046]** In some embodiments, and referring to FIG. 1B, the method further includes forming a plurality of thin film transistors TFT on the base substrate 10 for respectively driving light emission of the plurality of micro LEDs. Each of the plurality of thin film transistors TFT is formed to include an active layer ACT, a gate electrode G, a source electrode S, and a drain electrode D.

**[0047]** In some embodiments, the growth layer 30 and the active layer ACT are formed in a same layer using a same material, and in a single patterning process using a single mask plate. As used herein, the term "same layer" refers to the relationship between the layers simultaneously formed in the same step. In one example, the growth layer 30 and the active

layer ACT are in a same layer when they are formed as a result of one or more steps of a same patterning process performed in a same layer of material. In another example, the growth layer 30 and the active layer ACT can be formed in a same layer by simultaneously performing the step of forming the growth layer 30 and the step of forming the active layer ACT. The term “same layer” does not always mean that the thickness of the layer or the height of the layer in a cross-sectional view is the same.

**[0048]** When the growth layer 30 and the active layer ACT are formed in a same layer, optionally, the growth layer 30 is made of a semiconductor material, e.g., a same semiconductor material as the material for making the active layer ACT. In one example, the growth layer 30 and the active layer ACT are formed using a material including silicon, e.g., a polycrystalline silicon.

**[0049]** Referring to FIGs. 2A to 2C, the semiconductor material layer 50' can be a layer for making any semiconductor layer of the plurality of micro LEDs. For example, the semiconductor material layer 50' may be a layer for making an n-layer of the plurality of micro LEDs, and the semiconductor material for forming the semiconductor material layer 50' is an n-layer material such as n-GaN. In another example, the semiconductor material layer 50' is a layer for making a p-layer of the plurality of micro LEDs, and the semiconductor material for forming the semiconductor material layer 50' is a p-layer material such as p-GaN. In another example, the semiconductor material layer 50' is a layer for making a multiple quantum well layer of the plurality of micro LEDs, and the semiconductor material for forming the semiconductor material layer 50' is a quantum well material.

**[0050]** In some embodiments, the source electrode S, the drain electrode D, and the plurality of signal lines 20 are formed in a same layer using a same material, and in a single patterning process using a single mask plate. Optionally, the plurality of signal lines 20 are a plurality of data lines, which are formed in a same layer as the source electrode S and the drain electrode D. Various appropriate conductive materials and various appropriate fabricating methods may be used to make the source electrode S, the drain electrode D, and the plurality of signal lines 20. For example, a conductive material may be deposited on the substrate (e.g., by sputtering or vapor deposition); and patterned (e.g., by lithography such as a wet etching process) to form the source electrode S, the drain electrode D, and the plurality of signal lines 20. Examples of appropriate conductive materials for making the source electrode S, the drain electrode D, and the plurality of signal lines 20 include, but are not

limited to, aluminum, tungsten, copper, and molybdenum, and alloys or laminates containing the same.

**[0051]** Referring to FIGs. 1A to 1C again, in some embodiments, the method further includes forming an insulating layer 40 on a side of the active layer ACT and the growth layer 30 away from the base substrate 10. For example, subsequent to forming the active layer ACT and the growth layer 30, and prior to forming the plurality of signal lines 20, the source electrode S, and the drain electrode D, an insulating material layer may be deposited on a side of the active layer ACT and the growth layer 30 away from the base substrate 10, followed by patterning the insulating material layer to form the plurality of subpixel apertures SA to expose a surface of the growth layer 30.

**[0052]** In some embodiments, the method further includes forming a first via v1, a second via v2, and a third via v3 respectively extending through the insulating layer 40. As shown in FIG. 1B, the source electrode S is formed to be connected to the active layer ACT through the first via v1; and the drain electrode D is formed to be connected to the active layer ACT through the second via v2 and connected to the growth layer 30 through the third via v3. A portion of the drain electrode D (e.g., the portion extending through the third via v3) may be considered as a contact pad of a respective one of the plurality of micro LEDs.

**[0053]** FIG. 3A is a plan view diagram illustrating an intermediate step of fabricating a micro LED array substrate in some embodiments according to the present disclosure. FIG. 3B is a cross-sectional view along an E-E' line in FIG. 3A. FIG. 3C is a cross-sectional view along an F-F' line in FIG. 3A. Referring to FIGs. 3A to 3C, the method in some embodiments further includes patterning the semiconductor material layer to form a semiconductor layer 50 of the plurality of micro LEDs. The semiconductor layer 50 can be any semiconductor layer of the plurality of micro LEDs. For example, the semiconductor layer 50 may be an n-layer of the plurality of micro LEDs, and the semiconductor material for forming the semiconductor layer 50 is an n-layer material such as n-GaN. In another example, the semiconductor layer 50 is a p-layer of the plurality of micro LEDs, and the semiconductor material for forming the semiconductor layer 50 is a p-layer material such as p-GaN. In another example, the semiconductor layer 50 is a multiple quantum well layer of the plurality of micro LEDs, and the semiconductor material for forming the semiconductor layer 50 is a quantum well material.

**[0054]** Referring to FIG. 2C and FIG. 3C, during the patterning step, the semiconductor material layer 50' can be patterned so that the semiconductor layer 50 is spaced apart from the plurality of signal lines 20, thereby insulating the semiconductor layer 50 from the adjacent signal lines of the plurality of signal lines 20. Referring to FIG. 2B and FIG. 3B, any portion of the semiconductor material layer 50' outside the plurality of subpixel apertures SA can also be removed during the patterning process. For example, the semiconductor material deposited on a side of insulating layer 40 away from the active layer ACT and in a region between the source electrode S and the drain electrode D can be removed during the patterning process. Subsequent to the patterning step, only the semiconductor material in the plurality of subpixel apertures SA remains.

**[0055]** FIG. 4 is a cross-sectional view diagram illustrating a step of fabricating a micro LED array substrate in some embodiments according to the present disclosure. Referring to FIG. 4, the method in some embodiments further includes forming a pixel definition layer 60 defining the plurality of subpixel apertures SA. The pixel definition layer 60 is formed on a side of the plurality of signal lines 20 away from the base substrate 10. Optionally, a portion of the pixel definition layer 60 is formed on a side of an edge portion of the semiconductor layer 50 away from the base substrate 10.

**[0056]** In some embodiments, the method further includes forming a contact pad layer 70 on a side of the semiconductor layer 50 away from the base substrate 10. Optionally, the contact pad layer 70 is a n-contact pad layer. Optionally, the contact pad layer 70 is a p-contact pad layer.

**[0057]** In another aspect, the present disclosure provides a micro light emitting diode array substrate having a plurality of micro LEDs. FIG. 5 is a schematic diagram illustrating the structure of a micro LED array substrate in some embodiments according to the present disclosure. Referring to FIG. 5, the micro LED array substrate in some embodiments includes a base substrate 10; a growth layer 30 on the base substrate 10; a plurality of semiconductor layers 500 of the plurality of micro LEDs on a side of the growth layer 30 away from the base substrate 10; and a plurality of thin film transistors TFT on the base substrate 10. Each of the plurality of thin film transistors TFT includes an active layer ACT. Optionally, the growth layer 30 and the active layer ACT are in a same layer and includes a same semiconductor material. Optionally, the growth layer 30 and the active layer ACT include silicon, e.g., a polycrystalline silicon.

**[0058]** Optionally, the plurality of semiconductor layers 500 includes a n-layer 51, a multiple quantum wells layer 52, and a p-layer 53.

**[0059]** In some embodiments, referring to FIG. 3A and FIG. 5, the micro LED array substrate further includes an insulating layer 40 on a side of the growth layer 30 and the active layer ACT away from the base substrate 10; and a plurality of signal lines 20 on a side of the insulating layer 40 away from the base substrate 10.

**[0060]** Optionally, the insulating layer 40 includes multiple layers. Referring to FIG. 5, in some embodiments, the insulating layer 40 includes a first insulating layer 41 and a second insulating layer 42. The first insulating layer 41 is between the active layer ACT and a gate electrode G of a respective one of the plurality of thin film transistors TFT. The second insulating layer 42 is on a side of the gate electrode G away from the base substrate 10.

**[0061]** In some embodiments, each of the plurality of thin film transistors TFT includes a source electrode S and a drain electrode D. Optionally, the source electrode S, the drain electrode D, and the plurality of signal lines 20 are in a same layer and include a same material such as aluminum. Optionally, the plurality of signal lines 20 are a plurality of data lines of the micro LED array substrate.

**[0062]** In some embodiments, the micro LED array substrate includes a first via v1, a second via v2, and a third via v3 respectively extending through the insulating layer 40. The source electrode S is connected to the active layer ACT through the first via v1. The drain electrode D is connected to the active layer ACT through the second via v2 and connected to the growth layer 30 through the third via v3. A portion of the drain electrode D (e.g., the portion extending through the third via v3) may be considered as a contact pad of a respective one of the plurality of micro LEDs.

**[0063]** In some embodiments, referring to FIG. 3A and FIG. 5, the micro LED array substrate further includes a pixel definition layer 60 defining a plurality of subpixel apertures SA on a side of the plurality of signal lines 20 away from the base substrate 10. In some embodiments, the pixel definition layer 60 is in direct contact with at least one of the plurality of semiconductor layers 500 of the plurality of micro LEDs; and the pixel definition layer 60 is in direct contact with the plurality of signal lines 20. For example, the pixel definition layer 60 is in direct contact with a p-layer 53 of the plurality of semiconductor layers 500. In another example, the pixel definition layer 60 is in direct contact with a lateral side of at least one of the plurality of semiconductor layers 500. Optionally, a portion of the pixel definition

layer 60 is formed on a side of an edge portion of the plurality of semiconductor layers 500 away from the base substrate 10, an orthographic projection of the pixel definition layer 60 on the base substrate 10 overlaps with an orthographic projection of the edge portion of the plurality of semiconductor layers 500 on the base substrate 10. Optionally, an upper surface of the plurality of signal lines 20 away from the base substrate 10 are in direct contact with the pixel definition layer 60; and an upper most surface of the plurality of semiconductor layers 500 of the plurality of micro LEDs is in direct contact with the pixel definition layer 60.

**[0064]** FIG. 6 is a cross-sectional view of a micro LED array substrate in some embodiments according to the present disclosure. Referring to FIG. 6, in some embodiments, the plurality of semiconductor layers 500 in each of the plurality of subpixel apertures SA has a cross-section along a plane perpendicular to a main surface MS of the base substrate 10. The cross-section has a first side S1 away from the base substrate 10 and a second side S2 opposite to the first side S1 and facing the base substrate 10. Optionally, the first side S1 is wider than the second side S2 in each of the plurality of subpixel apertures SA. Optionally, the cross-section has an inverted trapezoidal shape.

**[0065]** Referring to FIG. 5, in some embodiments, the micro LED array substrate further includes a contact pad layer 70 on a side of the plurality of semiconductor layers 500 away from the base substrate 10. Optionally, the contact pad layer 70 is a n-contact pad layer. Optionally, the contact pad layer 70 is a p-contact pad layer.

**[0066]** In another aspect, the present disclosure provides a micro light emitting diode display panel having the micro light emitting diode array substrate described herein or fabricated by a method described herein. FIG. 7 is a schematic diagram illustrating the structure of a micro LED display panel in some embodiments according to the present disclosure. Referring to FIG. 7, the micro light emitting diode display panel in some embodiments includes a micro light emitting diode array substrate AS and a counter substrate CS assembled together. Optionally, the counter substrate CS includes a color filter CF and a black matrix BM.

**[0067]** In another aspect, the present disclosure provides a micro light emitting diode display apparatus having the micro light emitting diode display panel described herein or fabricated by a method described herein. Optionally, the micro light emitting diode display apparatus further includes one or more integrated circuits connected to the micro LED array substrate. Examples of appropriate display apparatuses include, but are not limited to, an

electronic paper, a mobile phone, a tablet computer, a television, a monitor, a notebook computer, a digital album, a GPS, etc.

**[0068]** The foregoing description of the embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form or to exemplary embodiments disclosed. Accordingly, the foregoing description should be regarded as illustrative rather than restrictive. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments are chosen and described in order to explain the principles of the invention and its best mode practical application, thereby to enable persons skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use or implementation contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents in which all terms are meant in their broadest reasonable sense unless otherwise indicated. Therefore, the term “the invention”, “the present invention” or the like does not necessarily limit the claim scope to a specific embodiment, and the reference to exemplary embodiments of the invention does not imply a limitation on the invention, and no such limitation is to be inferred. The invention is limited only by the spirit and scope of the appended claims. Moreover, these claims may refer to use “first”, “second”, etc. following with noun or element. Such terms should be understood as a nomenclature and should not be construed as giving the limitation on the number of the elements modified by such nomenclature unless specific number has been given. Any advantages and benefits described may not apply to all embodiments of the invention. It should be appreciated that variations may be made in the embodiments described by persons skilled in the art without departing from the scope of the present invention as defined by the following claims. Moreover, no element and component in the present disclosure is intended to be dedicated to the public regardless of whether the element or component is explicitly recited in the following claims.

WHAT IS CLAIMED IS:

1. A method of fabricating a micro light emitting diode (micro LED) array substrate having a plurality of micro LEDs, comprising:
  - forming a plurality of signal lines on a base substrate;
  - depositing a semiconductor material on the base substrate to form a semiconductor material layer; and
  - patterning the semiconductor material layer to form a semiconductor layer of the plurality of micro LEDs;wherein a surface of the plurality of signal lines away from the base substrate is uncovered during depositing the semiconductor material, the plurality of signal lines forming a grid for facilitating epitaxial growth of the semiconductor material.
2. The method of claim 1, prior to forming the plurality of signal lines, further comprising forming a growth layer on the base substrate, the epitaxial growth of the semiconductor material being formed on the growth layer.
3. The method of claim 2, further comprising forming a plurality of thin film transistors on the base substrate for respectively driving light emission of the plurality of micro LEDs;
  - wherein each of the plurality of thin film transistors is formed to comprise an active layer; and
  - the growth layer and the active layer are formed in a same layer using a same material, and in a single patterning process using a single mask plate.
4. The method of claim 3, wherein each of the plurality of thin film transistors is formed to comprises a source electrode and a drain electrode; and
  - the source electrode, the drain electrode, and the plurality of signal lines are formed in a same layer using a same material, and in a single patterning process using a single mask plate.
5. The method of claim 4, subsequent to forming the active layer and the growth layer and prior to forming the plurality of signal lines, the source electrode, and the drain electrode, further comprising:

forming an insulating layer on a side of the active layer and the growth layer away from the base substrate; and

forming a first via, a second via, and a third via respectively extending through the insulating layer;

wherein the source electrode is formed to be connected to the active layer through the first via; and the drain electrode is formed to be connected to the active layer through the second via and connected to the growth layer through the third via.

6. The method of claim 3, wherein the growth layer and the active layer are formed using a material comprising silicon.

7. The method of any one of claims 1 to 6, subsequent to patterning the semiconductor material layer to form the semiconductor layer of the plurality of micro LEDs, further comprising forming a pixel definition layer defining a plurality of subpixel apertures; and

forming a contact pad layer on a side of the semiconductor layer away from the base substrate.

8. The method of any one of claims 1 to 7, wherein the plurality of signal lines are a plurality of data lines of the micro LED array substrate.

9. The method of any one of claims 1 to 8, wherein the semiconductor layer of the plurality of micro LEDs is selected from a group consisting of an n-layer, a p-layer, and a multiple quantum well layer of the plurality of micro LEDs.

10. A micro light emitting diode (micro LED) array substrate having a plurality of micro LEDs, comprising:

a base substrate;

a growth layer on the base substrate;

a plurality of semiconductor layers of the plurality of micro LEDs on a side of the growth layer away from the base substrate; and

a plurality of thin film transistors on the base substrate;

wherein each of the plurality of thin film transistors comprises an active layer; and

the growth layer and the active layer are in a same layer and comprise a same semiconductor material.

11. The micro LED array substrate of claim 10, further comprising:  
an insulating layer on a side of the growth layer and the active layer away from the base substrate; and  
a plurality of signal lines on a side of the insulating layer away from the base substrate.
12. The micro LED array substrate of claim 11, wherein each of the plurality of thin film transistors comprises a source electrode and a drain electrode; and  
the source electrode, the drain electrode, and the plurality of signal lines are in a same layer and comprise a same material.
13. The micro LED array substrate of claim 12, further comprising a first via, a second via, and a third via respectively extending through the insulating layer;  
wherein the source electrode is connected to the active layer through the first via; and the drain electrode is connected to the active layer through the second via and connected to the growth layer through the third via.
14. The micro LED array substrate of claim 11, further comprising a pixel definition layer defining a plurality of subpixel apertures on a side of the plurality of signal lines away from the base substrate, the plurality of semiconductor layers being in the plurality of subpixel apertures;  
wherein the pixel definition layer is in direct contact with at least one of the plurality of semiconductor layers of the plurality of micro LEDs; and  
the pixel definition layer is in direct contact with the plurality of signal lines.
15. The micro LED array substrate of claim 14, wherein an upper surface of the plurality of signal lines away from the base substrate are in direct contact with the pixel definition layer; and  
an upper most surface of the plurality of semiconductor layers of the plurality of micro LEDs is in direct contact with the pixel definition layer.
16. The micro LED array substrate of claim 14, wherein the plurality of semiconductor layers in each of the plurality of subpixel apertures has a cross-section along a plane perpendicular to a main surface of the base substrate;  
the cross-section has a first side away from the base substrate and a second side opposite to the first side and facing the base substrate; and

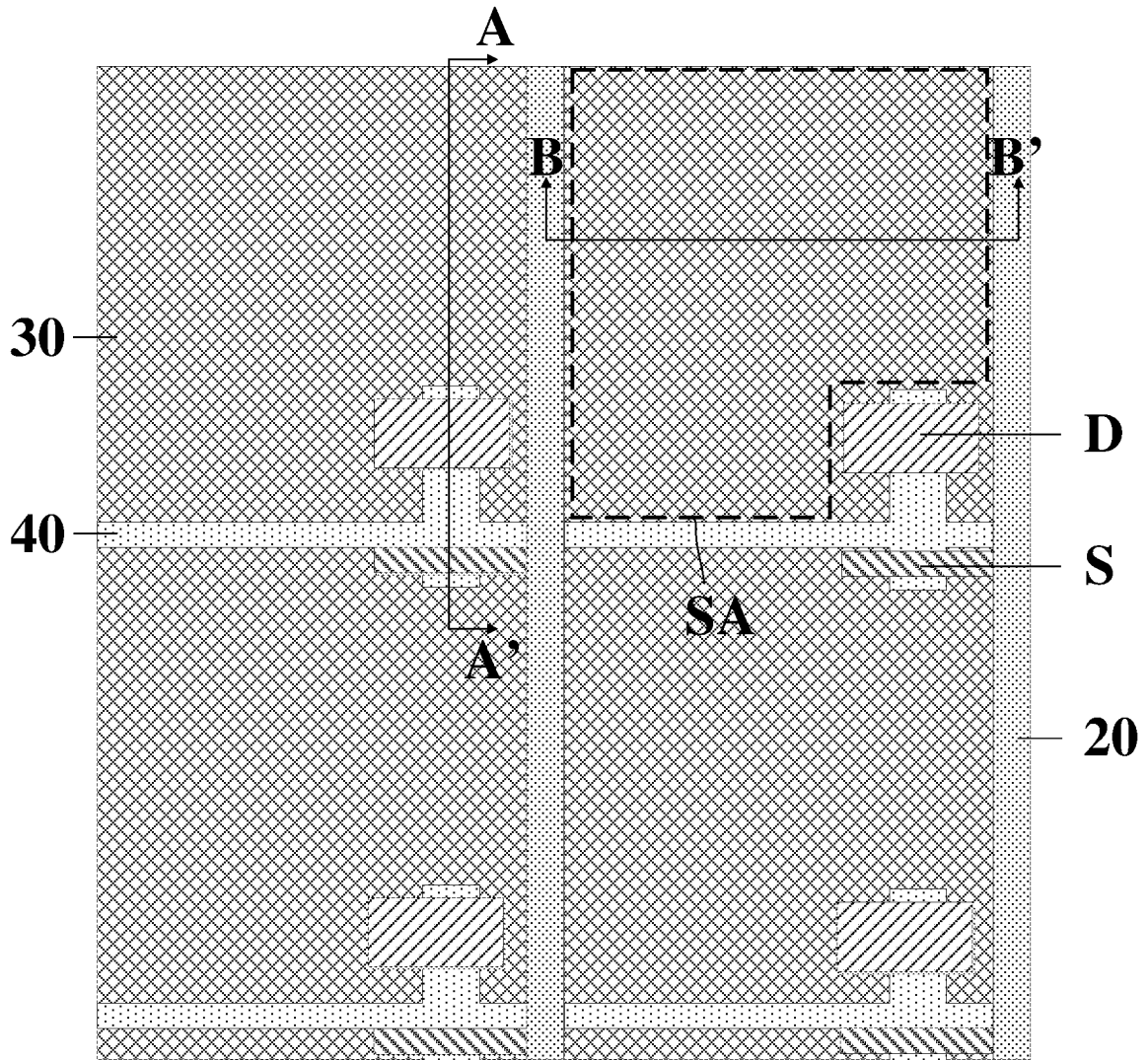
the first side is wider than the second side in each of the plurality of subpixel apertures.

17. The micro LED array substrate of claim 14, further comprising a contact pad layer on a side of the plurality of semiconductor layers away from the base substrate.

18. The micro LED array substrate of any one of claims 10 to 17, wherein the growth layer and the active layer comprise a material comprising silicon.

19. The micro LED array substrate of any one of claims 10 to 18, wherein the plurality of signal lines are a plurality of data lines of the micro LED array substrate.

20. A micro light emitting diode (micro LED) display apparatus, comprising the micro LED array substrate of any one of claims 10 to 19, and one or more integrated circuits connected to the micro LED array substrate.



**FIG. 1A**

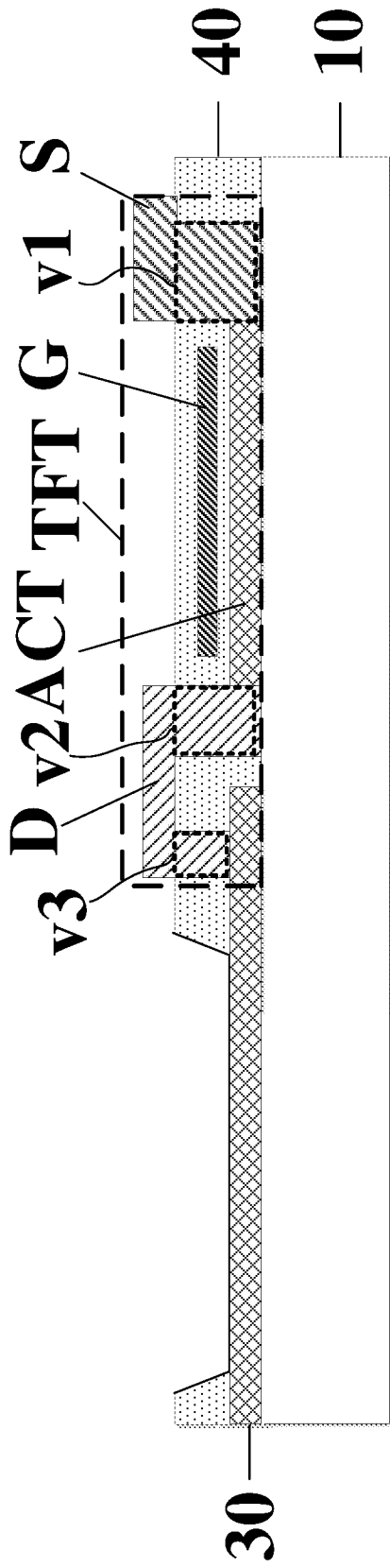


FIG. 1B

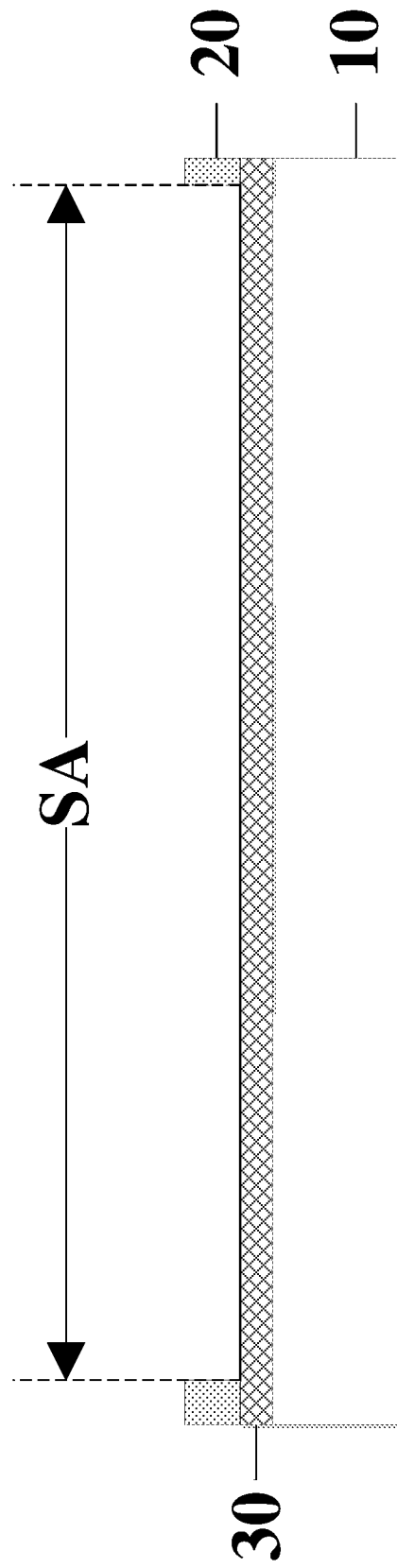
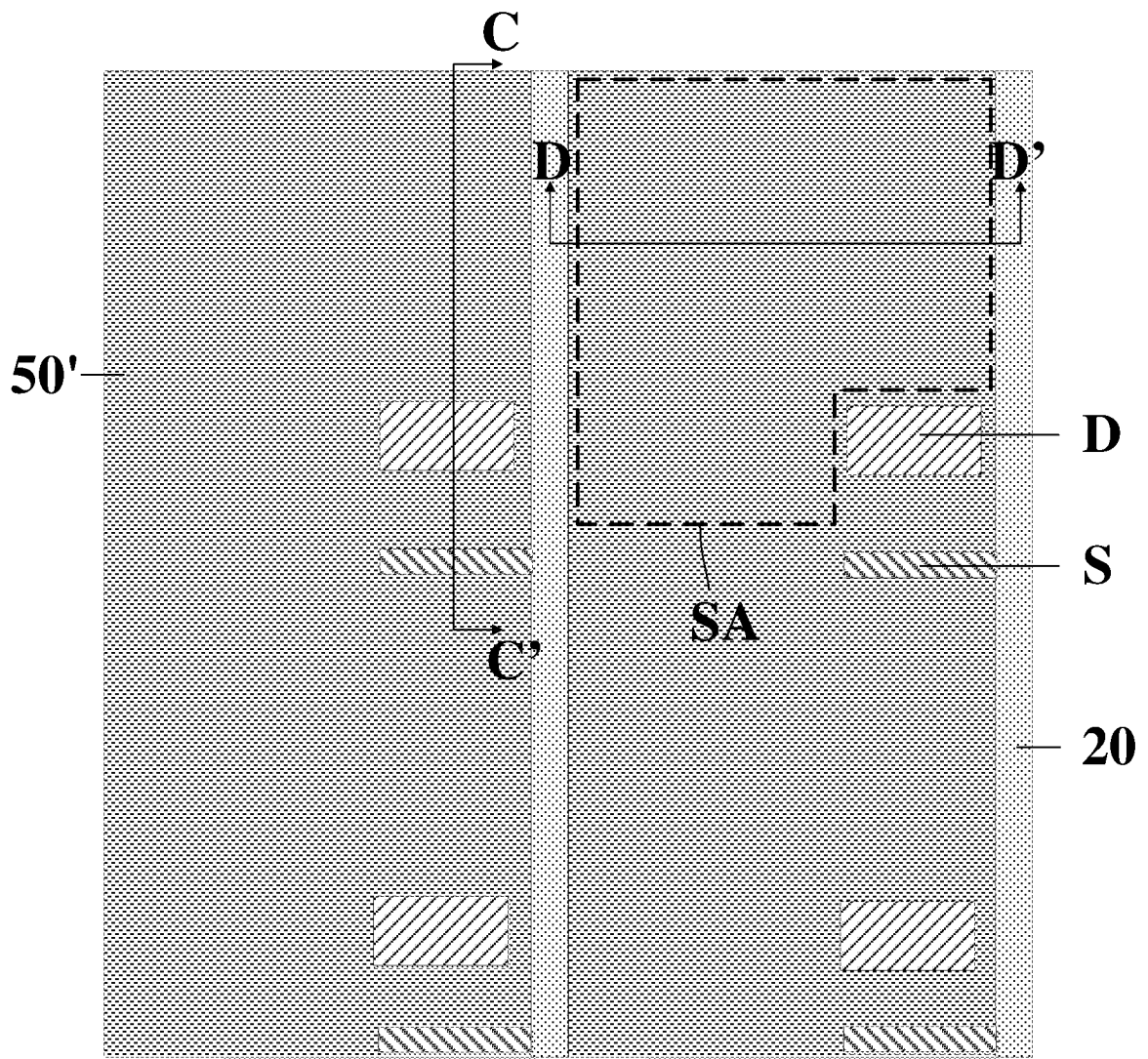


FIG. 1C



**FIG. 2A**



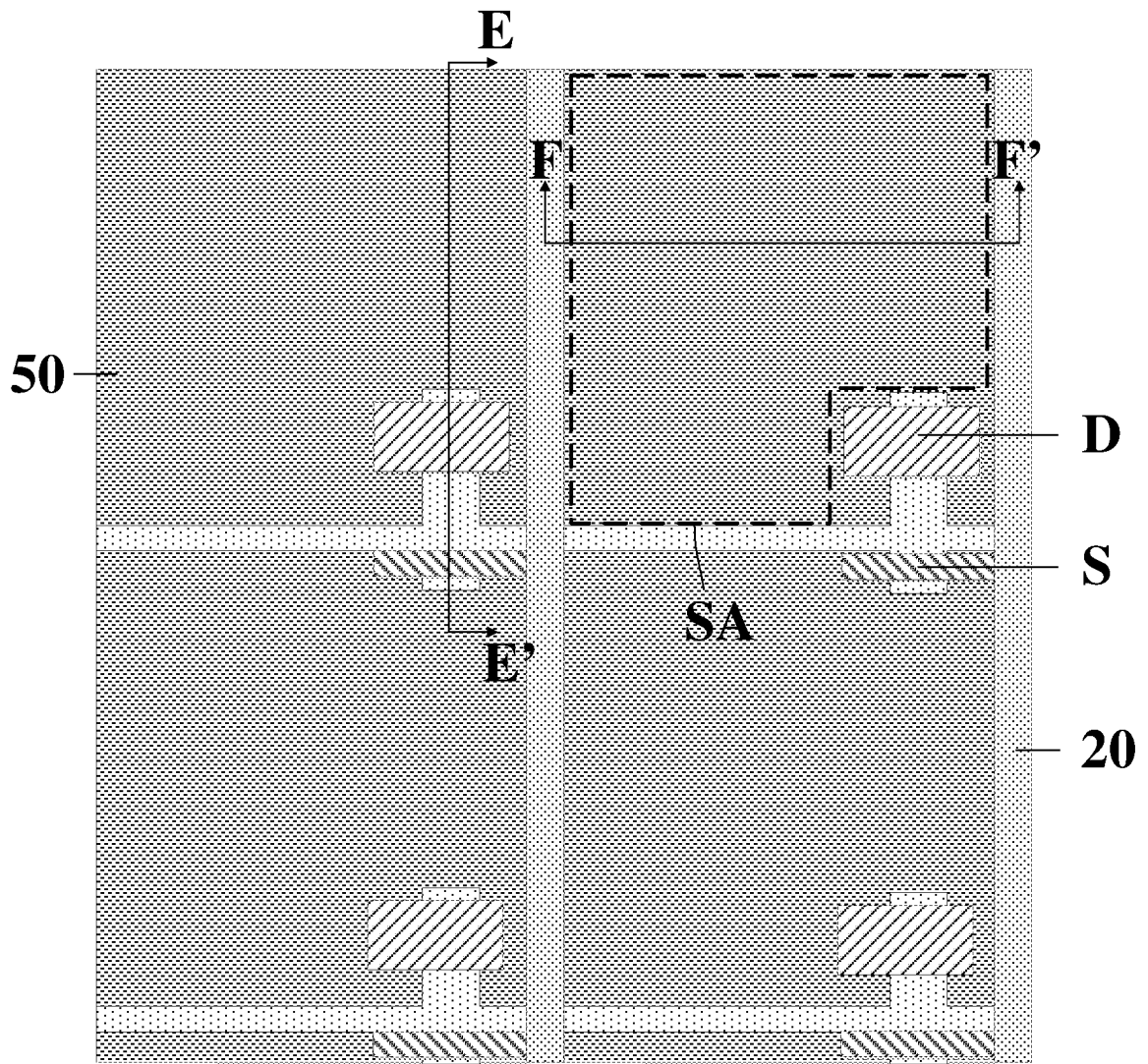


FIG. 3A

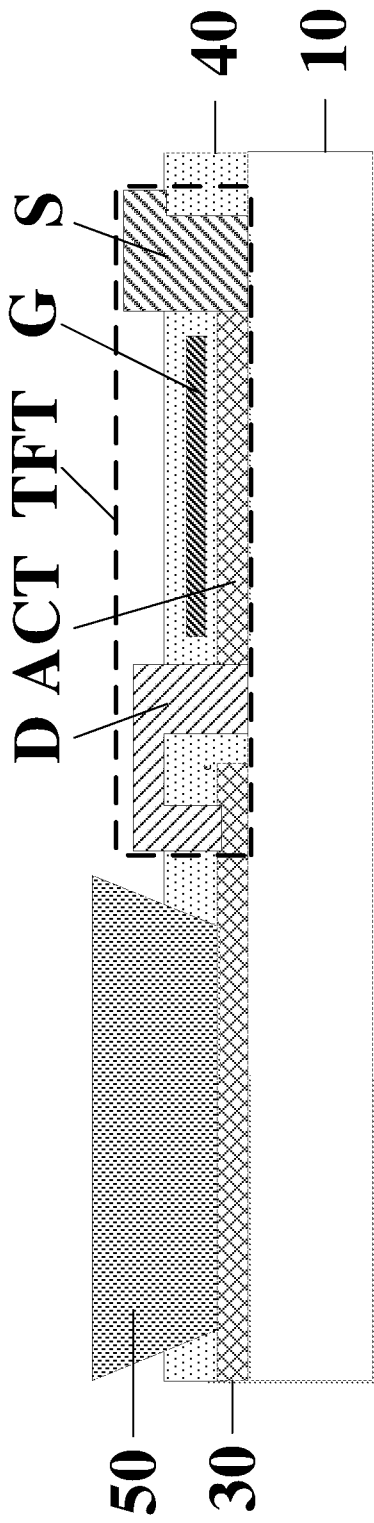


FIG. 3B

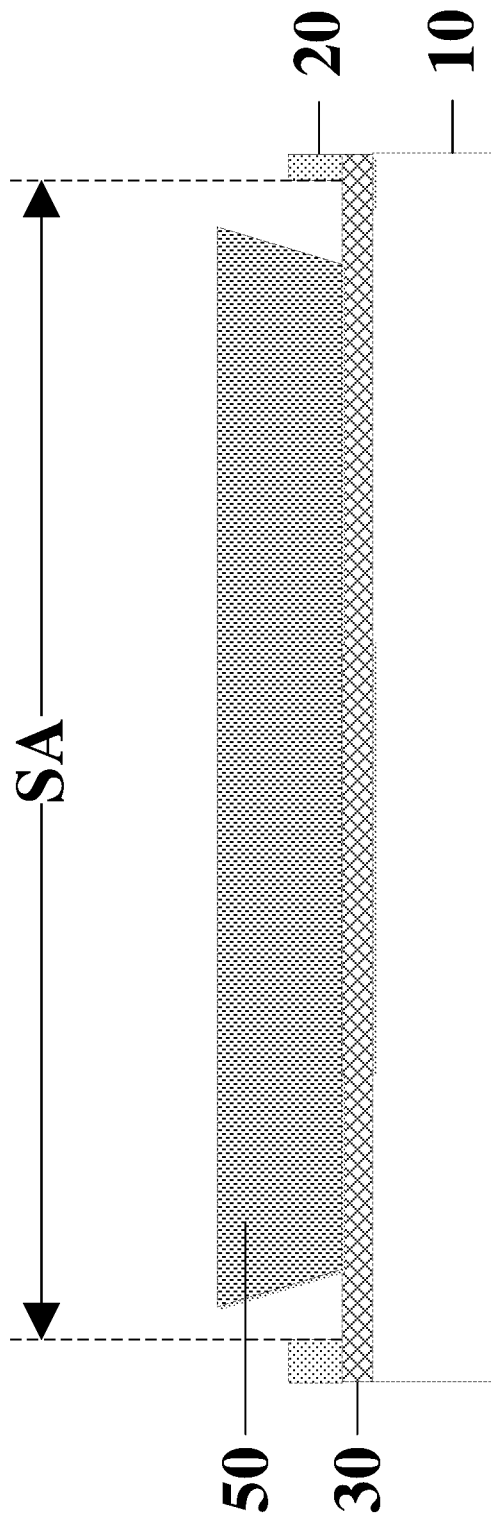
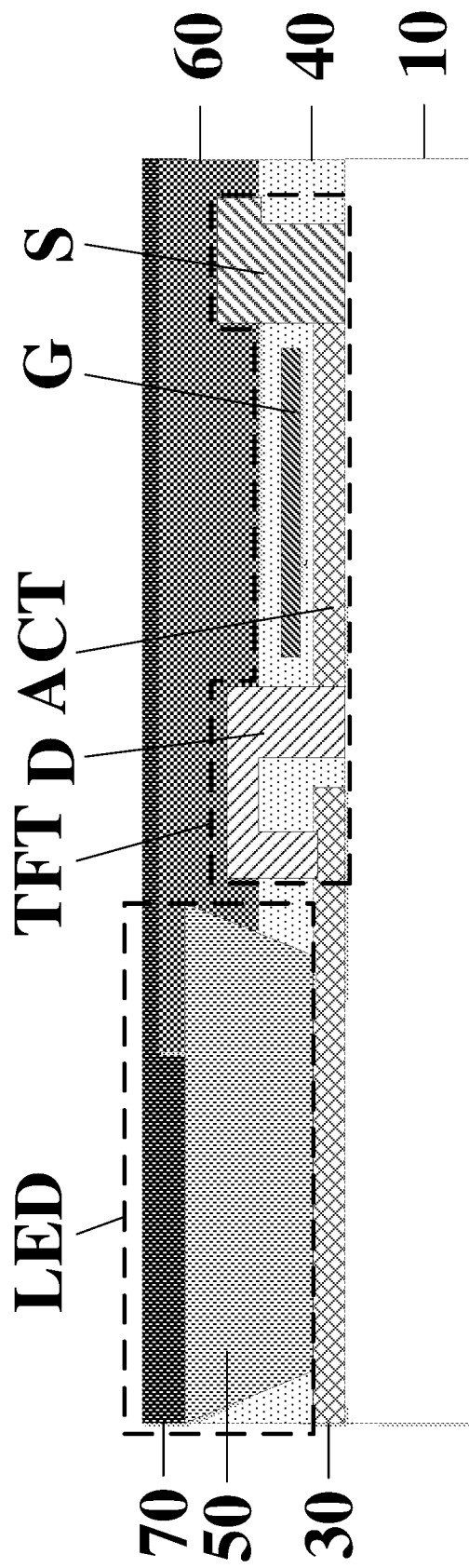


FIG. 3C



**FIG. 4**

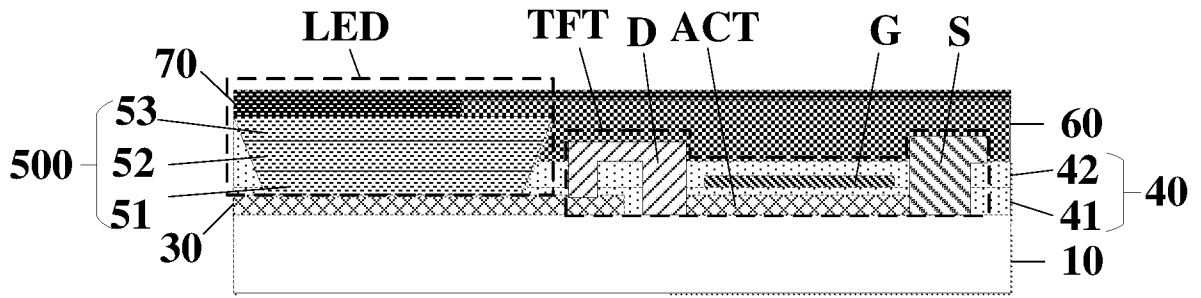


FIG. 5

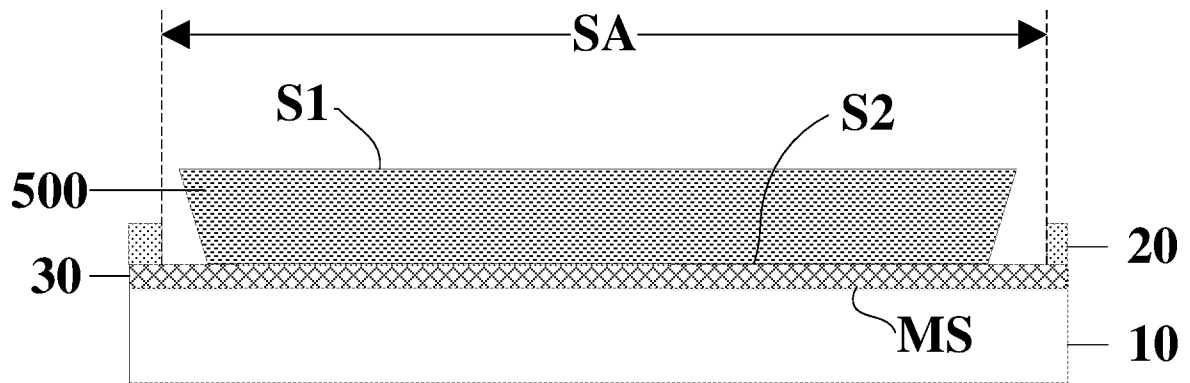


FIG. 6

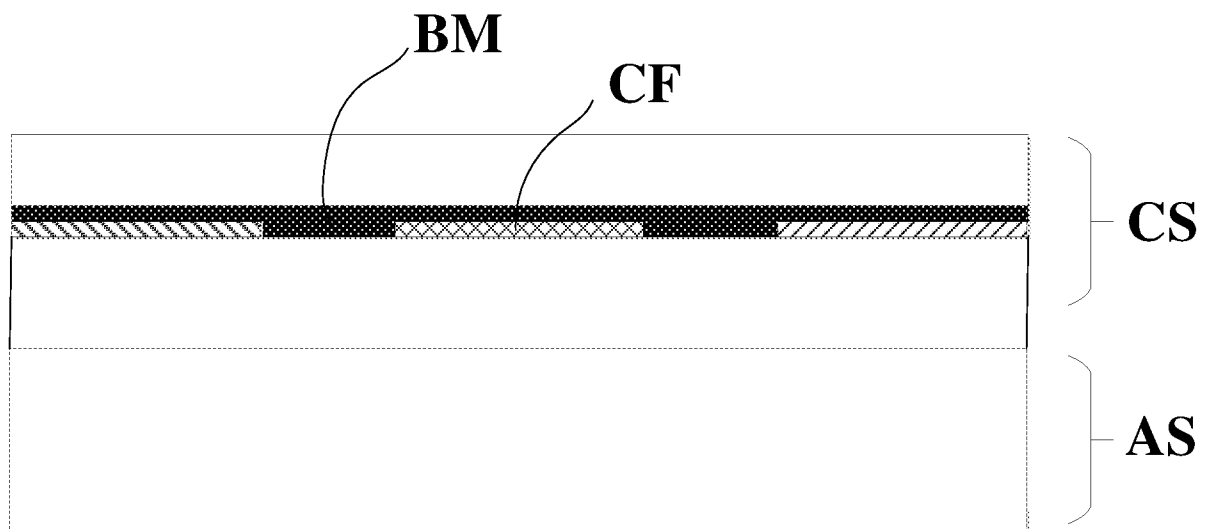


FIG. 7

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2018/117703

<b>A. CLASSIFICATION OF SUBJECT MATTER</b>		
H01L 27/15(2006.01)i; H01L 33/00(2010.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b>		
Minimum documentation searched (classification system followed by classification symbols)		
H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
WPI, EPODOC, CNPAT, CNKI, IEEE: fabricat+, micro, light, emitting, diode, LED, array, substrate, semiconductor, signal, line, material, growth		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2017337870 A1 (INNOLUX CORPORATION) 23 November 2017 (2017-11-23) claims 1-20	1-20
A	CN 108010933 A (GUANGDONG INSTITUTE OF SEMICONDUCTOR INDUSTRIAL TECHNOLOGY) 08 May 2018 (2018-05-08) the whole document	1-20
A	US 10002856 B1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 19 June 2018 (2018-06-19) the whole document	1-20
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
08 May 2019		30 May 2019
Name and mailing address of the ISA/CN		Authorized officer
National Intellectual Property Administration, PRC 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088 China		ZHANG,Tao
Facsimile No. (86-10)62019451		Telephone No. 86-(10)-53961356

**INTERNATIONAL SEARCH REPORT**  
**Information on patent family members**

International application No. <b>PCT/CN2018/117703</b>
---

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2017337870	A1	23 November 2017	CN	107403819	A	28 November 2011
				US	2017336690	A1	23 November 2017
				CN	107403820	A	28 November 2017
<hr/>							
CN	108010933	A	08 May 2018	None			
<hr/>							
US	10002856	B1	19 June 2018	US	2018219005	A1	02 August 2018
<hr/>							