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(54) **CONTROL DEVICE AND LIQUID CRYSTAL DISPLAY DEVICE**

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(57) **ABSTRACT**

Each pixel comprises: first and second sub-pixels; a buffer capacitance; first and second switching elements that connect the first and second sub-pixels to a source signal line; and a third switching element that connects the second sub-pixel to the buffer capacitance. The first and second switching elements operate according to a first gate control signal applied from a gate drive circuit. The third switching element operates according to a second gate control signal applied from the gate drive circuit. A power supply circuit generates a first power supply voltage and supplies same to the gate drive circuit during a first time period in which the first and second switching elements are turned ON, and thereafter, generates a second power supply voltage higher than the first power supply voltage, and supplies same to the gate drive circuit during a second time period in which the third switching element is turned ON.

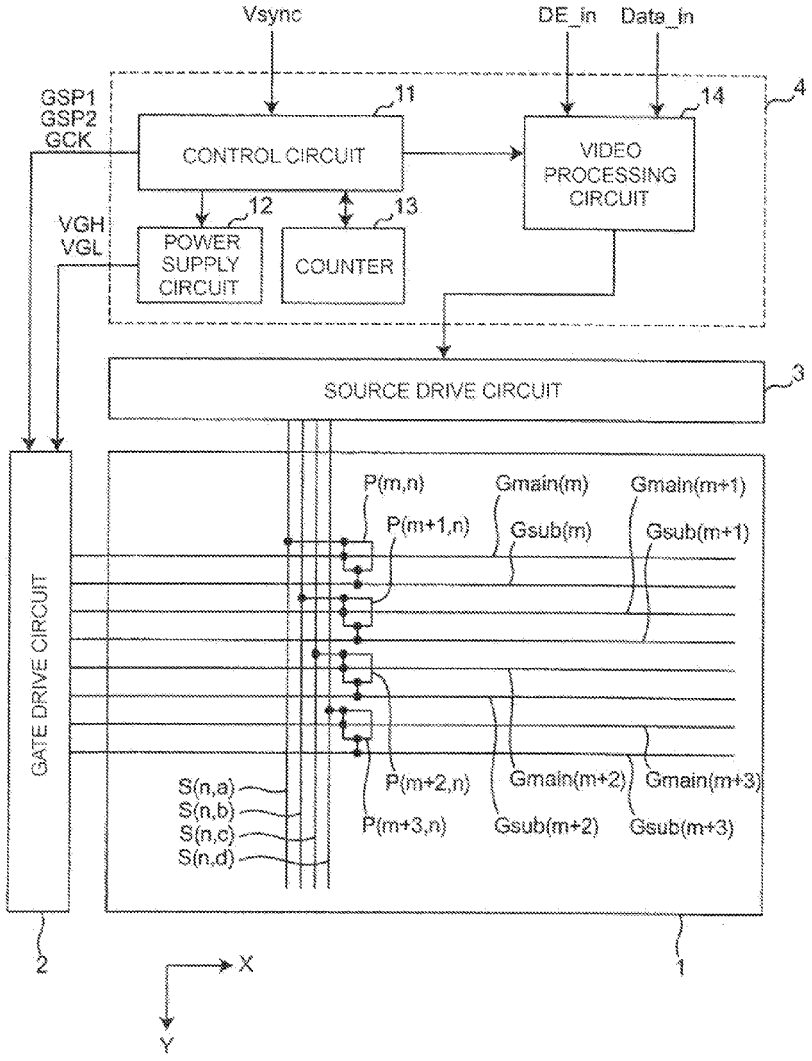


FIG. 1

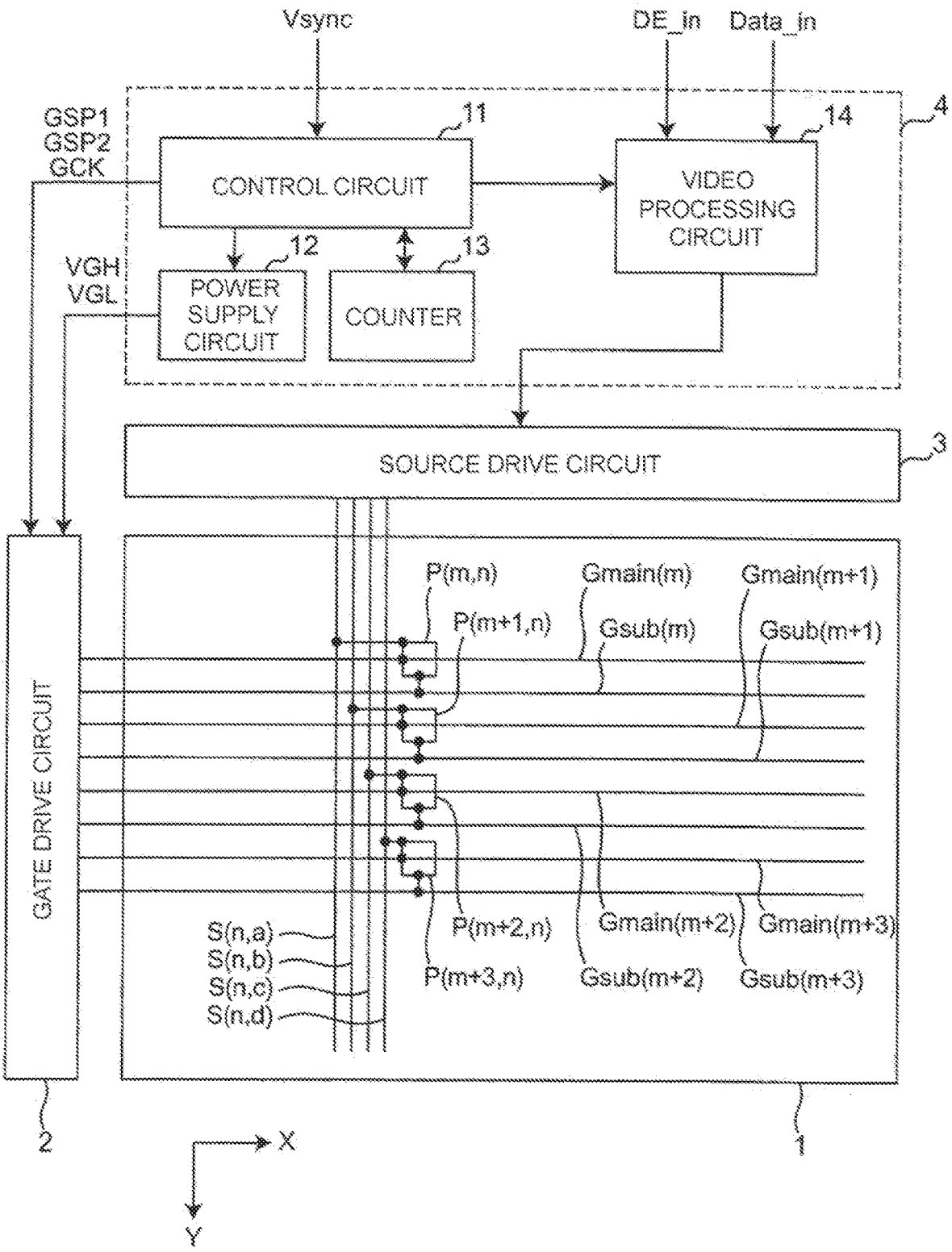

Vsync
DE_in
Data_in
GSP1
GSP2
GCK
11
14
4
CONTROL CIRCUIT
VIDEO PROCESSING CIRCUIT
12
13
VGH
VGL
POWER SUPPLY CIRCUIT
COUNTER
SOURCE DRIVE CIRCUIT
3
GATE DRIVE CIRCUIT
P(m,n)
Gmain(m)
Gmain(m+1)
P(m+1,n)
Gsub(m)
Gsub(m+1)
S(n,a)
S(n,b)
S(n,c)
S(n,d)
P(m+2,n)
P(m+3,n)
Gmain(m+2)
Gmain(m+3)
Gsub(m+2)
Gsub(m+3)
2
1
X
Y

FIG. 2

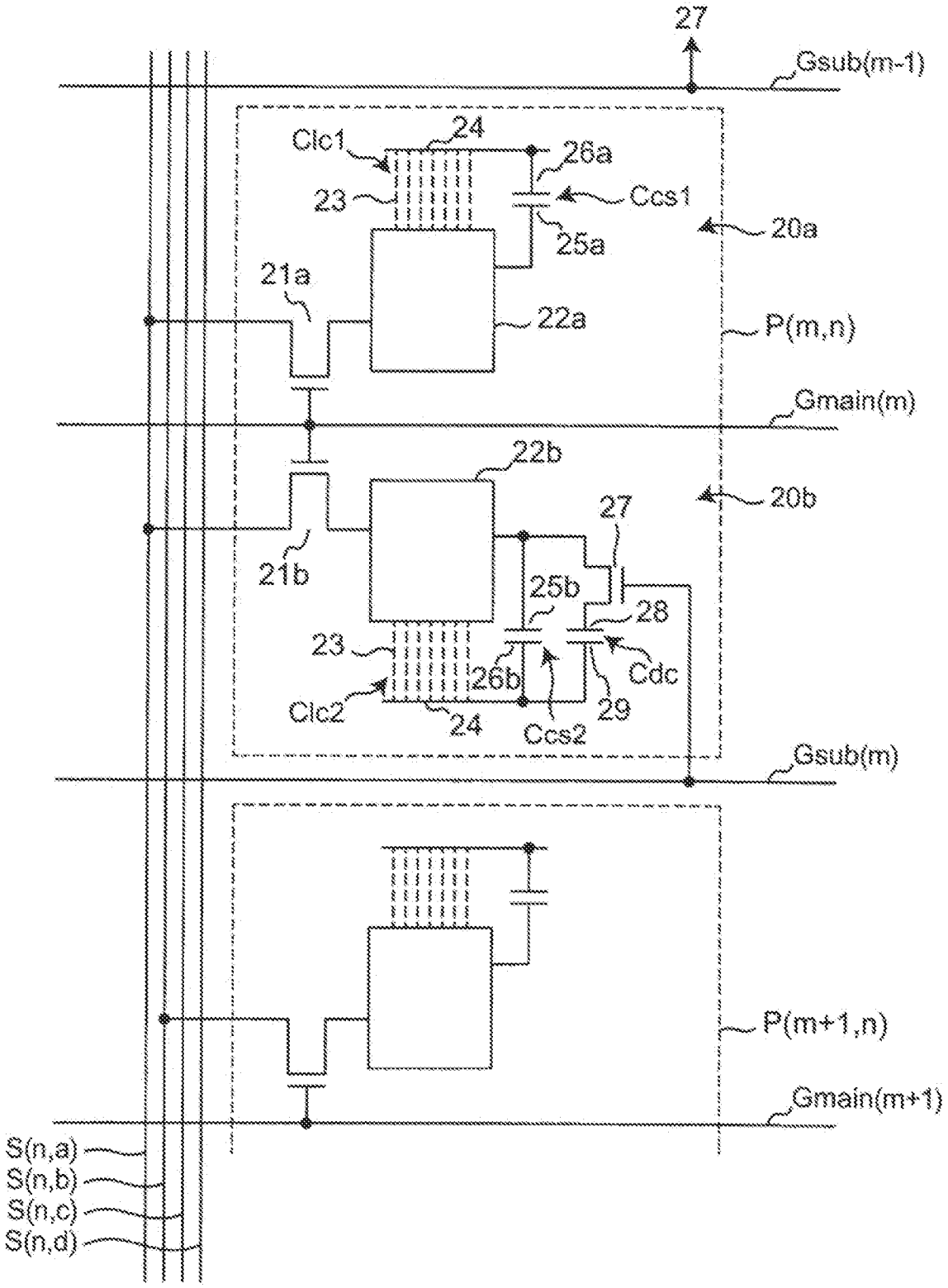

27
Gsub(m-1)
Clc1
24
26a
23
Ccs1
20a
25a
21a
22a
P(m,n)
Gmain(m)
22b
20b
27
21b
25b
28
23
26b
Cdc
Clc2
24
Ccs2
29
Gsub(m)
P(m+1,n)
Gmain(m+1)
S(n,a)
S(n,b)
S(n,c)
S(n,d)

FIG. 3

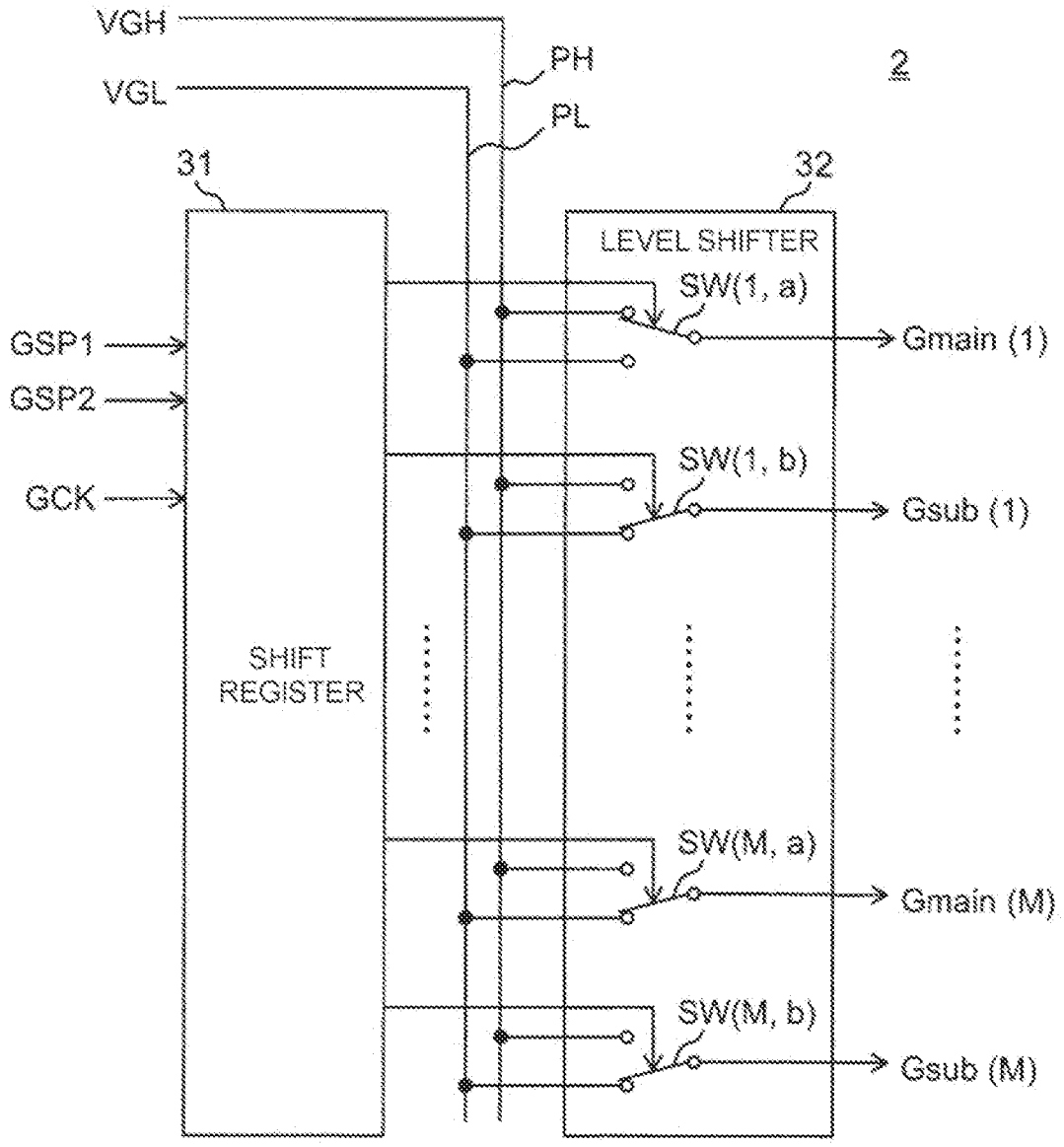

VGH
VGL
PH
PL
2
31
32
LEVEL SHIFTER
SW(1, a)
GSP1
GSP2
GCK
Gmain (1)
SW(1, b)
Gsub (1)
SHIFT REGISTER
SW(M, a)
Gmain (M)
SW(M, b)
Gsub (M)

FIG. 4

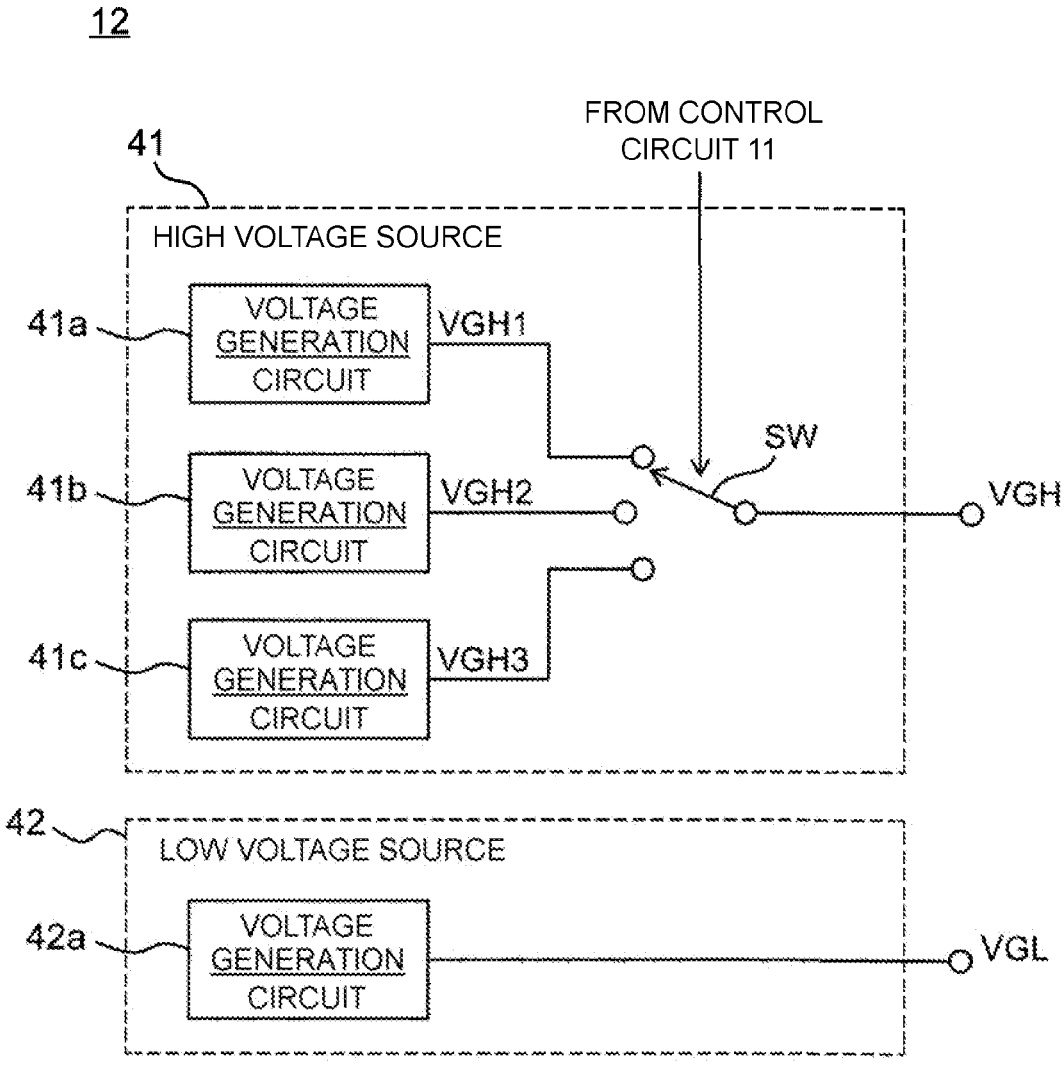

12
41
FROM CONTROL CIRCUIT 11
HIGH VOLTAGE SOURCE
41a
VOLTAGE GENERATION CIRCUIT
VGH1
41b
VOLTAGE GENERATION CIRCUIT
VGH2
41c
VOLTAGE GENERATION CIRCUIT
VGH3
SW
VGH
42
LOW VOLTAGE SOURCE
42a
VOLTAGE GENERATION CIRCUIT
VGL

FIG. 5

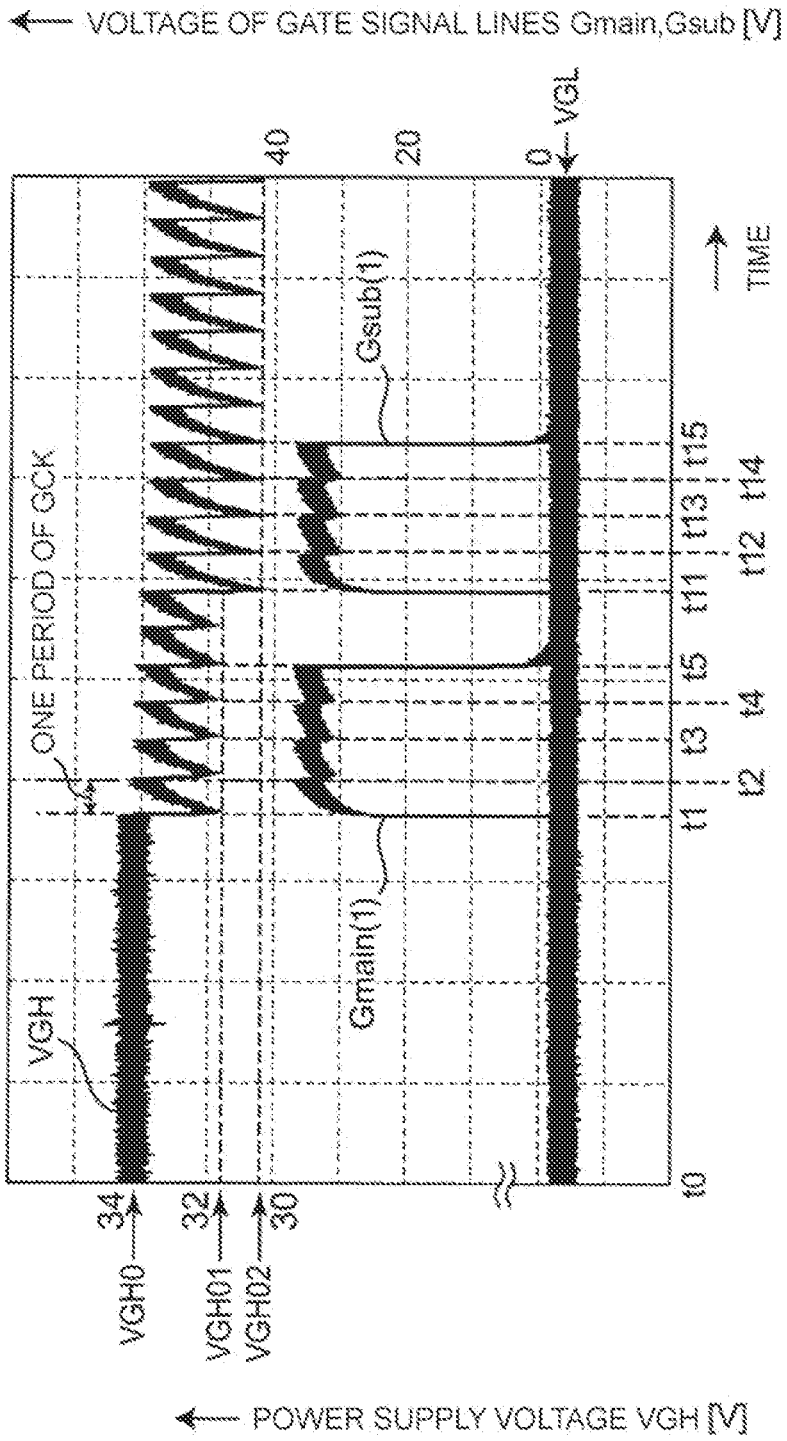

VOLTAGE OF GATE SIGNAL LINES Gmain,Gsub [V]
40
20
0
VGL
TIME
Gsub(1)
Gmain(1)
ONE PERIOD OF GCK
VGH
t0
t1
t2
t3
t4
t5
t11
t12
t13
t14
t15
34
32
30
VGH0
VGH01
VGH02
POWER SUPPLY VOLTAGE VGH [V]

FIG. 6

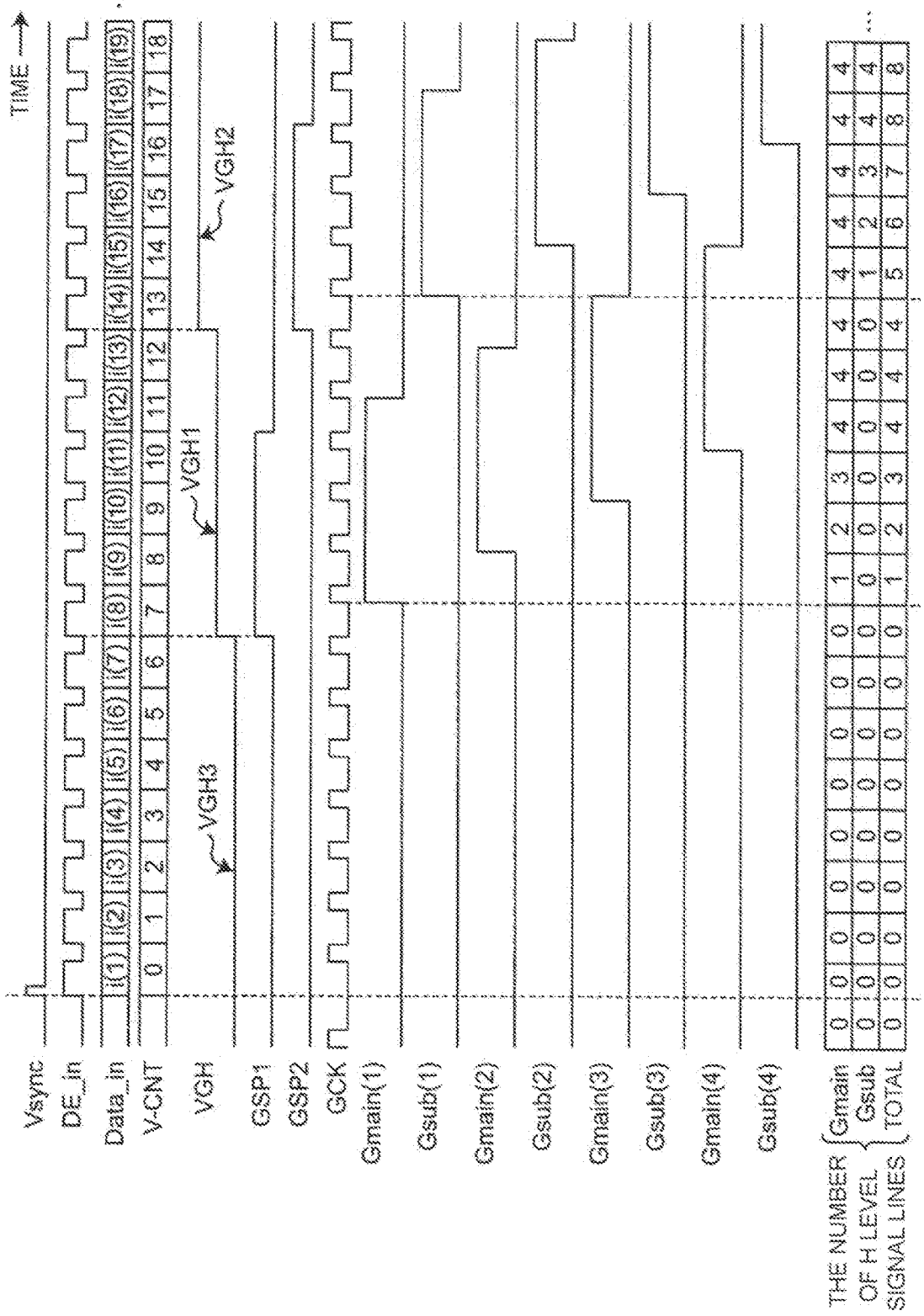

TIME
Vsync
DE_in
Data_in
V-CNT
VGH
GSP1
GSP2
GCK
Gmain(1)
Gsub(1)
Gmain(2)
Gsub(2)
Gmain(3)
Gsub(3)
Gmain(4)
Gsub(4)
VGH3
VGH1
VGH2
THE NUMBER OF H LEVEL SIGNAL LINES
Gmain
Gsub
TOTAL

FIG. 7

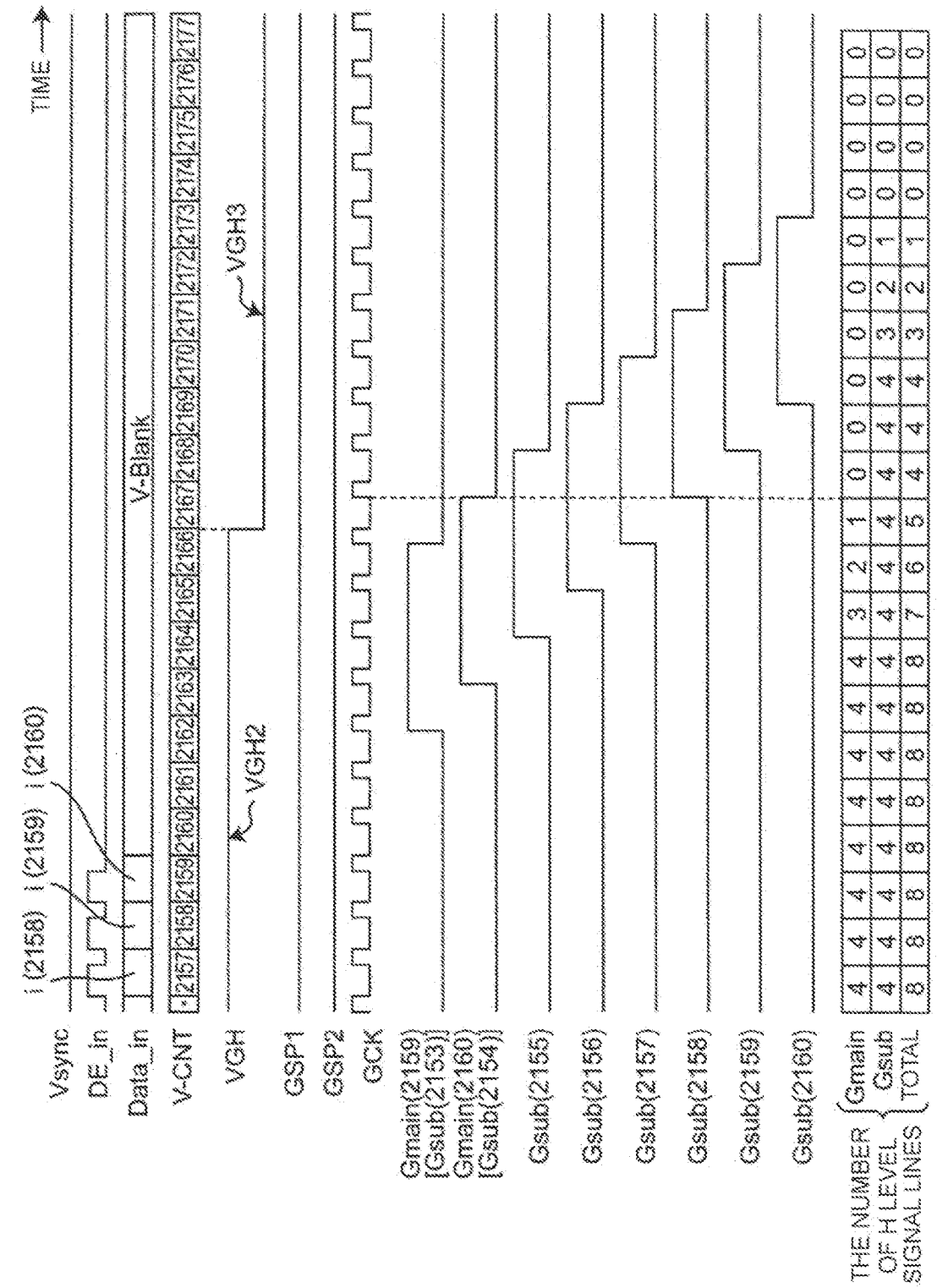
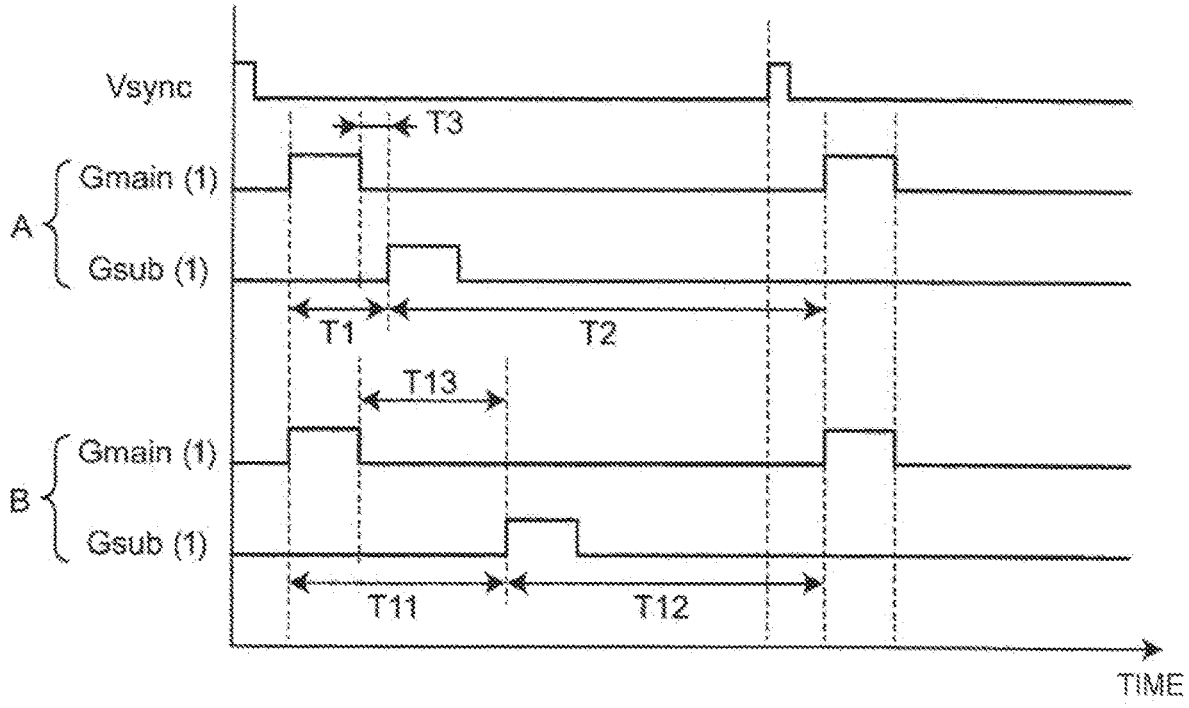

TIME
Vsync
DE_in
Data_in
V-CNT
VGH
GSP1
GSP2
GCK
Gmain(2159)
[Gsub(2153)]
Gmain(2160)
[Gsub(2154)]
Gsub(2155)
Gsub(2156)
Gsub(2157)
Gsub(2158)
Gsub(2159)
Gsub(2160)
i (2158)
i (2159)
i (2160)
V-Blank
VGH2
VGH3
THE NUMBER OF H LEVEL SIGNAL LINES
Gmain
Gsub
TOTAL

FIG. 8



CONTROL DEVICE AND LIQUID CRYSTAL DISPLAY DEVICE

TECHNICAL FIELD

[0001] The invention relates to a control device for a liquid crystal display apparatus and also relates to a liquid crystal display apparatus comprising such a control device.

BACKGROUND ART

[0002] In each of pixels of a liquid crystal display panel, changing the voltage applied to the pixel causes the orientation of liquid crystal molecules of the pixel to change, thereby causing the amount of light passing through the pixel to change to cause the pixel to light with a desired luminance. According to the operating principle, the viewing angle at which video can be viewed with a desired luminance is limited to the vicinity of the front of the liquid crystal display panel. When the liquid crystal display panel is viewed from an oblique direction, the video is seen with luminance being higher than the desired luminance (In other words, the video appears whiter). In particular, the amount of increase in luminance with respect to the desired luminance when the liquid crystal display panel is viewed from the oblique direction is the greatest when a voltage in the vicinity of a voltage corresponding to a halftone luminance is applied to the pixel.

[0003] To display video with a desired luminance over a greater viewing angle, a technique in Patent document 1, for example, is being proposed. According to Patent document 1, each of the pixels comprises a first subpixel and a second subpixel. The first subpixel and the second subpixel are connected to a source signal line via a first switching element and a second switching element, respectively. The second subpixel is further connected to a buffer capacitance via a third switching element. The first switching element and the second switching element are turned ON and OFF in accordance with a first gate control signal applied via a first gate signal line from a gate drive circuit. When the first switching element and the second switching element are turned ON, the first subpixel and the second subpixel are charged in accordance with the voltage of a source control signal applied via a source control line from a source drive circuit. The third switching element is turned ON and OFF in accordance with a second gate control signal applied via a second gate signal line from the gate drive circuit. When the third switching element is turned ON, the electric potential of the second subpixel decreases in accordance with the electric potential of the buffer capacitance.

[0004] According to Patent document 1, each of the pixels is divided into two subpixels, one subpixel of which is lit with luminance being greater than a desired luminance and the other subpixel of which is lit with luminance being less than the desired luminance, and the desired luminance is realized with the average luminance of these subpixels.

[0005] In the specification, realizing a desired luminance with the average luminance of subpixels as in Patent document 1 is below referred to as "a multi-pixel drive scheme".

PRIOR ART DOCUMENT

Patent Document

[0006] Patent Document 1: WO 2017/033341 A

SUMMARY OF THE INVENTION

Problem to be Solved by the Invention

[0007] In a liquid crystal display panel having a multi-pixel drive scheme, each of the pixels is controlled by at least two gate control signals, so that a greater load is applied to a gate drive circuit with respect to a case in which each of the pixels is controlled by one gate control signal. When the magnitude of the load applied to the gate drive circuit fluctuates, the voltage of the gate control signal also fluctuates. In this case, the ON time of switching elements of each of the pixels fluctuates, resulting in fluctuation in luminance of each of subpixels and each of the pixels. By such fluctuation in luminance of each of the pixels, non-uniformity can occur in luminance of the liquid crystal display panel.

[0008] An object of the invention is to solve the above-described problems and provide a control device that makes it possible to control a liquid crystal display panel having a multi-pixel drive scheme so as to make an occurrence of non-uniformity in luminance difficult. Moreover, an object of the invention is to provide a liquid crystal display apparatus comprising such liquid crystal display panel and control device.

Means to Solve the Problem

[0009] According to one aspect of the invention,

[0010] a control device for a liquid crystal display apparatus comprising a liquid crystal display panel, a gate drive circuit, and a source drive circuit, wherein

[0011] the liquid crystal display panel comprises a plurality of pixels arranged along a plurality of scanning lines; a plurality of first gate signal lines and a plurality of second gate signal lines connected to the gate drive circuit; and a plurality of source signal lines connected to the source drive circuit;

[0012] each pixel of the plurality of pixels comprises first subpixel and second subpixel; a buffer capacitance; first and second switching elements to connect the first subpixel and the second subpixel, respectively, to one source signal line; and a third switching element to connect the second subpixel to the buffer capacitance, wherein the first and second switching elements operate in accordance with a first gate control signal applied via one first gate signal line from the gate drive circuit and the third switching element operates in accordance with a second gate control signal applied via one second gate signal line from the gate drive circuit; and

[0013] the control device comprises a power supply circuit, wherein

[0014] in a first time period in which the first and second switching elements of each pixel, in the plurality of pixels, included in a first scanning line of a frame are transitioned from OFF to ON, the power supply circuit generates a first power supply voltage and supplies the first power supply voltage to the gate drive circuit, and, thereafter,

[0015] in a second time period in which the third switching element of each pixel included in the first scanning line of the frame is transitioned from OFF to ON, the power supply circuit generates a second power supply voltage higher than the first power

supply voltage and supplies the second power supply voltage to the gate drive circuit.

Effects of the Invention

[0016] A control device according to one aspect of the invention makes it possible to control a liquid crystal display panel having a multi-pixel drive scheme so as to make an occurrence of non-uniformity in luminance difficult by generating first and second power supply voltages using a power supply circuit as described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. **1** shows a block diagram of the configuration of a liquid crystal display apparatus according to an embodiment.

[0018] FIG. **2** shows a block diagram of the detailed configuration of each of pixels in FIG. **1**.

[0019] FIG. **3** shows a block diagram of the detailed configuration of a gate drive circuit in FIG. **1**.

[0020] FIG. **4** shows a block diagram of the detailed configuration of a power supply circuit in FIG. **1**.

[0021] FIG. **5** shows a graph of a change in power supply voltage supplied to a gate drive circuit of the liquid crystal display apparatus according to a comparative example.

[0022] FIG. **6** shows a timing chart of the operation of the liquid crystal display apparatus when a pixel in the vicinity of the upper end of the liquid crystal display panel in FIG. **1** is driven.

[0023] FIG. **7** shows a timing chart of the operation of the liquid crystal display apparatus when a pixel in the vicinity of the lower end of the liquid crystal display apparatus in FIG. **1** is driven.

[0024] FIG. **8** shows a timing chart to explain that luminance of the pixel changes by changing the delay time of a subgate control signal with respect to a main gate control signal in the liquid crystal display apparatus in FIG. **1**.

EMBODIMENT FOR CARRYING OUT THE INVENTION

[0025] With reference to the drawings, a control device and a liquid crystal display apparatus according to each embodiment of the invention will be described. In each Figure, the same reference numerals indicate the same constituting elements.

[0026] FIG. **1** shows a block diagram of the configuration of a liquid crystal display apparatus **100** according to an embodiment. The liquid crystal display apparatus **100** comprises a liquid crystal display panel **1**; a gate drive circuit **2**; a source drive circuit **3**; and a control device **4**.

[0027] The liquid crystal display panel **1** comprises a plurality of pixels P(m,n) ($1 \leq m \leq M$, $1 \leq n \leq N$); a plurality of main gate signal lines Gmain(m); a plurality of subgate signal lines Gsub(m); and a plurality of source signal lines S(n,x)(x=a,b,c,d).

[0028] The plurality of pixels P(m,n) is arranged along the row direction (X direction in FIG. **1**) and the column direction (Y direction in FIG. **1**) and, by these pixels P(m,n), a plurality of scanning lines is formed in the row direction of the liquid crystal display panel **1**. Each of frames of video to be displayed on the liquid crystal display panel **1** is scanned in order toward the lower end scanning line (also referred to as "the last scanning line") from the upper end scanning line (also referred to as "the first scanning line") of the liquid crystal display panel **1**. In FIG. **1**, for brevity of illustration, only four pixels P(m,n) to P(m+3,n) are shown.

[0029] As described below with reference to FIG. **2**, each of the pixels P(m,n) is configured to operate using a multi-pixel drive scheme. Therefore, each one of the pixels P(m,n) is connected to the gate drive circuit **2** via one of the main gate signal lines Gmain(m) and one of the subgate signal lines Gsub(m).

[0030] In the specification, the main gate signal line Gmain(m) and the subgate signal line Gsub(m) are also referred to as "a first gate signal line" and "a second gate signal line", respectively.

[0031] Moreover, in the example in FIG. **1**, the liquid crystal display panel **1** is configured to write video data in a temporally overlapping manner with respect to pixels P(m, n) to P(m+3,n) in four mutually adjacent rows. Therefore, pixels P(m,n) to P(m+3,n) on a certain column are connected to the source drive circuit **3** via four of the source signal lines S(n,a) to S(n,d). Pixels upper to the pixel P(m,n) and pixels lower to the pixel P(m+3,n) in FIG. **1** are also periodically connected to any one of the source signal lines S(n,a) to S(n,d) in the same manner as the pixels P(m,n) to P(m+3,n). Generally, to write video data into each of the pixels on one row, time having the length obtained by dividing time corresponding to one frame by the number of scanning lines can be utilized. However, in this case, as the number of scanning lines or the frame rate increases, the time to write video data into each of the pixels (or, in other words, the charging time of each of the pixels) can be insufficient. On the other hand, as in the example in FIG. **1**, by writing the video data in the temporally overlapping manner with respect to pixels P(m,n) to P(m+3,n) of a plurality of rows, the time of a sufficient length to write the video data into each of the pixels can be obtained even when the number of scanning lines or the frame rate increases.

[0032] The gate drive circuit **2** supplies a plurality of gate control signals, which selects each of the pixels P(m, n) for each row, to each of the pixels P(m,n) via the plurality of main gate signal lines Gmain(m) and the plurality of subgate signal lines Gsub(m) under the control of the control device **4**.

[0033] The source drive circuit **3** supplies a plurality of source control signals, which indicates the grayscale of each of the pixels P(m,n) of video along one of the scanning lines, to each of the pixels P(m,n) via the plurality of source signal lines S(n,x) under the control of the control device **4**. In detail, the source drive circuit **3** accumulates video data (digital serial data) supplied from the control device **4** by a horizontal scan period H to generate a source control signal (analog parallel data) representing one row of video and apply, in parallel, the generated source control signal to each of the source signal lines S(n,x). Here, the source control signal corresponding to one row is updated for each horizontal scanning period. Moreover, the polarity of the source control signal to be written to each of the pixels P(m,n) is inverted for each frame and for each line.

[0034] The control device **4** comprises a control circuit **11**; a power supply circuit **12**; a counter **13**; and a video processing circuit **14**.

[0035] The control circuit **11** controls the gate drive circuit **2** and the source drive circuit **3** so as to display one frame of video upon receiving a vertical synchronization signal Vsync from a pre-stage circuit (not shown). In particular, the control circuit **11** generates control signals GSP**1**, GSP**2** and

a clock signal GCK and supplies those to the gate drive circuit **2**. The control signal GSP**1** instructs the rise and the fall of the gate control signal of a main gate signal line Gmain(**1**) connected to a pixel P(**1**,n) included in the first scanning line of a frame. The control signal GSP**2** instructs the rise and the fall of the gate control signal of a subgate signal line Gsub(**1**) connected to the pixel P(**1**,n) included in the first scanning line of the frame. A fixed or variable delay time is set from when the gate control signal of the main gate signal line Gmain(**1**) is caused to transition from being at a low level to being at a high level to when the gate control signal of the subgate signal line Gsub(**1**) is caused to transition from being at a low level to being at a high level. A moment of the rise and the fall of the gate control signal for the pixel P(m,n) (2≤m≤M) included in the scanning line in a second row and beyond of the frame is determined by the gate drive circuit **2** based on the clock signal GCK so as to have a predetermined delay time with respect to the gate control signal for the pixel P(**1**,n).

[0036] The power supply circuit **12** generates power supply voltages VGH, VGL for the gate drive circuit **2** to generate the gate control signal and supplies the power supply voltages VGH, VGL to the gate drive circuit **2** under the control of the control circuit **11**. The power supply voltage VGL is used to generate the gate control signal at the low level. The power supply voltage VGH is higher than the power supply voltage VGL and is used to generate the gate control signal at the high level. The power supply circuit **12** generates the power supply voltage VGH being variable, in accordance with the number of main gate signal lines Gmain(m) and subgate signal lines Gsub(m) that supply the gate control signal at the high level.

[0037] The counter **13** generates a count value indicating the elapsed time from when the control circuit **11** receives the vertical synchronization signal Vsync. The count value of the counter **13** is used as an internal clock of the control device **4**. The control circuit **11** generates the clock signal GCK for the gate drive circuit **2** based on the count value of the counter **13**.

[0038] Upon receiving a data signal Data_in indicating video data and an enable signal DE_in indicating the beginning portion of each of the scanning lines in the video data from a pre-stage circuit (not shown), the video processing circuit **14** sends the video data to the source drive circuit **3** and controls the source drive circuit **3**.

[0039] The control device **4** is also referred to as "a timing controller".

[0040] FIG. **2** shows a block diagram of the detailed configuration of the pixels P(m,n) in FIG. **1**. As described previously, each of the pixels P(m,n) is configured to operate using the multi-pixel drive scheme. Therefore, the pixels P(m,n) comprise subpixels **20***a*, **20***b* being split equally into two in the vertical direction of the display screen of the liquid crystal display panel **1**.

[0041] The subpixel **20***a* comprises a switching element **21***a*; a subpixel electrode **22***a*; a liquid crystal layer **23**; a counter electrode **24**; and auxiliary capacitance electrodes **25***a*, **26***a*. The source of the switching element **21***a* is connected to the source signal line S(n,a), the drain thereof is connected to the subpixel electrode **22***a*, and the gate thereof is connected to the main gate signal line Gmain(m). In this way, the subpixel electrode **22***a* is connected to the source signal line S(n,a) via the switching element **21***a*. The switching element **21***a* operates in accordance with the gate control signal applied via the main gate signal line Gmain (m) from the gate drive circuit **2**. The switching element **21***a* is a thin-film transistor (TFT), for example. The subpixel electrode **22***a* and the counter electrode **24** face each other via the liquid crystal layer **23** and form a liquid crystal capacitance Clc**1**. Moreover, the auxiliary capacitance electrodes **25***a*, **26***a* oppose each other and form an auxiliary capacitance Ccs**1**. The subpixel electrode **22***a* and the auxiliary capacitance electrode **25***a* are electrically connected to each other. Moreover, the counter electrode **24** and the auxiliary capacitance electrode **26***a* are electrically connected to each other.

[0042] The subpixel **20***b* comprises a switching element **21***b*; a subpixel electrode **22***b*; the liquid crystal layer **23**; the counter electrode **24**; auxiliary capacitance electrodes **25***b*, **26***b*; a switching element **27**; and buffer capacitance electrodes **28**, **29**. The source of the switching element **21***b* is connected to the source signal line S(n,a) being the same as for the switching element **21***a*, the drain thereof is connected to the subpixel electrode **22***b*, and the gate thereof is connected to the main gate signal line Gmain(m) being the same as for the switching element **21***a*. In this way, the subpixel electrode **22***b* is connected to the source signal line S(n,a) via the switching element **21***b*. The switching element **21***b* operates in accordance with the gate control signal applied via the main gate signal line Gmain(m) from the gate drive circuit **2**. The buffer capacitance electrode **28** is connected to the subpixel electrode **22***b* via the switching element **27**. The gate of the switching element **27** is connected to the subgate signal line Gsub(m). The switching element **27** operates in accordance with the gate control signal applied via the subgate signal line Gsub(m) from the gate drive circuit **2**. The switching elements **21***b*, **27** are thin-film transistors (TFTs), for example. The subpixel electrode **22***b* and the counter electrode **24** face each other via the liquid crystal layer **23** and form a liquid crystal capacitance Clc**2**. Moreover, the auxiliary capacitance electrodes **25***b*, **26***b* face each other and form an auxiliary capacitance Ccs**2**. Furthermore, the buffer capacitance electrodes **28**, **29** face each other and form a buffer capacitance Cdc. In other words, the liquid crystal capacitance Clc**2** and the auxiliary capacitance Ccs**2** are connected to the buffer capacitance Cdc via the switching element **27**. The subpixel electrode **22***b* and the auxiliary capacitance electrode **25***b* are electrically connected to each other. Moreover, the counter electrode **24**, the auxiliary capacitance electrode **26***b*, and the buffer capacitance electrode **29** are electrically connected to one another.

[0043] The sizes of the subpixel electrodes **22***a*, **22***b* can be equal to each other, or can be different from each other. Moreover, the counter electrode **24** of the subpixel **20***a* and the counter electrode **24** of the subpixel **20***b* can be integrated with each other or can be provided separately. Furthermore, each of the pixels P(m,n) can be divided into three or more subpixels.

[0044] As shown in FIG. **2**, each of the main gate signal lines Gmain(m) can be arranged so as to cross the center of each of the pixels P (m,n). Moreover, as shown in FIG. **2**, each of the subgate signal lines Gsub(m) can be arranged between pixels P(m,n) and P(m+1,n) adjacent to each other. In this case, the main gate signal line Gmain(m) and the subgate signal line Gsub(m) in each row are appropriately

spaced, so that leakage of signal between the main gate signal line Gmain(m) and the subgate signal line Gsub(m) is suppressed.

[0045] In the specification, the subpixel **20***a* is also referred to as "a first subpixel", and the subpixel **20***b* is also referred to as "a second subpixel". Moreover, in the specification, the switching element **21***a* is also referred to as "a first switching element", the switching element **21***b* is also referred to as "a second switching element", and the switching element **27** is also referred to as "a third switching element". Furthermore, in the specification, a gate control signal applied via the main gate signal line Gmain from the gate drive circuit **2** is also referred to as "a first gate control signal" or "a main gate control signal". Moreover, in the specification, the gate control signal applied via the subgate signal line Gsub from the gate drive circuit **2** is also called "a second gate control signal" or "a subgate control signal".

[0046] FIG. **3** shows a block diagram of the detailed configuration of the gate drive circuit **2** in FIG. **1**. The gate drive circuit **2** comprises a shift register **31**; a level shifter **32**; and power supply lines PH, PL.

[0047] The power supply lines PH, PL are connected to the power supply circuit **12** in FIG. **1**. The power supply voltages VGH, VGL generated by the power supply circuit **12** are supplied to the level shifter **32** via the power supply lines PH, PL.

[0048] The level shifter **32** generates the main gate control signal and the subgate control signal from the power supply voltages VGH, VGL under the control of the shift register **31**. The level shifter **32** comprises switches SW (m,y) (1≤m≤M, y=a,b) to operate under the control of the shift register **31**. Each of the switches SW (m,a) comprises two input terminals connected to the power supply lines PH, PL, respectively, and an output terminal connected to the main gate signal line Gmain(m). When each of the switches SW(m,a) connects the power supply line PH to the main gate signal line Gmain(m), a main gate control signal being at the high level is generated; and when connecting the power supply line PL to the main gate signal line Gmain(m), a main gate control signal being at the low level is generated. Moreover, each of the switches SW (m,b) comprises two input terminals connected to the power supply lines PH, PL, respectively, and an output terminal connected to the subgate signal line Gsub(m). When each of the switches SW(m,b) connects the power supply line PH to the subgate signal line Gsub(m), a subgate control signal being at the high level is generated, and when it connecting the power supply line PL to the subgate signal line Gsub(m), a subgate control signal being at the low level is generated.

[0049] Based on the control signals GSP**1**, GSP**2** and the clock signal GCK supplied from the control circuit **11** in FIG. **1**, the shift register **31** controls each of the switches SW(m,y) so as to adjust the timing of the rise and the fall of the main gate control signal and the subgate control signal.

[0050] In the initial state, the shift register **31** controls each of the switches SW(m,y) so as to connect the power supply line PL to the main gate signal Gmain(m) or the subgate signal line Gsub(m).

[0051] After the control signal GSP**1** transitions from being at the low level to being at the high level, the shift register **31** controls the switch SW (**1**,a) so as to connect the power supply line PH to the main gate signal line Gmain(**1**) in conjunction with the first rise of the clock signal GCK. Thereafter, after the control signal GSP**1** transitions from being at the high level to being at the low level, the shift register **31** controls the switch SW (**1**,a) so as to connect the power supply line PL to the main gate signal line Gmain(**1**) in conjunction with the first rise of the clock signal GCK. With the main gate control signal of the main gate signal line Gmain(**1**) as a reference, the shift register **31** controls each of the other switches SW (m,a) so that the main gate control signals of the other main gate signal lines Gmain(m) (2≤m≤M) have a delay time corresponding to a predetermined number of clocks and have the same waveform.

[0052] Moreover, after the control signal GSP**2** transitions from being at the low level to being at the high level, the shift register **31** controls the switch SW (**1**,b) so as to connect the power supply line PH to the subgate signal line Gsub(**1**) in conjunction with the first rise of the clock signal GCK. Thereafter, after the control signal GSP**2** transitions from being at the high level to being at the low level, the shift register **31** controls the switch SW (**1**,b) so as to connect the power supply line PL to the subgate signal line Gsub(**1**) in conjunction with the first rise of the clock signal GCK. With the subgate control signal of the subgate signal line Gsub(**1**) as a reference, the shift register **31** controls each of the other switches SW (m,b) so that the subgate control signals of the other subgate signal lines Gsub(m) (2≤m≤M) have a delay time corresponding to a predetermined number of clocks and have the same waveform.

[0053] FIG. **4** shows a block diagram of the detailed configuration of the power supply circuit **12** in FIG. **1**. The power supply circuit **12** comprises a high voltage source **41** and a low voltage source **42**. The high voltage source **41** and the low voltage source **42** are connected to the power supply lines PH,PL, respectively, in FIG. **3**.

[0054] The high voltage source **41** comprises voltage generation circuits **41***a* to **41***c* and a switch SW. The voltage generation circuit **41***a* generates a power supply voltage VGH**1** to be used when the gate drive circuit **2** does not generate the subgate control signal being at the high level, but causes only the main gate control signal to transition from being at the low level to being at the high level. The voltage generation circuit **41***b* generates a power supply voltage VGH**2** to be used when the gate drive circuit **2** generates both the main gate control signal being at the high level and the subgate control signal being at the high level. The power supply voltage VGH**2** is higher than the power supply voltage VGH**1**. The voltage generation circuit **41***c* generates a power supply voltage VGH**3** to be used when the gate drive circuit **2** does not generate the main gate control signal being at the high level, but causes only the subgate control signal to transition from being at the low level to being at the high level. The power supply voltage VGH**3** is lower than the power supply voltage VGH**1**. The power supply voltages VGH**1** to VGH**3** are set so as to be higher than the gate threshold voltage of the switching elements **21***a*, **21***b*, **27** even if taking into account the voltage drop up to reaching the switching elements **21***a*, **21***b*, **27** (see FIG. **2**) of each of the pixels P (m,n). The switch SW supplies one of the power supply voltages VGH**1** to VGH**3** to the gate drive circuit **2** as the power supply voltage VGH under the control of the control circuit **11**.

[0055] In the specification, the power supply voltage VGH**1** is also referred to as "a first power supply voltage", the power supply voltage VGH**2** is also referred to as "a second power supply voltage", and the power supply voltage VGH**3** is also referred to as "a third power supply voltage".

[0056] The low voltage source **42** comprises a voltage generation circuit **42***a*. The voltage generation circuit **42***a* generates a power supply voltage VGL to be used when each of the pixels P(m,n) of the liquid crystal display panel **1** is not driven (in other words, when each of the switching elements **21**, **21***b*, **27** is turned OFF). The power supply voltage VGL is lower than the gate threshold voltage of the switching elements **21**, **21***b*, **27** (see FIG. **2**) of each of the pixels P (m, n).

[0057] According to the multi-pixel drive scheme, each of the pixels P(m,n) in FIG. **2** operates as follows.

[0058] When the main gate control signal of the main gate signal line Gmain(m) transitions from being at the low level to being at the high level, the switching elements **21***a*, **21***b* of the pixels P(m,n) are turned ON. In this way, the voltage of the source control signal of the source signal line S(n,x) is applied to the subpixel electrodes **22***a*, **22***b* and the auxiliary capacitance electrodes **25***a*, **25***b* of the pixels P(m,n) and, therefore, the voltage applied to the liquid crystal capacitances Clc**1**, Clc**2** and the auxiliary capacitances Ccs**1**, Ccs**2** equals the voltage of the source signal line S(n,x). Thereafter, when the main gate control signal of the main gate signal line Gmain(m) transitions from being at the high level to being at the low level, the switching elements **21***a*, **21***b* of the pixels P (m,n) are turned OFF.

[0059] After the main gate control signal of the main gate signal line Gmain(m) transitions from being at the high level to being at the low level, and through a predetermined delay time, the subgate control signal of the subgate signal line Gsub(m) transitions from being at the low level to being at the high level; and at this moment, the switching element **27** of the pixels P(m,n) is turned ON. In this way, the buffer capacitance Cdc is connected in parallel to the liquid crystal capacitance Clc**2** and the auxiliary capacitance Ccs**2**.

[0060] As described previously, the polarity of the source control signal written into each of the pixels P(m,n) is inverted for each frame and for each line. Before the switching element **27** is turned ON, the buffer capacitance Cdc has the polarity in reverse of that of charges accumulated in the liquid crystal capacitance Clc**2** and the auxiliary capacitance Ccs**2** since the buffer capacitance Cdc has charges accumulated one frame before. Therefore, when the switching element **27** is turned ON, positive charges (or negative charges) move to the buffer capacitance Cdc from the liquid crystal capacitance Clc**2** and the auxiliary capacitance Ccs**2**, and the absolute value of the voltage applied to the liquid crystal capacitance Clc**2** decreases. On the other hand, the voltage applied to the liquid crystal capacitance Clc**1** is not influenced by the switching element **27** being turned ON. Therefore, the absolute value of the voltage applied to the liquid crystal capacitance Clc**2** is less than the absolute value of the voltage applied to the liquid crystal capacitance Clc**1**, resulting in a decrease in luminance of the subpixel **20***b* with respect to luminance of the subpixel **20***a*. Since a desired luminance is realized by average luminance of the subpixels **20***a*, **20***b*, it is possible to realize a halftone luminance without applying, to the subpixels **20***a*, **20***b*, a voltage in the vicinity of a voltage corresponding to the halftone luminance. This makes it possible to display video with a desired luminance over a wide viewing angle.

[0061] As described previously, with the liquid crystal display panel having the multi-pixel drive scheme according to the conventional art, each of the pixels is controlled by at least two gate control signals, so that a greater load is applied to the gate drive circuit with respect to a case in which each of the pixels is controlled by one gate control signal. When the load applied to the gate drive circuit fluctuates, the voltage of the gate control signal also fluctuates, thereby resulting in the ON time of the switching element of each of the pixels to fluctuate.

[0062] FIG. **5** shows a graph of a change in power supply voltage supplied to a gate drive circuit of a liquid crystal display apparatus according to a comparative example. The example in FIG. **5** shows a case in which fixed power supply voltages VGH, VGL are supplied to the gate drive circuit **2** in the liquid crystal display apparatus comprising the liquid crystal display panel **1** and the gate drive circuit **2**, which liquid crystal display apparatus is described with reference to FIGS. **1** to **3**. FIG. **5** shows simulation results of the fluctuation of the power supply voltage VGH, the waveform of the main gate control signal of the main gate signal line Gmain(**1**), and the waveform of the subgate control signal of the subgate signal line Gsub(**1**).

[0063] A fixed power supply voltage VGH=VGH**0** is supplied to the gate drive circuit **2**. In the time interval t**0** to t**1**, all of the main gate control signals and all of the subgate control signals are at the low level.

[0064] When the main gate control signal of the main gate signal line Gmain(**1**) transitions from being at the low level to being at the high level at the time t**1**, the power supply voltage VGH decreased to the voltage VGH**01** due to increase of the loads that are connected to the main gate signal line Gmain. The main gate control signal of the main gate signal line Gmain(**1**) was maintained to be at the high level over four periods of the clock signal GCK and transitioned from being at the high level to being at the low level at the time t**5**. The main gate control signal of the main gate signal line Gmain(**2**) was generated with a delay time, corresponding to one period of the clock signal GCK, with respect to the main gate control signal of the main gate signal line Gmain(**1**). Similarly, the main gate control signal of the main gate signal line Gmain(**3**) and beyond was also generated with a delay time, corresponding to one period of the clock signal GCK, with respect to the main gate control signal of the immediately preceding main gate signal line Gmain(m). As shown in FIG. **5**, when the gate drive circuit **2** did not generate a subgate control signal being at the high level, but caused only the main gate control signal to transition from being at the low level to being at the high level (time t**1** to t**11**), the power supply voltage VGH decreased to the voltage VGH**01**.

[0065] At the time t**11** at which the subgate control signal of the subgate signal line Gsub(**1**) transitions from being at the low level to being at the high level while maintaining the main gate control signal of a part of the main gate signal lines Gmain(m) at the high level, the power supply voltage VGH decreased to the voltage VGH**02** due to increase of the loads that are connected to the subgate signal line Gsub(**1**) causes. The subgate control signal of the subgate signal line Gsub(**1**) was maintained to be at the high level over four periods of the clock signal GCK and transitioned from the high level to the low level at the time t**15**. The subgate control signal of the subgate signal line Gsub(**2**) was generated with a delay time, corresponding to one period of the clock signal GCK, with respect to the subgate control signal of the subgate signal line Gsub(**1**). Similarly, the subgate control signals of the subgate signal line Gsub(**3**) and beyond are also generated with a delay time, corresponding

to one period of the clock signal GCK, with respect to the subgate control signal of the immediately preceding subgate signal line Gsub(m). As shown in FIG. **5**, when the gate drive circuit **2** generated both the main gate control signal being at the high level and the subgate control signal being at the high level (at or after the time t**11**), the power supply voltage VGH decreased to the voltage VGH**02**.

[0066] When the power supply voltage VGH decreases, the voltage of the main gate control signal applied to the gate of the switching elements **21***a*,**21***b* of each of the pixels P(m,n) decreases, and the ON time of the switching elements **21**, **21***b* decreases. When the ON time of the switching elements **21***a*, **21***b* is insufficient, the charging time of the subpixels **20***a*, **20***b* by the voltage of the source control signal decreases, and consequently, the luminance of the subpixels **20***a*, **20***b* decreases.

[0067] Moreover, when the loads that are connected to the main gate signal line Gmain(m) decreases, the power supply voltage VGH increases. When the power supply voltage VGH increases, the voltage of the subgate control signal applied to the gate of the switching element **27** of each of the pixels P(m,n) increases, and the ON time of the switching element **27** increases. When the ON time of the switching element **27** increases, the time in which the switching element **27** is connected to the buffer capacitance Cdc increases, and consequently, the amount of decrease in luminance of the subpixel **20***b* increases.

[0068] Due to the fluctuation in luminance of each of the subpixels **20***a*, **20***b* and the fluctuation in luminance of each of the pixels P(m,n) that occur in this way, non-uniformity in luminance of the liquid crystal display panel **1** can occur.

[0069] In the liquid crystal apparatus **100** according to the embodiment, the control device **4** controls the liquid crystal display panel **1** having a multi-pixel drive scheme so as to make an occurrence of non-uniformity in luminance difficult. Below, the operation thereof is described.

[0070] FIG. **6** shows a timing chart of the operation of the liquid crystal display apparatus **100** when the pixel P (m,n) in the vicinity of the upper end of the liquid crystal display panel **1** in FIG. **1** is driven.

[0071] The vertical synchronization signal Vsync indicates the beginning portion of each frame. The control circuit **11** causes the counter **13** to start counting of a count value V-CNT in accordance with the rise of the vertical synchronization signal Vsync. In the initial state, the control circuit **11** controls the power supply circuit **12** so as to generate the power supply voltage VGH**3** and to supply the power supply voltage VGH**3** to the gate drive circuit **2**.

[0072] When the count value V-CNT=7 is reached, the control circuit **11** causes the control signal GSP**1** to transition to being at the high level from being at the low level. At the same time therewith, the control circuit **11** controls the power supply circuit **12** so as to generate the power supply voltage VGH**1** being higher than the power supply voltage VGH**3** and supply the power supply voltage VGH**1** to the gate drive circuit **2**. As described previously, the main gate control signal of the main gate signal line Gmain(**1**) is caused to transition from being at the low level to being at the high level in conjunction with the first rise of the clock signal GCK after the control signal GSP**1** transitions from being at the low level to being at the high level. In other words, in the time interval with the count value V-CNT=7, the switching elements **21***a*, **21***b* of each of the pixels P(**1**,n) included in the first scanning line of the frame are caused to transition from OFF to ON, and the load that is applied to the gate drive circuit **2** increases. The control circuit **11** controls the power supply circuit **12** so as to generate the power supply voltage VGH**1** and supply the power supply voltage VGH**1** to the gate drive circuit **2** in a predetermined time period including the time interval with the count value V-CNT=7, namely, a time period over the count value V-CNT=7 to 12 (also referred to as "a first time period"). In other words, the control circuit **11** controls the power supply circuit **12** so as to generate the power supply voltage VGH**1** and supply the power supply voltage VGH**1** to the gate drive circuit **2** in the first time period in which the switching elements **21***a*, **21***b* of each of the pixels P(**1**,n) included in the first scanning line of the frame are transitioned from OFF to ON. The control circuit **11** causes the control signal GSP**1** to transition from being at the high level to being at the low level when the count value V-CNT=11 is reached.

[0073] Thereafter, the control circuit **11** causes the control signal GSP**2** to transition from being at the low level to being at the high level when the count value V-CNT=13 is reached. At the same time therewith, the control circuit **11** controls the power supply circuit **12** so as to generate the power supply voltage VGH**2** being higher than the power supply voltage VGH**1** and supply the power supply voltage VGH**2** to the gate drive circuit **2**. As described previously, the subgate control signal of the subgate signal line Gsub(**1**) is caused to transition from being at the low level to being at the high level in conjunction with the first rise of the clock signal GCK after the control signal GSP**2** transitions from being at the low level to being at the high level. In other words, in the time interval with the count value V-CNT=13, the switching element **27** of each of the pixels P(**1**,n) included in the first scanning line of the frame is caused to transition from OFF to ON, and the load that is applied to the gate drive circuit **2** increases. The control circuit **11** controls the power supply circuit **12** so as to generate the power supply voltage VGH**2** and supply the power supply voltage VGH**2** to the gate drive circuit **2** in a predetermined time period including the time interval with the count value V-CNT=13, namely, a time period over the count value V-CNT=13 and beyond (also referred to as "a second time period"). In other words, the control circuit **11** controls the power supply circuit **12** so as to generate the power supply voltage VGH**2** and supply the power supply voltage VGH**2** to the gate drive circuit **2** in the second time period in which the switching element **27** of each of the pixels P(**1**,n) included in the first scanning line of the frame is transitioned from OFF to ON. The second time period continues up to a start of the below-described third time period, or, in other words, up to a time interval with the count value V-CNT=2166. The control circuit **11** causes the control signal GSP**2** to transition from being at the high level to being at the low level when the count value V-CNT=17 is reached.

[0074] In this way, when the switching element **27** of each of the pixels P(**1**,n) included in the first scanning line of the frame is turned ON, the power supply voltage VGH supplied to the gate drive circuit **2** is increased, and thereby it is possible to cancel out a decrease in the power supply voltage VGH (see FIG. **5**) due to an increase in load. In this way, the ON times of the switching elements **21***a*, **21***b* of each of the pixels P(m,n) are made uniform in length, consequently, making it difficult to occur for fluctuation in luminance of each of the subpixels **20***a*, **20***b* and each of the pixels P(m,n).

Therefore, it is possible to make an occurrence of non-uniformity in luminance of the liquid crystal display panel **1** difficult.

[0075] FIG. **7** shows a timing chart of the operation of the liquid crystal display apparatus **100** when the pixel P(m,n) in the vicinity of the lower end of the liquid crystal display apparatus **1** in FIG. **1** is driven.

[0076] In a case that the liquid crystal display panel **1** comprises M=2160 scanning lines, for example, when the subgate control signal of the Gsub (2158) that is a 2158-th subgate signal line from the top is transitioned from being at the low level to being at the high level, the main gate control signal of the last main gate signal line Gmain(2160) is transitioned from being at the high level to being at the low level.

[0077] The control circuit **11** controls the power supply circuit **12** so as to generate the power supply voltage VGH**3** being lower than the power supply voltage VGH**1** and supply the power supply voltage VGH**3** to the gate drive circuit **2** when the count value V-CNT=2167 is reached, or, in other words, after the count value V-CNT=2160 elapses from the time at which the control signal GSP**1** is caused to transition from being at the low level to being at the high level. The main gate control signal of the main gate signal line Gmain(2160) is caused to transition from being at the high level to being at the low level in conjunction with the first rise of the clock signal GCK after the count value V-CNT=2167 is reached. In other words, in the time interval with the count value V-CNT-2167, the switching elements **21***a*, **21***b* of each of the pixels P(2160,n) included in the last scanning line of the frame are caused to transition from ON to OFF, and the load that is applied to the gate drive circuit **2** decreases. The control circuit **11** controls the power supply circuit **12** so as to generate the power supply voltage VGH**3** and supply the power supply voltage VGH**3** to the gate drive circuit **2** in a predetermined time period including the time interval with the count value V-CNT=2167, namely, a time period over the count value V-CNT=2167 and beyond (also referred to as "a third time period"). In other words, the control circuit **11** controls the power supply circuit **12** so as to generate the power supply voltage VGH**3** and supply the power supply voltage VGH**3** to the gate drive circuit **2** in the third time period in which the switching elements **21***a*, **21***b* of each of the pixels P(2160,n) included in the last scanning line of the frame are transitioned from ON to OFF. The third time period continues up to a start of a first time period of the following frame, or, in other words, up to a time interval with the count value V-CNT=6 in the following frame.

[0078] In this way, when the switching elements **21***a*, **21***b* of each of the pixels P(2160,n) included in the last scanning line of the frame are turned OFF, the power supply voltage VGH supplied to the gate drive circuit **2** is decreased, and thereby it is possible to cancel out an increase in the power supply voltage VGH due to a decrease in load. In this way, the ON times of the switching element **27** of each of the pixels P(m,n) are made uniform in length, consequently, making it difficult to occur for fluctuation in luminance of each of the subpixels **20***a*, **20***b* and each of the pixels (m,n). Therefore, it is possible to make an occurrence of non-uniformity in luminance of the liquid crystal display panel **1** difficult.

[0079] In a 4K2K liquid crystal display panel comprising 2160 scanning lines, for example, the power supply voltage VGH**1** is set to 38.0V, the power supply voltage VGH**2** is set to 39.0V, and the power supply voltage VGH**3** is set to 36.0V. The power supply voltages VGH**1** to VGH**3** are construed to be not limited to these values, so that these voltages can be set in accordance with the number of pixels of the liquid crystal display panel, the gate threshold voltage of each of the switching elements **21***a*, **21***b*, **27**, and the like.

[0080] The timing to change the power supply voltage VGH from VGH**2** to VGH**3** changes in accordance with the number of scanning lines of the liquid crystal display panel **1**. In the 4K2K liquid crystal display panel comprising 2160 scanning lines, the power supply voltage VGH, as described previously, is changed when the main gate control signal of the main gate signal line Gmain(2160) is transitioned from being at the high level to being at the low level. In a 2K1K liquid crystal display panel comprising 1080 scanning lines, the power supply voltage VGH is changed when the main gate control signal of the main gate signal line Gmain(1080) is transitioned from being at the high level to being at the low level. In an 8K4K liquid crystal display panel comprising 4320 scanning lines, the power supply voltage VGH is changed when the main gate control signal of the main gate signal line Gmain(4320) is transitioned from being at the high level to being at the low level. In any one of the cases, the power supply voltage VGH is changed before the time period in which the main gate control signals of all of the main gate signal lines Gmain(m) are transitioned from being at the high level to being at the low level and only the subgate control signal of the subgate signal line Gsub(m) is at the high level.

[0081] In the liquid crystal display panel having the multi-pixel drive scheme according to the conventional art, luminance of each of the subpixels and each of the pixels could fluctuate due to fluctuation in magnitude of load applied to the gate drive circuit as described previously. Therefore, the delay time of the subgate control signal with respect to the main gate control signal needs to be set as a very small value (a fixed value, for example) so that fluctuation in luminance occurs in the vicinity of the upper end of the liquid crystal display panel (in other words, under the bezel of the liquid crystal display apparatus) and fluctuation in luminance does not appear substantially. On the other hand, in the liquid crystal display apparatus **100** according to the present embodiment, an occurrence of fluctuation in luminance of each of the subpixels **20***a*, **20***b* and each of the pixels P(m,n) is made difficult as described above, therefore, it is possible to set the delay time of the subgate control signal with respect to the main gate control signal arbitrarily, not limited to a very small value.

[0082] FIG. **8** shows a timing chart to explain that luminance of the pixels P(m,n) changes by changing the delay time of the sub-gate control signal with respect to the main gate control signal in the liquid crystal display apparatus **100** in FIG. **1**. In a case A in FIG. **8**, the subgate control signal of the subgate signal line Gsub(**1**) has a delay time T**3** with respect to the main gate control signal of the main gate signal line Gmain(**1**). In this way, in the time period T**1**, the subpixels **20***a*, **20***b* are lit with mutually the same luminance, while, in the time period T**2** being after the switching element **27** is turned ON, luminance of the subpixel **20***b* is lower than luminance of the subpixel **20***a*. Moreover, in a case B in FIG. **8**, the subgate control signal of the subgate signal line Gsub(**1**) has a delay time T**13** being longer with respect to the main gate control signal of the main gate signal line Gmain(**1**). In this way, in the time period T**11**, the

subpixels **20***a*, **20***b* are lit with mutually the same luminance, while, in the time period T**12** being after the switching element **27** is turned ON, luminance of the subpixel **20***b* is lower than luminance of the subpixel **20***a*. Luminance of the pixels P(m,n) is determined by the ratio of the time period in which the subpixels **20***a*, **20***b* are lit with mutually the same luminance and the time period in which luminance of the subpixel **20***b* is lower than luminance of the subpixel **20***a*. Increasing the time period in which luminance of the subpixel **20***b* is lower than luminance of the subpixel **20***a* (or, in other words, decreasing the delay time of the subgate control signal with respect to that of the main gate control signal) causes luminance of the pixels P(m,n) to decrease. Decreasing the time period in which luminance of the subpixel **20***b* is lower than luminance of the subpixel **20***a* (or, in other words, increasing the delay time of the subgate control signal with respect to that of the main gate control signal) causes luminance of the pixels P(m,n) to increase. Therefore, changing the delay time of the subgate control signal with respect to the main gate control signal makes it possible to change luminance of the pixels P(m,n).

[0083] The rise and the fall of the control signals GSP**1**, GSP**2** are controlled by the count value of the counter **13**, therefore, by changing the count value from the beginning portion of one frame up to the rise of the control signal GSP**2**, it is possible to change the delay time of the subgate control signal with respect to the main gate control signal.

[0084] The control device **4** can control the gate drive circuit **2** so as to have a variable delay time from when the switching elements **21***a*, **21***b* of each of the pixels P(m,n) included in the first scanning line of the frame are turned OFF to when the switching element **27** of each of the pixels P(m,n) included in the first scanning line of the frame is turned ON. Moreover, the control device **4** can control the gate drive circuit **2** so as to have an arbitrary fixed delay time from when the switching elements **21***a*, **21***b* of each of the pixels P(m,n) included in the first scanning line of the frame are turned OFF to when the switching element **27** of each of the pixels P(m,n) included in the first scanning line of the frame is turned ON.

[0085] In this way, in the liquid crystal display apparatus **100** according to the embodiment, changing the delay time of the subgate control signal with respect to the main gate control signal makes it possible to change luminance of the pixels P(m,n).

[0086] In the embodiment described above, the liquid crystal display panel **1** is configured such that video data is written into the pixels P(m,n) in four mutually adjacent rows in a temporally overlapping manner. In replacement thereto, video data can be written into the pixels in two, three, or five or more mutually adjacent rows in a temporally overlapping manner, or video data can be written into the pixel in each row in a temporally non-overlapping manner. In this case, pixels in each of the columns are connected to the source drive circuit via source signal lines in the same number as the number of rows in which video data is written in a temporally overlapping manner. Decreasing the number of source signal lines connected to the pixels in each of the columns makes it difficult to block light transmitting each of the pixels by the source signal lines, and thereby, it is possible to improve the transmittance of light in each of the pixels. On the other hand, by increasing the number of source signal lines connected to the pixels in each of the columns, it is possible to obtain a sufficient length of time in which video data is written into each of the pixels as described previously. Moreover, writing video data into pixels in mutually adjacent rows via mutually different source signal lines makes it possible to make an occurrence of ghost due to the voltage to be applied to a pixel in a certain row being applied to a pixel in an adjacent row difficult.

INDUSTRIAL APPLICABILITY

[0087] The present invention makes it possible to provide a liquid crystal display apparatus having a multi-pixel drive scheme in which non-uniformity in luminance is unlikely to occur.

DESCRIPTION OF REFERENCE NUMERALS

[0088] **1** . . . LIQUID CRYSTAL DISPLAY PANEL
[0089] **2** . . . GATE DRIVE CIRCUIT
[0090] **3** . . . SOURCE DRIVE CIRCUIT
[0091] **4** . . . CONTROL DEVICE
[0092] P . . . PIXEL
[0093] **11** . . . CONTROL CIRCUIT
[0094] **12** . . . POWER SUPPLY CIRCUIT
[0095] **13** . . . COUNTER
[0096] **14** . . . VIDEO PROCESSING CIRCUIT
[0097] **20***a*, **20***b* . . . SUBPIXEL
[0098] **21***a*, **21***b* . . . SWITCHING ELEMENT
[0099] **22***a*, **22***b* . . . SUBPIXEL ELECTRODE
[0100] **23** . . . LIQUID CRYSTAL LAYER
[0101] **24** . . . COUNTER ELECTRODE
[0102] **25***a*, **25***b*, **26***a*, **26***b* . . . AUXILIARY CAPACITANCE ELECTRODE
[0103] **27** . . . SWITCHING ELEMENT
[0104] **28**, **29** . . . BUFFER CAPACITANCE ELECTRODE
[0105] **31** . . . SHIFT REGISTER
[0106] **32** . . . LEVEL SHIFTER
[0107] SW(**1**,a)~SW(M,b) . . . SWITCH
[0108] **41** . . . HIGH VOLTAGE SOURCE
[0109] **41***a*-**41***c* . . . VOLTAGE GENERATION CIRCUIT
[0110] **42** . . . LOW VOLTAGE SOURCE
[0111] **42***a* . . . VOLTAGE GENERATION CIRCUIT
[0112] SW . . . SWITCH

1. A control device for a liquid crystal display apparatus comprising a liquid crystal display panel, a gate drive circuit, and a source drive circuit, wherein

the liquid crystal display panel comprises a plurality of pixels arranged along a plurality of scanning lines; a plurality of first gate signal lines and a plurality of second gate signal lines connected to the gate drive circuit; and a plurality of source signal lines connected to the source drive circuit;

each pixel of the plurality of pixels comprises first subpixel and second subpixel; a buffer capacitance; first and second switching elements to connect the first subpixel and the second subpixel, respectively, to one source signal line; and a third switching element to connect the second subpixel to the buffer capacitance, wherein the first and second switching elements operate in accordance with a first gate control signal applied via one first gate signal line from the gate drive circuit and the third switching element operates in accordance with

a second gate control signal applied via one second gate signal line from the gate drive circuit; and

the control device comprises a power supply circuit, wherein

in a first time period including a time period to transition the first and second switching elements of each pixel, in the plurality of pixels, included in a first scanning line of a frame from OFF to ON, the power supply circuit generates a first power supply voltage and supplies the first power supply voltage to the gate drive circuit, and, thereafter,

in a second time period including a time period to transition the third switching element of each pixel included in the first scanning line of the frame from OFF to ON, the power supply circuit generates a second power supply voltage higher than the first power supply voltage and supplies the second power supply voltage to the gate drive circuit.

2. The control device according to claim **1**, wherein

in a third time period including a time period to transition the first and second switching elements of each pixel included in a last scanning line of the frame from ON to OFF, the power supply circuit generates a third power supply voltage lower than the first power supply voltage and supplies the third power supply voltage to the gate drive circuit.

3. The control device according to claim **1**, wherein

the control device controls the gate drive circuit so as to have a fixed delay time from when the first and second switching elements of each pixel included in the first scanning line of the frame are turned OFF to when the third switching element of each pixel included in the first scanning line of the frame is turned ON.

4. The control device according to claim **1**, wherein

the control device controls the gate drive circuit so as to have a variable delay time from when the first and second switching elements of each pixel included in the first scanning line of the frame are turned OFF to when the third switching element of each pixel included in the first scanning line of the frame is turned ON.

5. A liquid crystal display apparatus comprising

the control device according to claim **1**;

a liquid crystal display panel;

a gate drive circuit; and

a source drive circuit.

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